Development of high density and high frequency substrate using B^{2}it^{TM} technology for next generation

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Satoru Kuramochi Tomoko Maruyama Miyuki Akazawa
Kouichi Nakayama Masataka yamaguchi Atsushi Takano
Kazuo Umeda * Osamu Shimada* Yoshitaka Fukuoka **

Dai Nippon Printing Co., Ltd.
*D.T.circuit technology Co., Ltd.
** Weisti(worldwide Electronic Integrated Substrate Technology Inc)

Contents

1, Background

Technology nodes for High density packaging substrate

	2002	2004	2005	2007	2010	2016
Technology Nodes (nm) MPU/ASIC	180	90	80	65	50	26
Needs for BGA Ball-Pitch (mm)	0.4	0.4	0.4	0.3	0.3	0.25
FcpadPitch (mm)	0.16	0.15	0.13	0.12	0.09	0.07
Line (um)	**10.7**	**10.7**	**9.2**	**9.2**	**6.4**	**5.0**
Space (um)	**10.7**	**10.7**	**9.3**	**9.3**	**6.4**	**5.0**
Performance On-chip(GHz)	**2.32**	**3.09**	**5.17**	**6.74**	**12**	**29**
Performance Chip-to-Board For peripheral Buses(GHz)	1.87	2.26	2.49	3.01	4.0	7.1

Source ITRS2001Edition

Calculated result of required line width

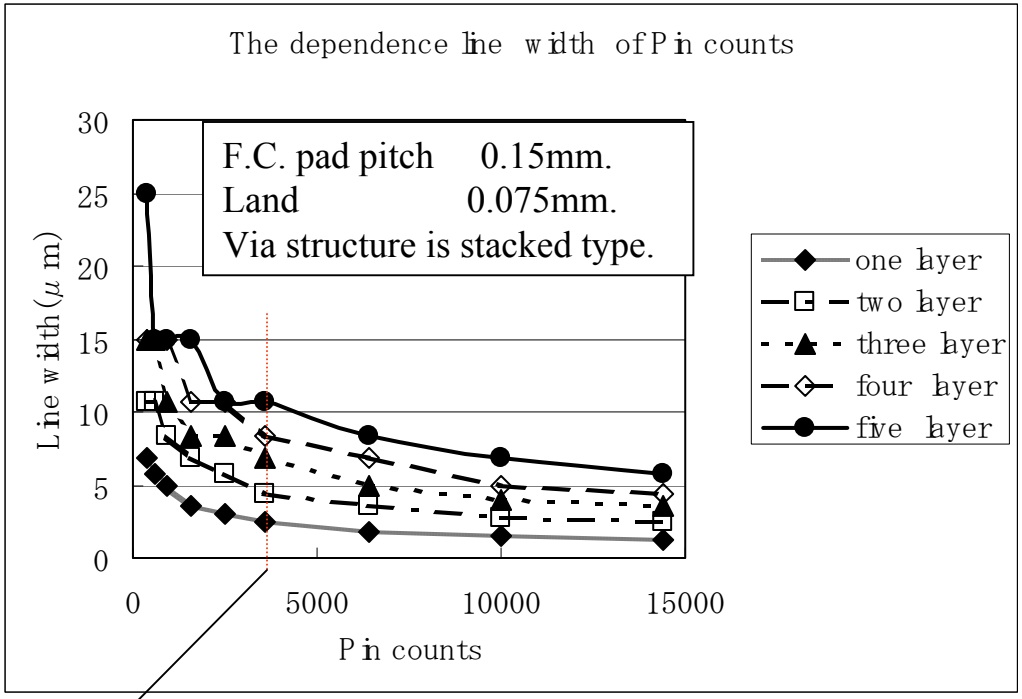


Fig.1 Calculated result of required line width

3600 pin count FC-package needs 8.3um line width by 4layer, or 10.7um line width by 5layer.

Motivation

Why do we conduct this study ?

Development of Substrate

Package pin count overflow

interconnection delay

Line width under 10um for fine pitch

High performance at high frequency over 9GHz

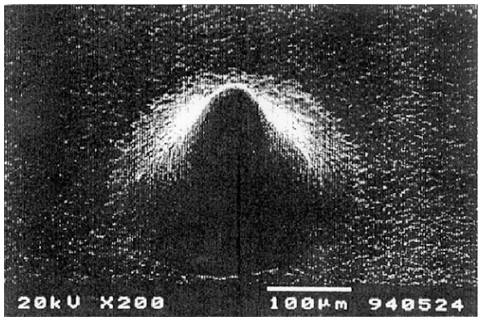
Based on new type of substrate

B²it™ technology

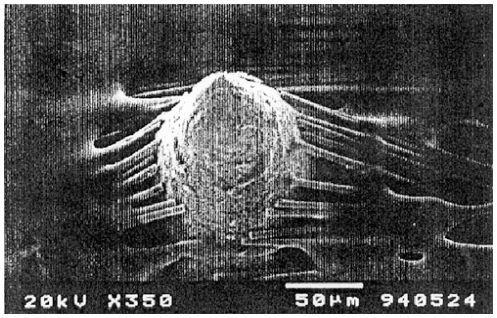
2, Concept of Development

We have developed B²it™ Printed Wiring Boards

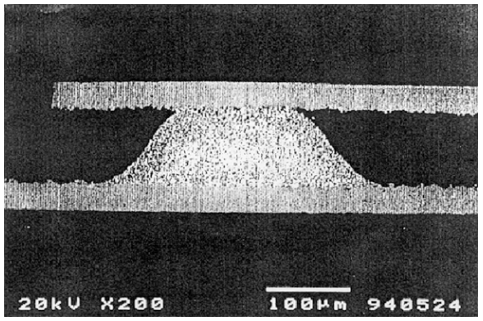
B²it™ Bump Shape (After Printing)

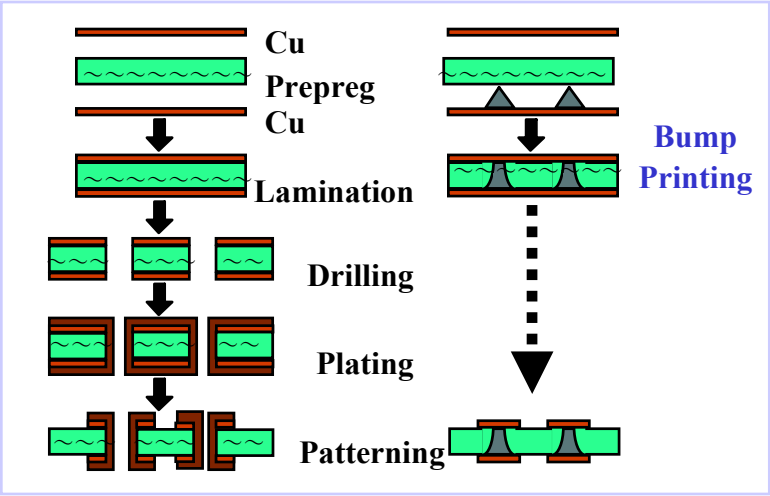


B²it™ Bump Shape (After Piercing)



B²it™ Bump Shape (After Lamination)





①**Great variety** of multilayer **structure and process**.

②**Stacked (Straight) via** holes of great advantage to area I/O terminal devices.

③**High cost-performance printed** wiring board.

Process Comparison between B²it™ & standard PWB.

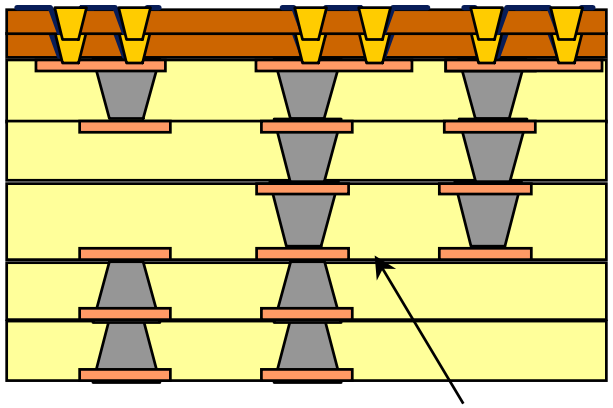
We propose new structure for next generation

Table 2 B^2it^{TM}Design Rules

	Standard	Fine Phase1	Fine Phase2	Fine Phase3
Build up layer				
L/S	-	-	-	Under 10/10
Via /Land	-	-	-	Under 20/30 stack
Core				
L/S	100 /100	75 /75	50 /50	30 /30
Bump Diameter	300	150	100	100
Pad Diameter	500	300	200	200
Bump Pitch	600	400	300	300

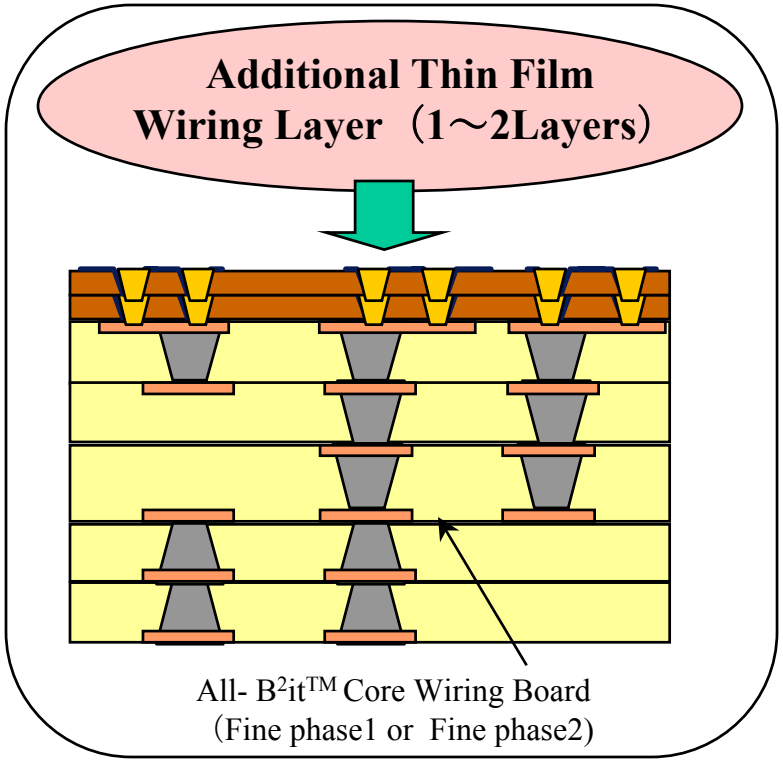
(um)

Combination Additional Thin Film Wiring Layer （1～2Layers）



All- B^2it^{TM} Core Wiring Board （Fine phase1 or Fine phase2）

B²it™ Fine phase 3 Concept

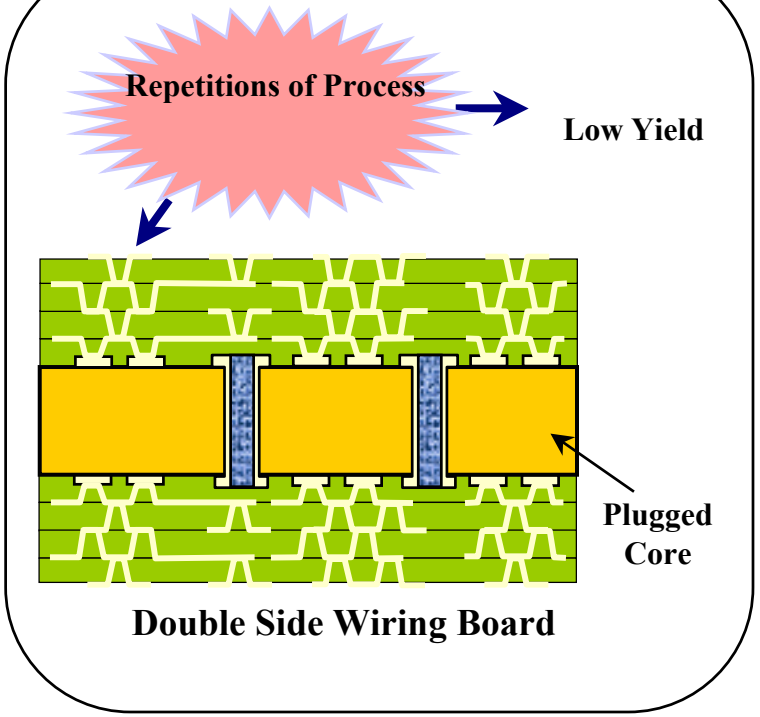


B²it™ Fine phase 3

900pin FC0.15
L/S=8.3/8.3

Fan out 2Layer

Equal Wiring Network



Conventional Plugged

900pin FC0.15
L/S=25/25

Fan out 7Layer

Features of B²it™ Fine phase 3

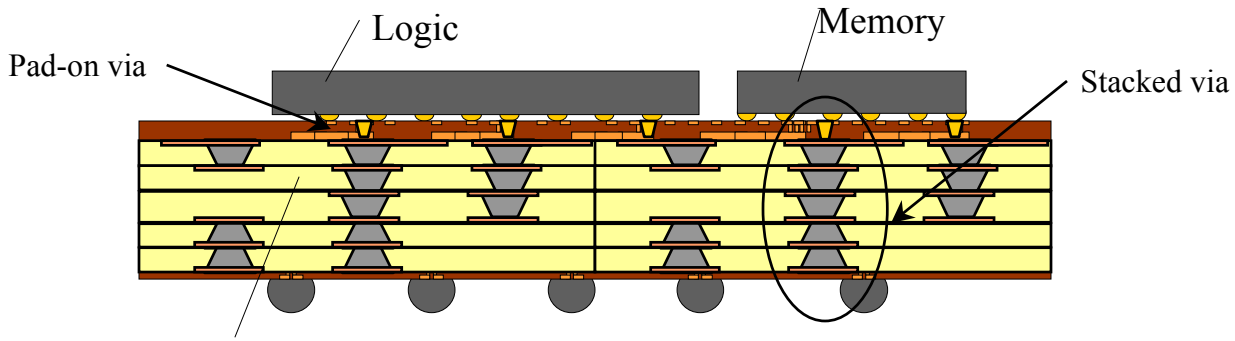
1, High- Performance ⇒ High speed transmission over 9GHz

2, Fine wiring, high density, precise

⇒L/S＝Under10um/10um、
V/L＝Under20/30um stacked
Straight Via (Stacking Via) holes are available.

3, Cost-performance

⇒ B²it™ Fine phase 3 substrate can be applied to all kinds of devices with grid I/O terminals . SIP is best application.

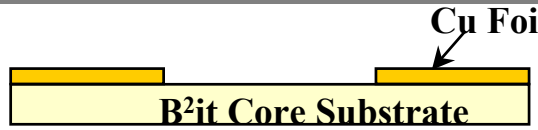


B²it™ Fine phase 3 Cross-sectional view

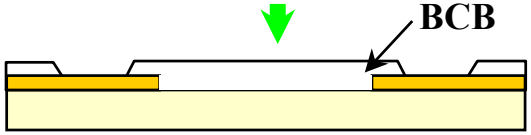
3, Fabrication Process

Process of B²it™ Fine phase 3

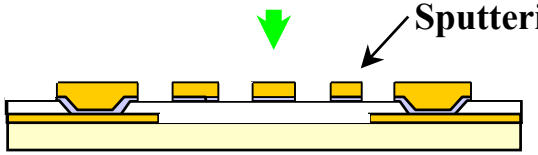
①Surface Conditioning



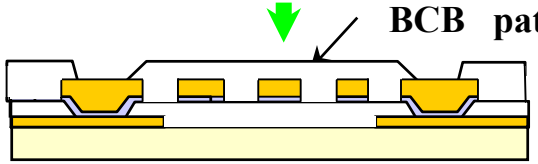
②1st Dielectric Layer



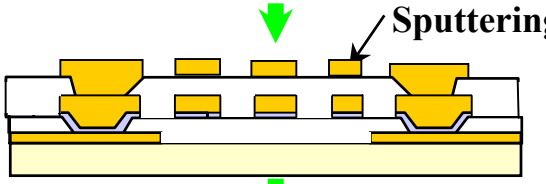
③ 1st Metal Layer



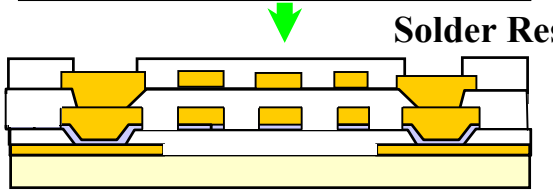
④2nd Dielectric Layer



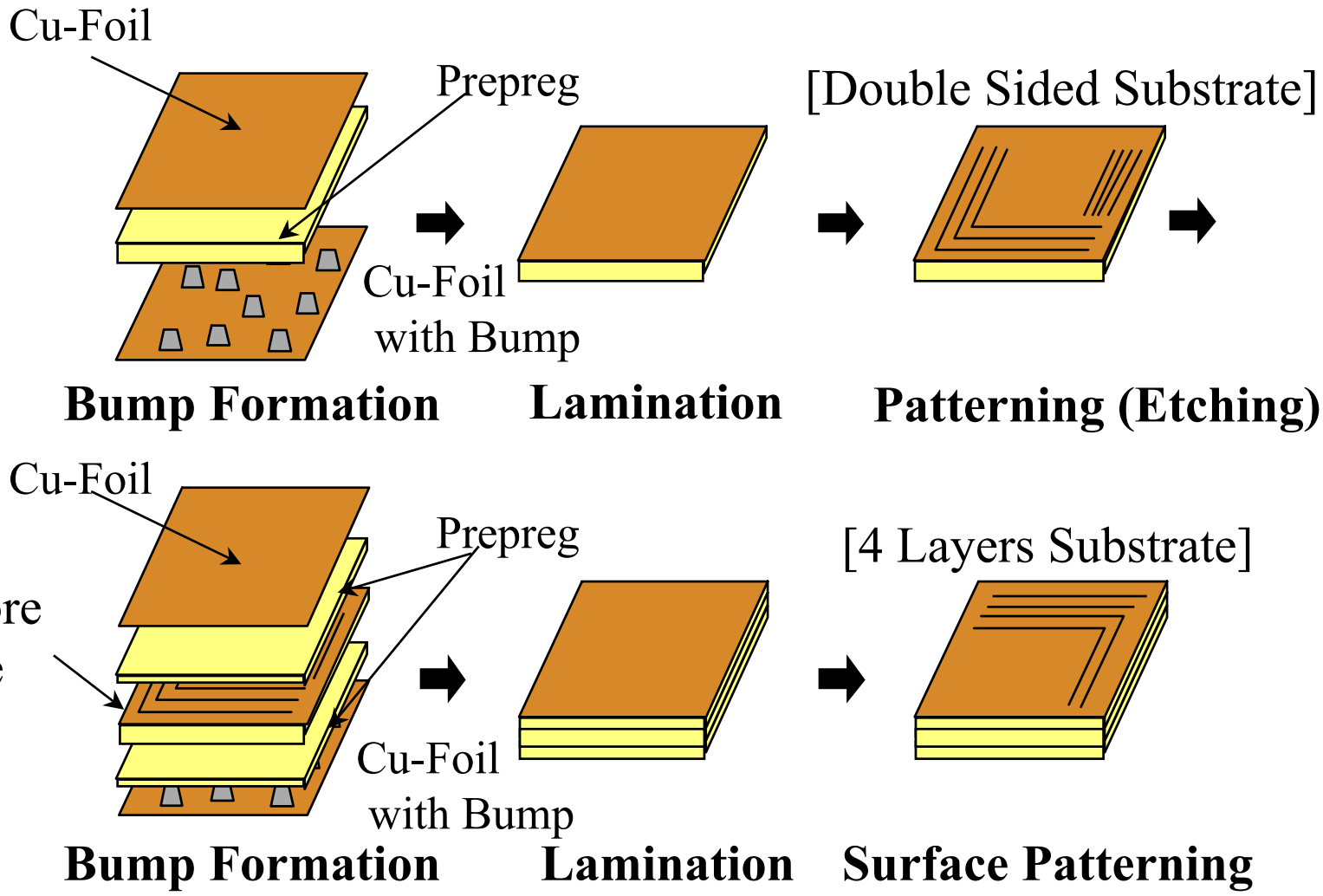
⑤2nd Metal Layer



⑥Solder Resist



B²it™ Core substrate Manufacturing Process



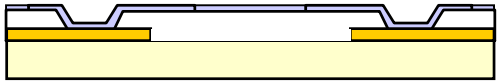
Reliability Test Results

No	Item	Condition	Criteria	Result
1	Peel Strength	Peeling Speed 500mm/min	1.4kN/m(1.43kgf/cm)	OK
2	Soldering Endurance	260℃, 20sec & 288℃, 10sec	Resistivity Changing Ratio less than 10%	OK
3	Insulating Voltage	DC500V, 60sec	No damage	OK
4	Temperature Humidity Cycle	25℃⇔65℃／90～98% 10Cycle（240H）	Insulating Resistance more than $5\times10^7\Omega$	OK
5	High Temperature High Humidity Bias	85℃／85%、DC12V&60V 500H	Insulating Resistance more than $5\times10^7\Omega$	OK
6	Temperature Cycling	-65℃（30min）⇔125℃（30min) 1000cycle	Resistivity Changing Ratio less than 10%	OK
7	Hot Oil (Thermal Shock)	260℃（10sec）⇔20℃（20sec) 100Cycle	Resistivity Changing Ratio less than 10%	OK
8	Pads Pull Strength	90° Pull head Speed :10mm/min	$10N/mm^2$	OK
9	High Temperature Operation	100℃、0.3A、1000H	Resistivity Changing Ratio less than 10%	OK
10	HAST	130℃／85%、DC10V、100H	Leak Current less than 10^{-10} A	OK
11	Bending	±10% Bending 100 Cycle	Resistivity Changing Ratio less than 10%	OK
12	Corrosion Gas	H2S：0.1ppm、SO2 ：0.5ppm 12V、500H	Insulating Resistance more than $5\times10^7\Omega$	OK

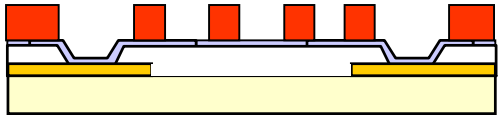
Fine wiring technology

Sputter-semi-additive method

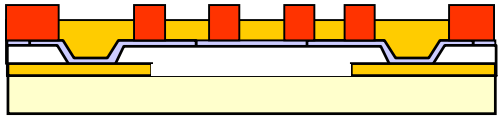
（1）Sputtering thin metal



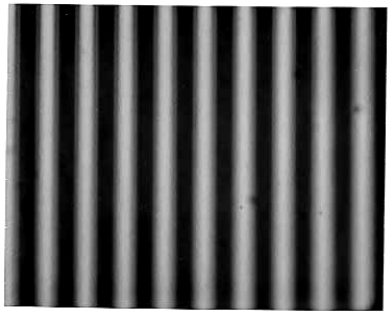
（2）Resist formation



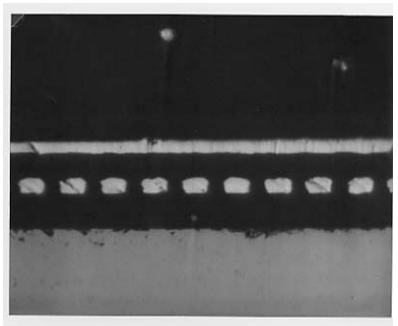
（3）Filled plating



（4）Remove resist and thin metal

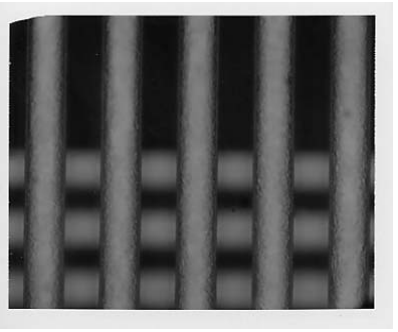


（a）L/S＝6um/4um
（3σ＝0.46um）



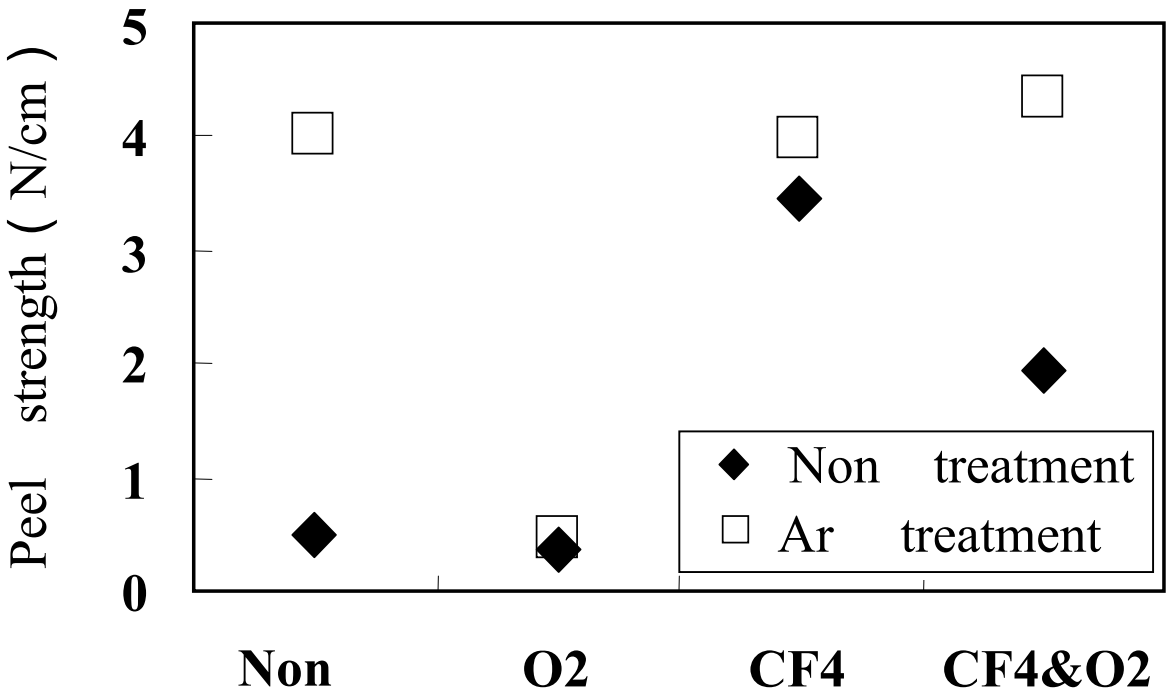
（b）L/S＝6um/4um
profile of 2Layer

（c）L/S＝8um/7um
（3σ＝0.53um）



（d）L/S＝11um/9um
（3σ＝0.41um）

Treatment effect before sputtering

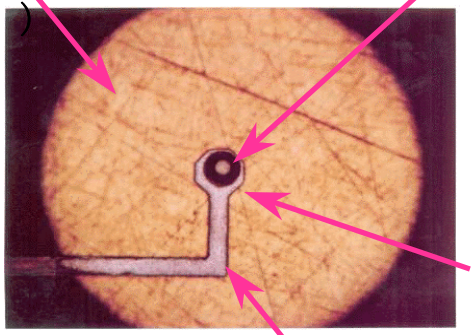


Pre-treatment surface of insulator
by dry etching gas

Photo Via on B²it™ Core

Core B²it™ Land （dia.400um ）

Via Diameter 30um

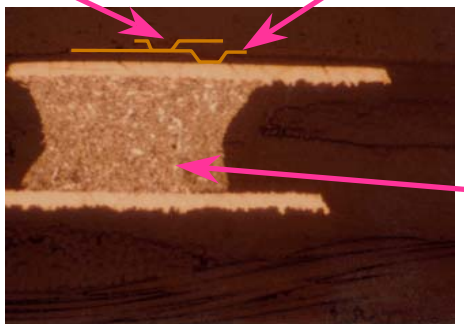


Land Diameter 60um

Line Width 30um

Interconnection Over View

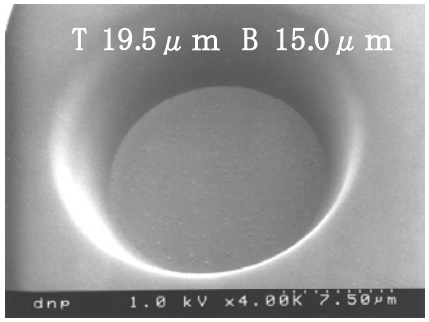
Photo Via （dia30um） L/S：30/30um

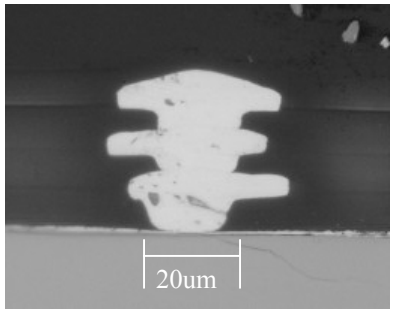


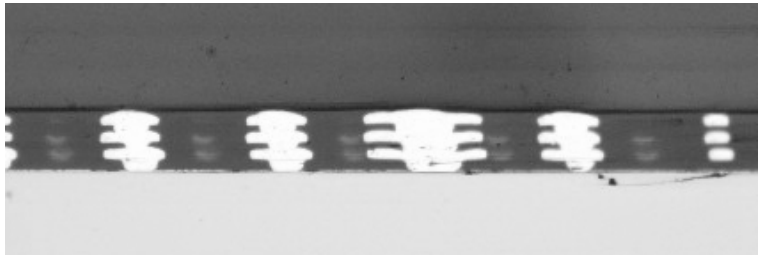
B²it™ Bump （dia.200um）

Interconnection Cross Sectional View

Filled via technology

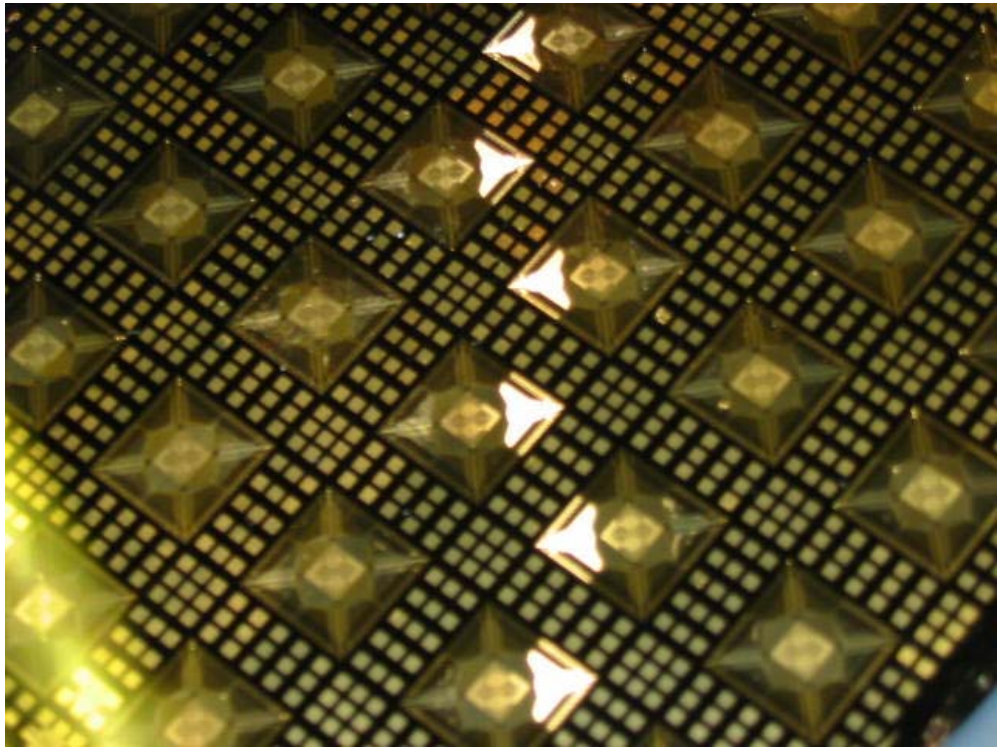






Via/Land=20um/30um stacked structure

Appearance of a prototype



4, Electrical Characteristic

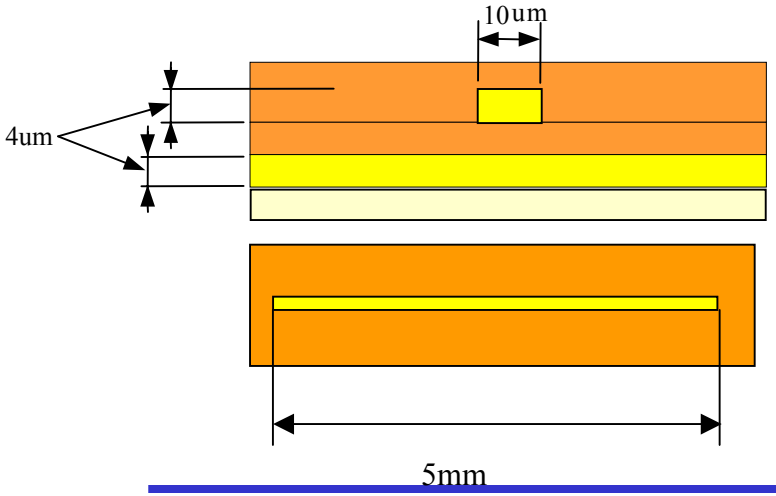
Simulation result of transmisson characteristic

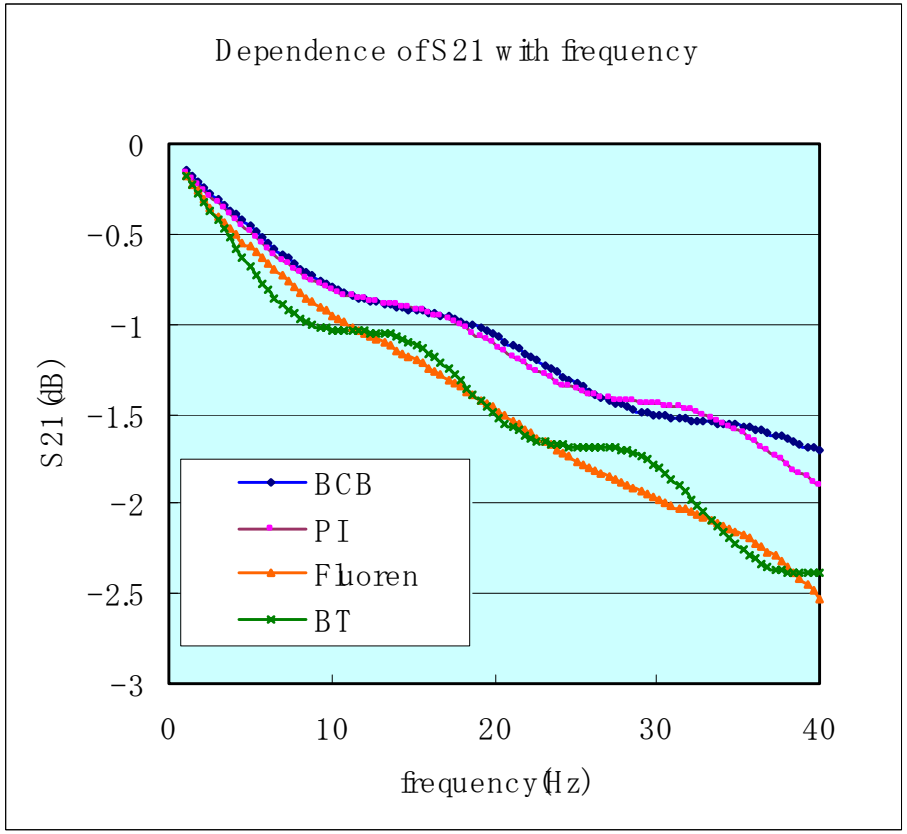
Simulator; HFSS(Ansoft) High frequency stress simulator

Model : Microstlip line with cover layer

Simulation structure

Insulator	ε	tan δ
BCB	2.7	0.0009
PI	3.2	0.0018
Fluorene	3.2	0.029
BT	4.2	0.012

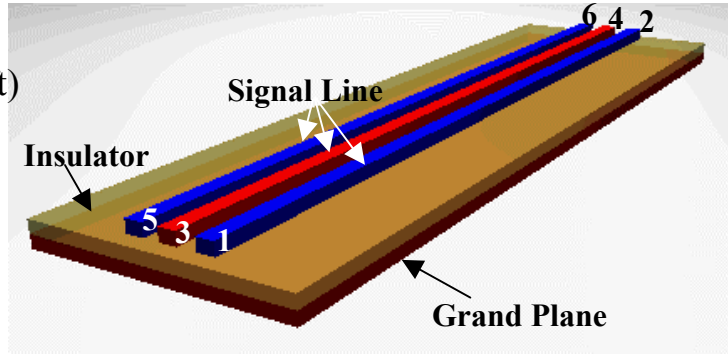




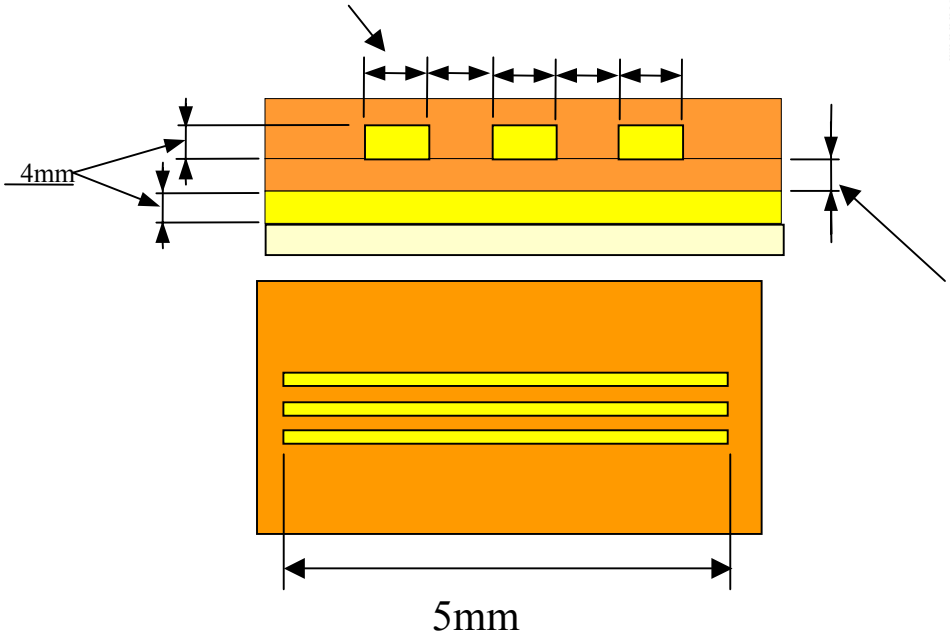
Simulation structure for evaluation of crosstalk

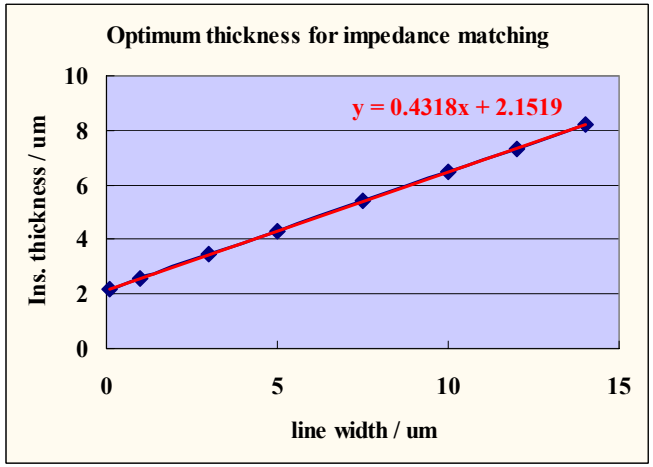
Simulator :

HFSS ; High Frequency s t rucre simulator (Ansoft)

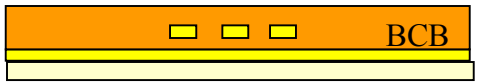


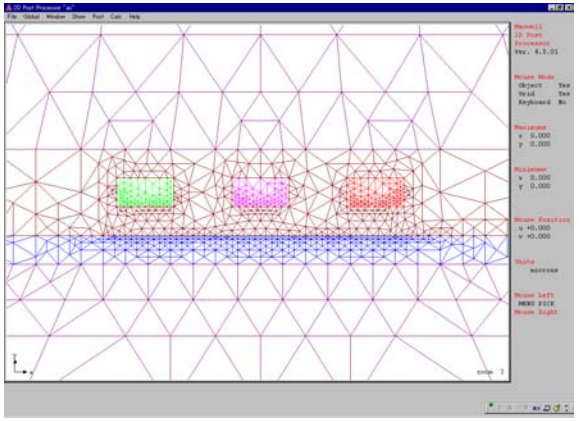
L/S=3/3, 5/5, 7.5/7.5, 10/10, 12/12, 14/14um

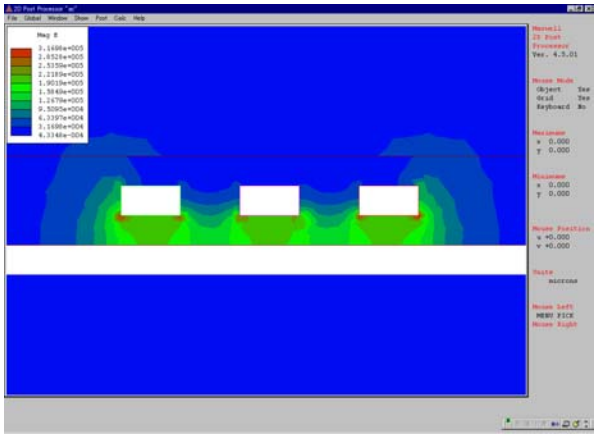


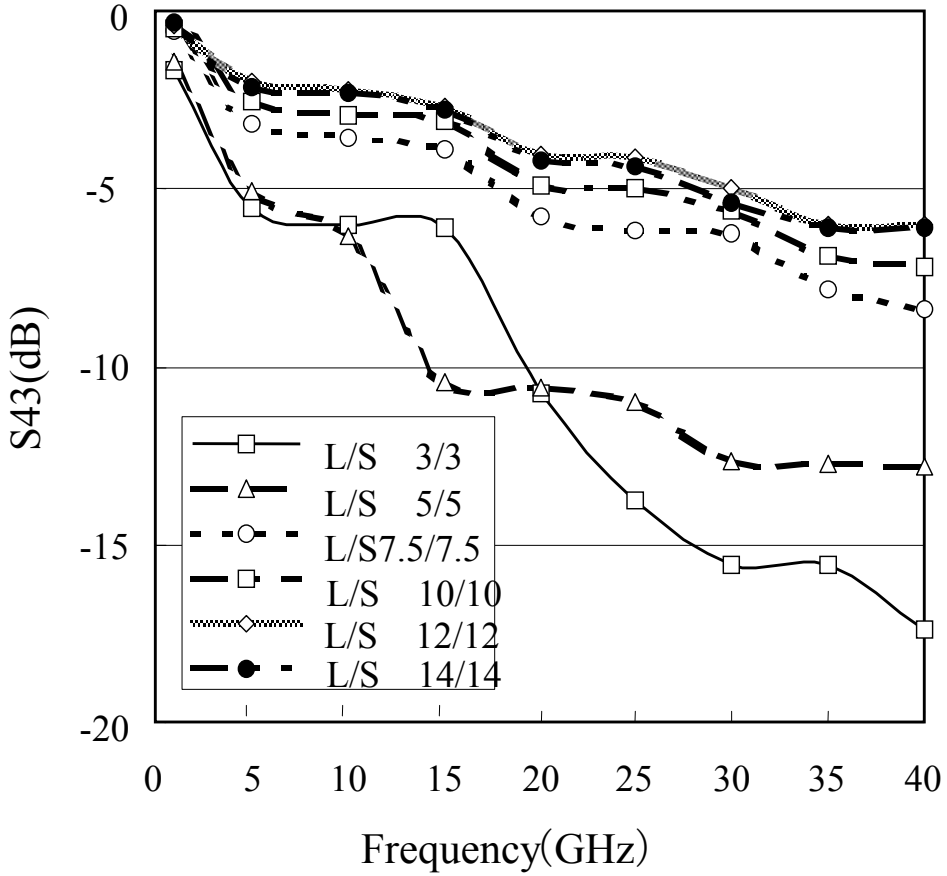


The dependence of insert loss on crosstalk of contiguity wiring







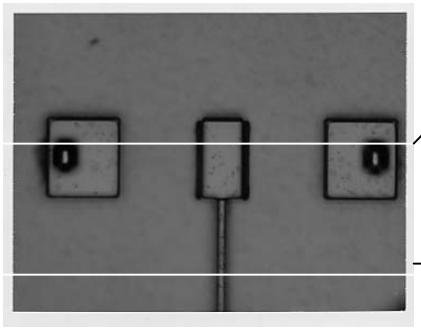


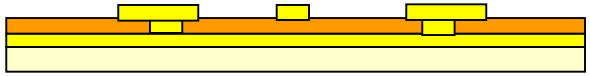
TEG structure for measurement of S-parameter

S-parameter measured using network analyzer , HP8722ES which made from Agilent technology

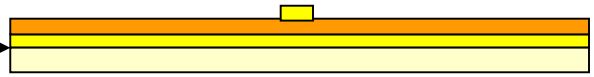
TEG structure

Insulator Material	BCB	Fluorene
Dielectric constant	2.7	3.2
tan δ	0.0009	0.029





(probing area)



(micro strip area)

Line length=15mm

Line width=11, 8, 6um

The dependence of transmission characteristics on line width

Line width **6um, 8um, 11um**

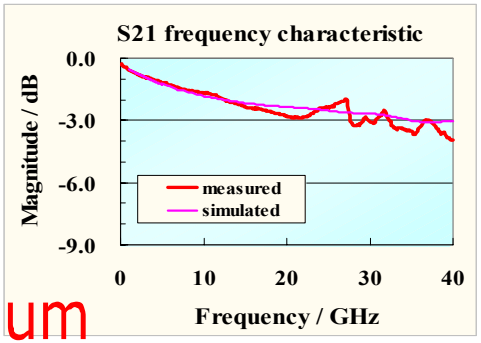
line length: **15mm**

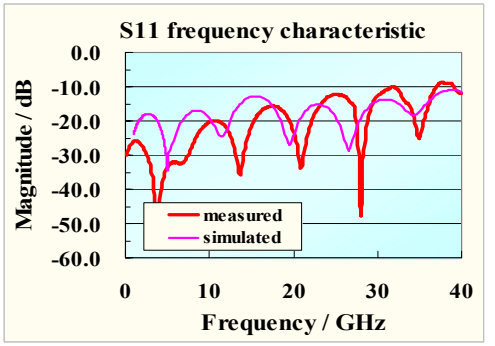
insulator: **BCB**

A transmission characteristic
does not become worth
even if line width becomes small.

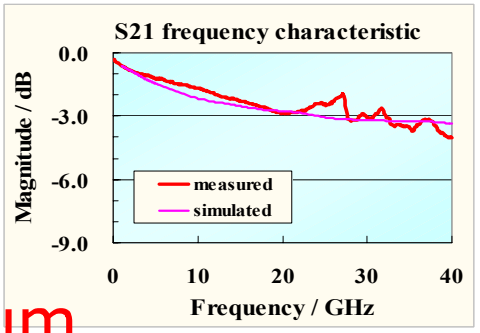
S21 S11

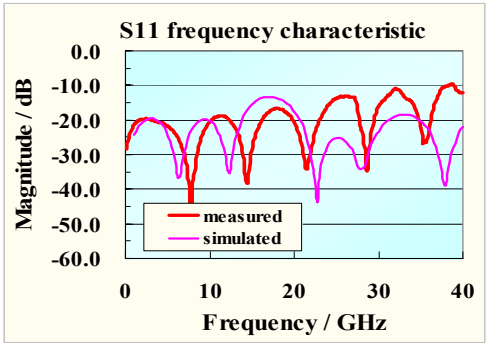
11um



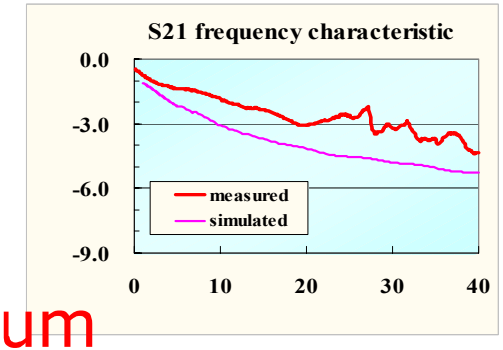


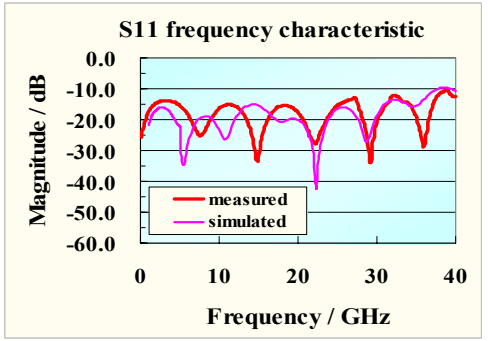
8um





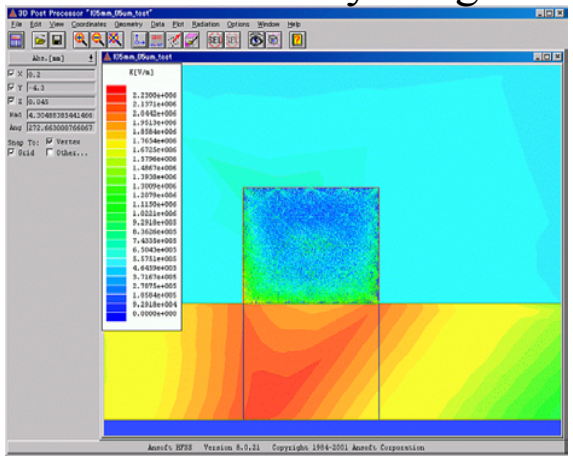
6um



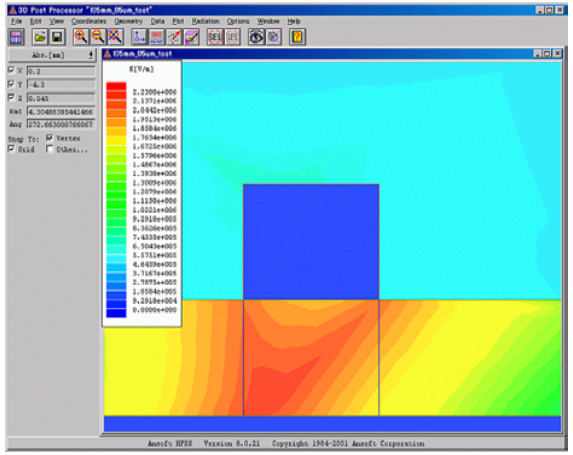


Comparison of measurement and simulation

Electric field intensity - edge of the lines

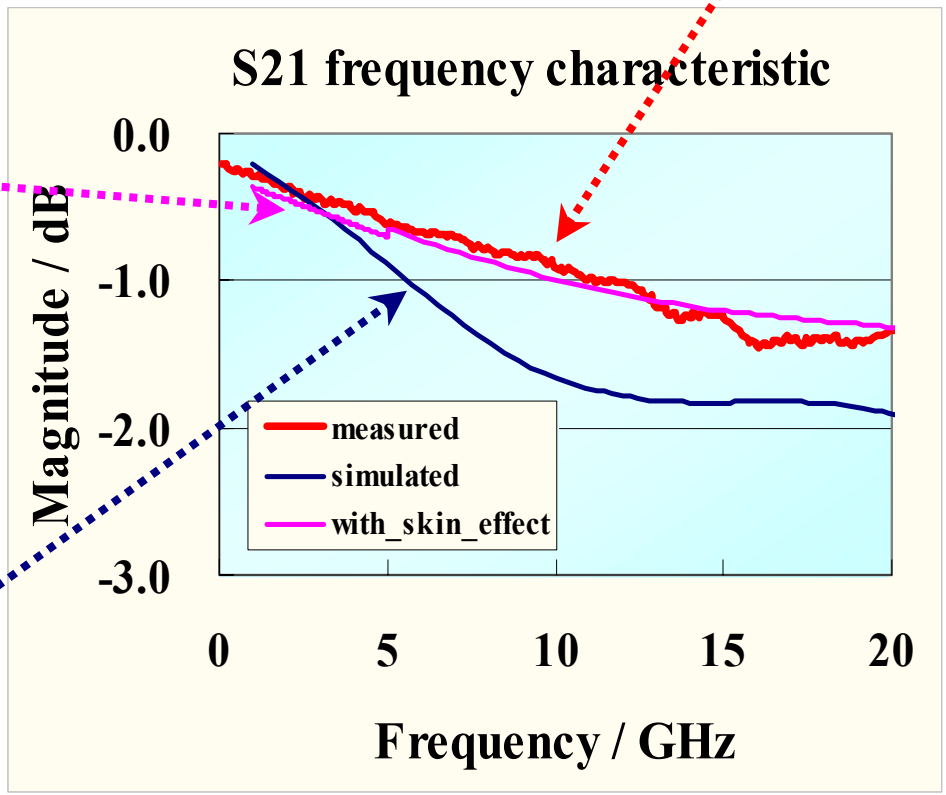


Solving the line inside (w/ skin effect)



Solving the line surface only (w/o skin effect)

Measured result



Better matching with measurement

Comparison of BCB and Fluorene

S_{21}*(insertion loss)*

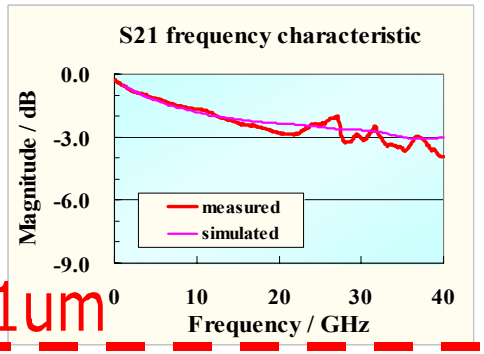
Line width **6um, 8um, 11um**

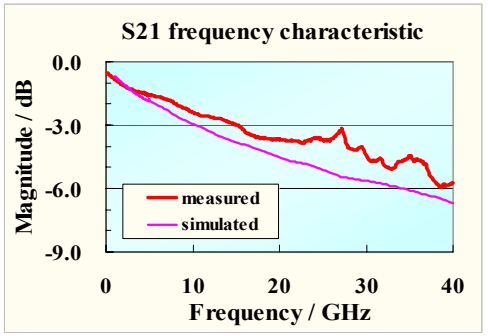
line length: **15mm**

insulator: **BCB / fluorene**

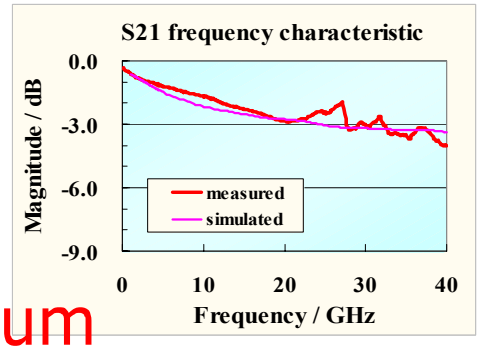
BCB fluorene

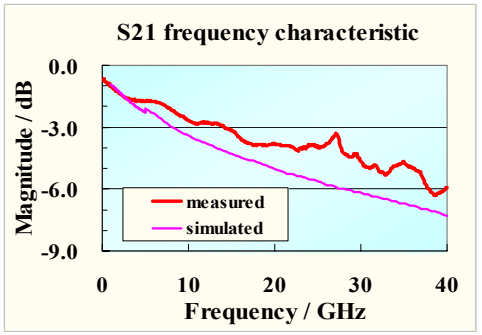
11um



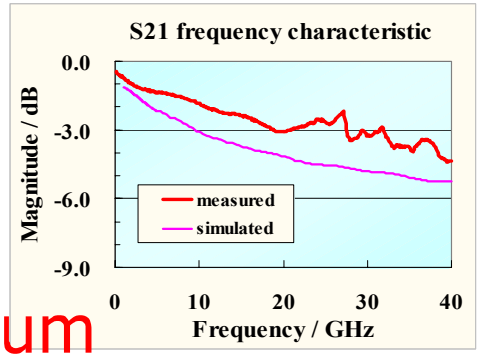


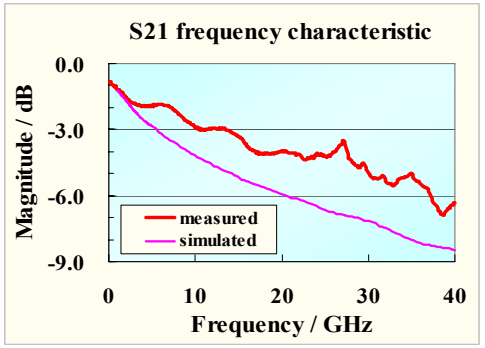
8um





6um





5, Summary and future plan

1, Very fine pitch Cu conductors with BCB on B^{2}it^{TM} core laminate was developed.
The minimum pitch was 10um (L/S=6 /4).
Filled plating process was possible for 20um via diameter

2, Cu conductors with BCB has excellent high frequency characteristic,
it was –3dB in 16GHz.
In case of single line , it does not become worth even if line width becomes small.
However, when the pitch became small at 10um or less with contiguity wiring,
transmission loss becomes large owing to the crosstalk.

3, As a optimal design rule of a the fine wiring layer, pitch is 15um (L/S=7.5 / 7.5),
and 20um of diameters filled via are the optimal designs,
and high density and high-speed substrate , B^{2}it^{TM} fine phase 3 was developed .

4, The reliability of interconnection has not conducted yet.
We plan to systematic and detailed reliability tests in next stage.
We will be sure that it becomes advantageous solution for a high-density and high-speed next-generation package.