Solid, Reliable and Planar Microvias Using (Mostly) Conventional Multilayer PCB Technology

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Abstract
Despite the strong increase in demand for high-density circuit boards, very few manufacturers are offering microvia architectures in high volume. Current microvia technologies require significant changes in multilayer manufacturing methods as well as new materials and new chemistries. The electroless plating chemistries most commonly used are costly and difficult to maintain, and the dimpled morphology of the resulting microvias is problematic. Transient-liquid-phase-sintered (TLPS) paste-filled microvias are solid, planarize during processing and will alloy to all conventional circuit finishes during standard lamination cycles. Although TLPS microvias, like most other microvia technologies, do require laser-drilling capabilities, no other significant change to standard multilayer PCB fabrication is needed. Use of advanced laminates/prepregs or resin-coated-foil is optional. The TLPS microvia technology was proven in cutting-edge multilayer-flex IC packages. It has since been adapted for use in multilayer PCB applications and can cost-effectively enable any multilayer board shop to offer HDI products.

Introduction
High volume microvia technologies are a requirement for high density interconnect (HDI). Over the last few years, several blind- and buried- microvia technologies have been proposed to relieve the density limitations imposed by plated through holes (PTH). Most of these techniques use additive sequential-build-up methods. Metallization of the microvias, regardless of how they are formed, is generally accomplished with electroless plating chemistries. Although there have been a number of improvements introduced in the last couple of years, electroless chemistries are notoriously difficult to maintain and are not otherwise generally used in multilayer PCB shops. In addition, the resulting microvias have a dimple-like morphology that is not conducive to microvia stacking, can entrap contaminants, and provides only a small contact area. Electroless plating is time-consuming, and each additional layer must be produced sequentially with compound yield losses which is not conducive to a high volume manufacturing operation.

A new category, known as the "paste microvia process," has been established[1] In this approach, microvia '"molds" are formed in a polymer dielectric material using photolithograpy, chemical etching or laser ablation. These microvia "molds" are then filled with a conductive paste material that is generally thermally processed to form a solid, electrically conductive microvia. The solid vias created by this approach can be stacked, which increases the circuit density potential, reduces the possibility of "blowouts" of entrapped contaminants, and provides a relatively large contact area that is less susceptible to breakout on small contact pads. The manufacturing flow for these processes offers the potential for either sequential or mass lamination, the potential for parallel processing of microvia layers, and generally requires only a simple stenciling operation to replace the lengthy electroless plating process.

Paste-filled vias have been offered in a number of sequential build-up processes. Matsushita's ALIVH technology, for instance, uses a copper polymer-thick-film (PTF) filled into laser drilled aramid-reinforced prepreg. The "microvia sheet" is laminated between an existing circuit and a sheet of copper foil.[2] As another example, Toshiba's B2IT technology uses stenciled-and-cured silver PTF bumps to puncture through dielectric during lamination.[3]

The flaw in the paste-filled microvia processes offered in recent years is their reliance on PTF conductors. There is no true metallurgical connection within the bulk of these passively metal-powder-loaded microvia fill materials. Likewise, there is also no alloyed connection to the contact pads. In addition, there is always the concern of silver migration in the silver-based PTFs and oxidation of the copper-based materials. Finally, the processes designed around the PTFs can be markedly different from conventional multilayer circuit formation.

The solid-microvia technology described in this paper addresses these shortcomings. The key to this solution is a microvia fill material that converts from a paste to a continuous metal network during standard lamination conditions. The network extends to the circuit pads and forms alloyed connections to all common circuit materials regardless of surface finish. Unlike the passively loaded PTFs, this conductor undergoes a transient liquid phase sintering (TLPS) reaction in which alloy particles melt, react with copper particles and form the solid metal network structure depicted in Figure 1. The resulting electrical and thermal conductivity is comparable to solder in both reliability and performance, but, unlike solder, the TLPS conductors discussed here do not remelt once processed.

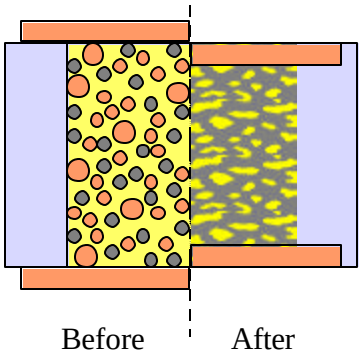

Figure 1 - TLPS Microvia Before and After Processing

The TLPS conductors discussed in this paper have been rigorously tested in mulilayer-flex IC package constructions (see Table 1), and have recently been adapted for application in HDI PCBs. Specialized pastes can be filled into laser drilled prepregs to create stand-alone microvia layers, or can be stenciled into microvia "molds" in the resin layers of resin-coated-foil products. Two potential processing schemes will be discussed in greater detail.

The advantages of using this unique microvia technology include the following:

- Microvia layers can be fabricated separately from circuitry layers
- Conventional double-sided PCBs can be joined or foil layers can be added and etched sequentially
- No electroless plating is required
- Solid, planar microvias can be stacked and offer greater ease of alignment
- High electrical and thermal conductivity (comparable to solder without the remelt)
- Reliable, alloyed connections to circuit pads form during standard lamination cycles
- Robust adhesion to a variety of PWB materials
- Microvia diameters down to 50 micron have been demonstrated

Parallel Build

A parallel build approach has been developed to directly replace plated through holes (PTH) in multilayer circuits. This approach is applicable to joining a number of double-sided circuits in a single mass lamination, or to adding single HDI layers to one or both sides of a conventionally produced PCB. The parallel build approach was used to build the multilayer-flex construction depicted in Figure 2, the reliability test structures summarized in Table 1, and the 14 layer PCB shown in Figure 3.

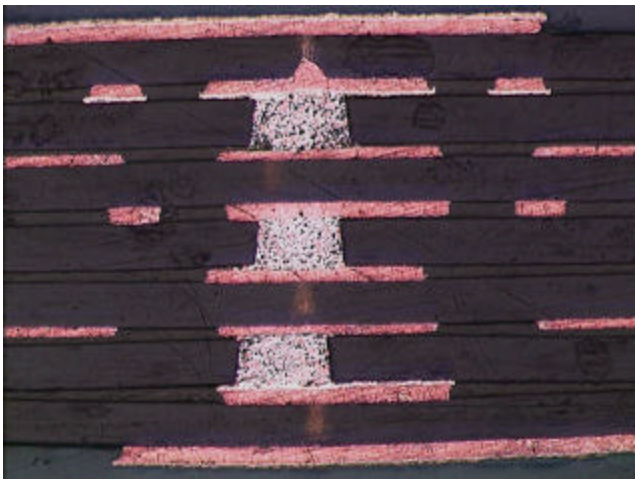

Figure 2 - 8-Layer Multilayer Flex Construction with 25 Micron Copper Vias in the Flex and 100 Micron TLPS Vias Connecting the Flex Circuits (Note: Alloying to Both Tinned and Bare Copper Pads)

Table 1 - TLPS Microvia Reliability Results in Multilayer Flex Packaging

Thermal Shock: Air to Air (-55C to +150C)	
Number of cycles	***Average change in resistance***
100	-0.9%
480	-2.4%
1000	-3.2%
Humidity - 7 day - (85°C / 85%RH)	
100 µm microvia in 4 layer	5%
125 µm microvia in 6 layer	6%

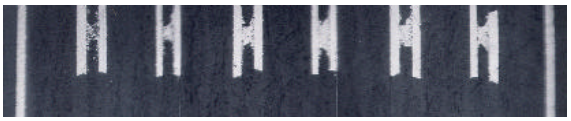

Figure 3 - 14 Layer PCB (Cross Section is Slightly Skewed)

For the multilayer flex package, a specialized paste was deposited into polyimide film that was laser drilled and coated on both sides with a polymer adhesive. The via holes in this construction were 100 µm. Typical constructions showed a via resistance of less than 10 mΩ. The TLPS connections were not sensitive to moisture uptake and showed little change in thermal cycling tests. Additional test vehicles evaluated vias ranging from 150µm down to 63µm in size. Even the 63µm vias typically demonstrated a resistance of less than 10mΩ per via. Fifty micron vias have been demonstrated in a multilayer flex construction, but have not been rigorously tested.

In the PCB parallel build process, this specialized paste is deposited into microvias that have been laser drilled into b-staged dielectric materials (e.g. prepreg). In the 14 layer construction depicted in Figure 3, 125µm vias were drilled in standard glass-reinforced prepreg, filled with the paste and laminated between seven double-sided circuits under standard 175°C conditions. This process was entirely analogous to conventional multilayer circuit fabrication - the only difference is that the interlayer connections were formed during lamination rather than in a subsequent drill, desmear and plate operation. Theoretically, smaller via diameters are feasible for this particular PCB-adapted microvia technology, but drilling costs are currently minimized using 100-150µm diameters, and these larger via sizes enable the use of a wider variety of prepreg styles and reinforcement materials. Incidentally, a 100µm TLPS via is not directly comparable to a 100µm electroless plated via because the larger contact area of the solid via can allow a change in design rules to reduce the size of the capture pads.

A generalized description of the parallel build process can be found in the conceptual diagram of Figure 4.

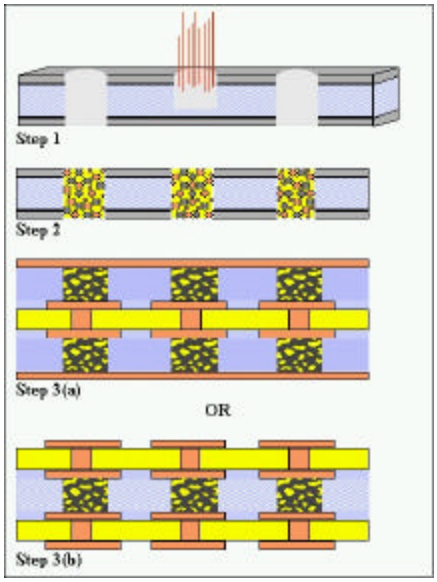

Figure 4 - General Description of the Parallel Build Process

In Step 1, b-staged dielectric or prepreg is laser drilled. In some cases, depending on the material used, cover sheets may be useful to improve handling of the uncured material

In Step 2, the laser drilled dielectric is filled with the specialized TLPS conductive paste. Again cover sheets may be useful in this step (they may be the same coversheets present in Step 1) so that any smear or overfill can be easily removed.

In Step 3(a), two of these unique microvia layers formed in Step 2 are laminated to either side of a conventional double-sided circuit (PTHs have been filled) and capped with copper foil. After lamination, these outer layers of foil can be etched to form circuitry or pads.

Additional microvia and foil layers could be added to this construction, but this concept will be presented more thoroughly in the sequential build section.

In Step 3(b) the microvia layer formed in Step 2 is laminated between two conventionally-produced double-sided circuits. The 14-layer board depicted in Figure 2 was produced using this method except that seven (7) double-sided circuits and six (6) microvia layers were laminated in a single step.

Sequential Build Processes

In the sequential build process, a layer of TLPS microvias and copper foil is added to one or both sides of a construction followed by circuit etching. (See Figure 5.) This process is then repeated in an iterative fashion to produce a many HDI layers as required. Conceivably, this method could be used to fabricate an entirely HDI structure starting from a single microvia layer and two sheets of copper foil. The basic building blocks for each microvia copper foil pair are: drilled-and-filled dielectric coupled with freestanding copper foil (see Step 3a of Figure 4), or a resin-coated-copper-foil (RCF) product that has been laser drilled through the resin (using the copper foil as a stop) and filled with specialized paste. Use of an RCF offers some handling advantages. In addition, because much thinner foils can be used in a RCF than would be possible if they were to be handled as independent sheets, higher density outer-layer circuits can be pattern-plated and flash-etched using RCF materials.

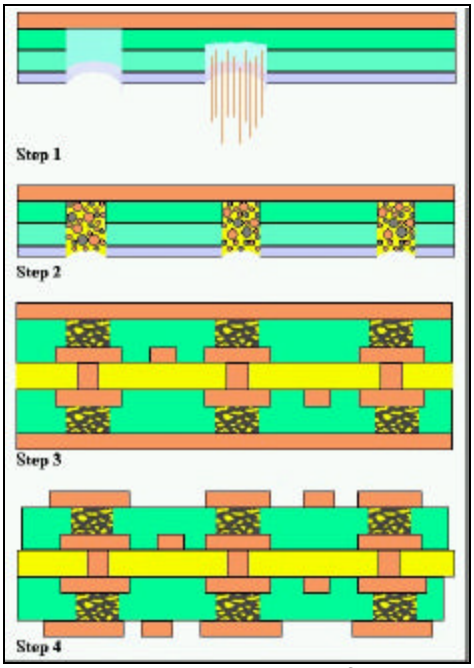

Figure 5 - Generalized Depiction of the Sequential Build Method using RCFs.

In Step 1, the RCF is laser drilled to form the microvia "molds." Because the laser intensity required to ablate the polymer material is much lower than the intensity required to ablate the copper foil, the copper acts a convenient drill stop. In addition, the copper foil dissipates the heat from the lazing operation so the hole walls are protected from premature curing, even at relatively high processing speeds.

In Step 2, the lazed RCF is filled with specialized TLPS paste.

In Step 3, two of the RCF microvia layers are laminated to either side of a conventionally produced double-sided circuit. Alternatively, a single microvia RCF layer could be laminated to a sheet of copper foil to create a core for an entirely HDI structure.

In Step 4, the construction formed in Step 3 is etched, or pattern-plated and flash-etched, to form the outer layer circuits.

Steps 1-4 may then be repeated as desired to form the total number of layers required. Because these particular microvia based structures are naturally self planarizing, the compounding topology issues encountered with electroless-plated microvia layers are eliminated.

Thus far, this unique microvia RCF has only been demonstrated in laboratory trials. Cross sections and resistance measurements indicate that good connections are being formed. Reliability results are anticipated to be similar to the parallel build constructions, but these studies have not yet been completed. It has been found that, unlike most conventional prepreg materials, the dielectric resins used in some RCF products react with the organic binder in the specialized paste composition and prevent connections from being formed. We are currently surveying RCF materials for compatibility based on our customers' preferences and application opportunities. It has also been found that it is very important to remove any residue remaining on the copper foil at the bottom of the via after the laser ablation process.

A maximum layer count has not been established for any of the unique microvia processes discussed here, but it is anticipated that the limit will be driven by the characteristics of the dielectric material chosen.

Summary

HDI PCBs require a blind and buried microvia technology that is conducive to high volume manufacturing and recaptures the majority of the real estate that is lost to plated through holes in conventional circuits. While electroless plated microvias are common today, solid microvia technologies are being developed to improve manufacturing speed and yield as well as enable unrestricted microvia placement.

This specialized microvia process is a proven, reliable technology that has been adapted for compatibility with PCB materials and typical lamination conditions. The solid microvias produced by this technology do not capture contaminants, do not distort outer layer topography, and can be stacked. Unlike solder and PTF materials, TLPS microvias will not remelt and are alloyed throughout the bulk of the material as well as to the capture pads. This unique microvia process is a patented technology currently available for specific application development and license.

References

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