Solid, Reliable and Planar Microvias Using (Mostly) Conventional Multilayer PCB Technology

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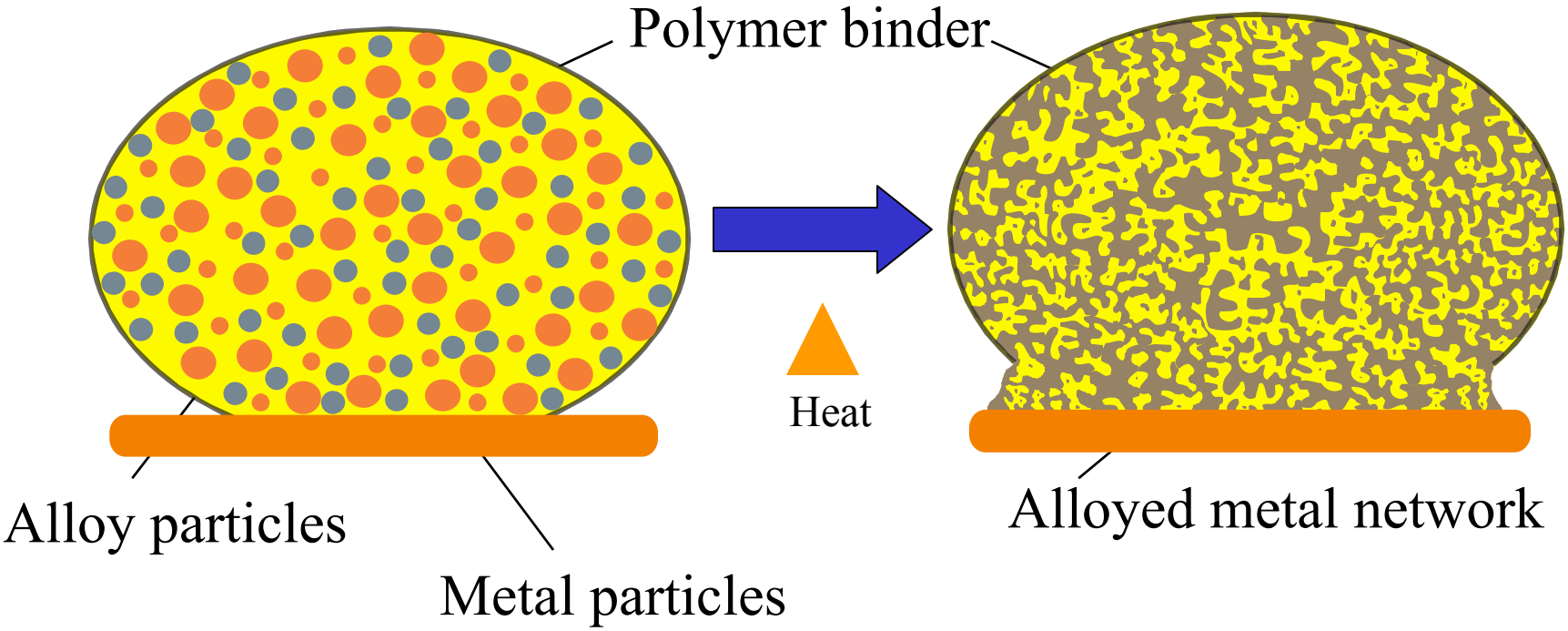
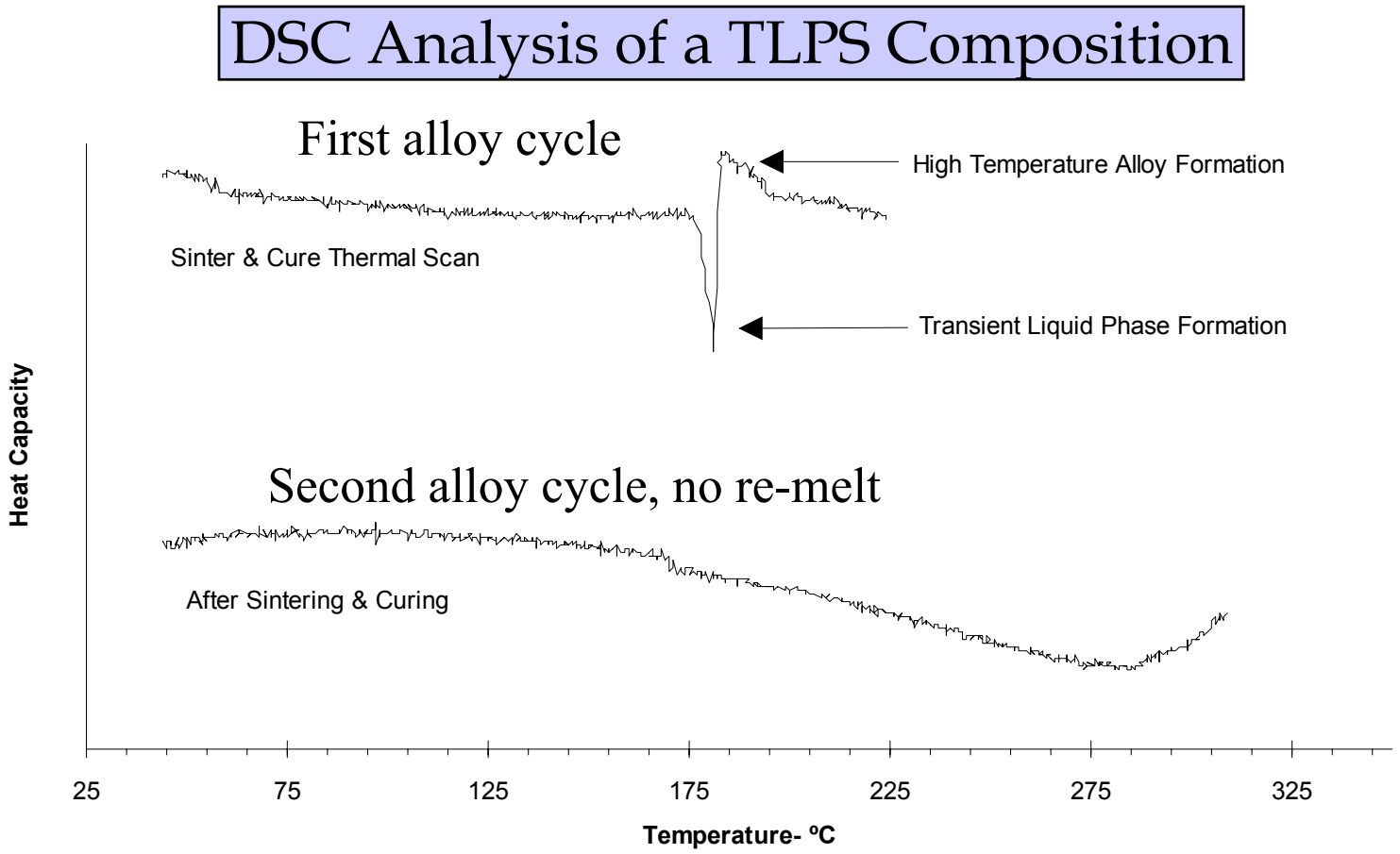
TLPS Composites: Conceptually

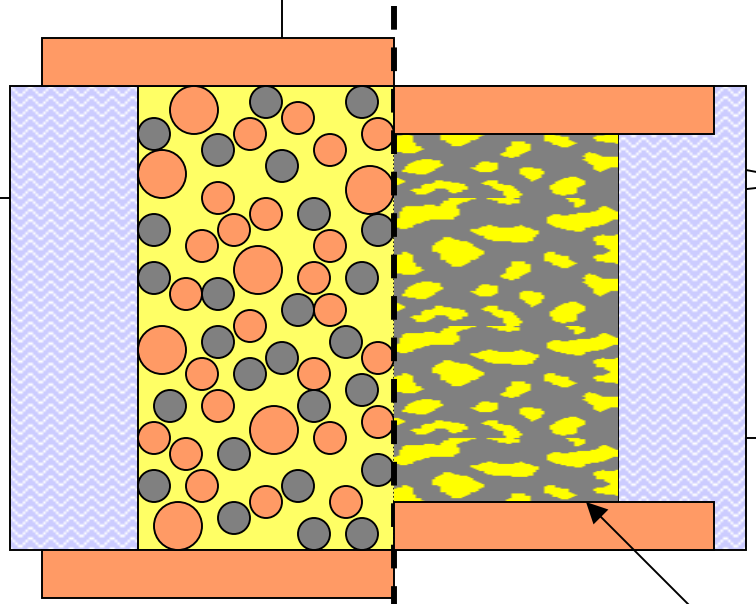


Conductor materials do not remelt - Transient Liquid Phase Sintering (TLPS)



TLPS Z-Axis Conductors

Paste joint is compliant during lamination



Paste solidly fills vias predrilled in dielectric /adhesive

Alloys to itself and pads

Hole sizes: 75 to 400 µm

Pad finish: copper, tin, nickel, gold, OSP, black/brown oxide

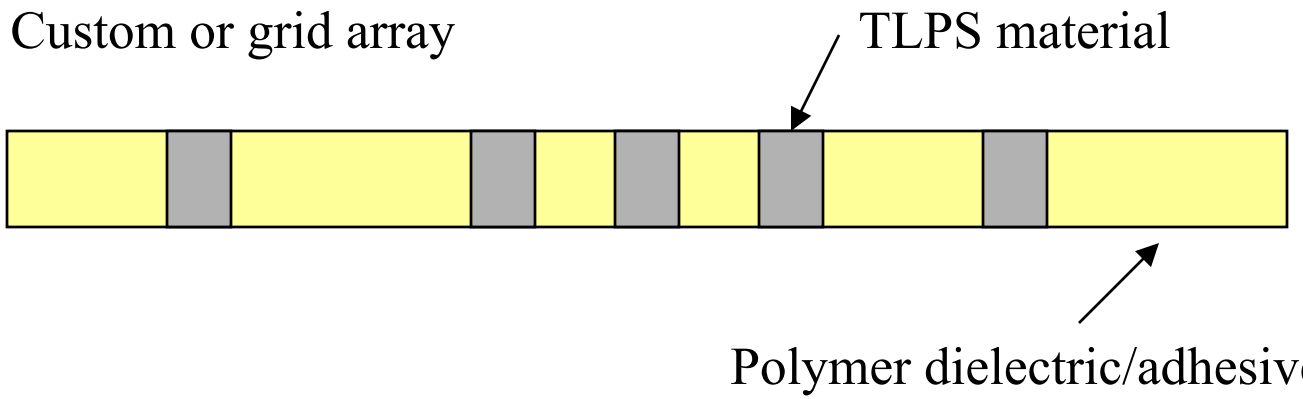
Align with circuits and laminate → Before

After

U.S. Patent No. 5,830,389

Unique TLPS Microvia Technology

A simple solution for layer-to-layer vertical interconnect



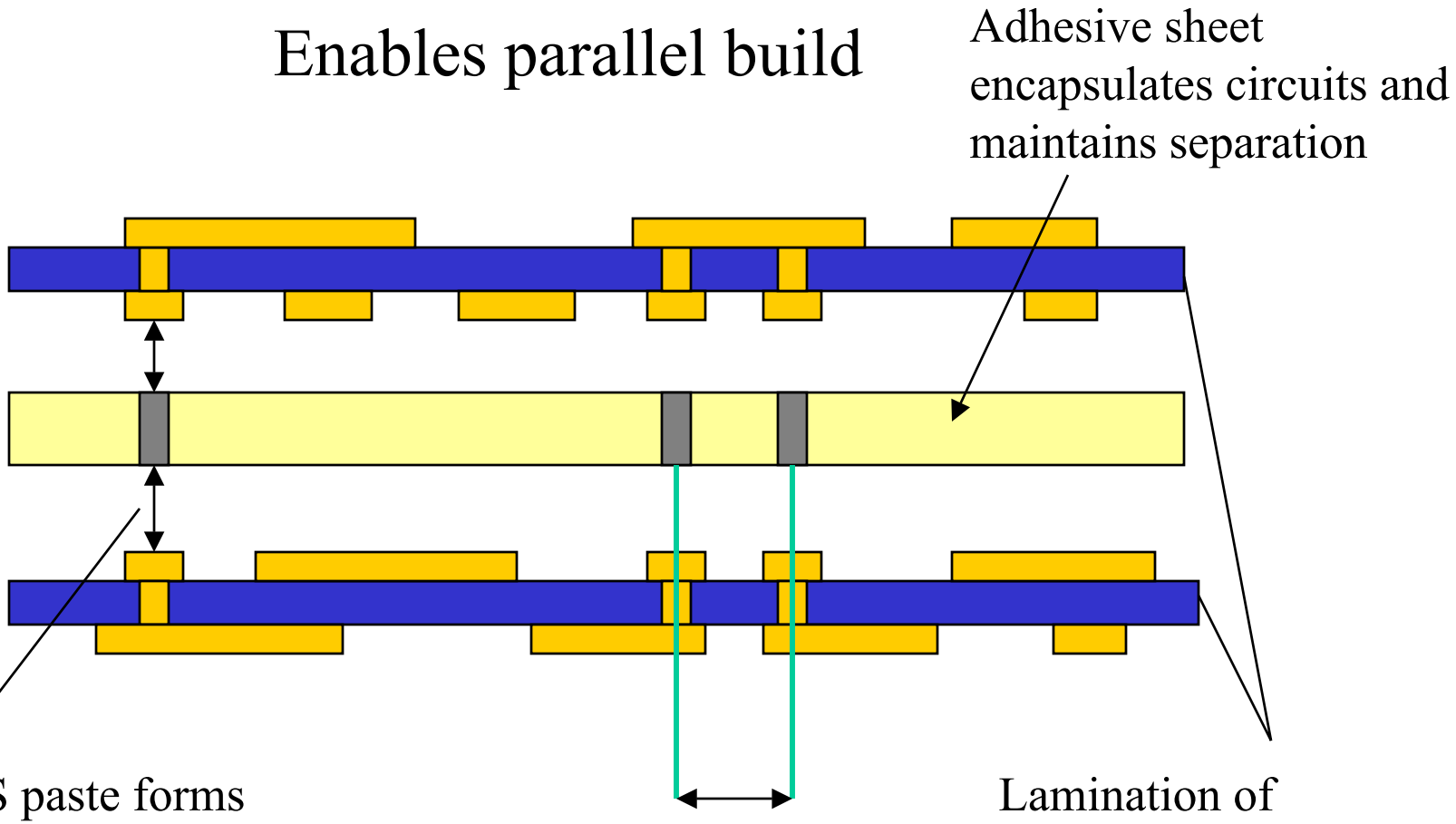
Connect:

- Conventionally produced double-sided circuits
- Dissimilar circuit types
- Dissimilar density circuits
- Double-sided flex circuits

U.S. Patent No. 5,948,533

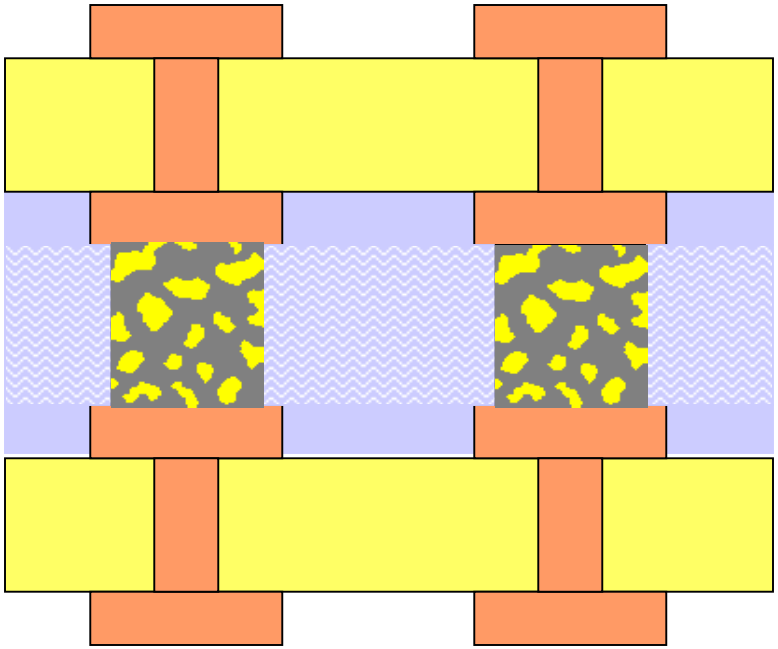
Unique TLPS Microvia Technology

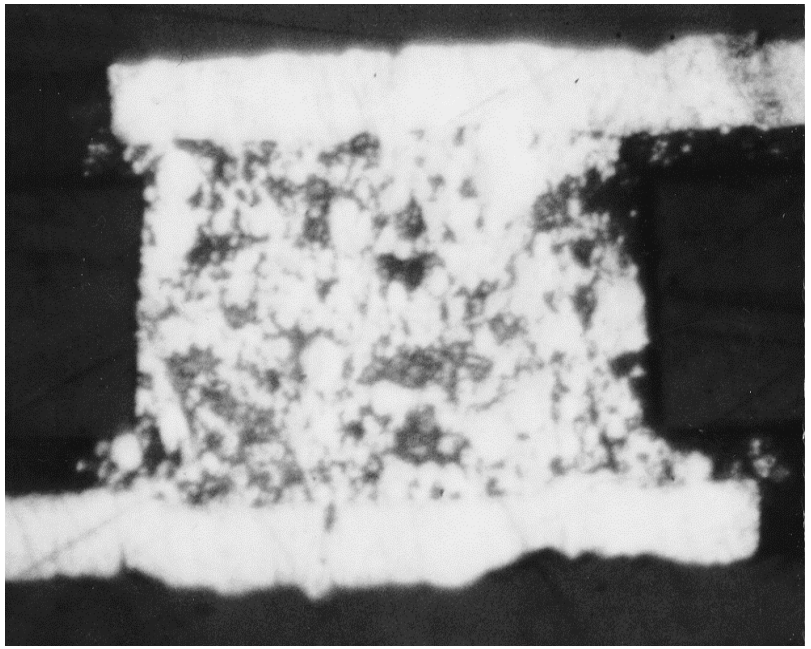
Enables parallel build



U.S. Patent No. 5,948,533

TLPS Composite Filled Bond-Ply

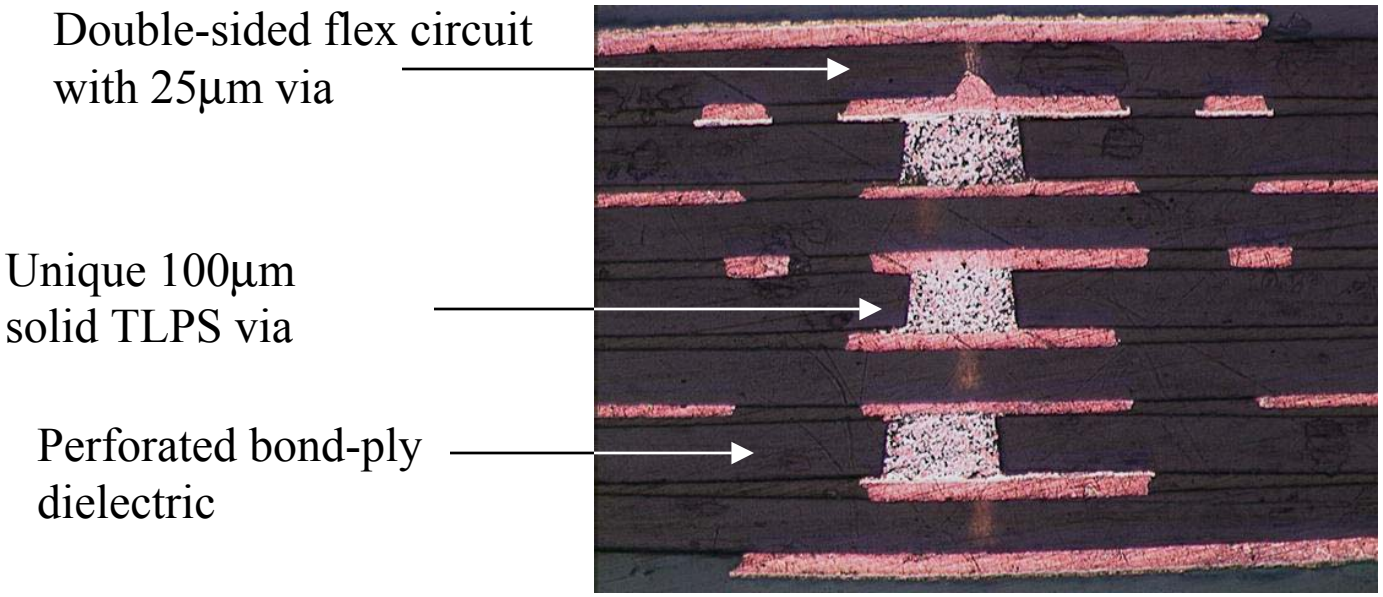




U.S. Patent No. 5,948,533

Advantages of this TLPS Microvia Technology

- Buried via layer-to-layer connections can be made at any location
- Via diameters range from75µm to 400µm (50µm feasible)
- Reliable, alloyed connection to the circuit pads



Cross-section of 8-layer multichip module

U.S. Patent No. 5,948,533

Reliability Results:

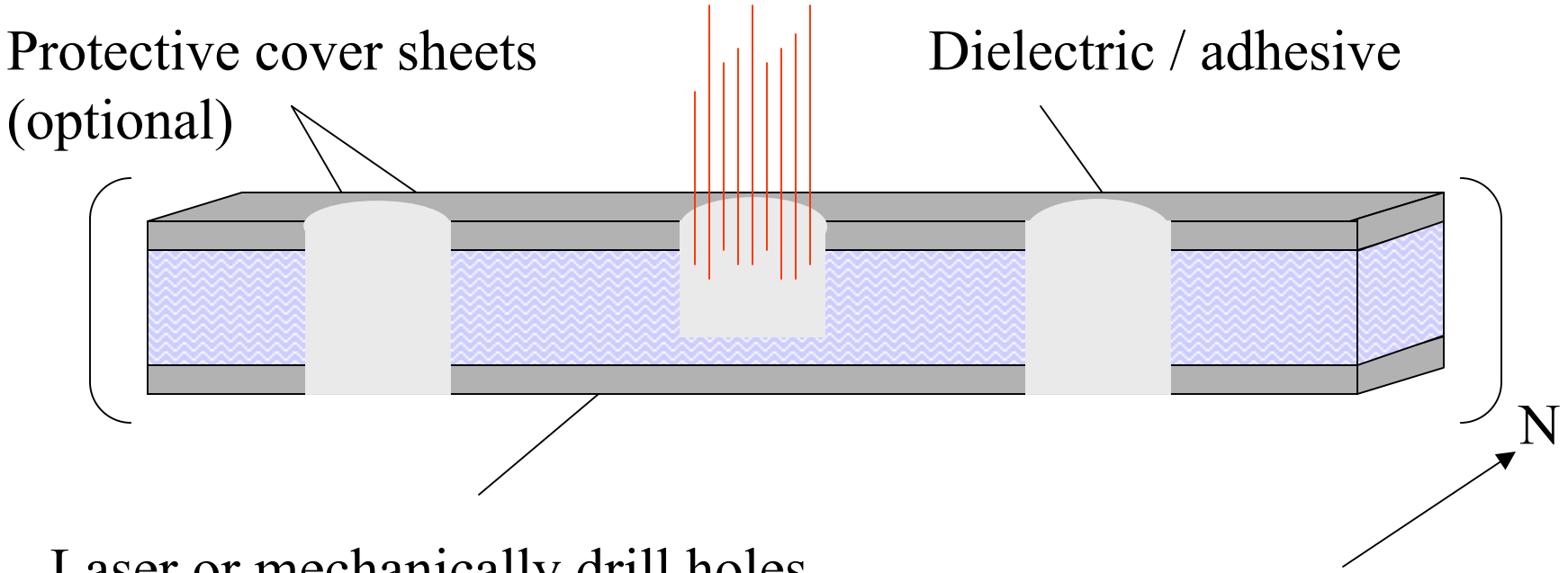
TLPS Filled Bond-Ply in Multilayer Flex Structures
(125 μm vias on 200 μm pads)

- Thermal Shock: Air to Air (-55C to +150C)
  - 100 cycles: Average ΔR = -0.9% (± 1.3%)
  - 480 cycles: Average ΔR = -2.4% (± 4.6%)
  - 1000 cycles: Average ΔR = -3.2% (± 3.2%)
- Humidity: 7 day, 85C/85 RH
  - 100 μm via in 4 layer: ΔR = 5% (± 8%)
  - 125 μm via in 6 layer: ΔR = 6% (± 20%)

U.S. Patent No. 5,948,533

Unique TLPS Microvia Process: Step 1

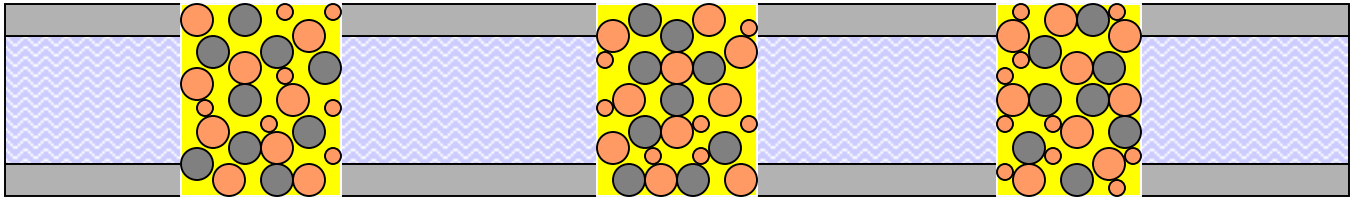
Prepare Dielectric / Adhesive Sheet



U.S. Patent No. 5,948,533

Unique TLPS Microvia Process: Step 2

Fill Holes with TLPS material



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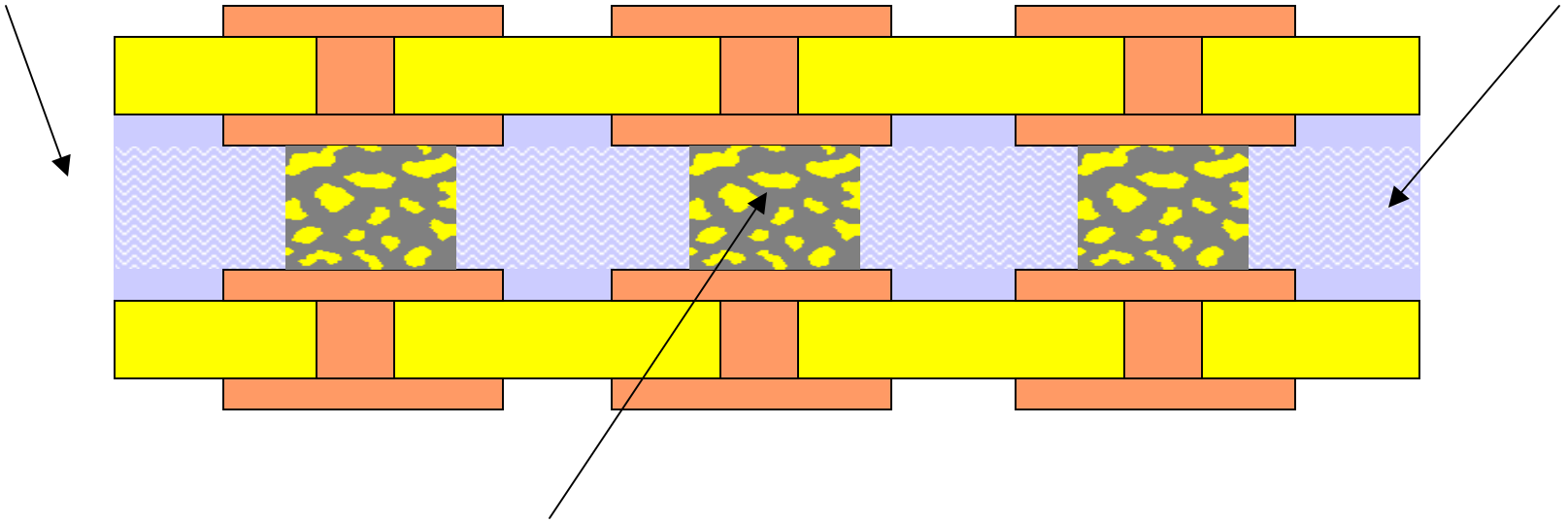
Unique TLPS Microvia Process: Step 3

Lamination

Protective sheets removed before lamination

Dielectric reinforcement maintains uniform separation

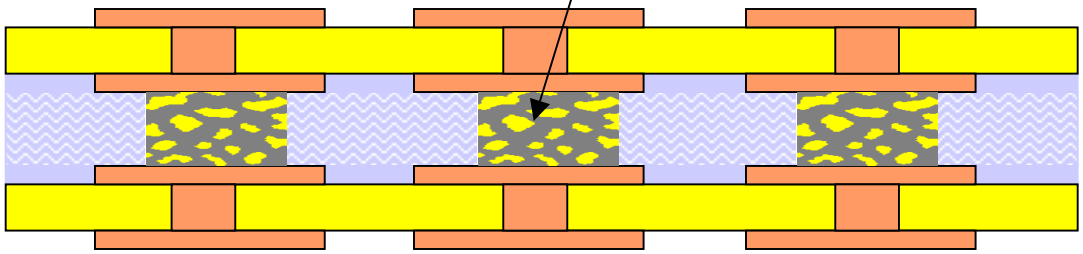


TLPS material co-processes under standard lamination conditions

U.S. Patent No. 5,948,533

Unique TLPS Microvia and FR4 PCE

TLPS material co-processes under standard lamination conditions



14-layer board made from seven 2-sided boards

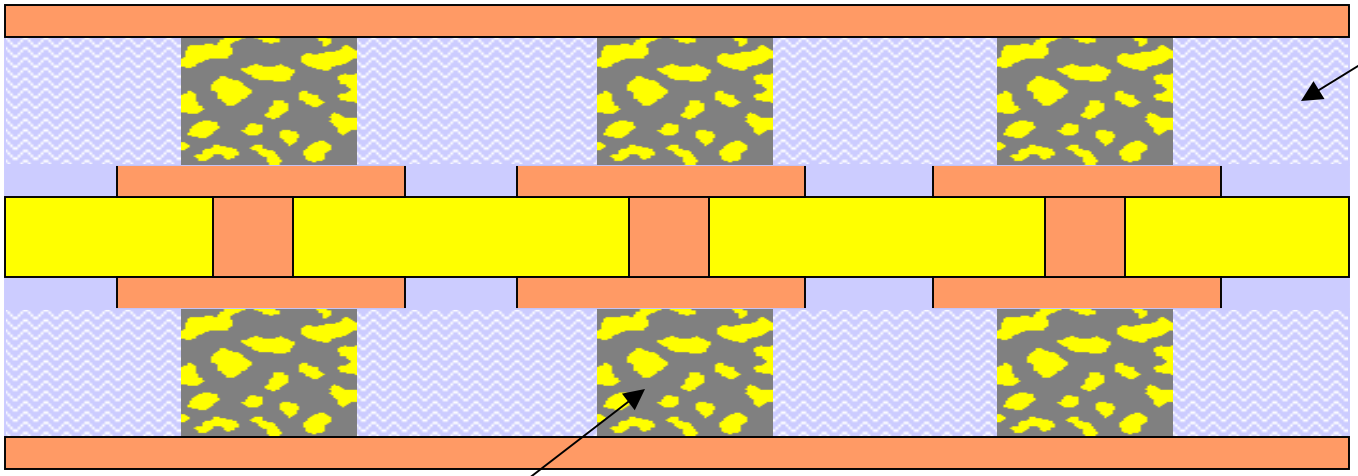
U.S. Patent No. 5,948,533

TLPS Microvia Process: Step 3 (alternate)

Lamination with Foil

Protective sheets removed before lamination

Dielectric reinforcement maintains uniform separation

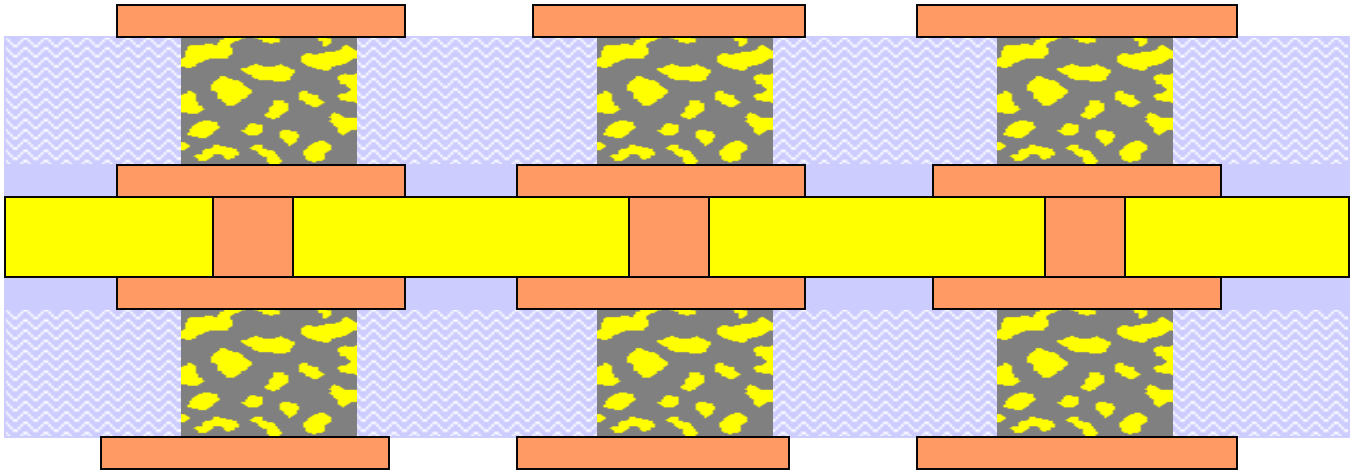


TLPS material co-processes under standard lamination conditions

U.S. Patent No. 5,948,533

TLPS Microvia Process: Step 4 (alternate)

Etch Foil



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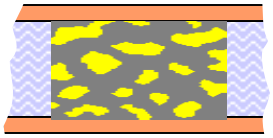
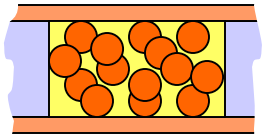
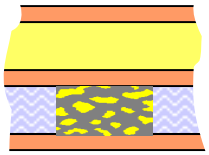
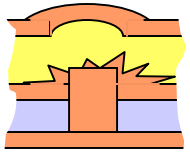
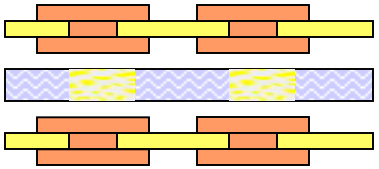
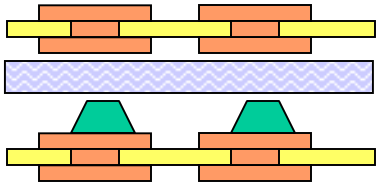
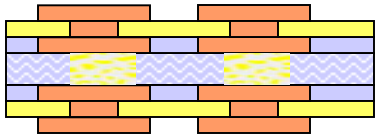
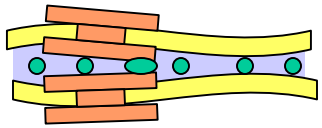
Unique TLPS Microvia Advantages vs. the Competition

TLPS Microvia	Others	TLPS Advantages
		Consistent and reliable alloyed connections - not just particle contact
		Compliant vias that won't 'punch through'
		Via layers fabricated in parallel with circuit layers
		Reinforced bond-ply gives consistent dielectric separation (However, TLPS is also compatible with single and dual stage RCFs.)

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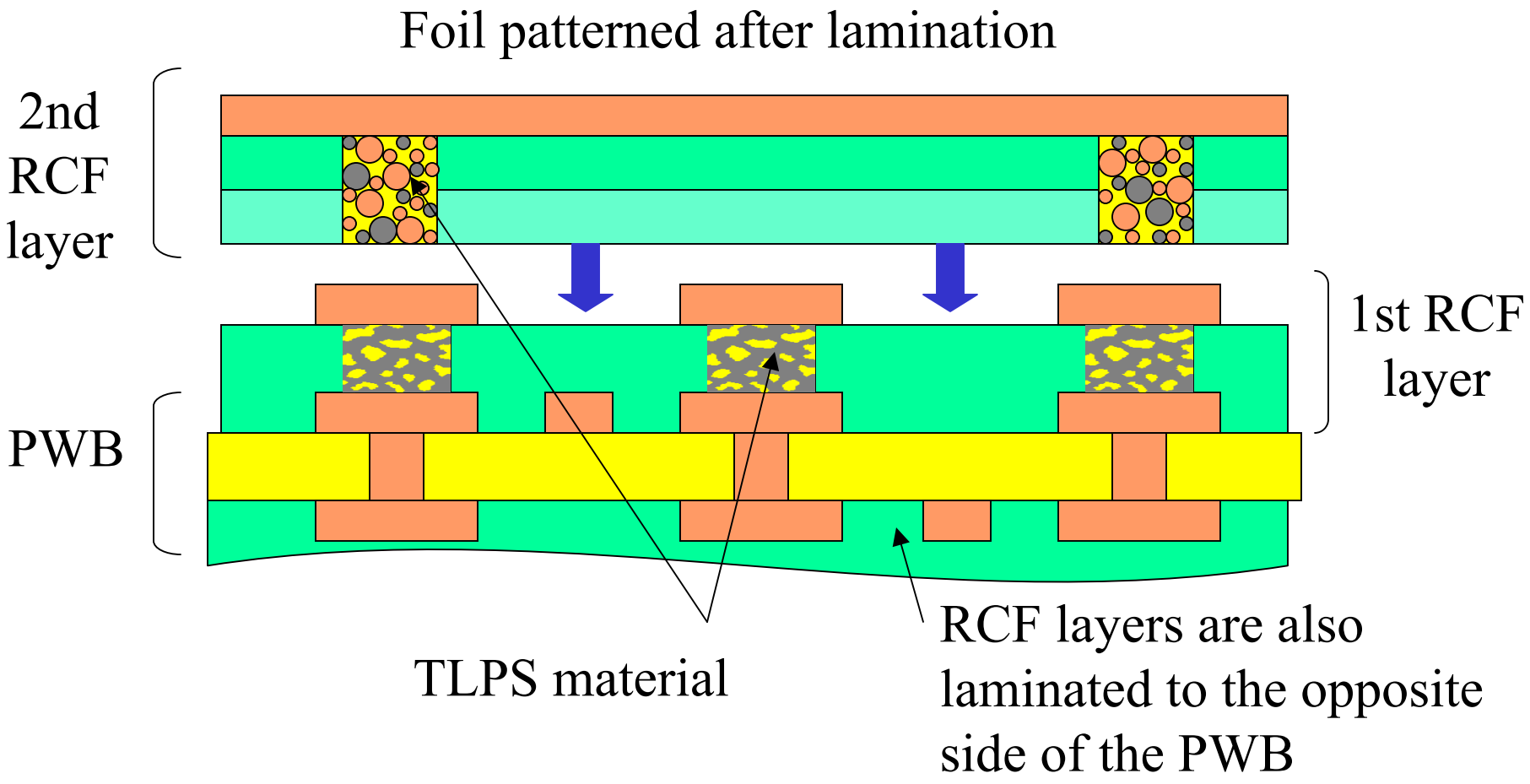
TLPS Microvias With Resin Coated Foils



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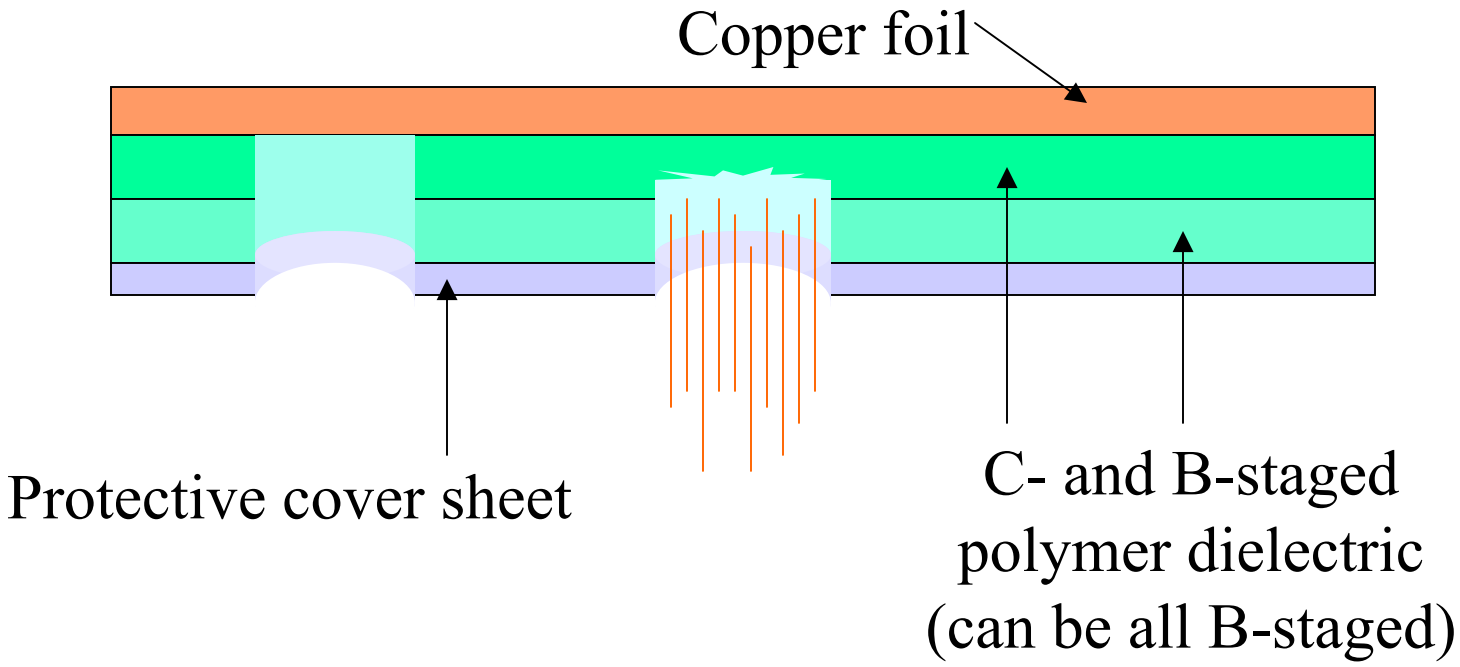
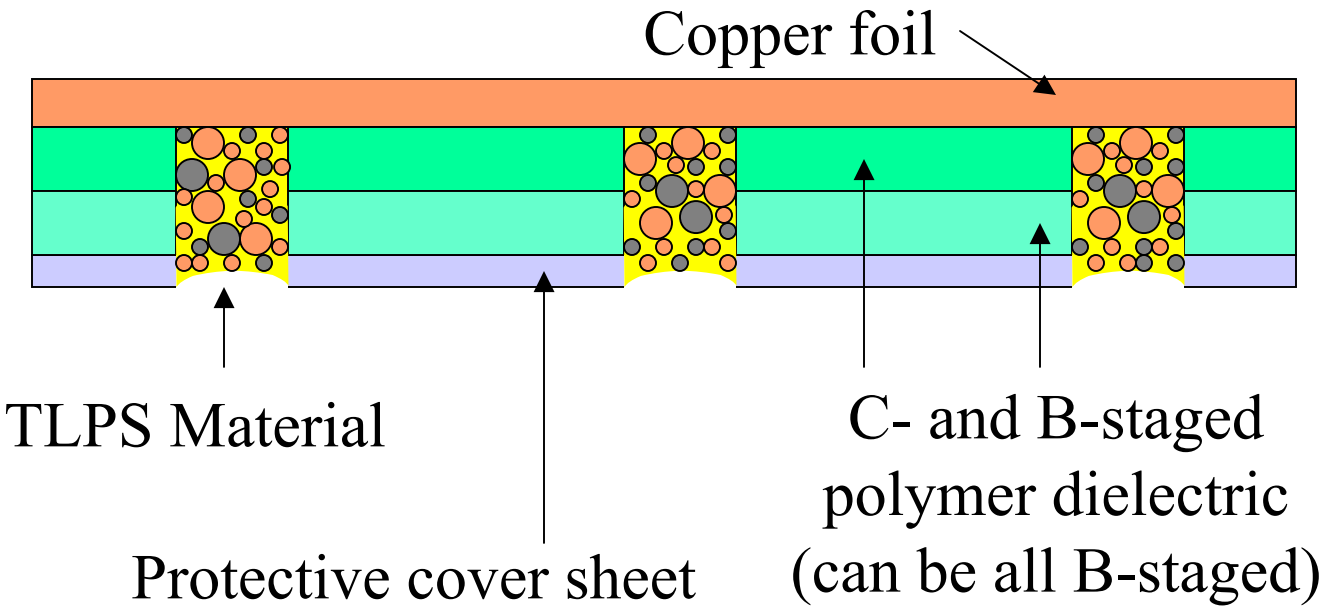
TLPS Microvias With Resin Coated Foils

Process step 1: Laser drill through polymer



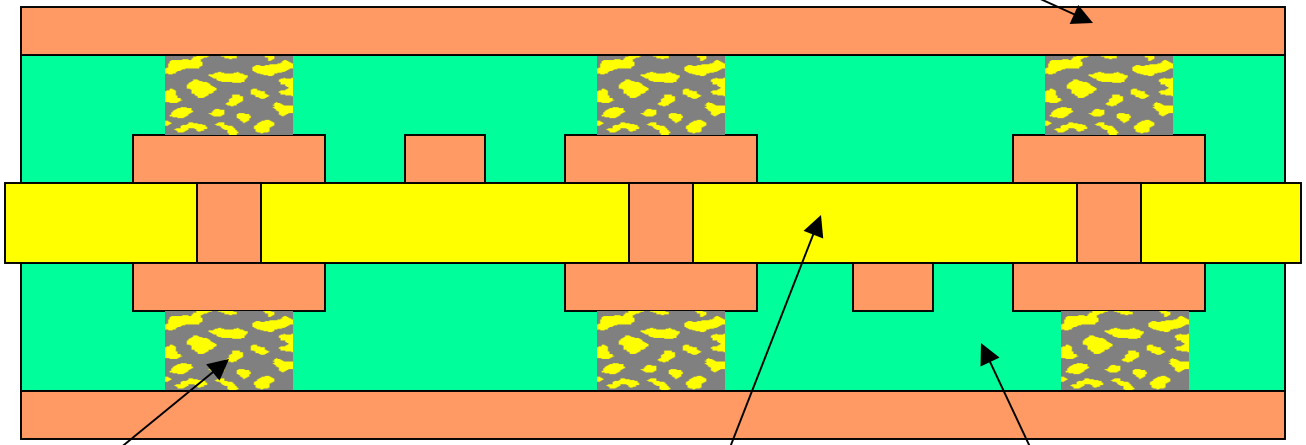
TLPS Microvias With Resin Coated Foils

Process step 2: Fill with TLPS Material



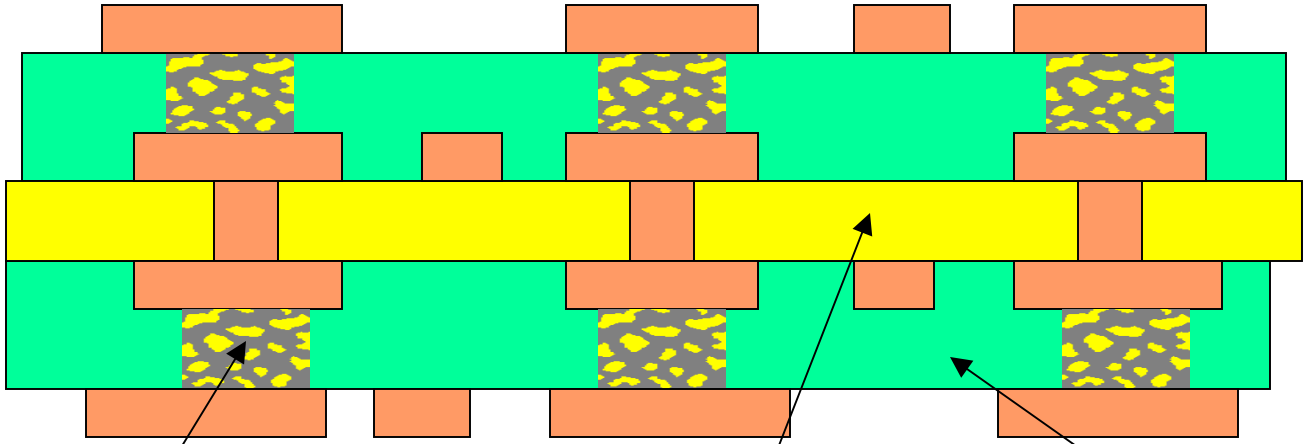
TLPS Microvias With Resin Coated Foils

Process step 3: Laminate to circuit board



TLPS Microvias With Resin Coated Foils

Process step 4: Etch copper circuit



Cured TLPS Material

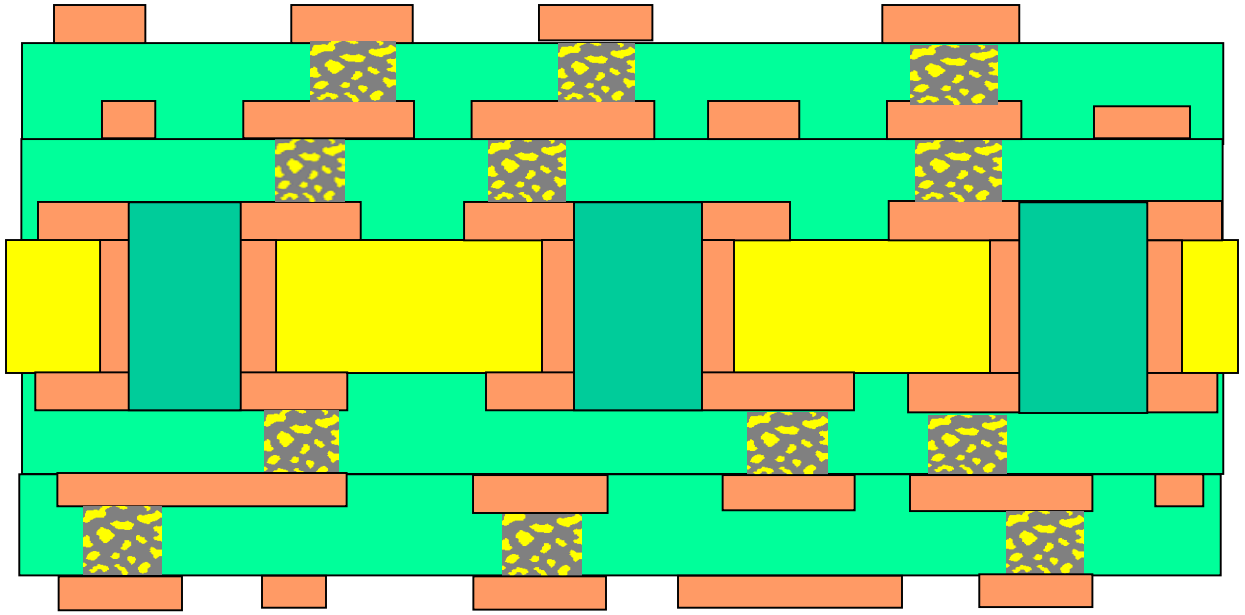
Double-sided PCB or double-sided flex circuit

Polymer dielectric

Repeat process steps 1-4 as required...

TLPS Microvias With Resin Coated Foils

2+2+2 Construction (PCB core)



Summary

- TLPS Microvia is a proven, reliable technology for HDI.
- TLPS Microvia has been adapted for compatibility with PCB materials and typical lamination conditions.
- TLPS microvias will not remelt and are alloyed to the capture pads.
- Solid TLPS microvias do not capture contaminants, do not distort outer layer topography, and can be stacked.
- TLPS Microvia is a patented technology currently available for specific application development and license.