Microvia PWBs Qualified for Avionics Microvias Can Enhance PWB Reliability

John Mather
Rockwell Collins
Cedar Rapids, IA

Lori Avishan
Merix Corporation
Forest Grove, OR

Abstract
Laser-drilled microvias are being added to the list of approved technologies for printed wiring boards destined for use in a rapidly increasing number of application types and environments. Microvias are frequently used on boards targeted for communication, test and measurement, and RF/microwave applications. The testing and results presented herein demonstrate that laser-drilled microvias are reliable for use in the aggressive environments experienced by avionics products.

Failure-free performance through 2000 temperature cycles is a Rockwell Collins guideline for printed circuit boards and assemblies intended for avionics applications. Reliability exceeding this requirement is established using temperature cycling as a test method, with results from plated through holes as a baseline. The test plan was comprehensive in scope, and independent variables included surface finish, hole aspect ratio, buried microvias and buried plated through holes, and 'microvia in pad' structures. Special consideration is given to evaluation of dielectric spacing less than the "3.5 mils minimum" typically required for avionics products.

Introduction
Microvias are an enabling interconnect technology. Compared to through-hole technology, microvias enable denser interconnect and broad freedom for double-sided parts placement, enhancing functional density and a compact form factor for products. Through-vias obstruct routing freedom on all board layers; the use of blind microvias reduces the number of through-vias with an accompanying improvement in available routing area. Additionally, the small pad size associated with blind microvias further improves available routing area and enables escape routing from dense, high I/O (input/output pin count) fine pitch components. One pair of routing layers connected by blind microvias provides an impressive amount of routing capacity. This routing capacity is a significant advantage for large, complex avionics assemblies having wide data buses serving a number of high I/O components. For critical signals, the blind microvia offers the advantages of low inductance and absence of an 'antenna effect' that might be associated with through vias.

Both sides of a printed wiring assembly for an avionics application are shown in Figure 1; its size and configuration are similar to the "Compact PCI" format. As is evident in the figure, this particular board design does not utilize high I/O devices or array packaging – the largest device is a 144-lead quad flatpack (QFP). However, microvia interconnect technology proved essential to its successful design. Because of the number of keep-out areas and a fixed connector location, the options for placing a number of physically large devices are limited. For this application, the key attribute of microvia technology is the ability to configure a board design that eliminates almost all of the through vias: this enables logical placement of devices according to the circuit "flow". It would not have been possible to obtain proper parts placement in the available board space if the components on the board's second side had to dodge the lands associated with an all through-via construction. A larger board profile is not an option, and space does not exist for additional cards. This is a real case where density is the bottom line, even though ultra-dense package I/O is not the challenge to be overcome. Adequate routing capacity and parts placement freedom are the two key attributes that microvia technology provided for this example.

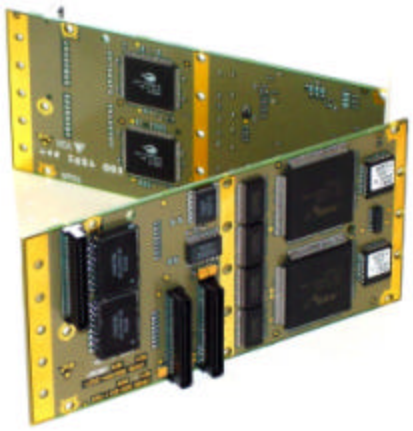

Figure 1 – Printed Wiring Assembly for Avionics Application

Productive utilization of microvia interconnect technology to create a PWB like the one shown above requires a few changes to traditional printed circuit design practice.

- Autorouting permits the best utilization of microvia design technology for complex avionics printed wiring boards: however, the autorouter tool needs to be tailored for technologies using a combination of blind vias, buried blind vias, through-vias and buried through-vias.
- There is a learning curve associated with beneficial operation of the autorouter application.
- Access for electrical test is another issue to consider: this must be deliberately designed into the printed wiring board, because the 'automatic' access to all circuits afforded by traditional through-via construction is not available in an aggressive microvia design.
- Traditional design practice for high reliability applications limits dielectric thickness to a minimum of 3.5 mils between metal layers. However, dielectric of 1.8-to-3.0-mil thickness is more appropriate for forming and metalizing microvias, and can result in smaller holes and lands that increase the space available for signal routing. Thus there is a need to understand the reliability/performance of 'thin' dielectric in various environments.

Establishing the Reliability of Microvia Printed Wiring Boards

General Approach

The reliability of this interconnect technology needed to be established before the technology could be utilized for avionics, military, and other applications requiring high reliability and long service life. Before boards could be designed, the combination of PWB design rules that provides the required performance had to be understood so the many benefits expected from this technology could be realized. The general test approach was to utilize various environmental tests to determine the reliability of the **interconnect boards**. No effort was expended to evaluate component attachment (solder joint) reliability because there is no reason to expect the behavior of solder-attached surface mount components to be any different for microvia boards than has been established for through-via boards.

Reliability test methods that were used in this test program included the following:

- Temperature cycling for evaluation of interconnect vias
- Component remove/replace actions to evaluate the ruggedness of microvias placed directly in component solder attach pads ("via-in-pad")
- Conductive Anodic Filament (CAF) biased humidity tests to ensure reliability of closely spaced blind vias and/or thin dielectric

As is discussed in detail below, the test design was broad and comprehensive, and test article variables included

- through vias and blind vias of various diameters
- three board thicknesses
- two laminate glass transition temperature (Tg) values
- two surface finishes
- various interior laminate thicknesses to provide a built-in basis for performance comparison

Test Board Design

Variables On Each Test Board

A photo of the circuit #1 side of the test board is shown in Figure 2. The image can be separated into four areas for this discussion.

- Section A contains the coupons used for dielectric withstanding voltage, moisture and insulation resistance evaluation, and layer to layer insulation resistance. A coupon developed by Merix specifically for conductive anodic filament (CAF) testing of microvias is used for the moisture and insulation resistance evaluation. These coupons are used to help determine the viability of thin dielectric layers.
- Section B contains the laser drilled blind vias and mechanically drilled through vias, for both the inner subpart and final board. Each set is connected in a daisy chain design for ease of electrical monitoring ("glitch detection") during temperature cycling evaluation. Through vias are an important part of this test program because their performance establishes a baseline for evaluating the blind microvia performance.
- Section C contains via-in-pad patterns. The ability to put a microvia in a component attach pad is a great space saver on the printed wiring board. Various component styles are solder reflow or hand solder attached in this area. The purpose of this section is to determine whether the assembly operation and/or the presence of a component lead/pin soldered directly to the blind via capture pad have a significant effect on the temperature cycling life of these structures. Note that comparing temperature cycling results from sections B and C provides direct assessment of the effect of solder attachment of components to via-in-pad structures.
- Section D is nearly identical to Section C. It was used to develop component assembly/repair/ replace methods for components that are solder assembled to the microvia-in-pad interconnect. This section permitted assessment of microvia interconnect reliability for cases where the microvias experience rapid, intense heating and/or mechanical abuse during solder joint touch-up or component removal and replacement.

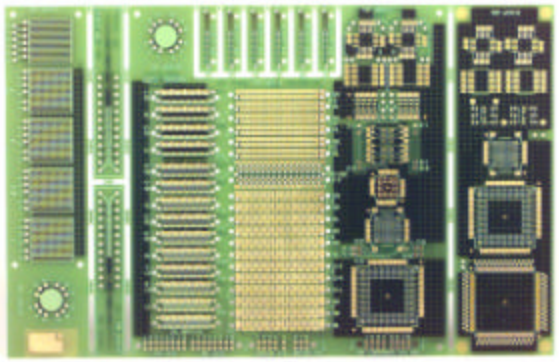

Figure 2 – Photo of Test Board, Viewed from Circuit #1 Side

A sketch depicting the cross section of an "n-layer" test board is shown in Figure 3. Note that the following structures are included in the design of the test board:

- Two layers of laser drilled microvias on both sides of the board.
  - A layer of microvias is produced on each face of the subpart, and they become buried within the final board.
  - A layer of microvias is produced on each face of the final board, connecting layers 1and 2 and n to n-1 respectively.
- Mechanically drilled vias in the subpart that become buried within the final board.
- Mechanically drilled vias through the entire board.

The original military printed wiring board design specifications and IPC-6012 default to a minimum 3.5 mils for dielectric thickness. In cases where the minimum dielectric thickness is not specified or when permitted by the customer, IPC allows thinner spacing. Often this is for parts designed to run at lower voltages. Thinner dielectric layers permit smaller diameter vias at the same aspect ratio. This is desirable since it adds flexibility in design. For this reason dielectric spacing is included in the test design. A minimum 3.5 mil dielectric spacing is used on one side of the board for both of the outer two layers. On the opposite side a single ply of 1080 prepreg is used on both of the outer two layers. For these test boards, the thickness of this 'thin' dielectric layer varied from 2.0 to 2.6 mils after lamination.

Microvias – Three sizes of laser drilled blind vias are tested on each side of the board. Since the dielectric spacing is different it is important to consider both diameter and aspect ratio. This information is shown in Table 1.

Table 1 - Microvia Sizes Tested and Corresponding Aspect Ratio

CALLOUT	SIDE 1 – TOP (3.5-mil minimum dielectric) SIZE IN MILS / ASPECT RATIO	SIDE 2 – BOTTOM ("thin" dielectric) SIZE IN MILS / ASPECT RATIO
Small	4.5 / 0.95	3.5 / 0.85
Medium	6.0 / 0.72	5.0 / 0.6
Large	7.5 / 0.57	6.5 / 0.46

For each microvia size a matrix of three pad sizes for both the target pad and capture pad are used in the test design. These are shown in Table 2 below. An 'X' in this table indicates pad/hole combinations that are tested in the subpart. A "✓" indicates pad/hole combinations that are tested in the outer layers of the finished board.

Table 2 - Microvia Landing and Capture Pad Sizes

Pad Diameter Over Microvia Diameter (mils)			
Microvia Diameter	+8	+12	+14
Small	✓,X	✓	✓,X
Medium	✓	✓	✓
Large	✓,X	✓	✓,X

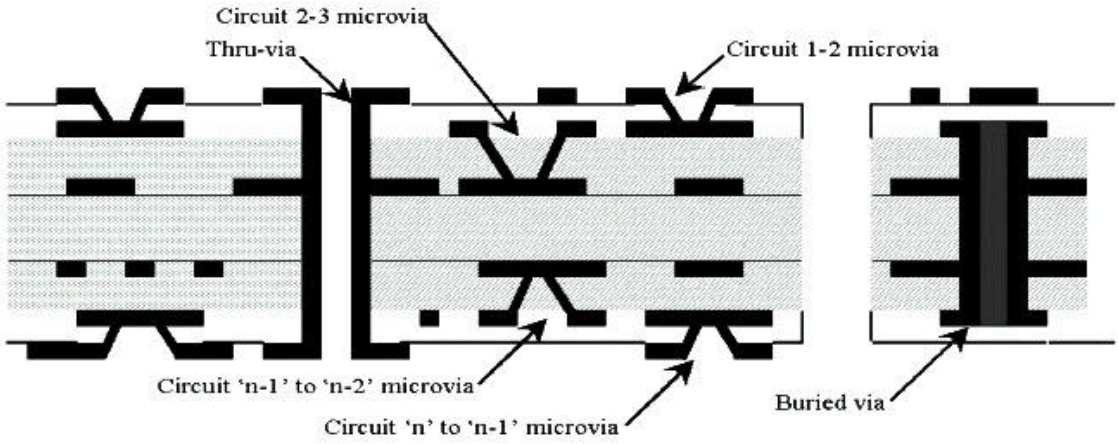

Figure 3 – Modified Microvia Type II Construction

Mechanically Drilled Vias - The test matrix for the mechanically drilled vias is shown in Table 3. The three smallest drill sizes represent typical small hole drill sizes for volume production of printed wiring boards having a thickness range covered in this test program. Although their diameters are close to each other, all three were intentionally included to determine whether there would be a dramatic shift in failure rate below a certain drill size. Additionally, because the failure mechanism for through vias typically changes from barrel fracture to post separation as hole diameter increases, the largest drill diameter is included to ensure both mechanisms are tested. As above, an 'X' in this table indicates pad/hole combinations that are tested in the subpart and a '✓' indicates pad/hole combinations that are tested in the finished board.

Table 3 - Mechanically Drilled Via Sizes Tested

Pad Diameter Over Drill Diameter (mils)			
Drill Diameter (mils)	+10	+12	+14
10	✓,X	✓	✓,X
12	✓	✓	✓
13.5	✓,X	✓	✓,X
18	✓,X	✓	✓,X
46	✓		

Panel Level Variables

- Full sets of test images were built of the constructions described above using 8, 10, and 12 total copper layers. This corresponds to final board thicknesses of 45, 62, and 80 mils. Layer count was intended to represent typical values for avionics boards of the tested thicknesses. The outer structures remained intact but the number of copper layers in the subpart was increased to raise the number of copper layers and overall board thickness. Copper layers in the center of the subpart were non-functional, but the copper content and distribution were representative of typical signal and plane layers, as appropriate.
- Sets were built with both Electroless Nickel / Immersion Gold (ENIG) and 'Hot Air Solder Leveled' (HASL) as a surface finish.
- It was also elected to build entire sets from both 135ºC T_g (min.) and 170ºC T_g (min.) fire retardant (FR-) epoxy resin systems.

In all, twelve (12) independent combinations of test variables are represented and as many as a dozen (12) test boards of each type were fabricated.

All production was built to meet IPC-6012 class III which specifies 1.0 mil minimum average copper plating in the plated through holes. For buried vias, IPC-6012 class III requires 0.6mil minimum average. Less plating at the subpart level results in less image transfer to the outer layers. Acceptance of less copper at the subpart level will permit flexibility in designs. All microvias are built and inspected to IPC-6016. This requires a minimum of 0.4mils of copper plating in the microvias.

Test Procedure and Results

Prior to any testing, the entire test board was subjected to thermal preconditioning, two convection heating cycles for solder attach of components to sections C and D, plus two cleaning cycles. Following component attach, Section A was removed for humidity related testing, and Section D was removed for process development. Sections B and C both underwent temperature cycle testing.

The impact of the independent variables on the PWB performance in the various tests are discussed below.

Temperature Cycling Performance

Temperature cycling is the dominant method for determining the 'ruggedness' of plated vias, and was used as the test method in this qualification effort. Test conditions for temperature cycling used temperature limits of –55º and +125ºC, a nominal ramp rate of about 10ºC/minute, and a dwell of about 15 minutes at each temperature extreme. Test data indicate ~63 minutes per temperature cycle.

Microvia Performance

Microvias are very rugged: they are substantially more reliable than through vias in temperature cycling. **NO** failures occurred in microvias built through the thinner dielectric construction (one ply of 1080 prepreg), regardless of material type or final finish. Microvia performance for this test is independent of material type and board finish up to 2000 temperature cycles. In addition, the range of pad and hole sizes tested here were not factors in microvia temperature cycling performance up to 2000 temperature cycles.

Three (3) microvia failures were detected and confirmed during the test duration of ~2000 temperature cycles. It is worth emphasizing that over 350,000 microvias were tested during this effort: the calculated failure rate is about 8 ppm. For reference, the 99% upper confidence limit for the defect level is computed to be ~28 ppm. The three failures were distributed across most variables, including buried and outer layers, ENIG and HASL finish, and two laminate types. An important observation is that the three failures occurred in the most aggressive condition: smallest hole diameter in the smallest pad size, and in the thickest dielectric selected for microvia evaluation. As will be presented in more detail later, the preferred construction uses thin dielectric for microvia layers, so the condition where the few microvia failures did occur is avoided.

This outstanding performance of microvias is superior to that of through vias, as is evident from the information below.

Through via Performance

The discussions in this section apply to drilled 'through vias' that penetrate the entire PWB thickness, or buried through vias that connect layers 2 through 'n-1' in an 'n-circuit' PWB.

Figure 4 summarizes the effects of three test variables on the temperature cycling performance results for through vias. The chart displays aggregate data for all hole/pad size combinations on a given 'category'. Each 'category' represents eight (8) test boards, and each board contains 1,140 tested through vias (9,120 vias per category). The plotted test variables are as follows:

- Board thickness (see RH side of graph): thin, medium, and thick.
- Material type: FR-4 with 135°C minimum Tg (left half of chart); and 170°C minimum Tg multifunctional epoxy (right half of chart)
- Finish: within each material type, half the board sets had HASL (hot air solder leveled) finish, and the other half had ENIG (electroless nickel immersion gold) finish.

The normalized data plotted in Figure 4 indicates the relative number of 'jumpers' that is applied to the test boards by the time 2000 temperature cycles had been experienced. The 'jumpers' are used to short across failed holes, to render the daisy chain continuous and functional so testing with the electronic 'glitch detection' system can continue. A jumper indicates an absolute failure, therefore, fewer jumpers are better.

For reference, the tallest (yellow) bar in Figure 4, which is associated with the 135Tg/HASL/Thick category represents a total of ~570 jumpers applied to the eight test boards (9,140 total through vias; ~6.2% failures). Alternately, the short yellow bar associated with the 170Tg/HASL/Thick category (typical of high reliability avionics designs) represents only eight (8) total jumpers applied to the eight test boards (9140 total through vias, ~0.09% failures).

The following trends/results are indicated by the graph.

- **High Tg boards performed better:** The vast majority of the jumpers were placed on boards made from FR-4 laminate having Tg ~ 135°C. Plated thru-holes in boards made from 170°C min. Tg epoxy laminate performed much better in temperature cycling than plated thru-holes in boards made from 135°C min Tg epoxy laminate.
- **Thinner boards are more reliable:** Most of the jumpers were placed on the thickest (0.080") boards. Small plated thru-holes in thin boards last much longer in temp cycling than small plated through-holes in thick boards.
- **ENIG finish is better than HASL:** For each board material type, the vast majority of the jumpers were placed on boards with HASL finish. Plated through-holes in boards with ENIG finish last much longer in temperature cycling than plated thru-holes in boards with HASL finish.
- Plated through-holes in **high Tg boards with ENIG finish** were virtually failure free in temperature cycling, for all thicknesses tested.

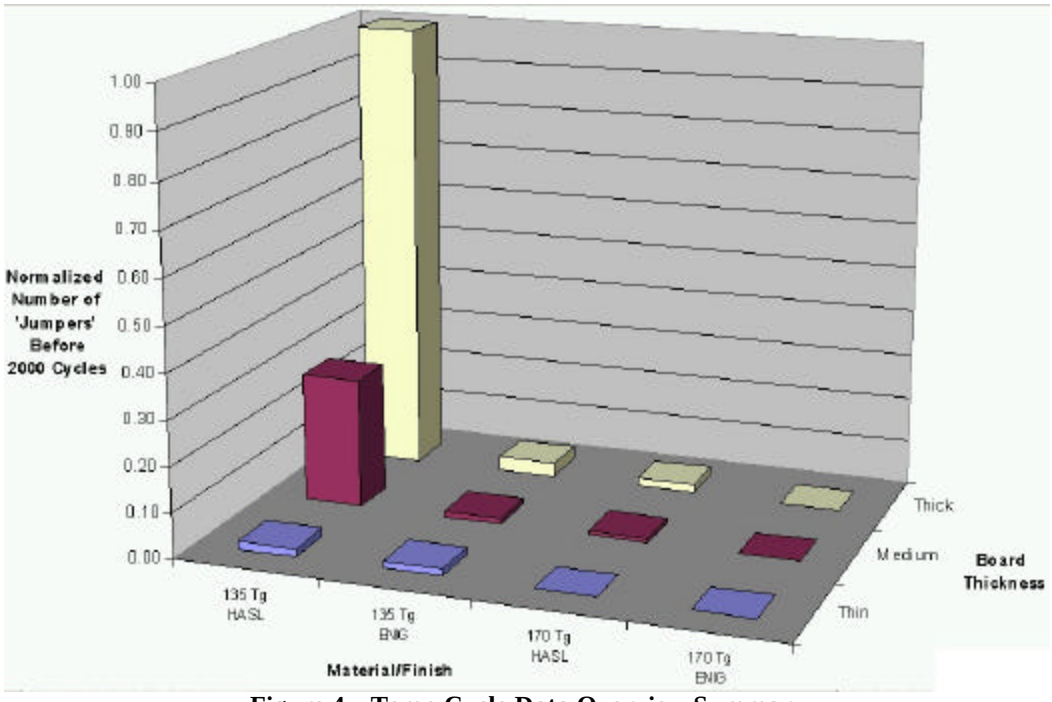

Figure 4 – Temp Cycle Data Overview Summary

For perspective, recall that the observed temperature cycling performance of microvias was essentially unaffected by laminate type and board finish, although these construction variables strongly affect through-via performance.

Conclusion: While through vias performed well (particularly those in 170 T_g boards with ENIG finish), microvias are substantially more rugged than plated through vias.

'Via-in-Pad' assessment
As discussed in section 2.2.1, two tests were performed to ensure that 'via-in-pad' constructions would be reliable. Microvias were placed in component attach pads on both faces of two coupons, and components were reflow solder assembled to both sides of selected boards. The test boards were then processed according to the flow chart illustrated in Figure 5 and discussed in the text below. The coupon area shown in detail in Figure 6 was detached from the right-hand end of each test board, and some of these coupons were subjected to component remove/replace operations to determine whether microvias are adequately rugged to survive "repair" actions. In all, 54 components were reworked: 28 components were removed without being replaced, and 26 components were removed and then replaced. These repair actions directly impacted ~6680 microvias across 30 coupons. Only one failure ("open") was detected as a direct result of the "repair" actions to the 54 components. It was concluded that microvias are not unusually failure prone as a result of typical repair actions.

To determine whether the repair actions **degraded** the microvias, all such coupons were placed in a thermal chamber and temperature cycled for 2000 cycles while being monitored for electrical opens using a "glitch detector". No failures (opens) were noted during this extended period of temperature cycling.

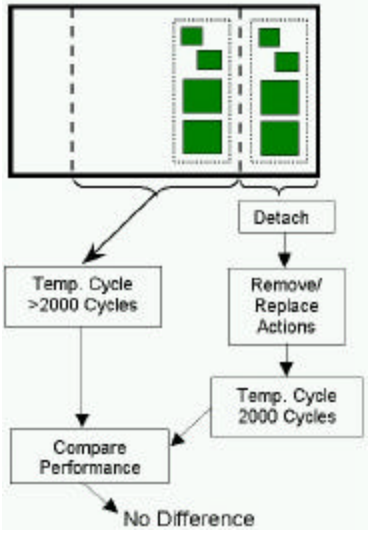

Figure 5 – Test Board Process Flow for 'Via-in-Pad' Assessment

Similarly, NO failures occurred in microvias of "preferred" configuration during temperature cycling of other areas of the test board, whether they were populated with components or not. It is concluded that microvias are adequately durable for via-in-pad structures.

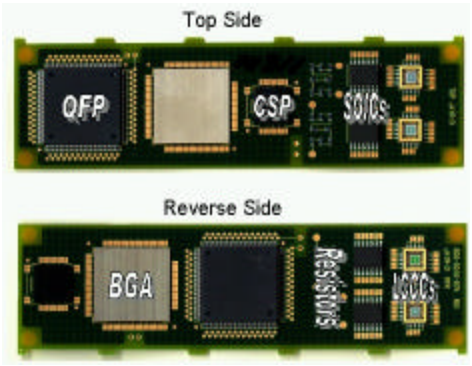

Figure 6 - Microvia Rework Coupons

Thin dielectric performance
Thin (~2-mil thick) dielectric facilitates microvia production, but is below the traditional 3.5-mil minimum used in avionics products. Accordingly, there is a need to understand the reliability/performance of 'thin' dielectric in various environments.

High voltage test
To evaluate performance under high voltage applications, coupons were tested per IPC-TM-650, 2.5.7, *Dielectric Withstanding Voltage*, Method B. The coupons followed the format of the standard IPC "E" coupon, shown in Figure 7. This coupon design allows a voltage bias to be applied across the dielectric between two traces 1) on the same circuit layer and 2) on adjacent circuit layers. A bias of 1000V is applied between the traces and held for 30 seconds. A coupon passes the test if a short does not develop between the biased features.

Sixteen coupons were tested in all, four from each of the four material and finish combinations. All the coupons passed this test.

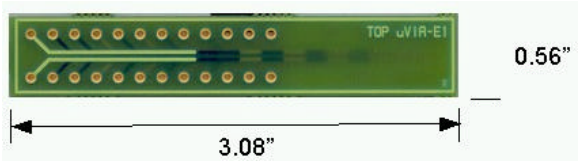

Figure 7 - IPC "E" Coupon

Biased-Humidity Test
In addition to the high voltage test (above), a Merix-developed coupon and test method was used to evaluate the acceptability of 'thin' dielectric layers and microvia structures. This biased humidity test employs a constant DC bias voltage of 8-to-10 volts per 0.001" (mil) and a 50°C/85%RH environment – conditions that are known to reveal printed wiring board 'weaknesses' that could result in functional failures during long exposure to typical

application environments. Coupon feature geometries were selected as appropriate for avionics printed wiring boards. A top view (Circuit 1) of the coupon is shown in Figure 8.

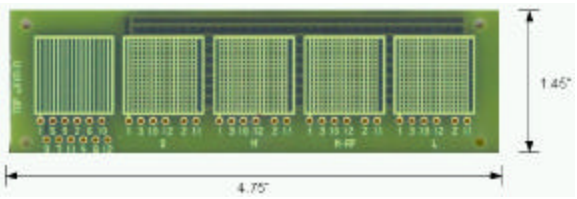

Figure 8 – Test Coupon, Top View

The first test pattern, at the left-hand end of the coupon, is used to evaluate z-direction (through the thickness of the board) performance of each layer of dielectric. There are no µvias or pads in this pattern. The series of lines is stepped down through every layer of the board, rotating 90-degrees with each successive layer so the lines appear crossed when viewed from Circuit 1. During the test, the circuit patterns on alternating layers were biased appropriate to the dielectric spacing.

The other four patterns were created to evaluate the likelihood of short circuits developing between adjacent, oppositely biased features as a result of resin or fiber bundle damage during the hole formation process. These patterns consist of appropriately sized microvias and related pads with relevant biasing circuitry, with each pattern representing slightly different feature (hole, pad) sizes consistent with the test design. A cross section sketch is provided in Figure 9 for reference.

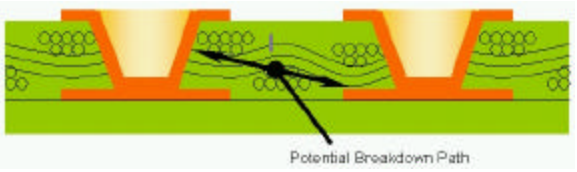

Figure 9 – Sketch of Potential Breakdown Path Between Adjacent Microvias

The DC biased coupons were exposed to the constant 50°C/85% RH environment mentioned above for a test duration of 20-plus days. An interface board was designed and incorporated into the test set-up such that periodic resistance measurements could be taken for each test pattern on each coupon. An ohmmeter was used to check the integrity of the dielectric between each pair of biased features. Thirty-two (32) coupons were placed on test. Data was collected from all coupons twice daily. An open circuit between features indicated no current leakage; if a measurable resistance was detected between features, that resistance was recorded and tracked.

Of the 800 sites that could be monitored, only one site failed to meet our acceptance criteria. This "failure" occurred in a non-preferred construction: NO failures occurred in microvia layers using the 'one ply of 1080 prepreg' construction. Similarly, no failures occurred in the z-axis test patterns.

The biased-humidity test did not reveal a significant difference between the two laminate materials or between the two final finishes. "Thin" dielectric as defined herein is considered reliable and acceptable for use in avionics applications.

Conclusions

It should be evident from the foregoing that the test design was quite broad, and comprehensive in scope. The test variables include material type, surface finish, hole diameter, hole aspect ratio, via-in-pad technology, and dielectric spacing. Microvias and plated through holes are produced and tested in the same coupons, and their performance is compared across all relevant conditions. The conclusions presented here are based on temperature cycling of >350,000 microvias and > 105,000 through vias for over 2000 temperature cycles.

Microvias are **very** reliable. Only 3 failures were found in the 350,000 microvias thermally cycled. This is a calculated failure rate of only 8ppm. The three failures **do not** correlate to material type or surface finish included in this test.

By contrast, through via failure rate **does** correlate to material type **and** to surface finish used in this test. Using the 'thick' board data as an example, the total number of jumpers applied was:

- ~570 (~6.2%) for the 135Tg/HASL category;
- ~8 (~0.09%) for the 170Tg/HASL category; and
- 0 (0%) for the 170Tg/ENIG category.

These failure data followed traditional, expected patterns. Fewer failures were seen in test coupons having 1) higher Tg laminate material, 2) ENIG surface finish (vs HASL), 3) thinner board thickness, and/or 4) lower hole aspect ratio. Although through via temperature cycling performance was very good for certain constructions, the results from this test program demonstrate that the life of the circuit board will be determined by the through vias and not by the microvias.

Microvias are rugged even when used in via-in-pad structures. Microvias were placed in component attachment pads, and components were solder assembled to those sites prior to temperature cycling. One set of coupons went through a component attach/remove/replace rework process. No failures were found in either set of coupons during 2000 temperature cycles.

Thin z-axis dielectric spacing, defined as a prepreg layer reinforced with a single layer of 1080 glass, is considered reliable and acceptable for use in avionics applications.

Thin dielectric spacing is evaluated in three ways

- Dielectric withstanding voltage per IPC-TM-650
- Biased humidity testing using a proprietary coupon designed by Merix Corporation.
- Extended temperature cycling of multiple microvia test structures that had << 3.5 mils of z axis dielectric spacing.

During these tests, only one failure site was documented, and it did not contain the thin dielectric.