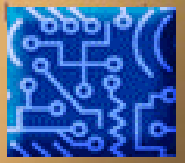
Microvia PWBs Qualified for Avionics

…….Microvias can enhance pwb reliability

John Mather Rockwell Collins
Lori Avishan Merix Corporation

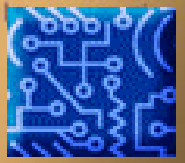
11/2002



Technology Drivers

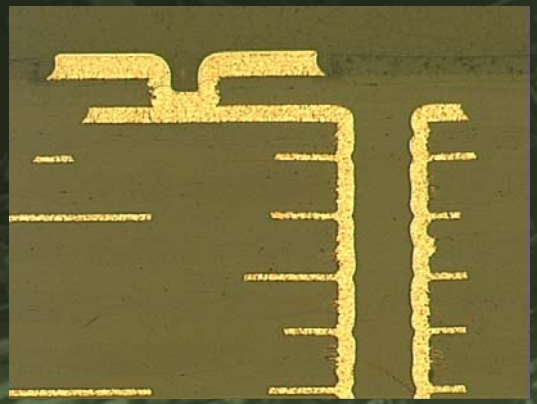
Microvias are an ***enabling*** interconnect technology

- Improves available routing area and enables escape routing from dense, high I/O fine pitch components
  - large BGA packages
  - required for .5mm BGA packages
- Reduces form factor (size and weight)
- Increase functionality in the same form factor
- Allows freedom in design
- Alternative to sequential blind vias.

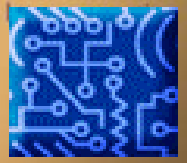


Fundamental Questions

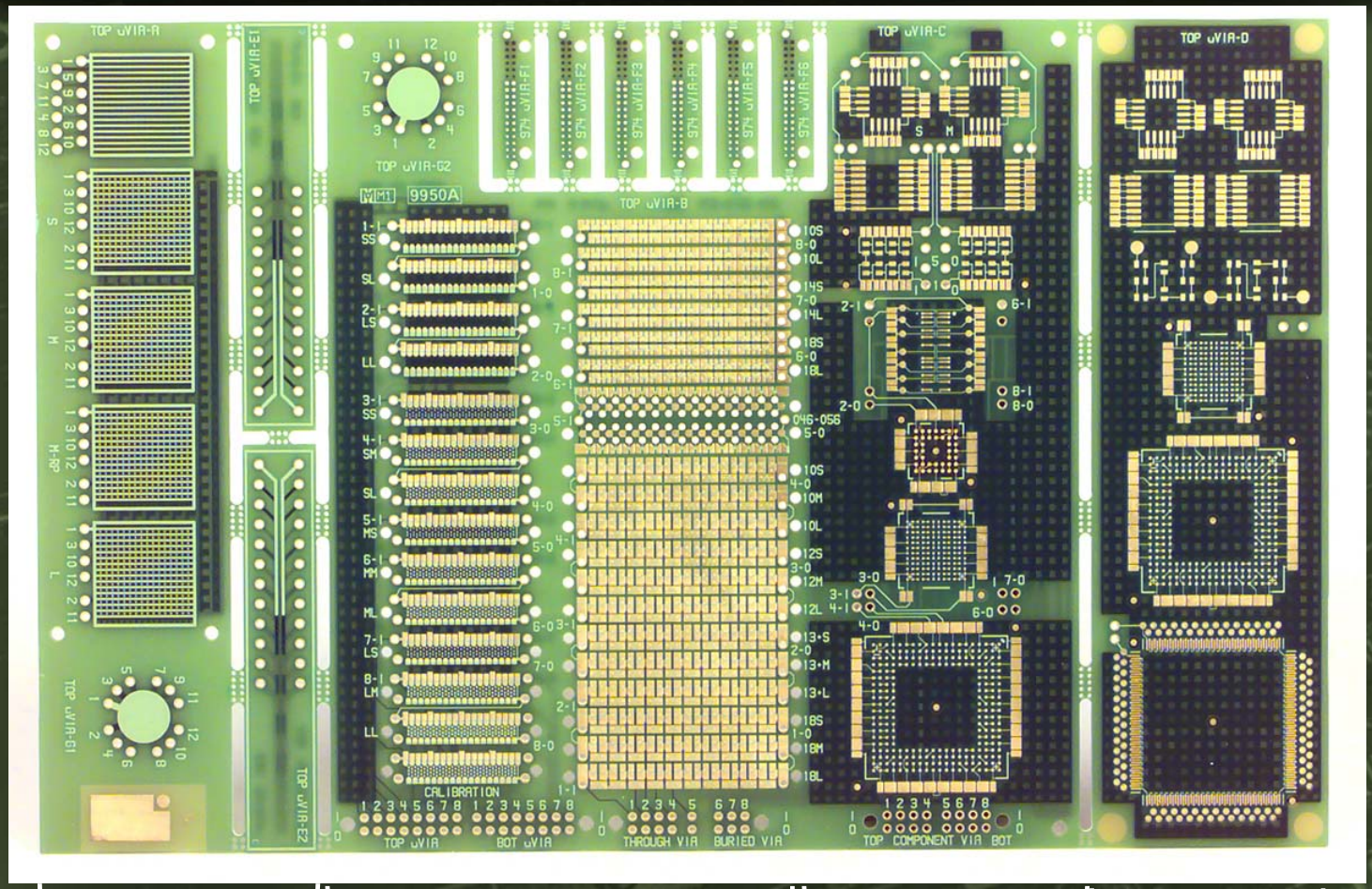
- Two Key Questions
  - Are microvias suitable for use in avionics?
  - Are closely spaced blind vias and/or thin dielectric OK?



- **Test Design**
- Test Results



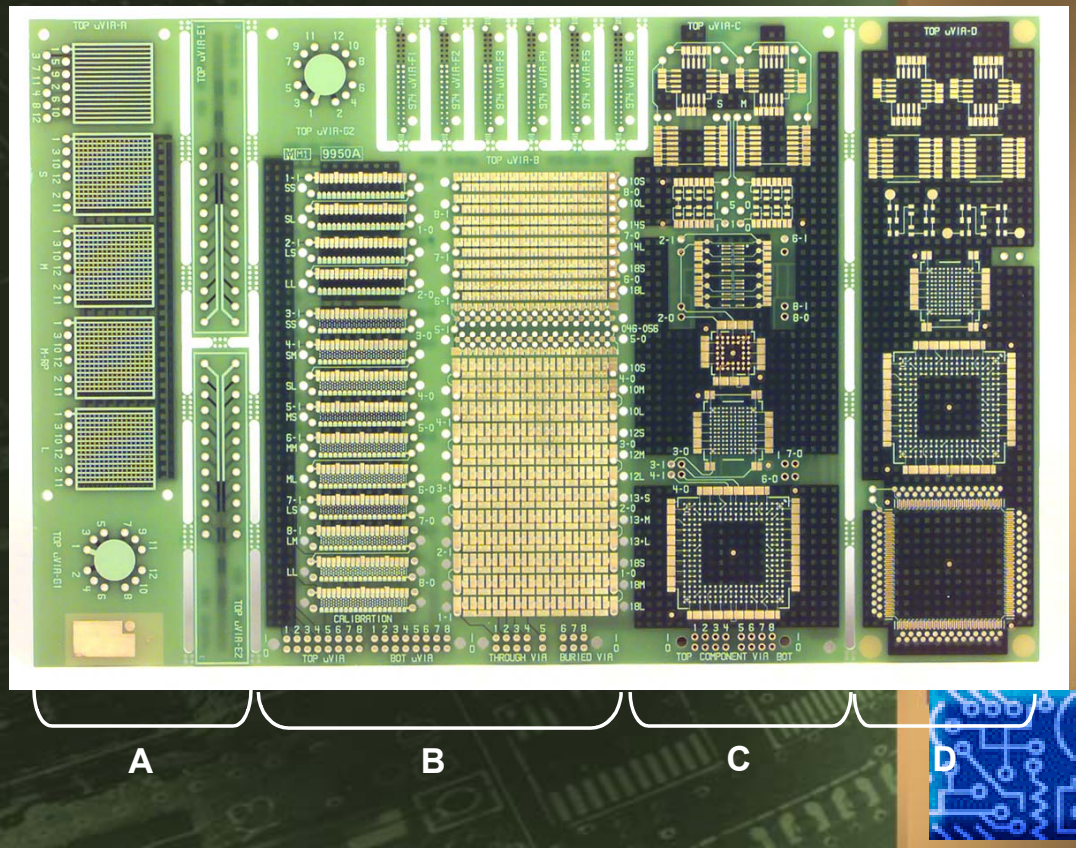
Microvia Test Board



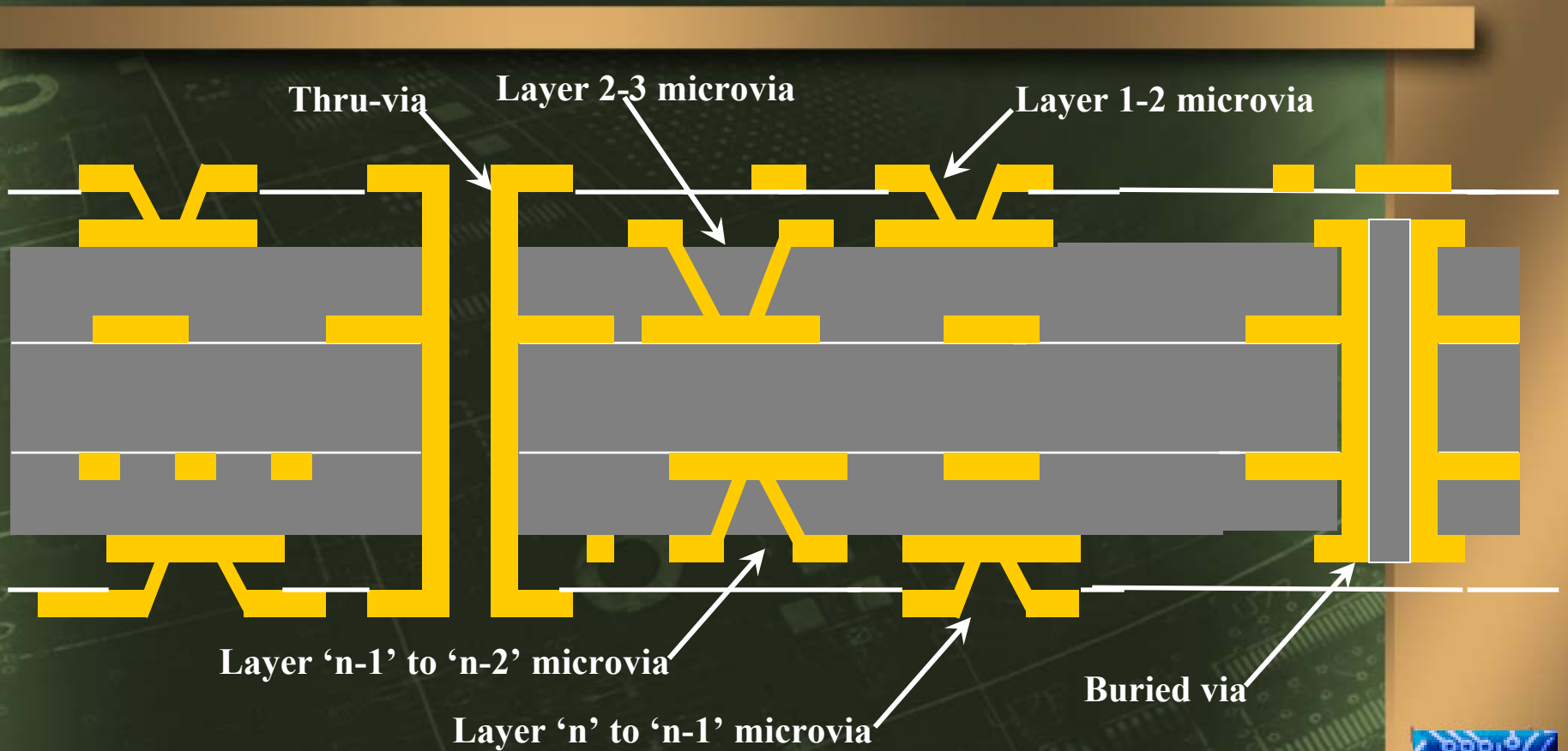
A B C D

Test Board Design

- **Section A**
  - CAF, dielectric withstanding voltage,
    moisture and insulation resistance
- **Section B**
  - laser drilled blind vias and mechanically drilled through vias, for both the inner subpart and final board
- **Section C**
  - via in pad patterns
- **Section D**
  - via in pad patterns for evaluation of component assembly/repair/replace

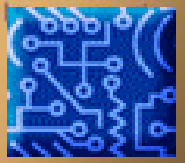


Test Board Construction



Test Variables

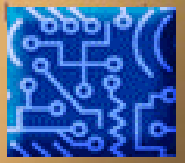
- Board Thickness / Number of Cu Layers
  - 0.045”/8 layers; 0.062”/10 layers; 0.080”/12 layers
- 2 Dielectric thickness selected for microvia formation
  - Overall aspect ratio ranged from 0.95:1 to 0.45:1
- Material
  - 130°C Tg FR-4; 170°C min Tg FR
- Surface Finish
  - HASL and Electroless Nickel/Immersion Gold



Test Variables (cont'd)

- Via type
  - Mechanically drilled thru via (1 to n)
  - Mechanically drilled buried thru via (2 to n-1)
  - Lasered blind via (1 to 2 and n to n-1)
  - Buried lasered blind via (2 to 3 and n-1 to n-2)
- Via diameter
  - 3 lasered via diameters - smallest is 3.5 mil
  - 5 mechanically drilled via diameters - smallest 9.8 mil drill
- Pad diameter: three per via size
- For drilled vias:
  - Some with pads on all layers
  - Some with pads on selected layers only

- In all this represents a total of
  - 12 panel level independent combinations.
  - 6 variables within each panel



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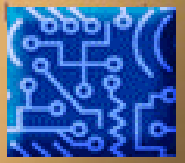
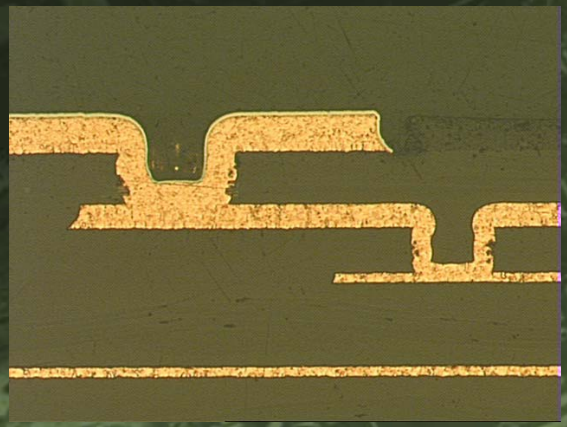


Microvia Interconnect Technology

- Two Key Questions
  - Are microvias RUGGED?
  - Is thin dielectric OK?
- Test Board Design Ensured an Answer
  - Numerous features/variations
  - Including ‘traditional’ features provided basis for comparison



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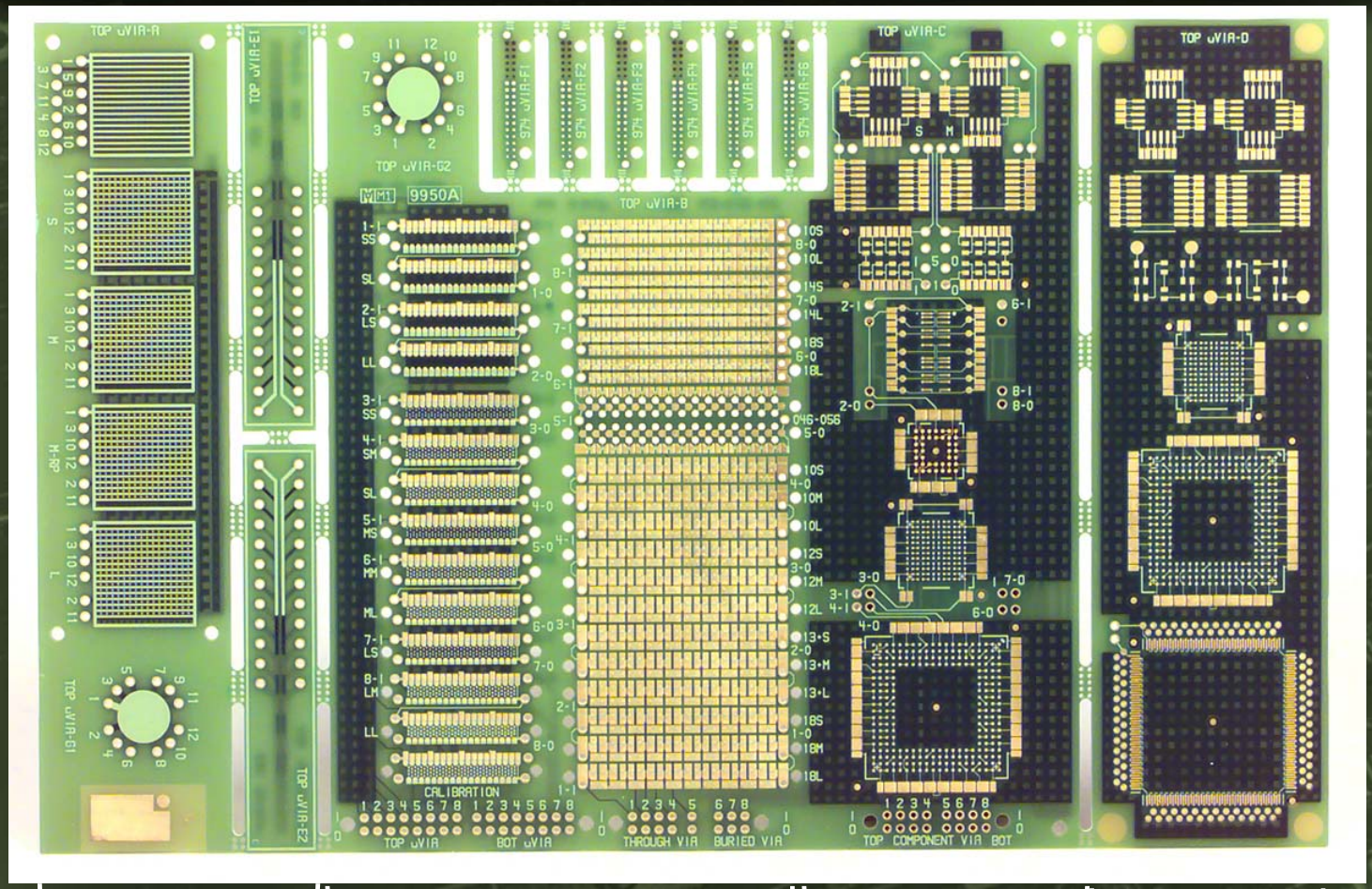
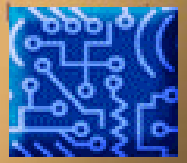


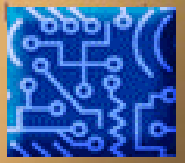
Temperature Cycling

- Used to establish via ruggedness
- Microvias and through vias tested together on same board
- Numerous variables, replicates
  - >350,000 microvias tested
  - >105,000 through vias tested
  - Various board thicknesses, via diameters, board finishes

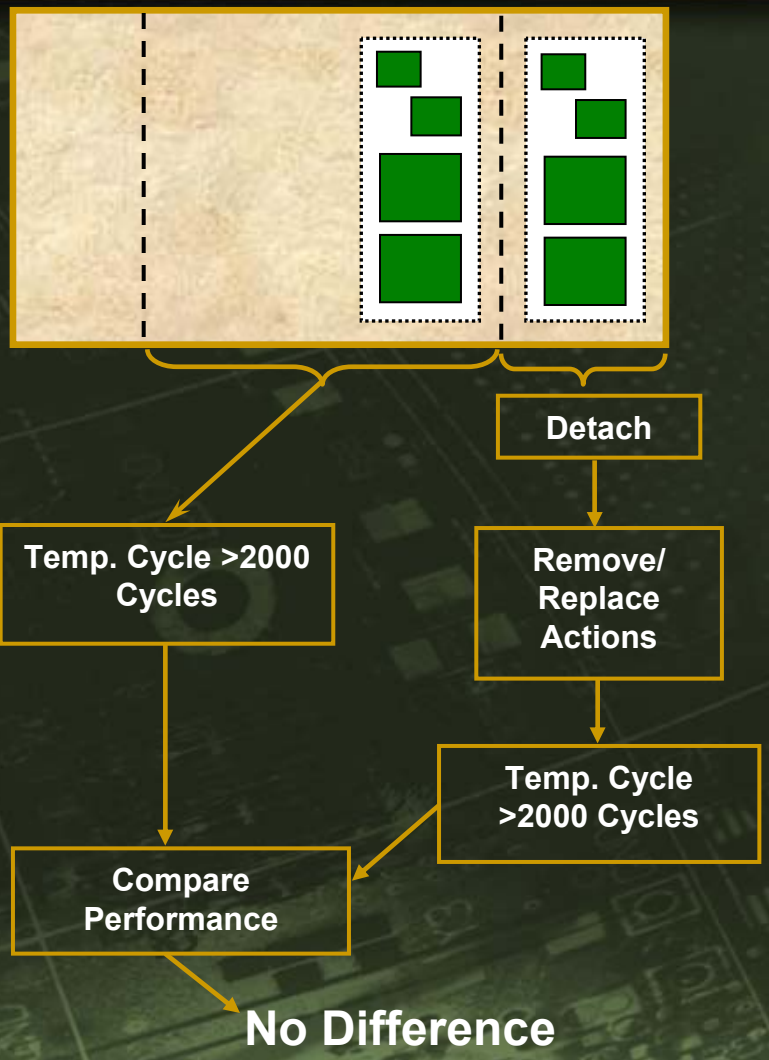


Microvia Temp Cycling Results

- Merix-fabricated microvias are **VERY** reliable
- Three (3) failures through 2000 temp cycles (3 out of >350,000 $\cong$ 8 ppm)
- Failures **DO NOT** correlate to finish or material type
- No failures in via-in-pad structures
- No confirmed failures following component remove/replace actions



Evaluating Via-In-Pad Structures



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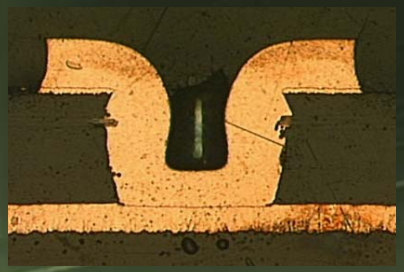
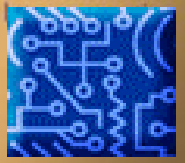
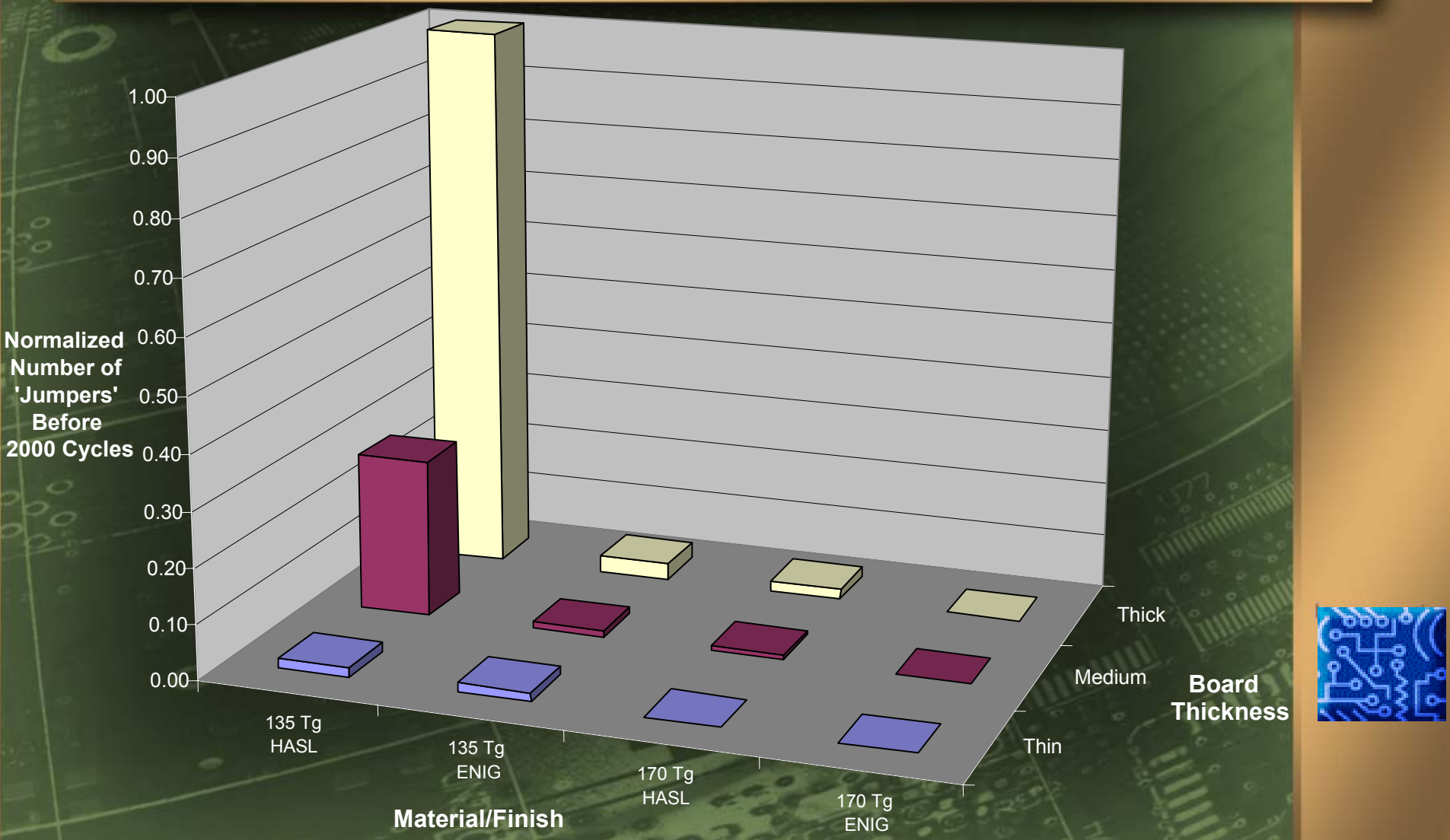


Through-Via Temp Cycling Results

- Numerous failures noted through 2000 temp cycles
- Failures DO correlate to material type and surface finish.
  - Fewer failures in higher Tg laminate
  - Fewer failures with ENIG (vs HASL) finish
  - Fewer failures with thinner boards
  - Fewer failures with lower hole aspect ratio



Through Via Temp Cycle Summary



Through-Via Temp Cycling Results

- Example from “Thick” board performance
  - ~570 (6.2%) jumpers applied to 135°C Tg/HASL
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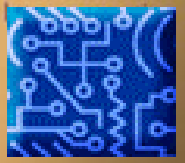
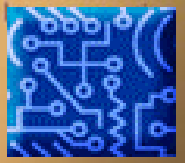
- PWB temperature cycling life will be determined by the through vias, not the microvias!



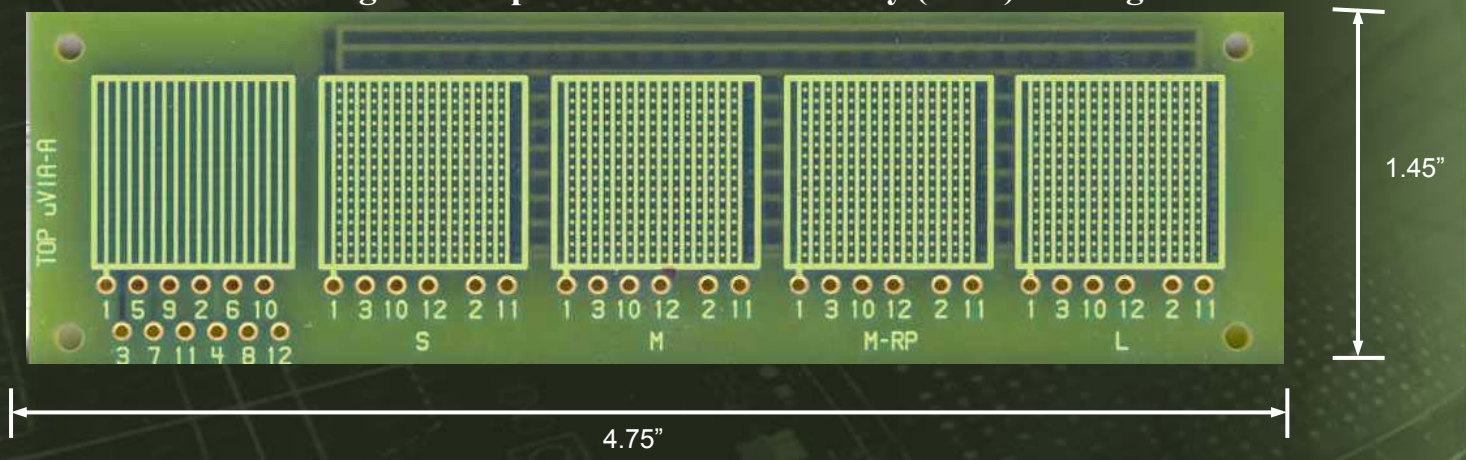
Thin Dielectric Performance

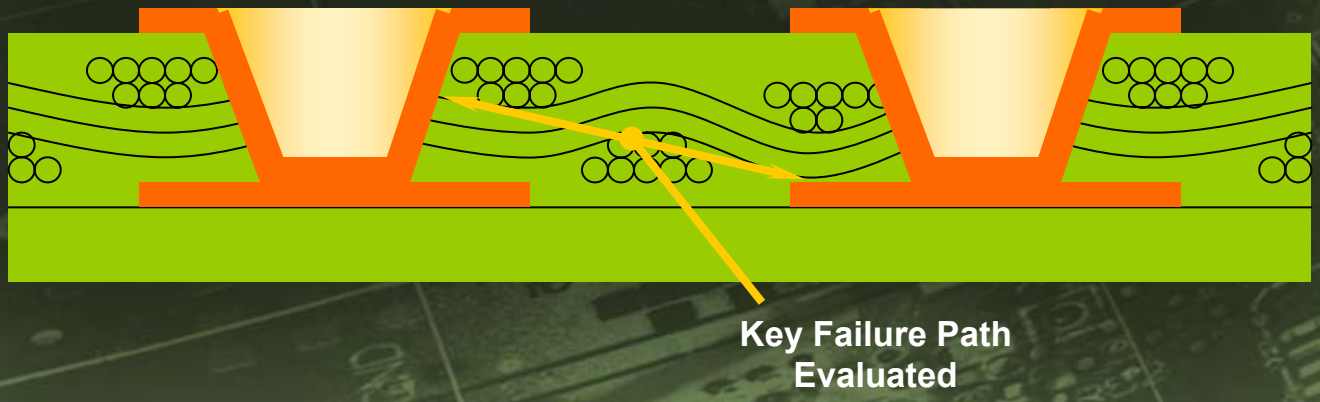
- For this study, “Thin” dielectric is a prepreg layer reinforced with **one** layer of 1080 glass.
- Metal separation was ≥ 0.002”
- Evaluated using
  - Dielectric withstanding voltage
  - Biased humidity (CAF) testing
  - Extended temperature cycling
- Thin dielectric reliable/acceptable for military/avionics applications



Evaluating Thin Dielectric

Merix-Designed Coupon for Biased Humidity (CAF) Testing





Conclusion

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  - Offers design flexibility
  - Enables dense interconnect, escape routing
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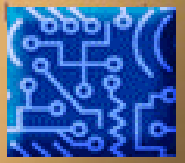

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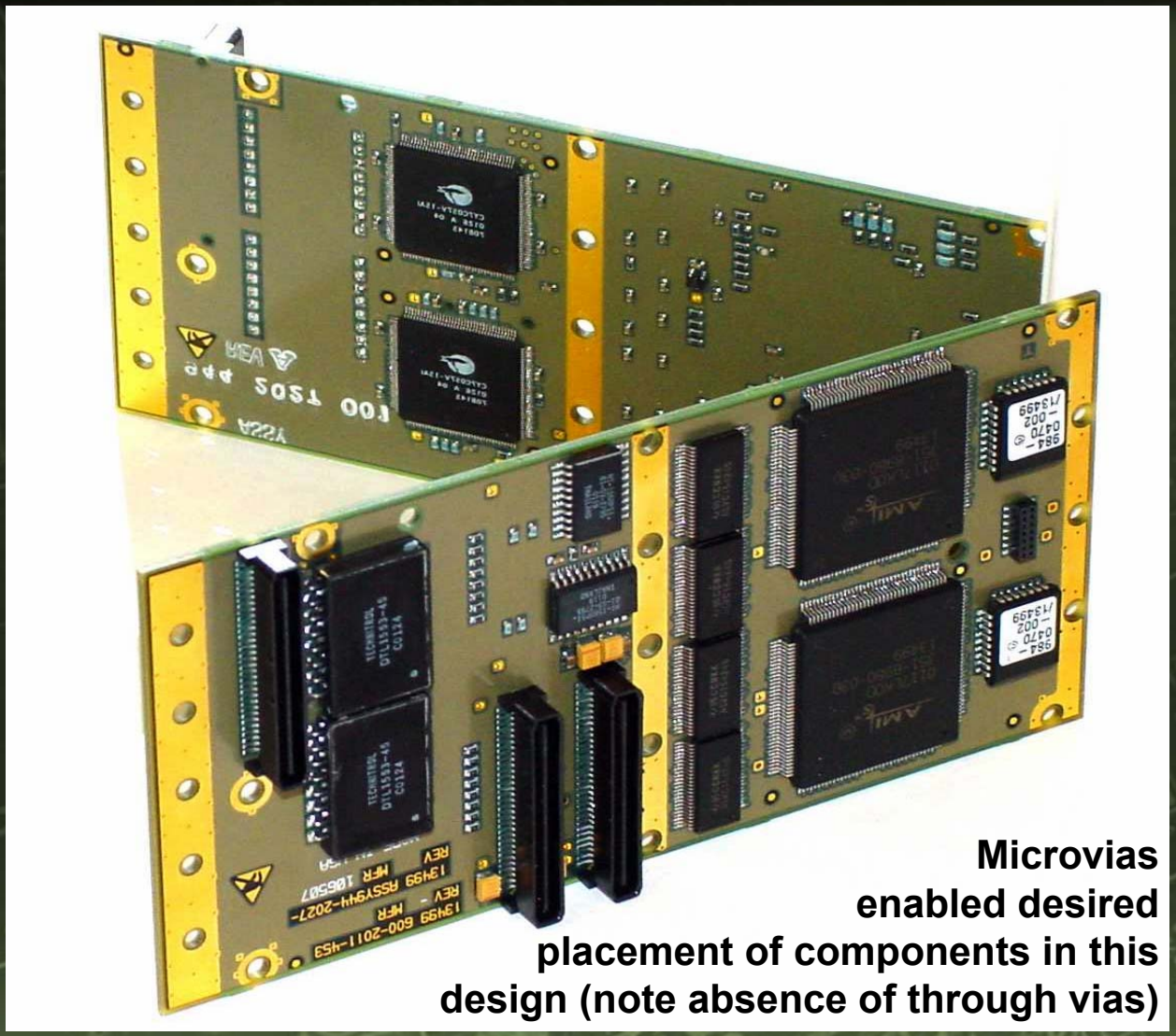

Microvias enabled desired placement of components in this design (note absence of through vias)

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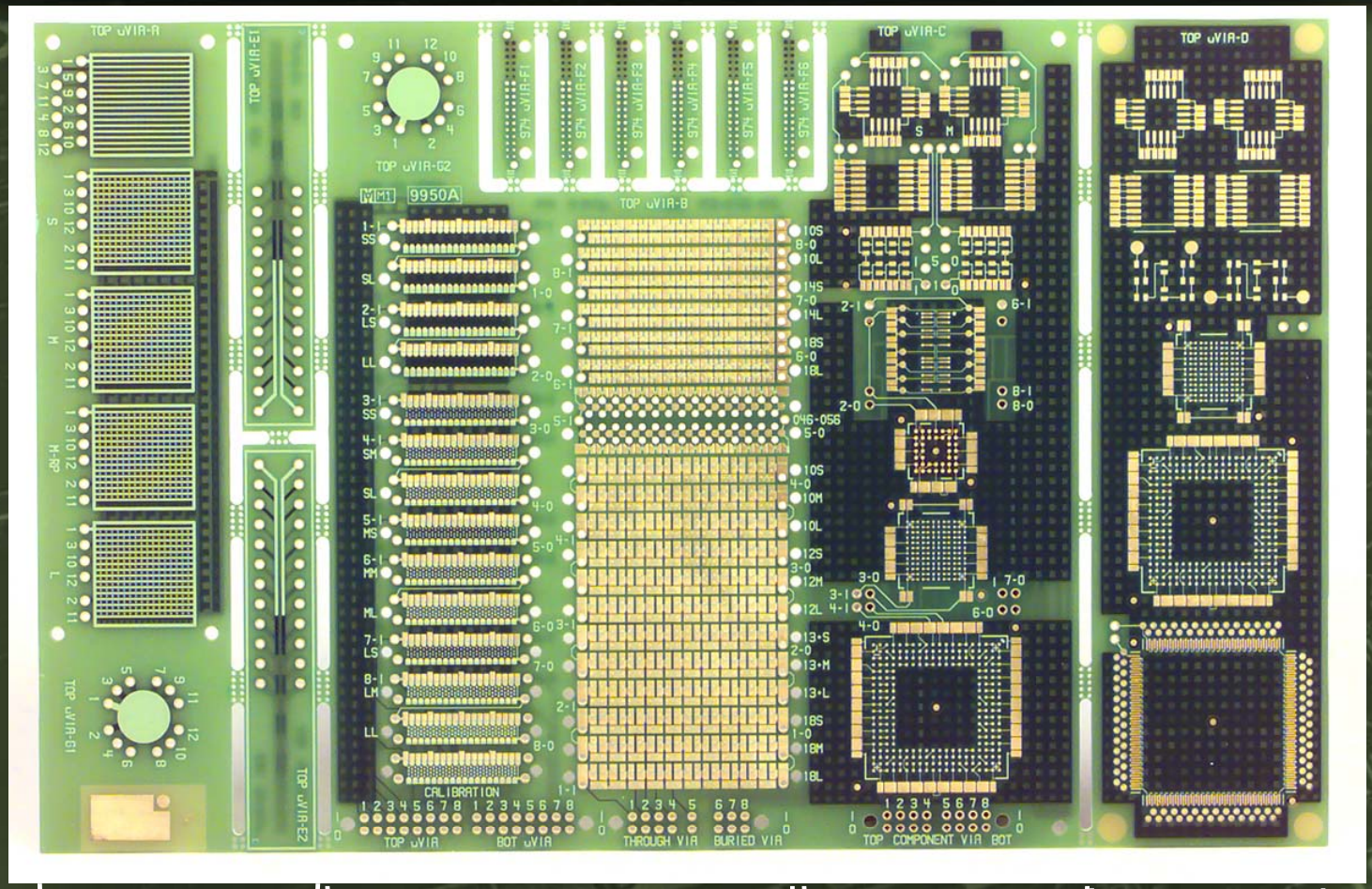

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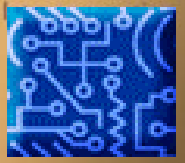

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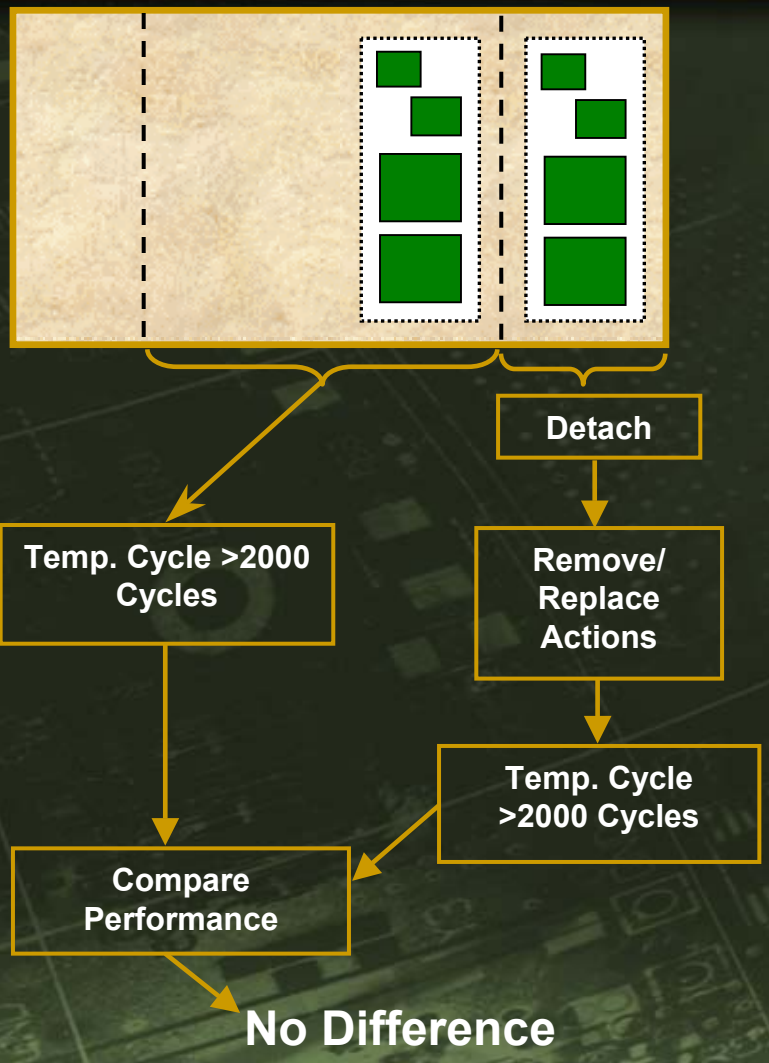

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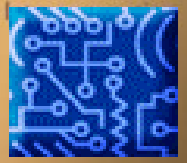

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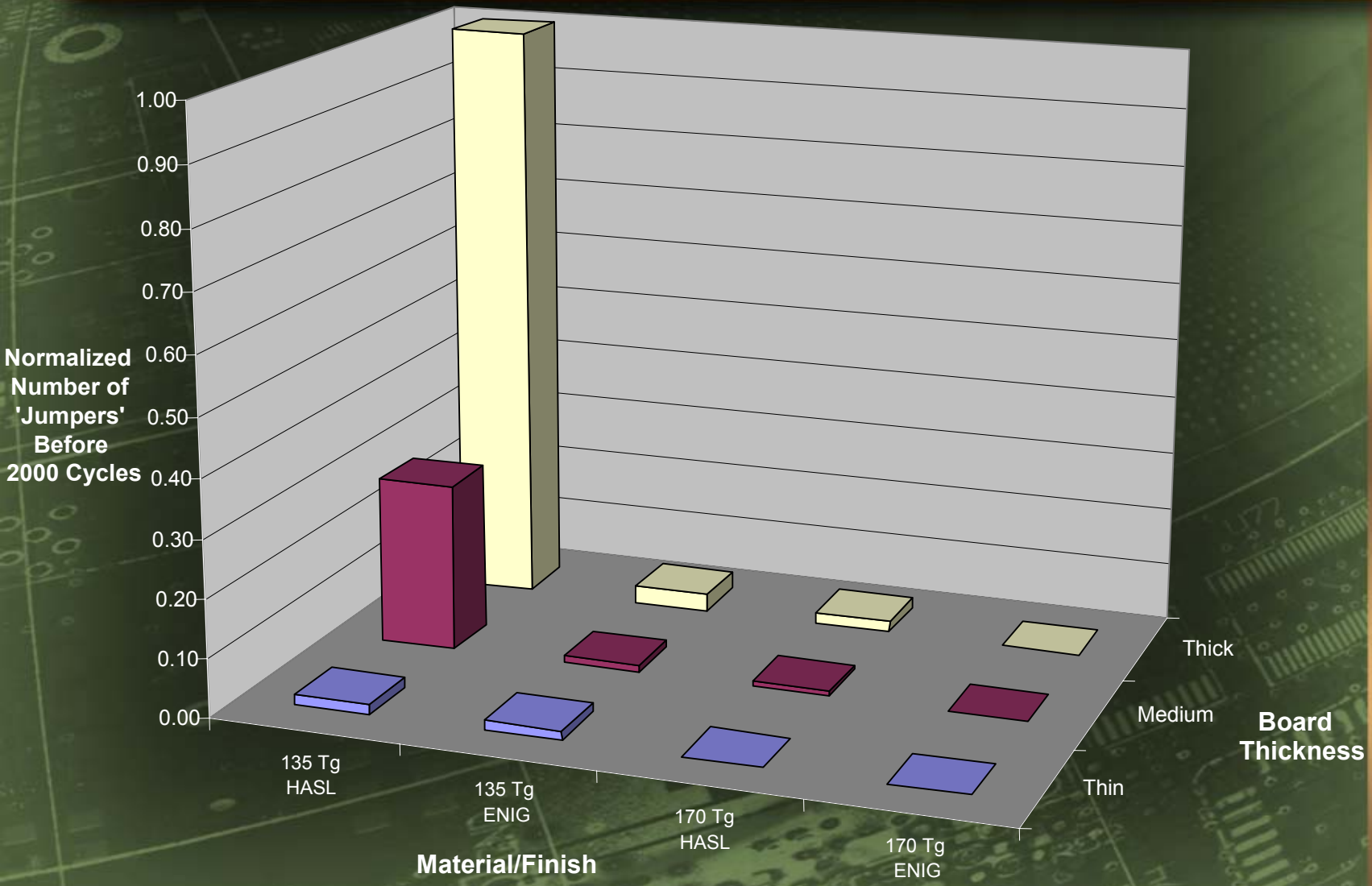

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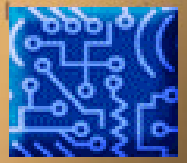

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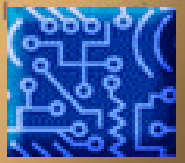

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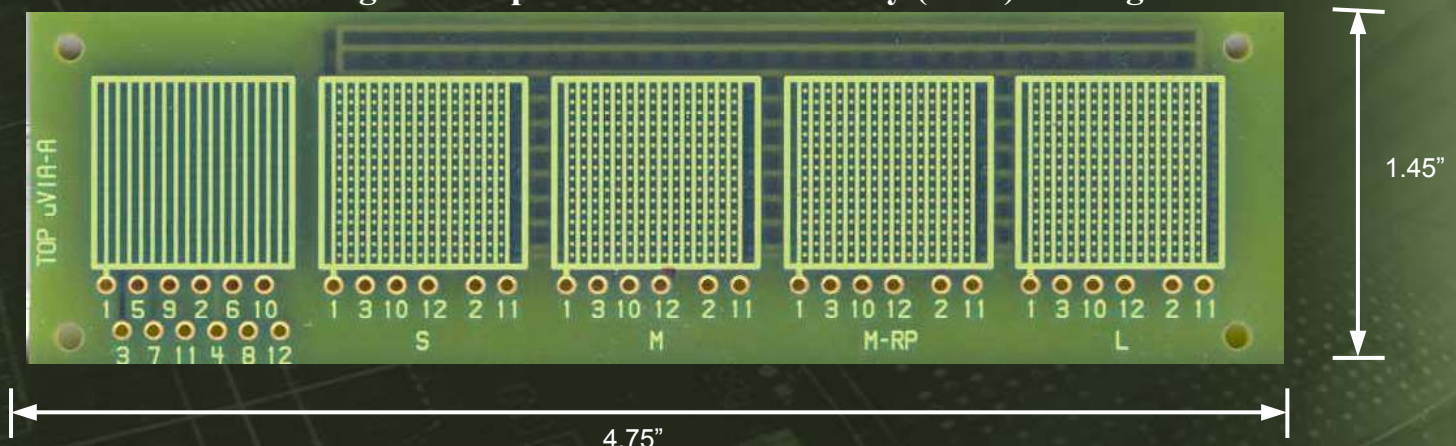

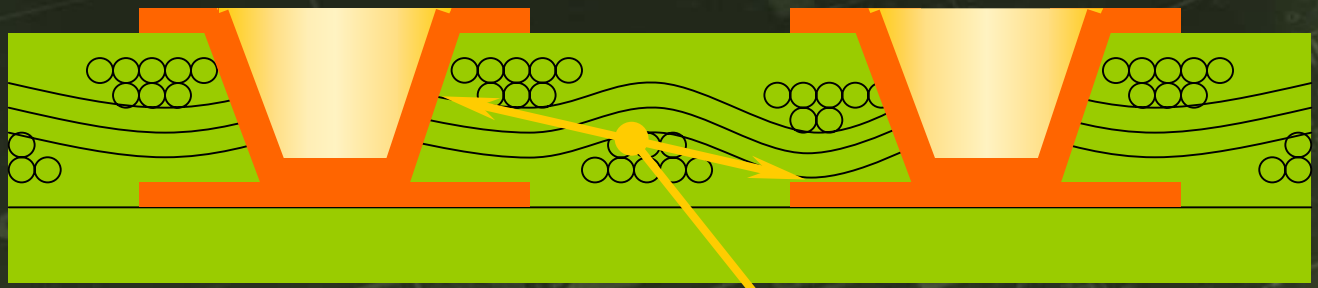

Key Failure Path Evaluated

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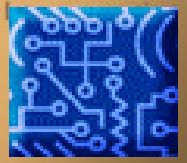

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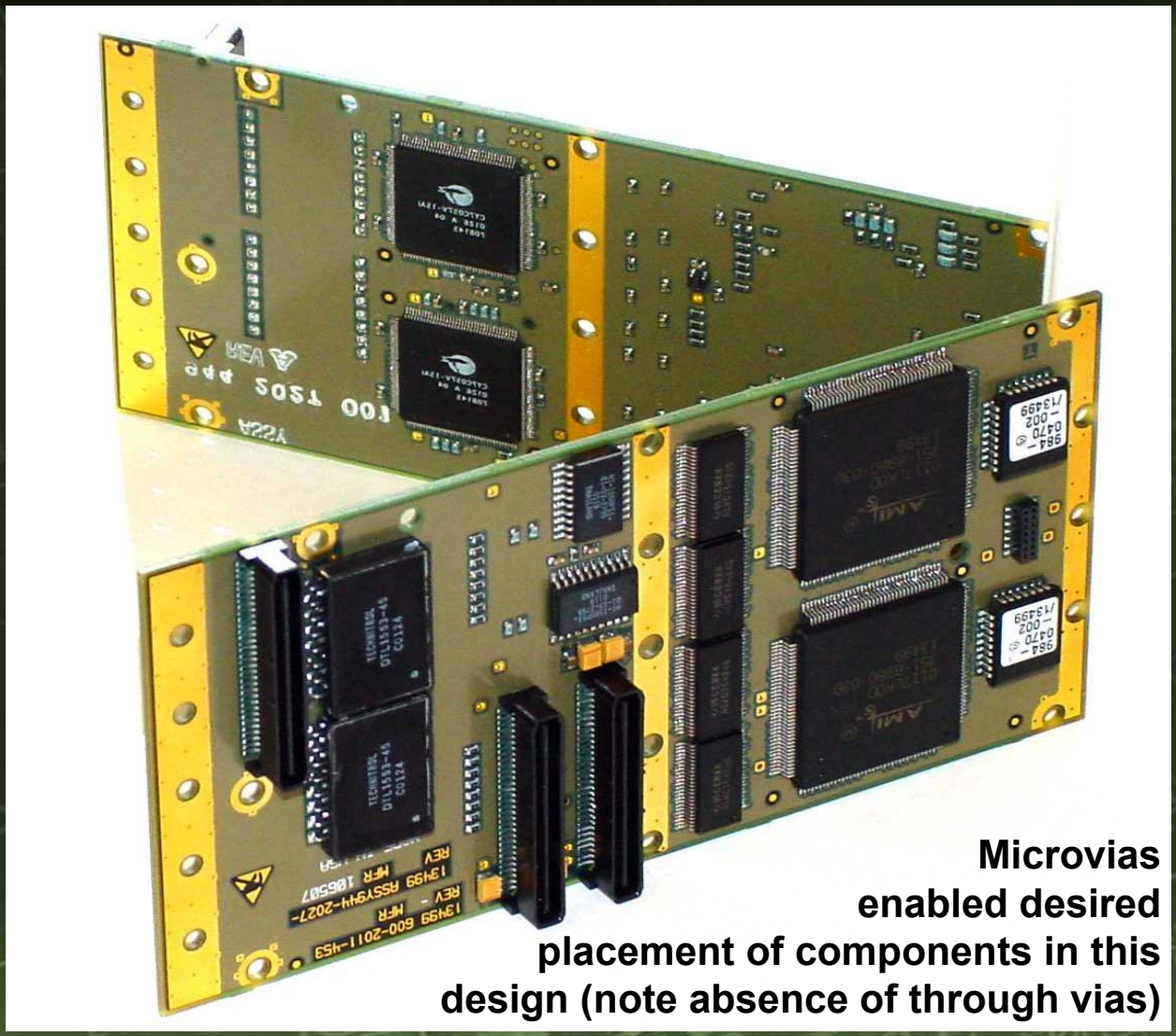

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