Folded-Flex and Stacked CSP
The 3D Solution for SiP Applications

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Abstract
The multiple die chip-scale package technology (identified as the µZ™) is a truly innovative, folded-flex stacked packaging technology. The concept has already been proven in a collaborative development effort between Tessera and two customer companies. A two-die package, developed for a leading medical electronics company, has been qualified and is currently in limited production. The three and five-die package developed for a leading IC manufacturer was targeted for the new generations of wireless electronics. The folded-flex stacked die package meets the lower height target defined by many OEM customers (a significantly lower height than many of the two-die stacked wire-bond solutions available today). Implementations are now being requested by the industry that requires the inclusion of different types of silicon technologies (including memory and logic) into a single package footprint resulting in a solution that is in essence a system-in-package. However, due to differing wafer-level yield rates, multiple silicon sources and testing methodology, the packaging yield and logistics issues can be very difficult to resolve (at both the technical and the business levels). In order to meet this growing demand for further integration, an innovative solution is required that brings all of the benefits of more conventional chip-scale packaging, including size, performance and reliability, while addressing testing, yield and logistics issues.

This paper examines several alternative multiple-die package solutions that solve many of the problems identified above while delivering the expected benefits. The package technology adapts one and two metal layer, flexible substrate materials, allowing two, three, four or more die in a single die BGA outline. Most of the multi-die packages developed for memory applications use classic CSP processes for die interconnect, though, other conventional interface techniques can be employed as well. The enabling technology for this "fold-over" approach allows the different sub-structures to be electrically connected while still maintaining a small footprint. The individual die included in the stack can be packaged, tested, and marketed as individual sub-structures, allowing each die to be sourced separately by each silicon vendor. This "layered" approach to packaging is designed to improve yield, resolve test concerns and overcome the business issues hindering the wide-scale adoption of multi-die solutions.

Introduction
Circuit board fabrication technology has made exceptional improvements over the years, providing higher circuit density and more physically robust materials. These advances have enabled IC manufacturers to focus on reducing package size, as evidenced by the rapid growth in fine-pitch and chip-size devices. These smaller, mostly BGA outlines are a welcome departure from their bulky lead-frame predecessor. Although miniature BGA packages are being used to support many new applications, the industry continues to demand more integrated multiple-chip and/or multiple-function packaging technology. Two and three ICs encased in a single package outline can be far more efficient in both size and performance, as a great deal of die interconnection can be accommodated within the substrate. This can free up routing within the circuit board and allow for substantial cost reduction. Some of the current offerings simply attach die to a single substrate, wire bond and over-mold, providing an application-specific modular solution. Wire-bond solutions are capable of furnishing two, three, four-die stacks and more.

Market Drivers for Multiple-Die Packaging
Portable and wireless electronics represent the most aggressive growth area for high-density package technology. In both circuit board fabrication and IC packaging, the technology for compressing even the most sophisticated electronic functions into a smaller and lighter finished product continues to evolve.

Portable or hand-held electronics are a natural target. Digital cameras and camcorders, for example, must consider ease of use, lighter weight and performance. Cellular phones, pagers, personal communicators, palm top computers, industrial and automotive electronics, personal GPS, medical and diagnostic products, are all viable candidates for more efficient device miniaturization.

Memory devices such as Flash, SRAM and SDRAM are the first commodity type products in the market to adapt CSP in high volume. However, digital signal processors, controllers, CPUs and any number of application specific IC devices are also prime candidates for multiple die packaging.

Benefits and Obstacles
The primary benefit in multiple die packaging is the dramatic increase in component density. The size and weight of the product is likely to be reduced and functionality enhanced. The functional enhancement is achieved through the integration of several device types.

Other benefits include decreased circuit board complexity, improved product quality through higher reliability and reduced risk in getting the product to market. With multiple sourcing of already proven and mature die, time to market and cost of ownership can be minimized.

The task of developing a multiple-die product are not without some obstacles. Some of the key issues are:

- Managing multiple vendors
- Known good die test and burn-in methods
- Die and wafer availability
- Combining high and low yield devices
- Overall product quality and reliability

Typically, multi-die packages contain die from several vendors. An issue that must be addressed early in the planning is who is responsible for the die quality? Known good die test methods vary from one supplier to another and KGD programs often are hard to manage across multiple silicon vendors. Test and burn-in of die is also an issue. Some memory technologies, for example, must be burned-in separately from other memory and processors. Further challenging the material supply logistics is that many memory technologies will not be sold in die or wafer form due to test vector confidentiality issues. In addition, multi-chip packages have significant yield issues that are compounded with each die that is added to the stack. This is exacerbated when combining high-yield devices with lower-yield devices. This factor further supports the importance of using pre-tested or known good die.

Memory die, such as Flash and SRAM, have relatively high fabrication yields. Damage can take place during assembly processing and handling but overall, the memory packaging process and testing has a very high pass ratio. Processors and ASIC, on the other hand, are not as predictable and wafer level fabrication yield, especially for new products, is difficult to gauge. Combining these two very different yielding products into the same finished package can be very risky. To minimize risk, the idea of building up the multiple-die package sequentially becomes highly attractive. With the ultimate goal of combining several functions in a single package footprint still achievable, assembling and testing individual devices prior to final integration appears ideal. The issues associated with compound yield and test can be easily addressed by stacking separate packages. One package contains the ASIC and the other, the memory. Separate the devices, separate the test and yield issues. Through a process of folding and surface mount attachment, the two pre-tested parts become a single, high yielding multiple-function component. Furthermore, by providing the memory interface on the topside of the ASIC package, currently available memory products in CSPs or MCPs can be soldered directly to the ASIC package. New exotic packaging is not required for stacking the memory. Existing memory footprint standards can be leveraged.

Overview of Multiple Die Chip-Scale Package Technology Package Methodology

The packages technology developed by Tessera Technologies represent a patented system of materials and die-to-package interface design that is compliant to ensure high reliability. For highest reliability, the ribbon lead process is incorporated. The lead-to-die interface design is critical. The length and profile of the lead has been engineered to furnish a controlled shape, that when retained in its encapsulation material, allows a limited flexation or compliance. These attributes combine forces to compensate for the wide differences in the coefficient of thermal expansion between the silicon die and the circuit board. In alternative CSP structures, additional reinforcement processes are necessary (typically an epoxy under-fill) to compensate for the physical incompatibility between the packaged component and circuit board.

The substrate developed for the multiple die chip-scale package technology folded-flex stacked-die package uses a high-grade polyimide film as its base structure. For electrical interconnect it relies on a pattern of narrow gold plated copper-core conductors for the electrical interconnection between aluminum lead bond site on the die, the interconnection between die and ultimately, the contact (solder ball) array needed for the circuit board interface. The die–to-substrate electrical interface is made with either wire-bond or lead-bond processes. The actual interface between die sets will typically require two circuit layers to provide for higher wiring density. This two metal layer process allows for very narrow circuit routing (less than 25µm) and enables a more direct, in-package interconnect.

The actual design of the multiple die package requires a clear understanding of the relationship between devices, the on-package interconnect requirements and ultimately, the interface between package and the circuit board. The company's design engineering team, working closely with an independent substrate supplier and the company's in-house assembly process development team, has (as a service) developed a number of multiple die packages. During the learning curve typically associated with most innovative technologies, the engineers have developed design guidelines for several variations, some having the same size die while others have different die sizes. Tessera has learned that the substrate design for multiple die applications will generally require the use of two circuit layers. To assist customers with the evaluation and/or adoption of the technology, Tessera offers package design and simulation services.

The 'folded-flex, stacked-die package' development programs typically use die types and suppliers specified and qualified by the customer company. The development engineers, in their planning phase of the package

substrate, rely on computer simulation models to help define the best position for each die. During this design and planning process the in-package circuit routing is refined and modeled to verify that the package, when fabricated, meets the customer's performance expectations.

Because of the minimal surface area of the substrate, the inter-package circuit design requires adapting very small via pads, holes and circuit conductor widths. The via holes, for example, are only 125µm in diameter and 25µm to 35µm wide conductors are the rule for most applications. Although both sides of the substrate are utilized for interconnect, the circuit path between die is routed on the inside surface of the flex material. With the exception of the 'fold zone' on the substrate, the circuit pattern remaining on the outer surface is coated with a photo-imaged dielectric mask material specially formulated for flexible applications.

Fabrication of the substrate requires very precise process controls and monitoring. In preparation for pattern plating the circuit, the basic copper-coated polyimide film will undergo a pre-etching step to selectively remove copper from areas requiring laser ablation. Using a digital design file, the laser removes the polyimide base material in what will become the lead-bonding area, micro-via holes and vias holes located on the ball attachment sites.

Following the laser process, the circuit pattern mask is imaged onto the thin copper base. The first stage plating for the outer layer surface relies on a pure electroplated gold build-up to 18µm in thickness. The second stage also uses an electroplating process to build-up the copper thickness on what becomes the inside surface. The copper is electroplated to a thickness of 10µm to 11µm followed by a final plating step that applies 1µm of gold over the remaining copper circuit pattern. The pattern mask coating is stripped from the thin base coat of copper. The exposed raw copper surface is chemically etched away, retaining only the circuit pattern, bond-leads and plated micro-vias. An insulating coating is finally applied over the gold circuit pattern to what will become the outer surface. This surface is now photo-imaged and developed to clear the bond-leads and ball attachment sites.

Five Die Multiple Die Chip-Scale Package Technology Folded-Stack Package Assembly

Although each device area is often relatively small, multiple unit arrays can be closely clustered on the flex-tape material. A common width for the polyimide flex-tape substrate is 48mm. Suppliers can also furnish flex-tape in a narrower 35mm wide format or, for larger multiple die applications, 70mm in width. The following describes the joining process for a two section five-die package. The four die on the upper section provide memory and other functions and lower, or base section, accommodates a single ASIC die.

In preparation for upper section assembly, the flex tape is mounted to a rigid carrier-frame. The tape design typically accommodates several die sets arranged in a side-by-side format. Device sets can then be processed using conventional systems for die-attach, wire-bond or lead bond and efficiently transferred through each of the sequential process steps. Although wire-bond can be used for many applications, the following process sequence describes the package assembly sequence utilizing the standard lead-bond process.

Prior to die attachment, a pattern of liquid elastomer encapsulant is dispensed onto the top of a spacer site that is applied during tape preparation. Immediately following the encapsulant application, each die is aligned and attached to the substrate. After a short cure cycle the leads (furnished within the flex-tape design) are sequentially thermal-sonically bonded to the aluminum bond pads on the die completing the basic assembly. The attachment and lead bond sequence completed, the assembled carrier-frame is inspected and transferred to the encapsulation stage. The encapsulation process for the multiple die folded-flex applications typically uses vertical dispensing of a low modulus elastomer.

Singulation of the packaged device set from the flex-film carrier must be very precise. Several techniques proved successful. For example, sawing, rotary and straight blade cutting as well as die-punch methods, have proven to be efficient. Each method has advantages and disadvantages. The saw, rotary and straight blade cutter can be programmed, allowing for several package variations and requiring minimal tooling. The die-punch methodology has a higher rate of throughput but it requires precision tooling that must be prepared for each multiple package configuration.

The final configuration of the multiple-die memory section is accomplished through a sequence of liquid bonding material dispensing and precise mechanical folding. The material used for retaining the folded configuration is a modified composition of the materials used during the initial encapsulation process. When the encapsulant finishes its curing cycle, the memory section of the package is electrically tested at operating temperature, graded and laser marked. The ASIC section is also processed and tested separately. Figure 1 illustrates the two package sections before folding and stacking.

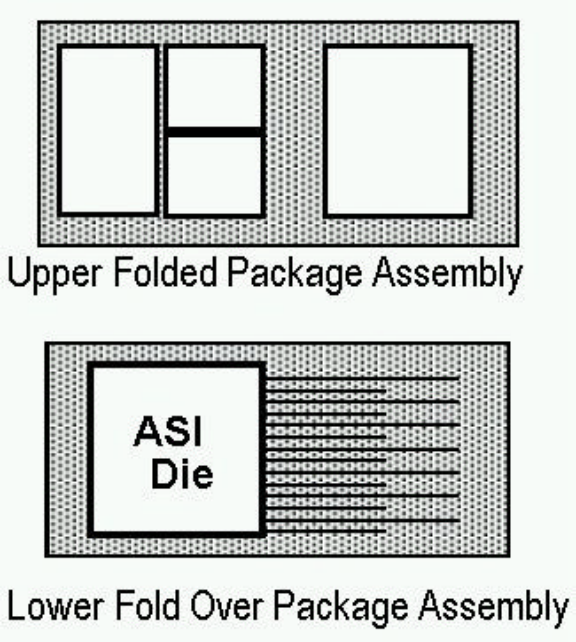

Figure 1 - The Multiple Die Chip-Scale Package Technology Lower and Upper Package Assemblies with Memory are Processed and Tested prior to the Folding and Joining Operation

In the example application, the ASIC die is attached to the substrate face-up using the same elastomer material family as that described above and electrically interfaced using a wire-bond process. Following visual inspection, the area of the die and wire-bond are over-molded or capped with an epoxy compound and made ready for the ball contact attachment process.

Several alloy compositions can be considered for the solder ball contacts. The standard package is furnished with Sn63/Pb37 alloy solder ball contacts but lead-free contacts are available as well. Examples of some of the alternative lead-bearing and lead-free solder alloy compositions are shown in Table I.

Table 1 - Solder Alloy Selection Guide

Composition	Liquidus Reflow	
	Temp	Temp.
63*Sn*/37*Pb*	183°C	210-220°C
62*Sn*/36*Pb*/2*Ag*	179°C	210-220°C
62*Sn*/36*Pb*/2*I*	179°C	210-220°C
Sn96.5 / Ag3.5	221°C	240-250°C
Sn99.3 / Cu0.7	227°C	245-255°C
Sn95/Ag4.0/Cu1	218°C	238-248°C

In preparation for solder ball attachment on the lower fold-over section of the package, flux is applied to each solder contact site using a pattern printing process. The contacts are deposited onto the flux and transferred to a surface conduction heating process to complete the ball-to-package attachment process.

The ASIC section is electrically tested, marked and made ready for the final folding process. For lower the single die section, a snap-cure adhesive is utilized to adhere the extended circuit section to the top of the mold cap. At this point, two scenarios can be considered. The two sections can be supplied as separate units and joined together at the board level assembly stage as shown in figure 2 or furnished as a single package level product, tested and ready for PCB mounting.

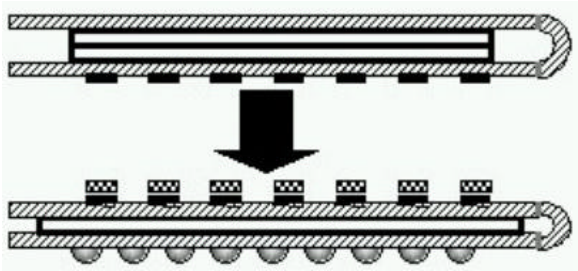

Figure 2 - The Two Sections of the Multiple Die Chip-Scale Package Technology Folded and Stacked Package are Joined by a Reflow Soldering Process before or during Board Level Assembly

Optional combinations may be considered including alternative die combinations or die supplied by multiple vendors. The examples detailed in Figure 3 are typical of the combinations that may be selected for specific product applications.

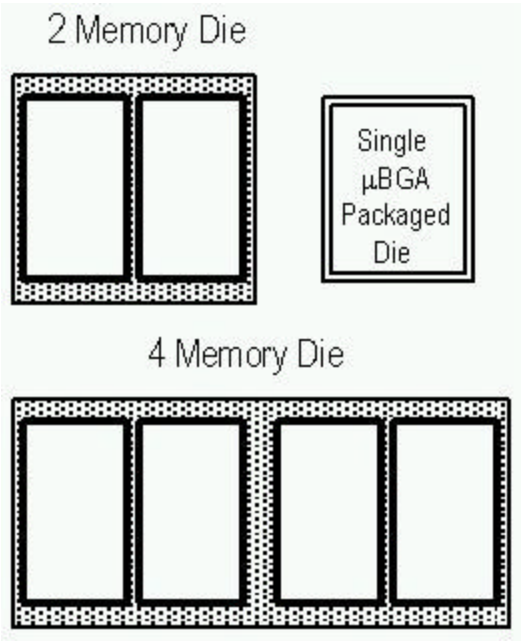

Figure 3 - Several Die Combinations can be Considered for the Upper Section of the Multiple Die Chip-Scale Package Technology Package Maximizing Product Configuration Options

This is a business decision that maybe influenced by the specific die required for the application or the logistics for managing multiple source suppliers.

The testing for memory, is somewhat specialized and the handling and testing of the proprietary ASIC portion of the package may require more dedicated fixturing, software and system support. Furthermore, the concern of ownership of total quality and reliability can be alleviated. The ASIC manufacturer is responsible for the ASIC, the memory manufacturer is responsible for the memory, and the board assembler is responsible for the surface mount attachment of the two: just as is the case today.

If the decision is to join the two sections at the board-level assembly, the base package (in this case, the ASIC) can be placed onto the board and the memory placed sequentially onto the ASIC's mating contact matrix for simultaneous reflow soldering. This scenario has two benefits. It allows the user to specify multiple variations (different memory functions, data rate and so on) as well as accommodating secondary sources of supply. Memory price and supply can often become volatile as the general market gains strength. If desired, the ASIC and the memory package can be combined into a single package unit off-line so as not to impact the throughput or efficiency of a conventional board assembly process.

Folded and Stacked Package Variations

A number of package variations have been developed for specialized applications. Although many are still classified as confidential as far as their application and function, a few physical examples of multiple-die structure are described below.

Example 1. A three die folded package having a uniform ball contact matrix under the center die allowed the simple wing-fold process. The package outline is only slightly greater than the largest of the three-die set.

Example 2. The basic 'ball-stack' package provides a great deal of versatility with minimal risk. A common application is combining two to four of the same size die (or layers) vertically. The electrical interface is made through ball contacts at the package perimeter or edge extension.

Example 3. As an extension of the ball-stack described above, a single processor or controller die is mounted to a flexible, fold-over substrate as a base unit. Mounted sequentially to the base are one or more memory functions. An example would be a processor and SRAM on the second layer and perhaps two Flash die on the third.

Example 4. A very thin two die stacked µBGA package assembly was developed for a customer company. In this application, one die is significantly smaller than the other allowing it to be solder attached to the underside (ball matrix side) of the larger package structure. Utilizing extremely thin die and package methodology, the lower die assembly can be made less than 300µm in overall thickness. The package is furnished with a 500µm ball contact, providing a bottom surface clearance of approximately 200µm.

In addition, several applications have evolved requiring a combination of RF die, filters and integrated passive devices within the single, 3D package outline. The benefit in this concept is the very close in-package coupling between component parts. The minimal interface ensures lower inductance, lower resistance and when engineered properly, superior impedance control.

Conclusion

The most significant result achieved in the development of multiple die chip-scale package technology package technology is the dramatically small outline, a real benefit to developers of miniature hand-held electronic products. The package technology not only offers the smallest overall outline possible, the unique combination of materials, thin die, lead or wire-bonding and folding methodologies can furnish one of the lowest profile, highest yielding multiple-die package systems available.

The multi-chip package technology developed by Tessera is proving to be an excellent cost-effective 3D package solution for a number of real and practical applications; it allows optimization of individual die function and greater design flexibility, reducing risk and time to market. Unlike some of the earlier over-molded multiple die, wire-bond packaging techniques, no new assembly lines are required for adapting the methodology. With minimal investment to the OEM or user, the standard µBGA assembly infrastructure can quickly initiate the stacked-die package technology.

References

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