Overcoming Technical and Business Issues Associated with System in Package Adoption.

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Abstract
In today's world of electronics the keywords are smaller, faster and cheaper. With more and more circuitry going onto existing circuit boards, the designers are searching for ways to contain this additional functionality in the same, or smaller, space envelope. To accomplish this, the semiconductor die used in the circuit design must shed the traditional packaging enclosures.

One solution is to create sub-systems as building blocks that can be assembled on a motherboard to provide a complete functional solution. Twenty years ago we called these sub-systems "Hybrids". When the die became larger than the discretes, we called them MCM's. While searching for a descriptor for MCM, it was suggested that "if you can't afford it, it must be an MCM)". Now "system in a package" is in vogue.

Many of the issues faced twenty years ago are still issues today. However, more have been added. These of course include die quality and reliability including tradeoffs, assembly quality and reworkability and in some cases substrate quality and reliability. This paper primarily looks at die quality and reliability issues and discusses solutions or work-arounds.

Preface
Whether COB, CSP or SiP, there is little doubt about the increased performance and circuit board area gained when bare die shed their traditional packages.

System in a package usually yields 50 to 60 percent active silicon (plus discrete) density. Packaged parts on a printed circuit board yield 10 to 15 percent density.

However, the inclusion of multiple die in a common enclosure magnifies the need for high levels of die quality and reliability.

Complex semiconductor die are manufactured in "wafer" form. After fabrication the individual die on the wafers are electrically probed for some simple set of electrical parameters to identify candidates for subsequent assembly into packages. These packages facilitate complete electrical screening and provide a convenient interconnect to the outside world.

While this is a simple and inexpensive way to provide building blocks for circuit designers, the resultant multi-package assembly is, by today's standards, rather large and heavy.

Many years ago, in order to reduce both size and weight of assemblies, the military and space industries turned to the use of bare die wire bonded onto a ceramic substrate. These assemblies were subsequently referred to as "Hybrids".

In those days the die were relatively simple using plus micron geometry's and as a result exhibited rather high quality and reliability after only a cursory probe. The die were small and with few bond pads. Die that failed at assembly test were easy to replace.

As die became more complex, and line widths dropped below one micron, two things were becoming apparent. Wafer probe alone was not sufficient to provide acceptable quality, and unscreened infant mortality was causing too many failures in time in modules in service.

It then was obvious that developing a method for producing bare die with the same quality and reliability of the comparable packaged part was paramount - thus the beginning of Known Good Die (KGD).

Die Quality and Reliability
To obtain packaged part die quality and reliability, some sort of Known Good Die (KGD) process must be done on the bare die prior to assembly. Without this process, and dependent upon number of die on the SiP, first time assembly yields and field failure rates may be unacceptable. (See Figure 1.)

As is evident from Figure 1, a 10 die MCM assembled using die that yield 95 percent good at first electrical test, will only yield 60 percent good MCM's.

In addition, assuming the failures in time to be 3 percent, approximately 20 percent of the MCM's that pass first electricals will fail in service.

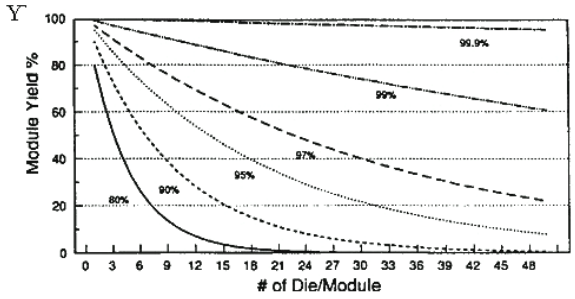

Figure 1 - First Time Assembly Yields and Field Failure

One can deduce from this curve that a SiP with 20 die, (a data storage SiP for example) each with a quality level of 99.00 percent, will yield only 80 percent good SiP's at first assembly. Furthermore, there is the potential that up to 20 percent of the good SiP's will fail in the first year of field use. This of course is unacceptable.

In the packaged part world a die that had been probed at wafer level will be assembled onto a lead frame and plastic encapsulated. The packaged parts will then be tested and burned-in using automatic handlers and testers.

Even today, screening of bare die is not trivial. Examples of two methods available today include Aher Test's carrier (Figure 2) process and Chip Supply's SofTAB™. Aher's carrier process requires that a bare die be loaded from a sawn wafer face down into a membrane carrier. The carrier is designed in such a way so as to cause the membrane contacts to scrub the aluminum bond pads in order to break the native aluminum oxide. The cost of these carriers is not inexpensive, but according to the manufacturer they can be reused at least 200 times before requiring rebuild. Special equipment is also required to load and unload these carriers. Once the die are loaded into the carriers, further handling for test and burn-in is similar to packaged parts. To the best of the authors knowledge, this process is not offered by any semiconductor manufacturer.

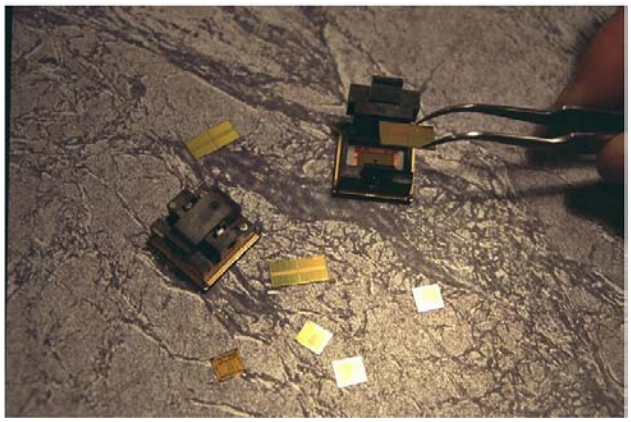

Figure 2 – Screening of Bare Die by way of Membrane Carriers

Chip Supply's carrier (Figure 3) process requires that the die bond pads be gold bumped at wafer level. A Tape Carrier Package (TCP) is designed that matches the die bond pad locations and is customized to facilitate assembly and dis-assembly. After singulation the die is Inner Lead Bonded (ILB) to the TCP. This assembly is then compatible with standard off the shelf TAB sockets. After test and burn-in the TCP is removed from the die using a proprietary process, and the die is ready for assembly. The process is labor intensive and is more suited for small volume production. It is also only available on die products furnished by Chip Supply, Inc.

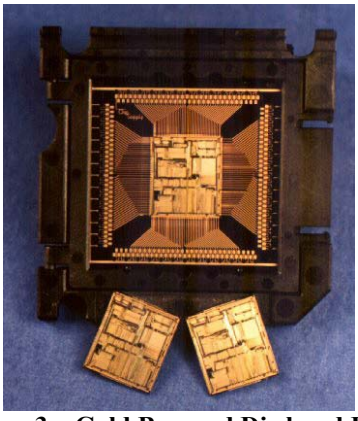

Figure 3 – Gold Bumped Die bond Pads

To demonstrate the significance of this let's look at a three die SiP that we manufacture. The SiP is a ceramic BGA with one microprocessor die and two cache SRAM's. Flip chip with underfill is the assembly process. To place value on this let's say that the cost of each SRAM die is 7 percent of the total MCM cost and the processor 30 percent. The rest is for the substrate, assembly, ball attach, test and burn-in. If the SiP is completely assembled then subjected to burn-in stress prior to final test, the parts that pass test will exhibit excellent quality and reliability. However, at what cost? If an SRAM failed, we will have discarded an SiP that had 93 (cost) percent of it working and only 7 percent not working. If we assume normal quality and reliability yields for the three die and also normal assembly yields, the total final SiP yield should be about 85 percent. This now means that the cost of the SiP has risen by 15 percent. This cost multiplied by SG and A, commission and profit, can result in an unacceptable product selling price.

The proper approach to reducing the cost of the SiP is to first assemble the processor onto the substrate then burn-in and test the processor only. Only the higher cost items in the SiP will cause yield losses here. The SRAM's will be burned-in and tested as KGD (easier than a processor because of fewer number of bond pads and less complex testing). The yielded SRAM's will then be assembled onto the substrate and a simple functional test run.

This is a rather simple example of the effects of die quality and reliability, however the effects multiply exponentially with the increase in the number of die in the SiP.

T_{CE} Differences
Silicon has a temperature coefficient of expansion of about 3 parts per million per degree centigrade. Organic substrate materials such as FR4 and BT are around 17-19 PPM/°C, and ceramic about 7 to 10 PPM/°C. When a silicon die is assembled onto one of these substrates, consideration must be given to the T_{ce} mismatch. If the die assembly process is wire bonding or TAB, the die attach material is usually sufficient to restrain differential motion through normal industrial temperatures. If however the assembly process is flip chip, an underfill material must be used to prevent bump fracturing during temperature excursions. While underfill helps with this problem, it eliminates rework, placing more of a premium on KGD.

Rework Capability
When unscreened (probe only) die are used to assemble a SiP, in most cases the first assembly yield will be unacceptable. Many assemblers have developed methods for removing the defective die and replacing them. Of course the replacement die may also fail, but the odds are rather good that one rework will suffice. In many cases rework will solve the first assembly yield problem. However, it is important to understand that if
the die used are subject to infant mortality failures, some of your SiP's will fail in the field.

SiP Assembly
There are several ways to assemble bare die onto a SiP substrate. Tape Automated Bonding (TAB), die attach and wire bond and flip chip.

Some COB assembly technologies afford easier rework than others. i.e. Wire bond and TAB are the easiest processes to rework because the electrical connections are usually on the die periphery. Flip chip is more difficult because the electrical connections are under the die and surrounded by underfill epoxy.

Bare Die Handling
Bare die in unpackaged form are extremely susceptible to physical damage. The active surface of the die is covered by a very thin layer of passivation typically silicon nitride or oxy-nitride. Scratches in this passivation layer can easily penetrate through to the active area of the die. This damage most often is to the top metal layer and via interconnects.

Die used for flip chip assembly are generally pre-processed to redistribute (RDL) the bond pads into an array that facilitates solder bumping and flip chip assembly.

In either flip chip or wire bond assembly extreme care must be taken in handling placing and attaching the bare die to the substrate. The Die Products Consortium (DPC) is producing a document detailing recommended die handling procedures. This document should be available soon on the DPC home page (www.dieproduct.com).

Assembly Technologies
As stated earlier COB can be accomplished in several ways.

Wire Bond - The most common assembly technique used today is wire bonding. In this process, the backside of the die is attached to the substrate using thermally conductive epoxy. Electrical connection is then made by wire bonding the die bond pads to comparable pads on the substrate. While this process is considered mainstream in today's assembly world it also occupies the most substrate area per die.

Flip Chip - Flip chip assembly offers the smallest substrate area usage and the lowest impedance electrical interconnect. It does however necessitate underfill thereby reducing rework capabilities. An issue with flip chip is that bond pad redistribution is usually necessary in order to provide an acceptable bond pad pitch for solder bumping. This process is done at wafer level and has an associated yield issue. Another issue involves alpha contamination from solder bumps. This error producing contamination is most
critical in memory die. Care should be taken in designing the RDL so as to not place bumps over memory cells. As this is near impossible in most memory designs, the alternative is to use low alpha solders. These solders while containing similar alloys to high lead solder will exhibit different melting characteristics.

A new paradigm and an old technology revisited are going to make life easier for the SiP manufacturers in the near future.

The RDL and solder bumping described earlier is still considered Flip Chip. The new twist on flip chip is called Wafer Level Chip Scale Packaging (WLCSP).

The RDL is performed as in flip chip, however instead of solder bumping the new pads, solder spheres are attached that are larger and more consistent in shape and size than solder bumps. These WLCSP's can be tested in normal fine pitch sockets. The caveat to this technology is that the number of bond pads (I/O) must fit into the periphery of the die when redistributed into an array with a pitch consistent with available test sockets.

The old technology revisited is called Iddq testing. Die in wafer form are subjected to voltage bumps and pattern testing at elevated voltage. Quiescent current is measured before and after each test and delta's recorded. Recently completed studies by members of the DPC indicate that

this process shows promise in greatly improving the quality and reliability of die at wafer probe. Recent advances in hardware will make it easier to make more measurements in an acceptable period of time thus further increasing fault coverage. Again there is a caveat to this process and that is that it is only effective on semiconductor devices with quiescent current in the micro-amp range. This is because we are looking for nano-amp changes in quiescent current. The good news is that 4T logic is going away.

Tape Automated Bonding (TAB) – Tape automated bonding offers advantages and disadvantages to the assembler. Die assembled into a tape carrier package (TCP) can be screened to KGD quite easily using off the shelf sockets. The tape carrier packages can be designed for either face up or face down (flip TAB) assembly. In face up assembly the TCP is excised and formed into a small leaded chip carrier type package. In flip TAB the TCP is excised to a length of approximately 2mm. The die is attached face down to the substrate using epoxy and the TCP leads hot bar soldered to the SiP substrate.

Chip Scale Packaging (CSP)
In some cases, Chip Scale Packaged die can be used in a SiP project. CSP resolves some of the issues associated with die quality and reliability but provides some of its own unique challenges.

CSP Quality and Reliability
Beginning die quality and reliability is not as important in CSP as COB. A CSP assembler/supplier can begin with die as probed by the manufacturer at wafer level. The reason for this is that in most cases the resultant ball pitch of the CSP can meet current socket standard pitches while remaining in the required space envelope.

Form Factor
CSP form factor can reduce a 17mm square 44 pin PLCC to a 7mm square CSP, or a 31mm square 160 pin PQFP to a 12mm square CSP (see Figure 3).

Ball pitches on CSP's can range from .5mm to 1.27mm. Ball pitch alone does not define chip scale packaging. The ball pitch should always be as large as maximum design of substrate will allow. Larger pitches equal lower cost CSP's and circuit boards (see Figure 4).

Summary and conclusions
This paper has dealt primarily with the use of bare die in SiP manufacturing. There are of course many other issues a SiP manufacturer must deal with. The substrate material must be selected. Factors involved in this selection are Tce, ceramic or laminate, thin film or thick film, etc. A package technology must also be selected. SiP products range from flip chip die on a substrate, to folded tape stacked die, to sealed metal header packages.

Two of the business issues faced by SiP are; convincing the market that this little building block is functional and reliable, and designing and building a product that is cost effective.

Technical issues tie directly to cost issues. Tradeoffs must be considered as to die quality and reliability. Is KGD needed or is pretty darn good die good enough and how do you tell the difference.

Some semiconductor manufacturers and independent die processors recognize the increasing need for KGD and are working toward solutions for this market.