Overcoming Technical and Business Issues Associated with System in Package Adoption

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Introduction

- This paper will first place into perspective the roll of unencapsulated semiconductors (bare die) as applied to System in Package technology.
- It will present a historical look at die usage and efforts to define and deliver “KGD”.
- Assembly and rework will also be discussed.
- Author will present his conclusions.

Bare Die Perspective

- First a test. Pick the word in the group of words that does not belong.
- MCM, Hybrid, SiP. Answer: All belong.
- Smaller, Lighter, Cheaper. Yeah, your right. Smaller and Lighter cannot always be accomplished for lower cost.

- In the *old* days of Hybrids, the die were smaller, cheaper, and easy to replace.
- The advent of MCM's brought us expensive, large die that were difficult to rework.

Bare Die Perspective

- Complex semiconductor die are manufactured in “wafer” form. After fabrication the individual die on the wafers are electrically probed for some simple set of electrical parameters to identify candidates for subsequent assembly into packages that facilitate complete electrical screening and provide a convenient interconnect to the outside world.

- While this is a simple and inexpensive way to provide building blocks for circuit designers, the resultant multi-package assembly is, by today’s standards, rather large and heavy.

Bare Die Perspective

- Many years ago, in order to reduce both size and weight of assemblies, the military and space industries turned to the use of bare die wire bonded onto a ceramic substrate. These assemblies were subsequently referred to as “Hybrids”.

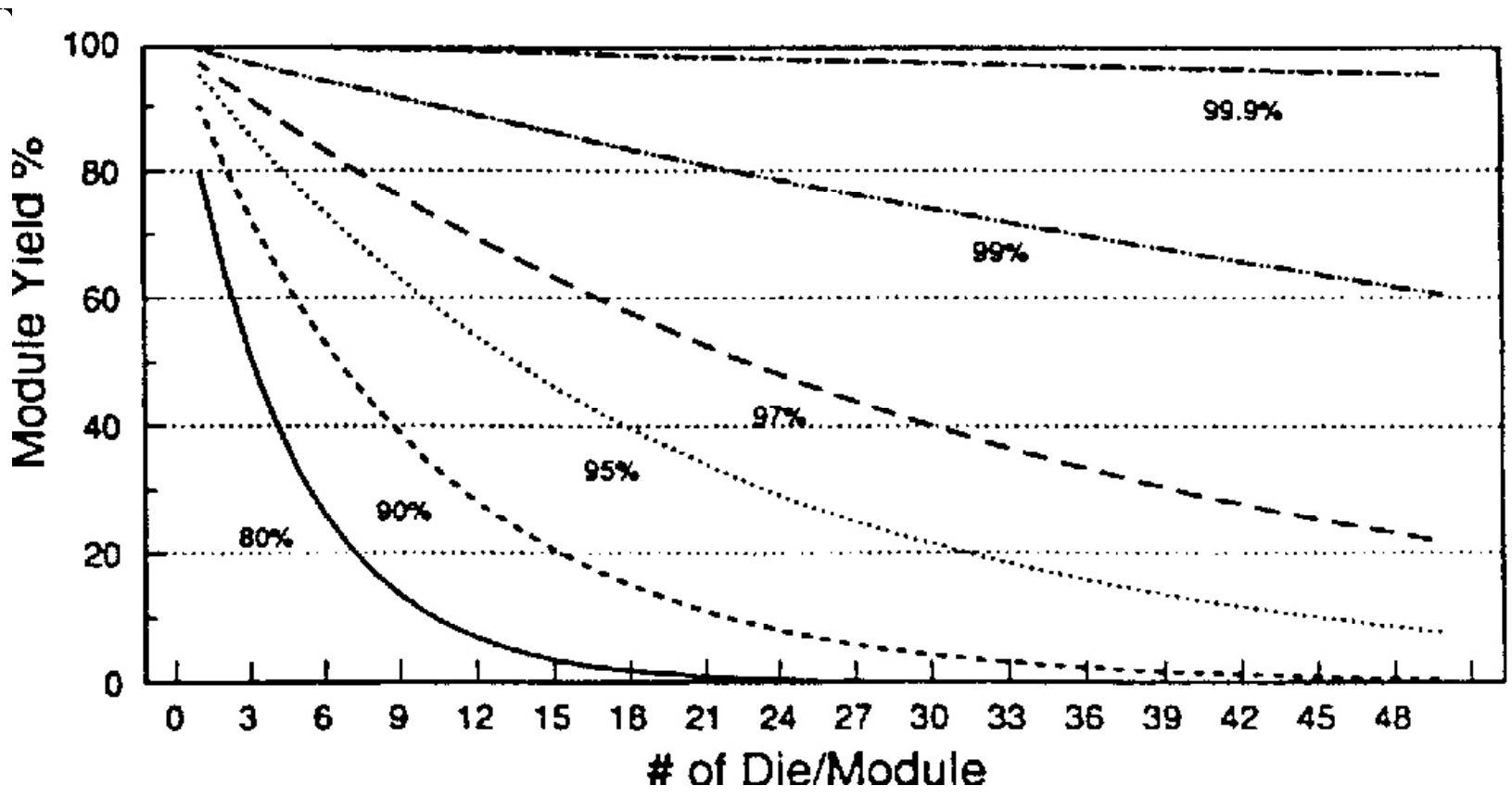
- In these days the die were relative simple using plus micron geometry's and as a result exhibited rather high quality and reliability after only a cursory probe.

- The die were small and with few bond pads. Die that failed at assembly test were easy to replace.

Bare Die Perspective

- As die became more complex, and line widths dropped below one micron two things were becoming apparent.
- In complex die, notably memories, wafer probe alone was not sufficient to provide acceptable quality and reliability.
- Un-screened infant mortality defects in these die were causing too many failures in time of modules in service.

Bare Die Perspective



KGD in the 1990's

- The challenge to provide KGD was first accepted by SEMATEC and MCC. MCC, under US government (DARPA) sponsorship, began a study of KGD processes that would last several years.
- In the end over thirty different approaches to enabling test and burn-in were examined by MCC and a group of industry KGD pioneers.
- Most of these approaches involved some sort of die "carrier".

KGD in the 1990's

- Several semiconductor manufacturers ventured into the arena, with most withdrawing soon after.
- It soon became evident that providing bare die of the quality and reliability of a comparable packaged part was not trivial.
- This spawned terms such as "Pretty darn good die"

KGD in the new Millennium, Good News and Bad News.

- Good news first.
- Due to advances in photolithography and wafer fabrication equipment, several manufacturers of small low I/O devices have eliminated wafer probe from their process. With wafer probe, they can furnish die with fairly high quality and reliability.

- Wafer Level Chip Scale Packaging (WLCSP) is becoming more popular. In this process, the die bond pads are re-located into an array and solder balls are applied to the new pads.

KGD in the new Millennium, Good News and Bad News.

- This is of course done at wafer level, and provides a die that can be post fab screened in sockets similar to standard packages. Many semiconductor manufacturers are considering this process and several are offering a limited number of part types as KGD.

- Iddq testing is back. Advances in test hardware have breathed new life into this old technique. The Die Products Consortium (DPC) has just completed a project to place metrics on the effectiveness of this process.

KGD in the new Millennium, Good News and Bad News.

- See www.dieproduct.com for details of this project.
- Aehr Test and and Chip Supply, Inc offer KGD processes that are adaptable to many different die products.

SiP Packaging

- There are a variety of packaging techniques for SiP, but most involve some sort of a ceramic, silicon or laminate substrate or interposer that the die and other components are assembled onto. This substrate can then be wire bonded into a metal header or a ceramic cavity package.

- The substrate can be an integral part of the package and in fact contain embedded SCAN circuitry that allows die isolation for trouble shooting.

Substrate Mechanical Quality/Reliability

- Substrates, particularity laminates, have physical properties that must be addressed.
- De-lamination and warping at temperature can cause quality issues at assembly and reliability issues in the field.
- Copper trace adhesion under temperature and humidity conditions ranges must be verified.
- And again solder mask integrity must be verified.

Assembly Considerations

- Die attach is probably the area where most quality and reliability problems can be caused.
- Die attach material must be of sufficient quantity and distribution in order to provide long term reliability.
- If Flip Chip is used, underfill must me used to control Tce mismatches between the die and the substrate.
- Handling of bare die, both manual and automatic, must be done with utmost care. The top surface of a semiconductor die is VERY susceptible to damage.

Assembly Considerations

- If the electrical attach method is wire-bond, attention must be paid to the cleanliness of the bond pads.
- If flip chip assembly is used for electrical interconnect, and other surface mount components are to be assembled onto the substrate, temperature profiles must be correct.
- FR4 glass transition temperature can be as low as 140°C, and BT as high as 180ºC. If reflow temperatures exceed the Tg of the substrate, you may wind up with a glob of a module.

Assembly Considerations

- If “glob top” is to be used to protect the die, the Tce of the epoxy must be considered in order not to pull off the bond wires during temperature excursions.

- SiP interconnect attach must be coordinated with module assembly. If the module is to connect to the outside world as a BGA, solder ball attach temperature must be coordinated with surface mount and flip chip attach temperatures.

Module Level Test

- At best it is very difficult to completely test individual semiconductor die after assembly. As stated earlier, die quality and reliability assurance is better done prior to assembly.
- However, the module can be tested “in-situ” to determine if it is accomplishing it’s intended purpose.
- This testing will identify bad die, assuming KGD were not used, or die that were damaged during assembly.

Module Level Burn-in

- Again eliminating infant mortality in semiconductor die after assembly is difficult at best. Memories need various patterns run during burn-in in order to completely stress all of the cells. This is difficult in-situ.

- Module burn-in temperature is limited to the lowest allowable component temperature. This may not be sufficient for other components.

- Module burn-in will provide some degree of reliability improvement, but it's ROI is questionable.

Conclusions

- This paper was intended to point out many of the areas that require attention when planning, designing, assembling and testing a SiP.

If not tended to before, during and after assembly they surely will make the process difficult and in the

end

cost