The Era of the 3-D System In Package (SIP) will be Ushered in by Japanese Mobile Phones

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Abstract
It is becoming impossible to realize the latest mobile phones and other mobile equipment without Chip Size Packages (CSP) and other high-density semiconductor package technology. At present, the most advanced mobile phones in the world are being made in Japan with a compact size and lightweight, but these rely for the most part on chip stacked CSP technology. This paper describes how mobile phone packaging technology has changed in Japan, from 1996 to 2001-2002, and how packaging is being done in the most recent mobile phones. In preparation for the coming era of 3-D System In Package (3-D SIP), this paper also describes the kind of technologies that are possible today, and how they will develop in the future.

Introduction
For Japanese mobile phones, 3rd-generation W-CDMA test service began in 2001, and began moving toward full-scale operation in the spring of the following year (2002). However, after 2nd- generation service started in 1993, progress was not innovative and limped along in typical Japanese fashion. Throughout the long life of the 2nd-generation, new functions were added a little at a time.

According to a survey by the Telecommunications Carriers Association, the cumulative total of subscribing mobile phones in Japan was 70.7 million at the end of June 2002 (a dissemination rate of almost 56% relative to population). In order to capture the small remaining portion of this already saturated market, as well as users looking to upgrade, communications companies are competing intensely by providing high-level functions like digital cameras and GPS in their newest models, which are serving as a bridge to the 3rd- generation. Aside from communication speed, the latest 2nd-generation mobile phones in Japan (typified by "i-Mode" compatible units) already have excellent 3rd-generation capabilities.

The fact that these most recent mobile phones achieve high-functionality in a compact, lightweight body is mainly due to high-density packaging technologies like Chip Size Package (CSP) technology (which came into use around 1996) and chip stacked CSP (which is a Japanese specialty); today, it is impossible to make a mobile phone without these technologies. Almost all Japanese mobile phones today use multiple chip stacked CSP, and phones in Europe, America and Asia will likely follow suit in the future.

This technology originally arose when memory chips (flash memory and SRAM) were stacked in three dimensions into a single CSP, but in the future, the technology will not be limited to combinations of memory chips and will evolve into the so-called "System In Package" where memory and logic chips are combined. In this paper, I will look at the latest packaging technologies for Japanese mobile phones, which are the most advanced in the world, and consider the future outlook for 3D System In Package.

The Latest Trends in Mobile Phones
In Japan, 2nd-generation mobile phone digital communication service (PDC system) began in the Tokyo area in 1993. In 1996, the number of subscribers exceeded 10 million units, and after that service areas were expanded and prices were lowered, resulting in explosive growth. Communication shifted from voice to data. The communication speed itself has not changed, so these phones are called "2nd- generation", but functionally they are almost the same as 3rd-generation. By connecting to services like "i-Mode", "J-sky" and "eZweb", these units are linked seamlessly with the Internet, and their multi-media capabilities already go beyond a mere "telephone". It is likely that Japanese mobile phones will continue to evolve while leading the world. In the next few years, we will see a shift to the 3rd-generation IMT2000 (W-CDMA, cdma2000).

Photo 1 shows some examples of the latest Japanese mobile phones in 2002, and Table 1 shows trends in current and future Japanese mobile phone functions and appearances, compared against 1996.

Photo 1 - The Latest Japanese Mobile Phones in 2002 (upper left: SH251i, lower right: SH51)

Latest Package Trends for Mobile Phones
Aside from the battery and the input/output section that acts as the user interface, a mobile phone is basically comprised of an RF section, base band section, and power supply section. The base band section in particular is

equipped with many core ICs, and the design of this part has a significant effect on functionality and size. Tables 2 through 6 give information such as the number of main packages and the number of memory chips in the base band section of mobile phones in Japan and Europe.

From the left, the Tables list: model name, total number of main packages, number of logic IC packages, number of memory IC packages, total flash memory/SRAM/pseudo-SRAM capacity, the number of individual chips contained in memory packages, and their memory capacity.

Tables 2 and 3 are for typical 2nd-generation (2G) mobile phones in Japan; Table 4 is for 3rd-generation (3G) in Japan, and Table 5 is for the 2.5th-generation (2.5G) in Europe. These Tables clarify a number of points.

Generally speaking, the latest 2nd-generation mobile phones in Japan are equipped with a total of 6-7 packages: 3 packages for logic, and 3 for memory. The key point here is that although Japanese mobile phones are equipped with a total of 5-6 memory chips, the number of memory packages is half of that. In other words, on the average, one package contains 2 chips and chip stacked technology is used for all of these.

As for the type of memory, not all of the increased capacity is provided with conventional flash memory and SRAM. As shown, low-cost pseudo-SRAM is also being used.

In the 3rd-generation, the number of packages and memory chips will increase greatly due to system expansion, but European mobile phones (which can be called 2.5G) still have a small system and a low package/memory count, so they are quite a bit behind Japanese mobile phones in their functional evolution.

Table 1 - Function and Appearance Trends for Japanese Mobile Phone, in 2001-2002 and the Future

2001-2002 (compared against 1996)	Future
1. Folding type is mainstream	1. Thinner, lighter weight
2. Larger display area	2. Shift to 3rd- generation, improved communication speed
3. Shift to color LCD, toward use of TFT liquid crystal	3. IR, BT, USB, and other interface support
4. More models with twin LCDs	4. Improved display picture quality
5. Models equipped with digital camera entering the mainstream	5. Security functions
6. Expansion of data transfer functions other than voice (mail, image etc.)	6. Roaming function
7. Connection to the Internet is an expected feature	7. Video phone functions
8. Expansion of applications using Java	8. TV signal reception
9. Expansion of functions like GPS, moving pictures and MP3…	9. Mobile banking support
10. Support for card interface	10. ....
11. Not much change in weight and size	
12. More colorful appearance	

Table 2 - Latest 2nd-Generation Mobile Phones in Japan, Main Package and Memory Chip Situation (1)

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap. Flash	TTL Cap. S/PSRAM	Memory Contents
J2G-1	6	3	3	64M	20M	32MF+4MS 32MF+8MS 8MS
J2G-2	7	4	3	64M	24M	32MF+4MS 32MF+4MS 16MPS
J2G-3	6	4	2	64M	16M	32MF+8MS 32MF+8MS
J2G-4	6	3	2	80M	20M	64MF +16MPS 16MF+4MS
J2G-5	7	5	2	64M	32M	32MF+8MS+8MS 32MF+8MS+8MS
J2G-6	6	4	2	48M	12M	32MF+8MS 16MF+4MS
J2G-7	6	4	2	48M	10M	16MF+4MS+2MS 32MF+4MS

Table 3 - Latest 2nd-Generation Mobile Phones in Japan, Main Package and Memory Chip Situation (2)

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap. Flash	TTL Cap. S/PSRAM	Memory Contents
E2.5G-1	6	5	1	64M	0M	64MF
E2.5G-2	8	6	2	96M	4M	32MF+4MS 64MF
E2.5G-3	6	3	3	48M	4M	32MF 16MF 4MS

Table 4 - 3rd-Generation Mobile Phones in Japan, Main Package and Memory Chip Situation

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap. Flash	TTL Cap. S/PSRAM	Memory Contents
J2G-8	7	5	2	64M	12M	32MF+8MS 32MF+4MS
J2G-9	7	4	3	72M	16M	32MF+8MS 32MF+8MS 8MF
J2G-10	11	7	4	96M	10M	32MF 32MF+4MS 16MF+4MS 16MF+2MS

Table 5 - 2.5th Generation Mobile Phones in Europe, Main Package and Memory Chip Situation

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap. Flash	TTL Cap. S/PSRAM	Memory Contents
J3G-1	10	7	3	160M	72M	32MF+ 8MS 64MF+64MF+16MPS 16MS +32MPS
J3G-2	12	6	6	192M	136M	64MF +16MPS 64MF +16MPS 64MF+ 8MS 32MPS 32MPS 32MPS

Table 6 - Summary of Main Package and Memory Chip Situation for Latest Mobile Phones in 2001-2002

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap. Flash	TTL Cap. S/PSRAM	Memory Chips
J2G/A	6-7	3-5	2-3	48-64M	10-32M	4-6
J2G/B	6-11	3-7	3-4	64-96M	10-16M	4-7
Japan3G	10-12	6-7	3-6	160-192M	72-136M	7-9
ER 2.5G	6-8	3-6	1-3	48-96M	0-4M	1-3

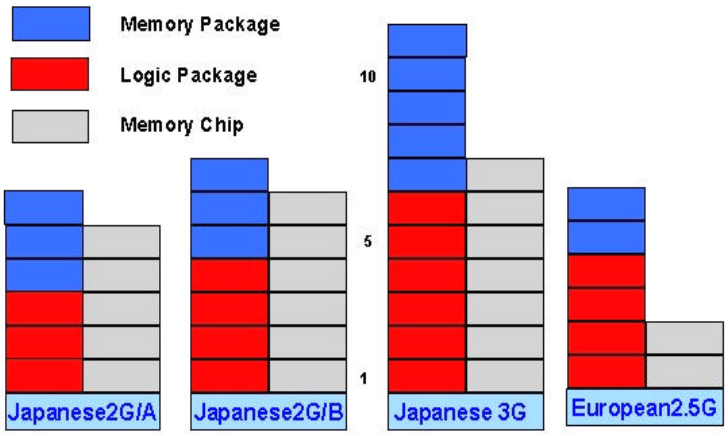

Figure 1 - Main Package Count and Memory Chip Count in Latest Mobile Phones

Changes and Future Development in Mobile Phone Package Technology

Starting around 1996, mobile phones achieved a weight/size of 100g/100cc, and the battle for greater compactness and lighter weight began. The key technologies for winning that battle were CSP and chip stacked CSP. Today's Japanese mobile phones lead the world in performance, compactness and lightness, and CSP and chip stacked CSP have definitely become de facto standard technologies.

IC chips increase in number as functionality grows, but increases in mounting area can be prevented by stacking those chips. In chip-stacked technology, the number of stacked chips is increased without changing the external form of the package. Figure 2 gives the mobile phone packaging situation for 1996 and 2001-2002. As shown, mounting boards have become smaller, but there has been almost no change in the number of main IC packages. In other words, although the number of chips has increased with evolution of function, an increase in the number of packages is suppressed by stacking multiple chips in a single package, and greater compactness is also achieved by mounting at higher density.

Since the survey for this paper was conducted (beginning of 2002), new mobile phones have already gone on sale in Japan. The 4-chip stacked CSP, which we were the first in the world to develop, has been incorporated into a number of models, and the increase in memory capacity has been striking.

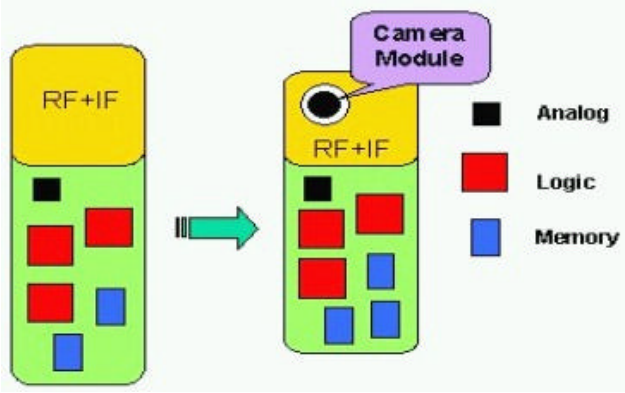

Figure 2 - Mobile Phone Packaging Situation in 1996 and 2001-2002

The types of memory are also increasing in order to maximize the advantages of each type; in the future, it is thought that mobile phones will also be equipped with types like NAND flash memory and SDRAM. Table 7 shows trends in system composition and packaging for Japanese mobile phones in 2001-2002 (compared against 1996), as well as predications for the future.

Mobile phones will continue to evolve without losing their "portability". Evolution in required functions will not wait for evolution in process technology. This evolution will affect not only memory ICs, but also logic ICs, and with expansion of functionality, we are already seeing separation into two CPUs -- a communication processor for communication functions, and an application processor. In order to build these growing systems into compact lightweight mobile phones, System In Package (SIP) is becoming indispensable because it offers a Time To Market (TTM) solution with high-density like that of stacked CSP.

Table 7 - System Composition and Packaging Trends for Japanese Mobile Phones in 2001-2002 and the Future

2001-2002 (compared against 1996)	Future
1. Almost no change in number of main packages 2. Almost all packages are CSP 3. Number of memory chips has increased 2 to 3 times, and chip stacked technology is used almost 100% 4. Memory capacity is 10~20 times greater, and is still increasing 5. Increased number of memory types (Flash, SRAM, PSRAM) 6. Chip stacked CSP for logic ICs is still uncommon	1. Reduction in board area for mounting main packages -> Requires greater thinness and multi-layer stacking 2. SIP will be used 3. Memory capacity will continue to increase 4. More memory types (NAND, SDRAM) 5. Separation in communication processor and application processor (2 CPUs)

On the other hand, there is no doubt that European and American mobile phones will continue to follow Japan's lead. Predictable trends are:

- Incorporation of digital cameras
- Switch to color liquid crystal display
- Increased memory capacity
- Stacked technology will become essential

SHARP has already begun exporting GSM standard models with digital camera capability and color liquid crystal display. In areas of Asia (Taiwan) with the same standard as Europe, i-Mode service began last summer, and the signs of that can already be seen.

Chip Stacked CSP Technology for Realizing 3-Dimensional System In Package

For a long time in the past, bare-chip packaging has been said to be the ultimate mounting technology. However, from the standpoint of silicon mounting efficiency, chip stacked CSP is clearly superior to this "ultimate mounting technology". The term "silicon mounting efficiency" refers to the function of a single silicon chip, per unit of mounting area. In other words, the maximum mounting efficiency for a bare-chip package is 100%. However, by stacking chips, it is possible to raise this value to 200% or 300%. The previous approach of increasing the resolution of the wafer process requires huge investment and development costs, and only involves two dimensions. In that sense, chip stacked CSP -- a technology where stacking is done while maintaining chip size -- is a revolutionary form of 3-dimensional integration. Figure 3 shows the development timeline and silicon mounting efficiency of chip stacked CSP.

The history of the 3-D System In Package actually began in 1998. In 1998, we stacked flash memory and SRAM (previously supplied in two packages) into a single CSP, and were the first in the world to install a package of this type in a mobile phone. At that time, there was an intensification of the battle for mobile phone compactness and lightness, but we regard this as the beginning of the history of the 3-D System In Package.

Of course, the combination at that time involved memory and memory (not memory and logic), but the basic chip stacked CSP technology has developed as is into a technology for achieving practical implementation of 3-D System In Package.

With current practical technology, it is possible to stack up to 4 chips, and the number of stacking layers will increase in the future. How fast will this happen? And how many layers will it ultimately be possible to stack? The author has proposed an empirical law for chip-stacked packages, as shown in Figure 4. If this chip stacked law continues to hold in the future, like Moore's Law, the number of chip stacking layers will increase at a rate of 1 layer every 18 months, and in 2009, 10 layer stacks will be achieved.

However, the "invisible ceiling" for package thickness (i.e. package height) is tacitly understood to be 1.4mm. The situation is shown in Figure 5. In other words, multi-layer stacking technology is linked with technology for achieving greater thinness. It may not be necessary to stack 10 layers, but it will be possible to achieve thinner packages stacking multiple chips with this technology.

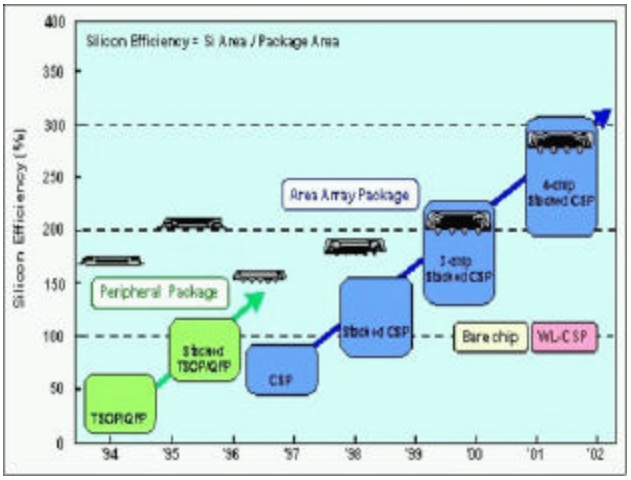

Figure 3 - Chip Stacked CSP Development Timeline and Silicon Mounting Efficiency

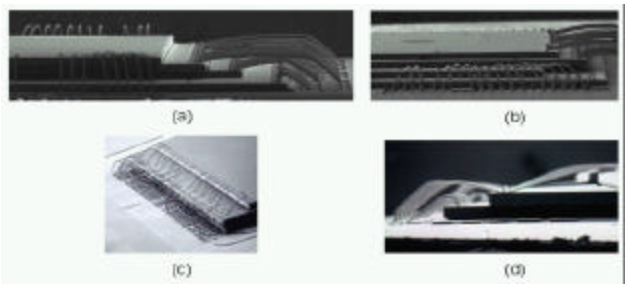

Photo 2 - Basic examples of Chip Stacked CSP

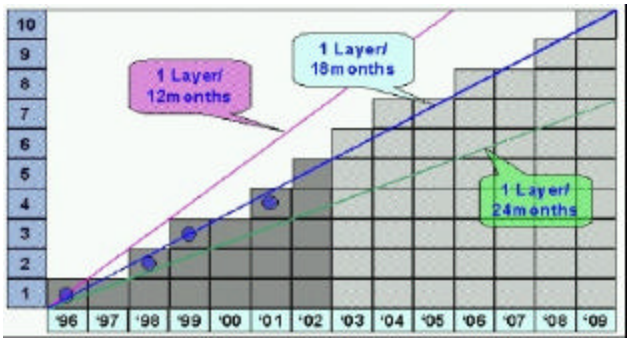

Figure 4 - Empirical Law for Chip Stacking

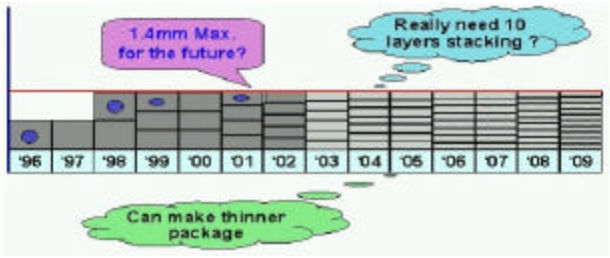

Figure 5 - Is the Ceiling a 1.4mm Package Height?

Package Stacked Technology for Realizing 3 Dimensional System In Package

There are various forms of stacking: wafer stacking, chip stacking and package stacking. For the last few years we have focused our development on stacking chips. However, today we can stack 4 chips, so should we still continue to concentrate on development of chip-stacked technology? We looked into package stacking for the answer, and in March 2002, we announced "3-D SIP with a new structure" to propose guidelines for the differential use of chip and package stacking. Figure 6 shows the dividing line in different cases for memory stacking, and System In Package (SIP) combining memory and logic.

In combining memory chips at the present time, higher mounting density can be obtained by chip stacking, up to about 4 chips, and in this case it is better to use chip stacking. On the other hand, in a so-called System In Package combining logic and memory chips, package stacked technology is the optimal solution, even for 4 chip combinations. Photo 3 and Figure 7 show a package stacked SIP we have developed.

Even though this package can be called package stacked, it is basically two chips stacked in a single package, and the package height is only 0.5mm. Naturally, one chip can be used alone, and in that case the height is 0.4mm.

Combining these chips, we obtain (for example) the left side, which shows a cross-sectional diagram where 6 memory chips are stacked with a package height of 1.5mm. The right side shows an example where one logic chip is stacked with 4 memory chips (for a total of 5 chips), and the height comes in under 1.4mm.

We want to make this package the de facto standard package for SIP.

Table 8 shows the advantages of chip stacking and package stacking, and our proposal for creating a de facto standard is shown in Figure 8. We want to standardize not only the package outer form; we also want to standardize use of both ends of the rectangular package for memory terminals, and use of the other parts for logic ASIC terminals. We also plan to standardize various types to memory terminals to handle different memory combinations.

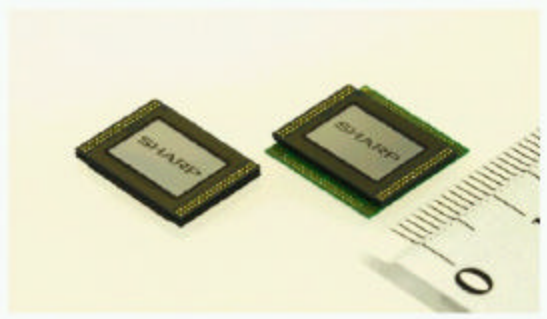

Photo 3 - Package Stacked SIP

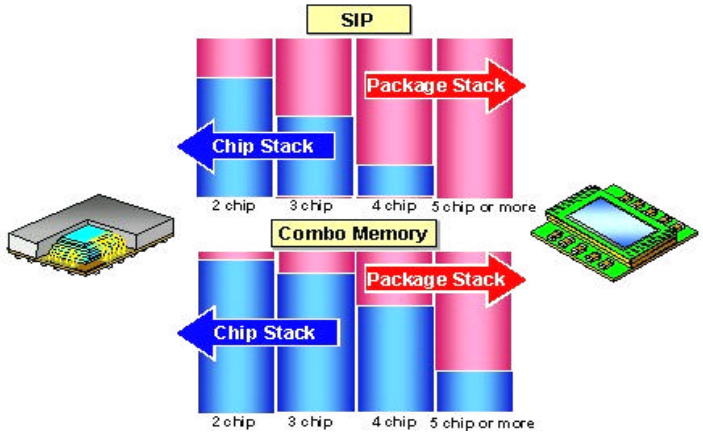

Figure 6 - Differential Use of Chip and Package Stacking

Figure 7 - Package Stacked SIP Cross-section Diagram

Table 8 - Advantages of Chip Stacked Technology and Package Stacked Technology

Chip Stacked Technology	Package Stacked Technology
1. Small package size 2. Current production equipment can be used 3. Low package cost	1. Few limitations on combinations (stacked chip type, number) 2. Stacking can be done after testing, so there is no test yield loss 3. Passive components can be incorporated 4. Easy combination with other company's chips

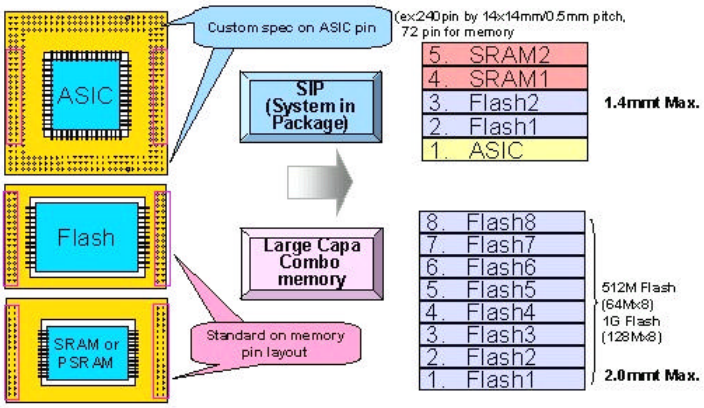

Figure 8 - Standardization Plan for Package Stacked SIP

The Era of the 3-dimensional System In Package

The first 10 years of the 21st century will be the era of the 3-dimensional System In Package. Why will the industry be in favor of 3-dimensional SIP rather than to go with System On Chip (SoC) and 2-dimensional technology?

Behind the evolution of electronic appliances in the past, there was the evolution of wafer processing, notably the process dimensional reduction of the wafers. As 0.1 micron processing is becoming real, however, the deterioration of electronic characteristics caused by size reduction is also becoming apparent. On the other hand, the cost of wafer manufacturing has been skyrocketing; building a factory to produce such wafers can cost several billion dollars, and it is said to cost a million dollars to prepare a masking set per product. Plans to make the financial ends meet with such products have not yet hit the table. It is therefore unrealistic to expect SoC to materialize as a solution for systematization while relying solely on the evolution of the wafer processing technology.

System In Package technology, on the other hand, is capable of incorporating several different processes, such as memory and logic, or even analog aspects, into a single package; it is suitable for developing products while optimizing characteristics, cost, and production time. To realize the SIP, chip stacked technology at the core is proven feasible by hundreds of millions of products, while successfully bundling logic IC and memory IC.

Moreover, Figure 9 shows the silicon mounting efficiency of SOB (System On Board), SoC and 2- and 3-dimensional SIP. It is clear that 3-dimensional SIP is superior. In other words, 3-dimensional SIP has superior function per unit area, compared with both SOB and SoC.

Naturally, this does not mean that SIP is always superior; with clock speed of one GHz or more, systems may have performance speed issues. For devices like calculators and electronic clocks with limited function and a fixed system size, SoC is probably the better choice as technology evolves. However, mobile equipment like mobile phones is still evolving while maintaining low power consumption. That is, functionality is still growing. For equipment like this, SIP (and 3-dimensional SIP in particular) is superior, and future products will likely be commercialized using SIP.

In the future, mobile phones will haul us to the era of the true 3-dimensional System In Package. We are already seeing the development of package technology for that purpose.

The question as to whether the System In Package will be successful is not a technical problem. Even the best company cannot supply all the optimal system solutions, and it is difficult for one company to cover an entire business. The problem is how to build a business model between multiple companies, including both manufacturers and customers.

Since 1970, the package industry has developed decade by decade, and in conclusion the author predicts that the era of 3-dimensional SIP will arrive in the first 10 years of the 21st century.

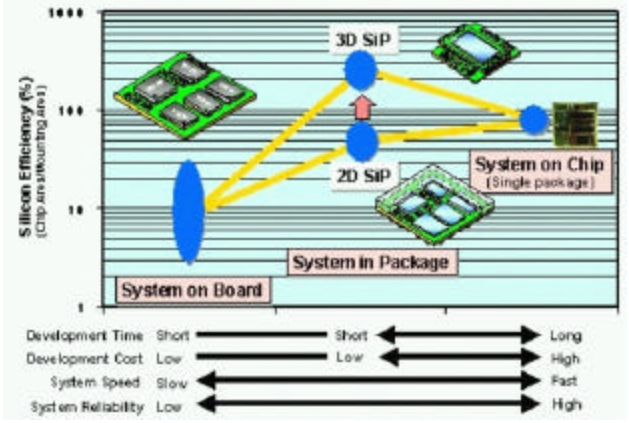

Figure 9 - Silicon Mounting Efficiency of SOB, SIP and SoC

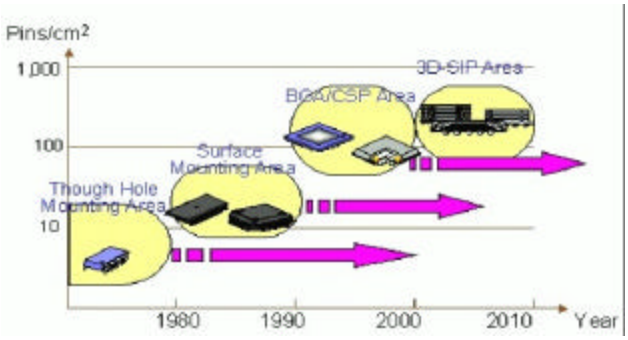

Figure 10 - The Era of the New Package "3-dimensional SIP"

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