3D-System In Package(SIP) Era Driven by Japanese Mobile Phones

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- Latest Trends in Mobile Phones
- Latest Trends in Packaging of Mobile Phones
- History of Packaging of Mobile Phones
- Chip Stacked CSP Technology for 3D-System In Package(SIP)
- Package Stacked Technology for 3D-System In Package(SIP)
- 3D-System In Package(SIP) Era

- Latest Trends in Mobile Phones

Function and Appearance Trends for Japanese Mobile Phones, in 2001-2002 and the Future

End of July 2002,digital camera equipped model went over 6 million out of 70.7milion subscribers

2001-2002 (compared against 199	Future
1. Folding type is mainstream	1. Thinner, lighter weight
2. Larger display area	2. Shift to 3rd Generation, improved communication speed
3. Shift to color LCD, toward use of TFT liquid crystal	3. IR, BT, USB, and other interface support
4. More models with twin LCDs	4. Improved display picture quality
5. Models equipped with digital camera entering the mainstream	5. Security functions
6. Expansion of data transfer functions other than voice (mail, image etc.)	6. Roaming function
7. Connection to the Internet is an expected feature	7. Video phone functions
8. Expansion of applications using Java	8. TV signal reception
9. Expansion of functions like GPS, moving pictures and MP3…	9. Mobile banking support
10. Support for card interface	10. ….
11. Not much change in weight and size	
12. More colorful appearance	

-Latest Trends in Packaging of Mobile Phones

Main Packages and ICs in Japanese 2G Mobile Phones (2001-2002)/1

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Contents
				Flash	S/PSRAM	
J2G-1	6	3	3	64M	20M	32MF+4MS 32MF+8MS 8MS
J2G-2	7	4	3	64M	24M	32MF+4MS 32MF+4MS 16MPS
J2G-3	6	4	2	64M	16M	32MF+8MS 32MF+8MS
J2G-4	6	3	2	80M	20M	64MF +16MPS 16MF+4MS
J2G-5	7	5	2	64M	32M	32MF+8MS+8MS 32MF+8MS+8MS
J2G-6	6	4	2	48M	12M	32MF+8MS 16MF+4MS
J2G-7	6	4	2	48M	10M	16MF+4MS+2MS 32MF+4MS

Main Packages and ICs in Japanese 2G Mobile Phones (2001-2002)/2

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Contents
				Flash	S/PSRAM	
J2G-8	7	5	2	64M	12M	32MF+8MS 32MF+4MS
J2G-9	7	4	3	72M	16M	32MF+8MS 32MF+8MS 8MF
J2G-10	11	7	4	96M	10M	32MF 32MF+4MS 16MF+4MS 16MF+2MS

Main Packages and ICs in Japanese 3G Mobile Phones (2001-2002)/3

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Contents
				Flash	S/PSRAM	
J3G-1	10	7	3	160M	72M	32MF+ 8MS 64MF+64MF+16MPS 16MS +32MPS
J3G-2	12	6	6	192M	136M	64MF +16MPS 64MF +16MPS 64MF+ 8MS 32MPS 32MPS 32MPS

Main Packages and ICs in European 2.5G Mobile Phones (2001-2002)

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Contents
				Flash	S/PSRAM	
E2.5G-1	6	5	1	64M	0M	64MF
E2.5G-2	8	6	2	96M	4M	32MF+4MS 64MF
E2.5G-3	6	3	3	48M	4M	32MF 16MF 4MS

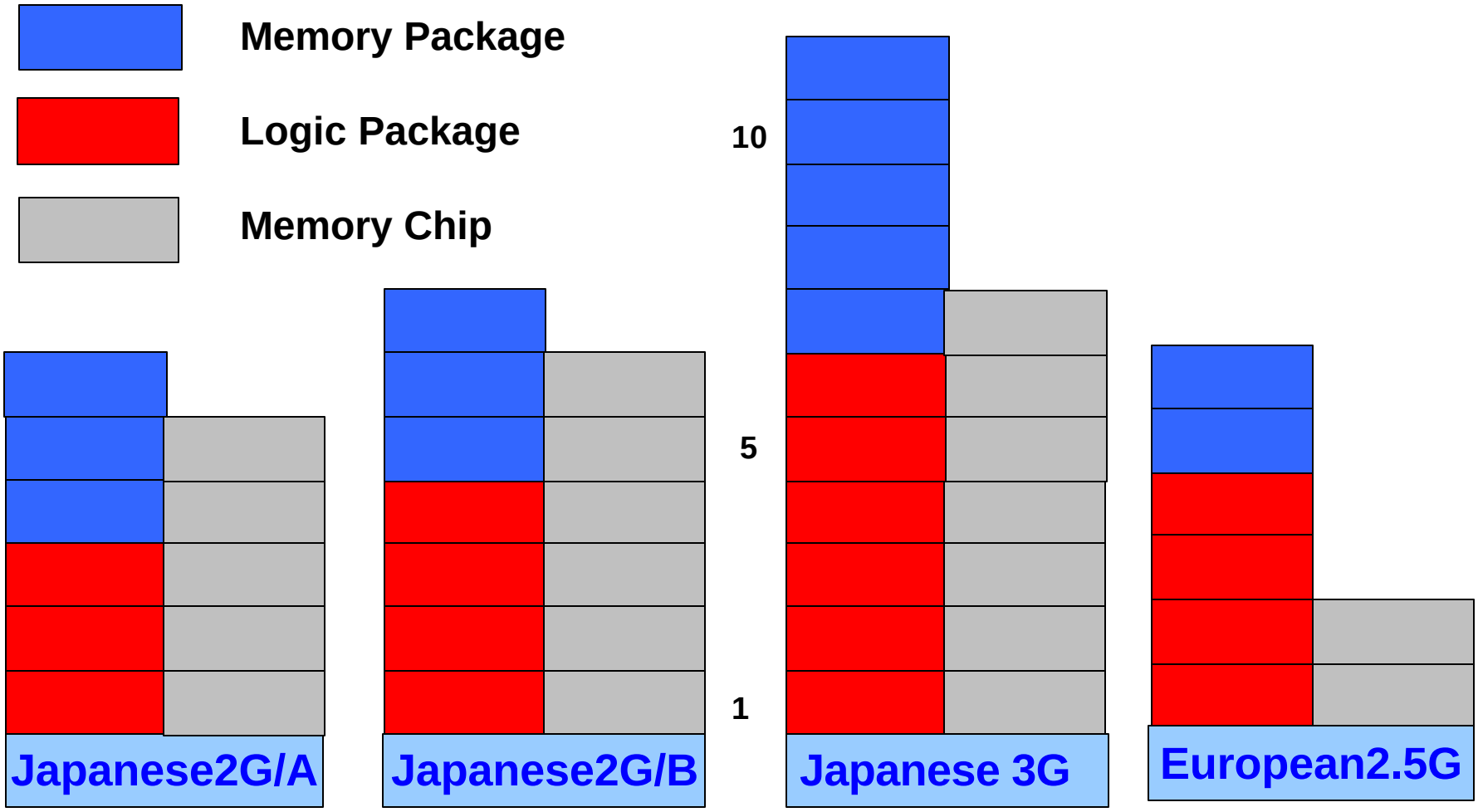
Main Packages and ICs in Latest Mobile Phones(2001-2002)

2002 Latest 2G model in Japan

Memory PKG :2-3
Flash 96-192M
S/PSRAM 36-72M
Memory Chip: 5-8

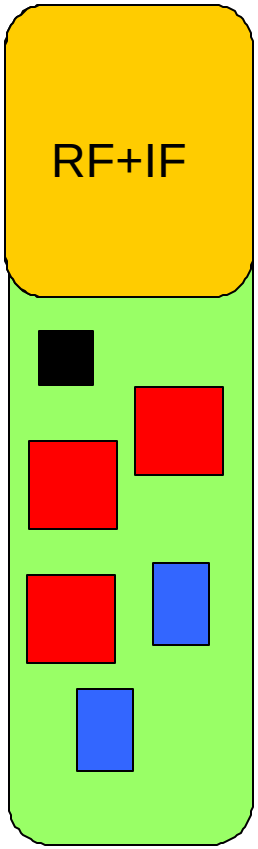
Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Chips
				Flash	S/PSRAM	
J2G/A	6-7	3-5	2-3	48-64M	10-32M	4-6
J2G/B	6-11	3-7	3-4	64-96M	10-16M	4-7
Japan3G	10-12	6-7	3-6	160-192M	72-136M	7-9
ER 2.5G	6-8	3-6	1-3	48-96M	0- 4M	1-3

Main Package Count and Memory Chip Count in Latest Mobile Phones (2001-2002)

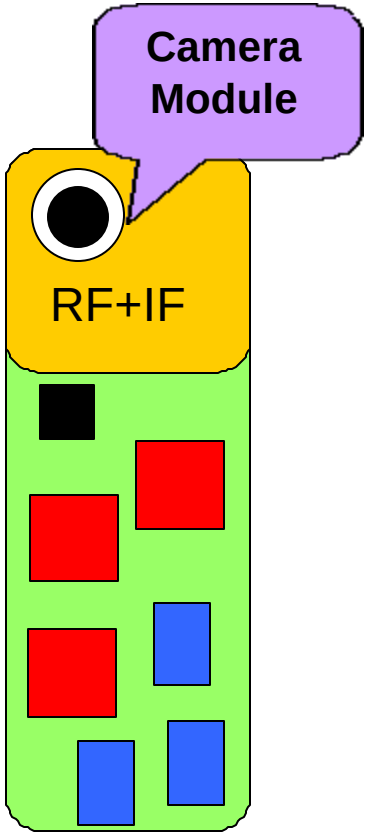


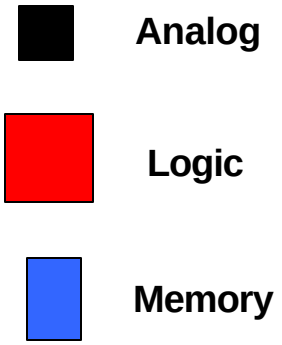
- History of Packaging of Mobile Phones

Mobile Phones Packaging Situation in 1996 and 2001-2002



1. Almost no change in number of main packages
2. Almost all packages are CSP
3. Number of memory chips has increased 2 to 3 times, and chip stacked technology is used almost 100%
4. Memory capacity is 10~20 times greater, and is still increasing
5. Increased number of memory types (Flash, SRAM, PSRAM)
6. Chip stacked CSP for logic ICs is still uncommon

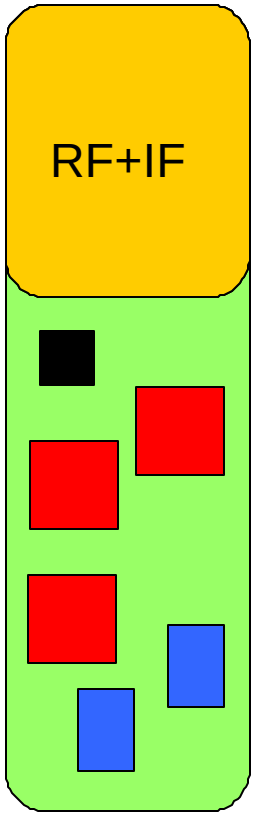




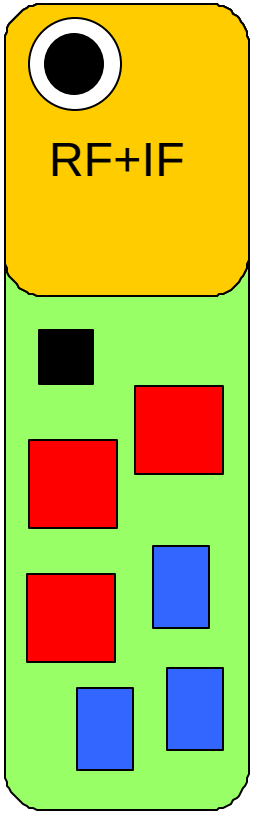
1996

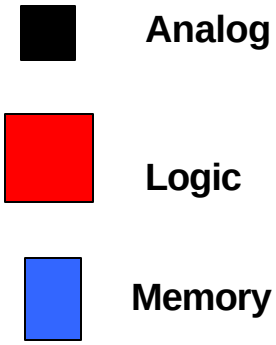
2001 ~ 2002

There is No Doubt that European and American Mobile Phones will Continue to Follow Japan's Lead.

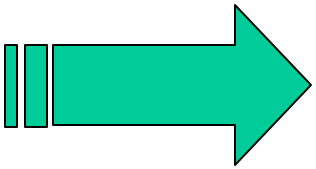


1. Incorporation of digital cameras
2. Switch to color liquid crystal display
3. Increased memory capacity
4. Stacked technology will become essential





Current 2.5G



Future Phones

System Composition and Packaging Trends for Japanese Mobile Phones in the Future

1. Reduction in board area for mounting main packages
   -> Requires greater thinness and multi-layer stacking

2. SIP will be used

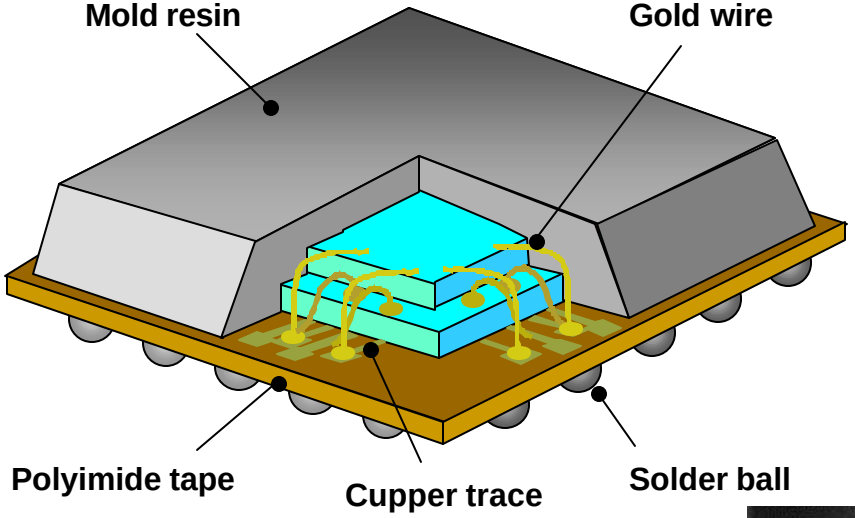
3. Memory capacity will continue to increase

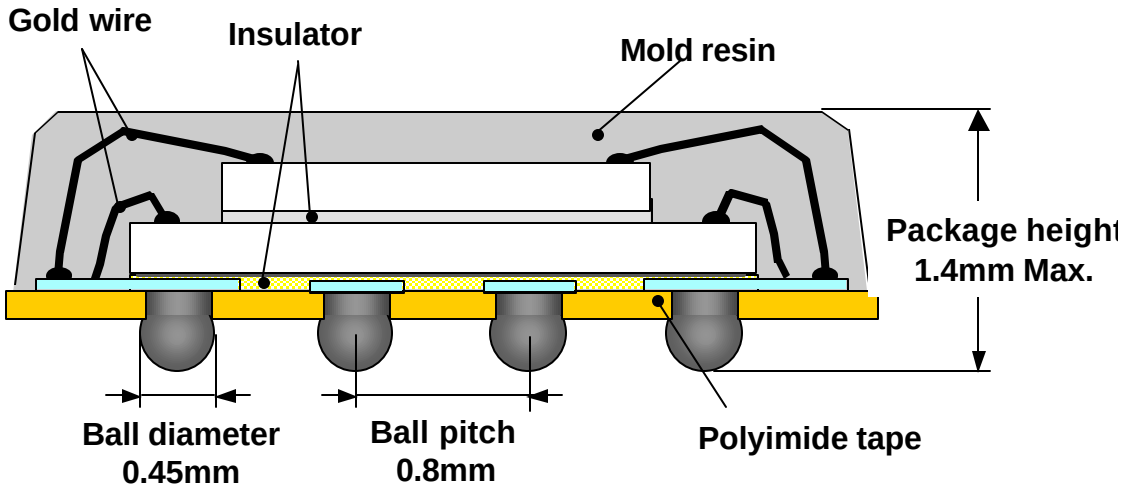
4. More memory types (NAND, SDRAM)

5. Separation in communication processor and application processor (2 CPUs)...

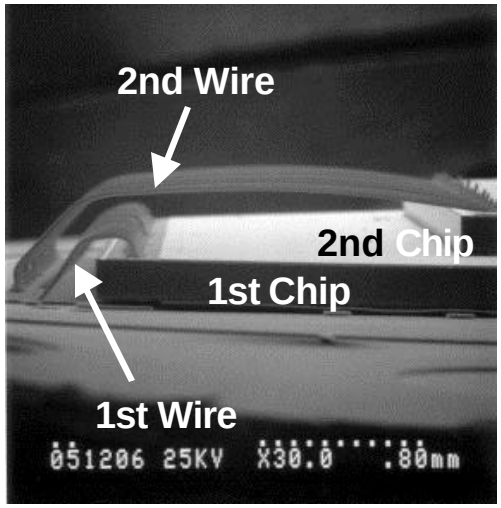
-Chip Stacked CSP Technology for 3D-System In Package(SIP)

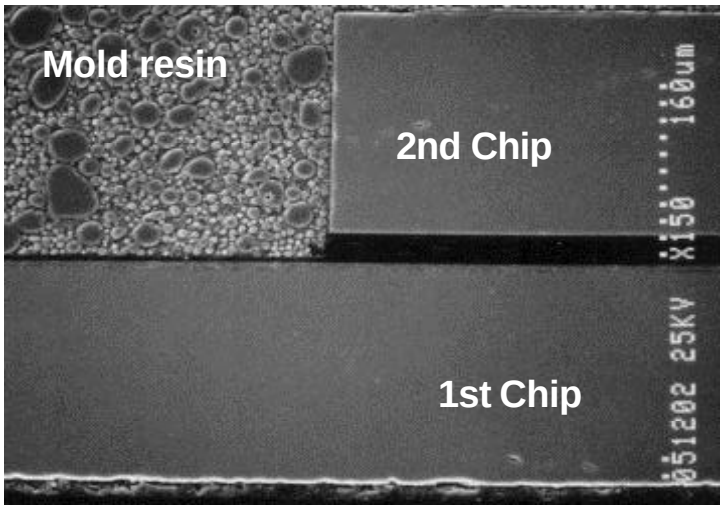
2-Chip Stacked CSP



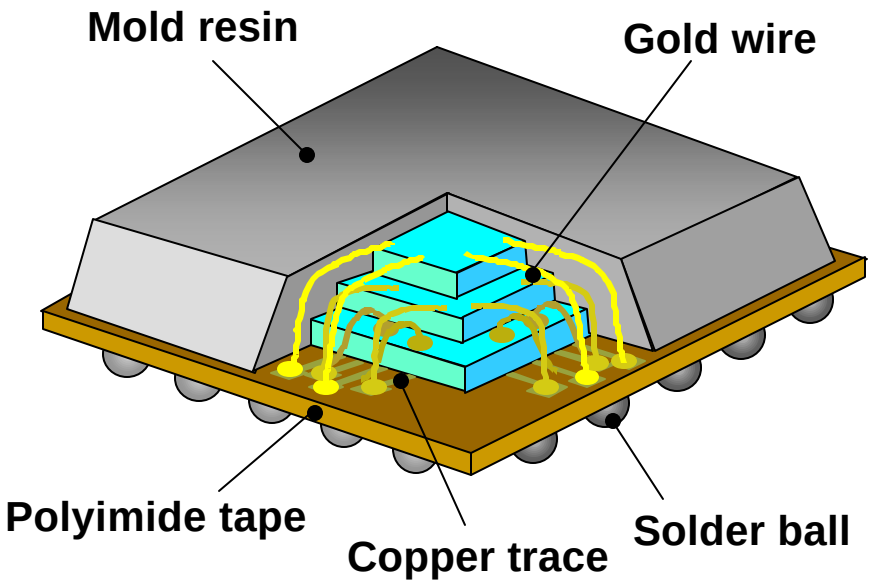


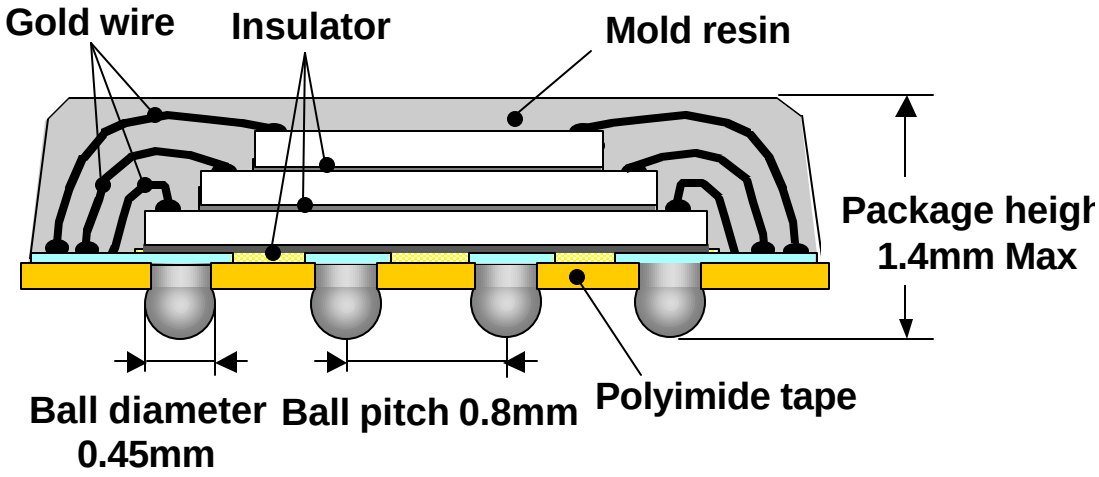
World First 1998



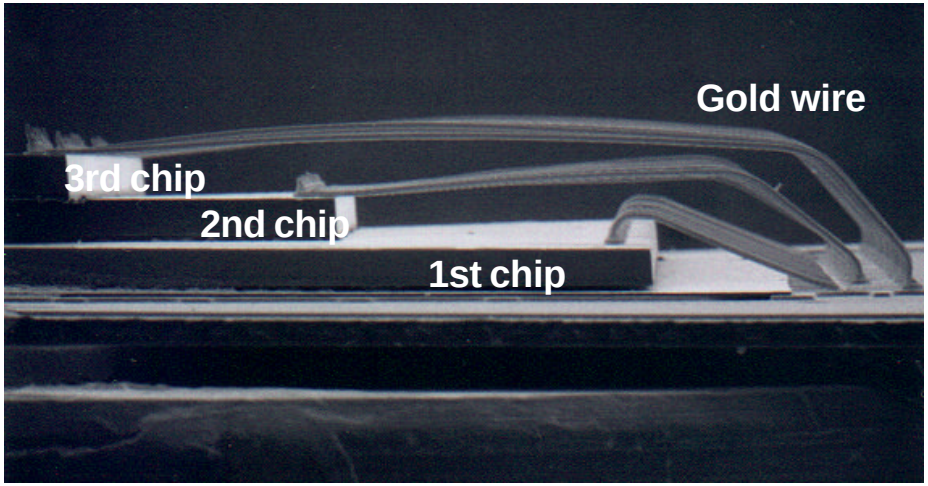


3-Chip Stacked CSP

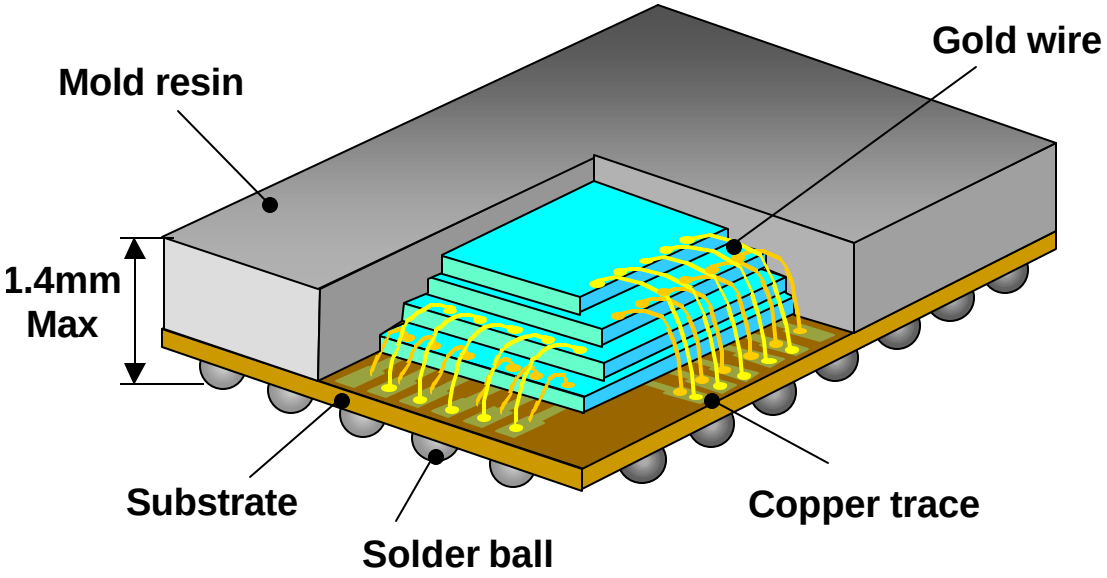


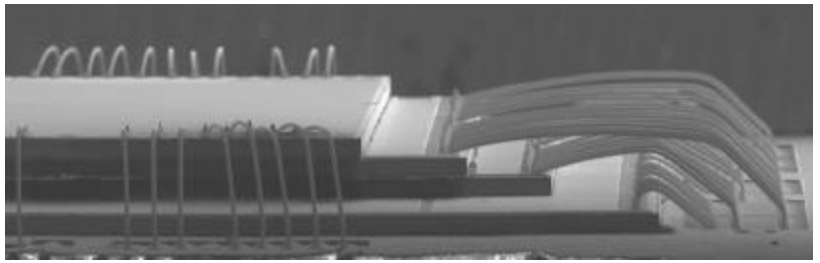


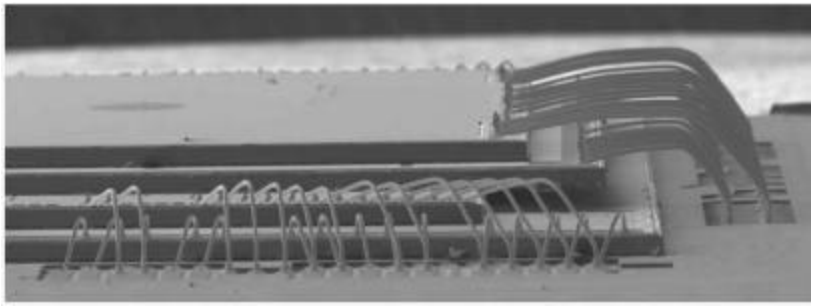
World First 1999

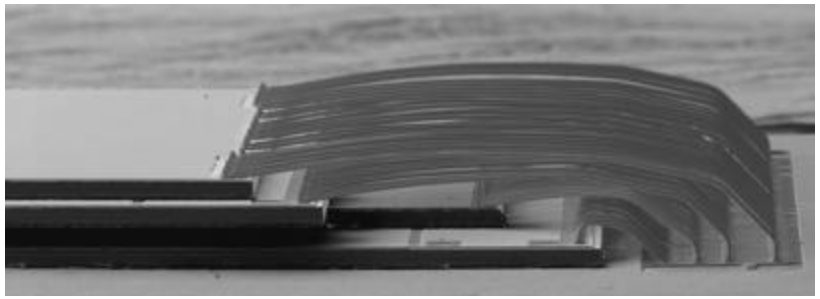


4-Chip Stacked CSP



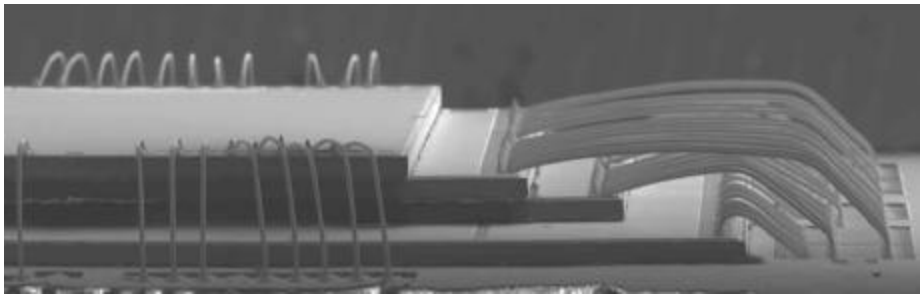




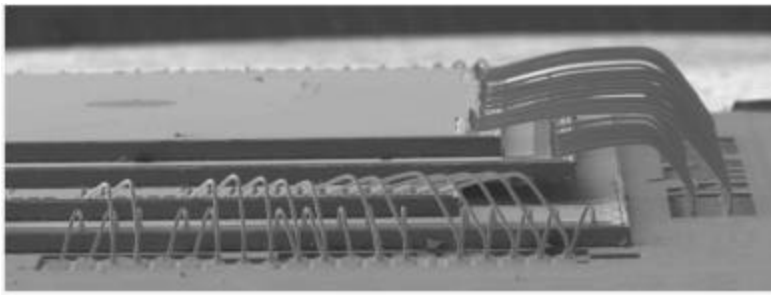


World First 2001

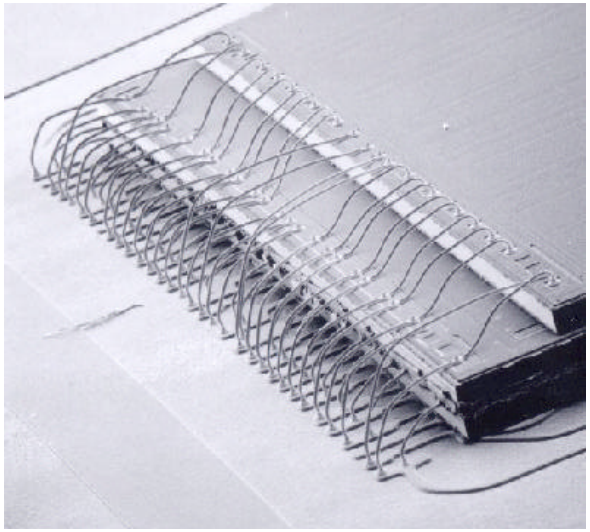
Eliminating Limitation on Combinations



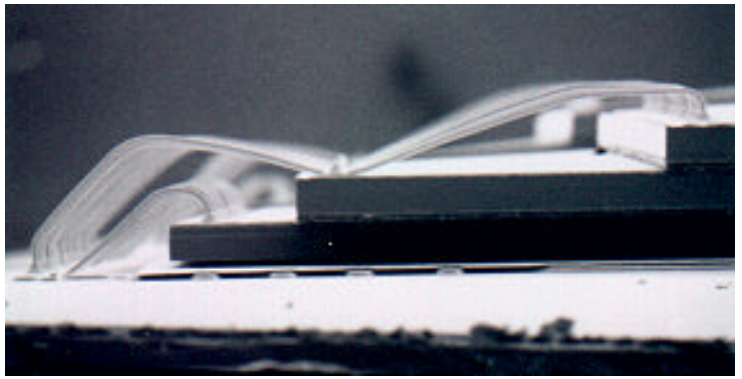
(a) Pyramid system



(b) Over hanging structure

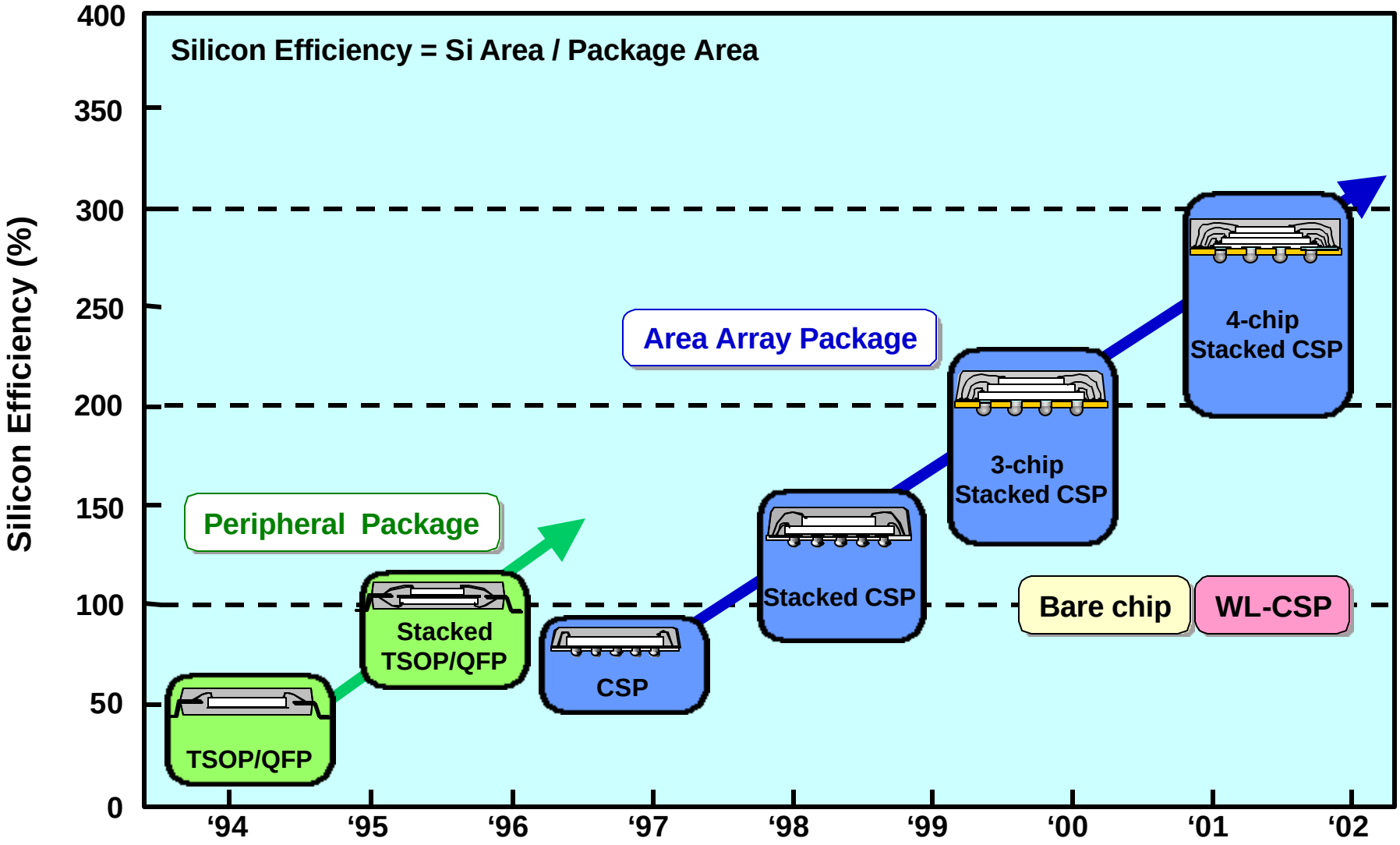


(c) Same chip structure

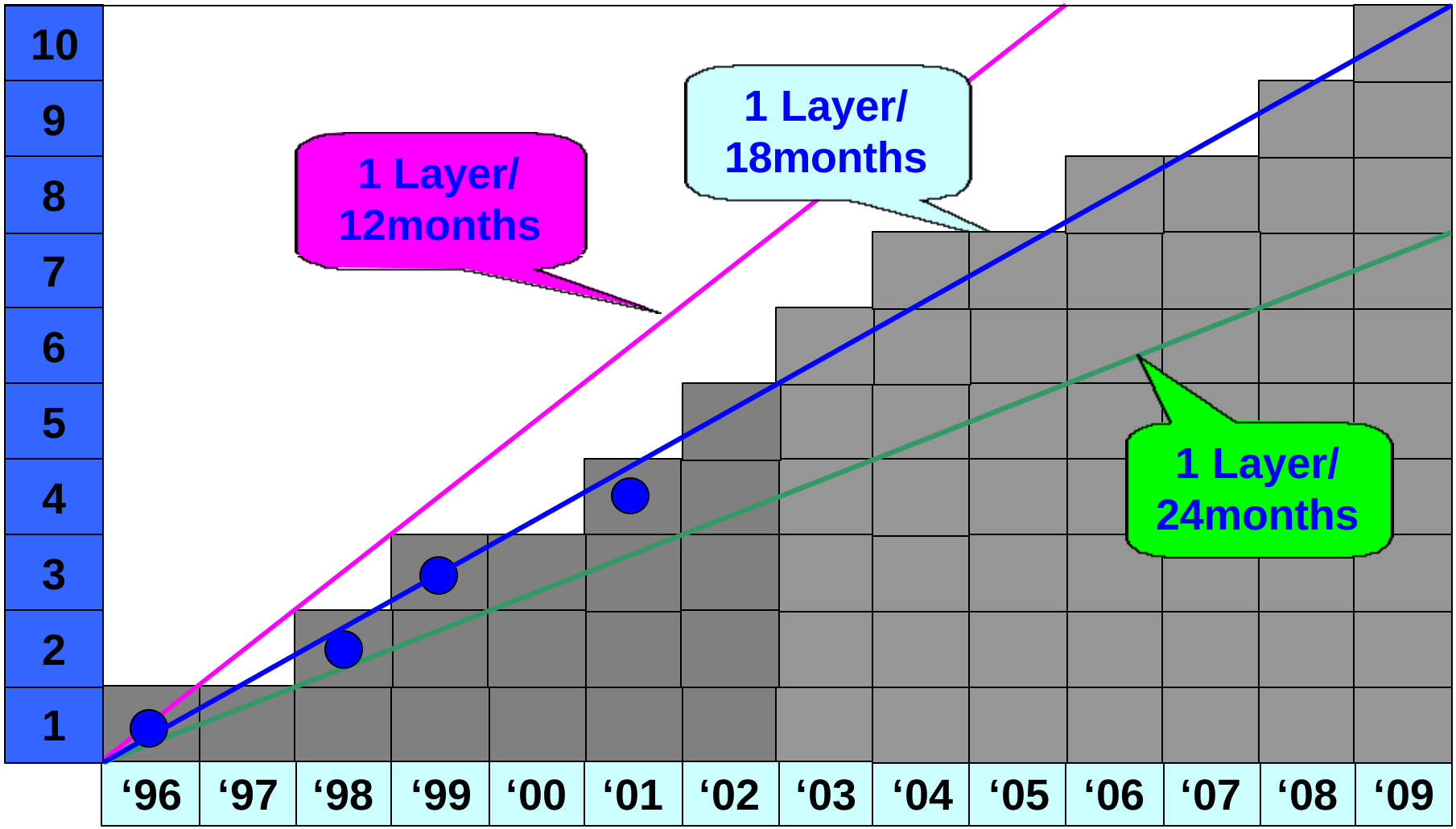


(d) Chip to Chip Wire bonding

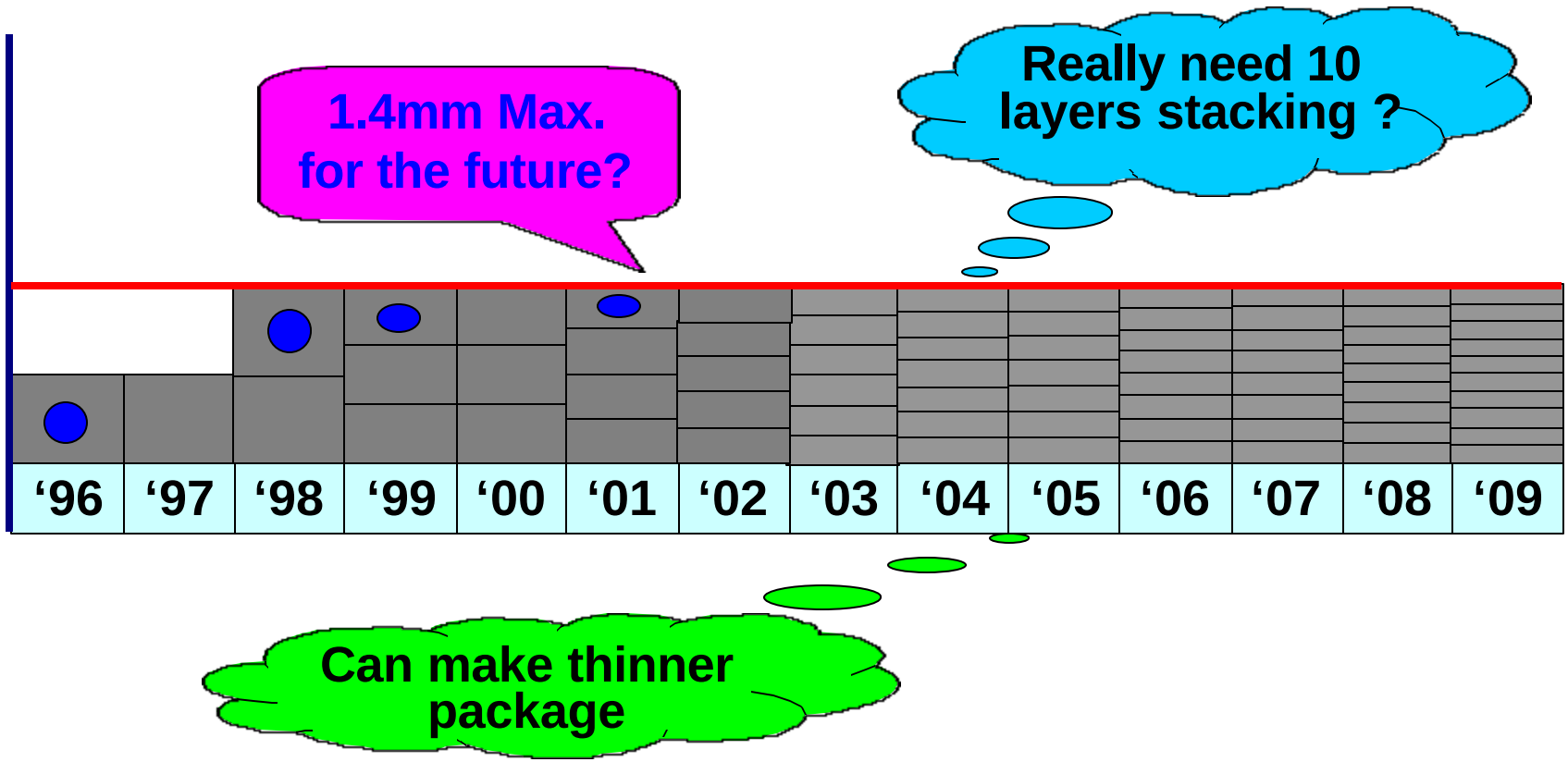
Silicon Efficiency



Empirical Law for Chip Stacking

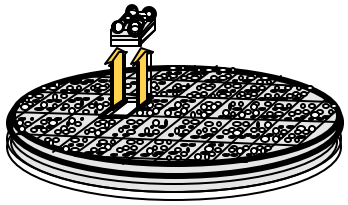


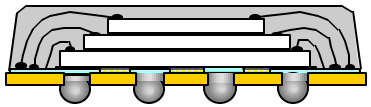
Is the Ceiling a 1.4mm Package Height?

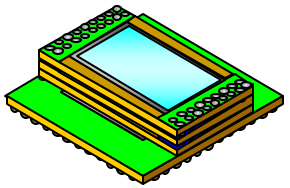


-Package Stacked Technology for 3D-System In Package(SIP)

Comparison of Stacking Technology



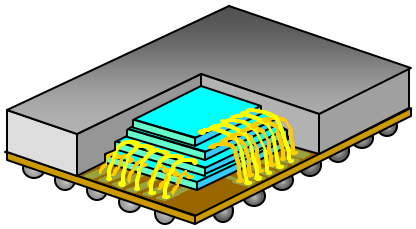


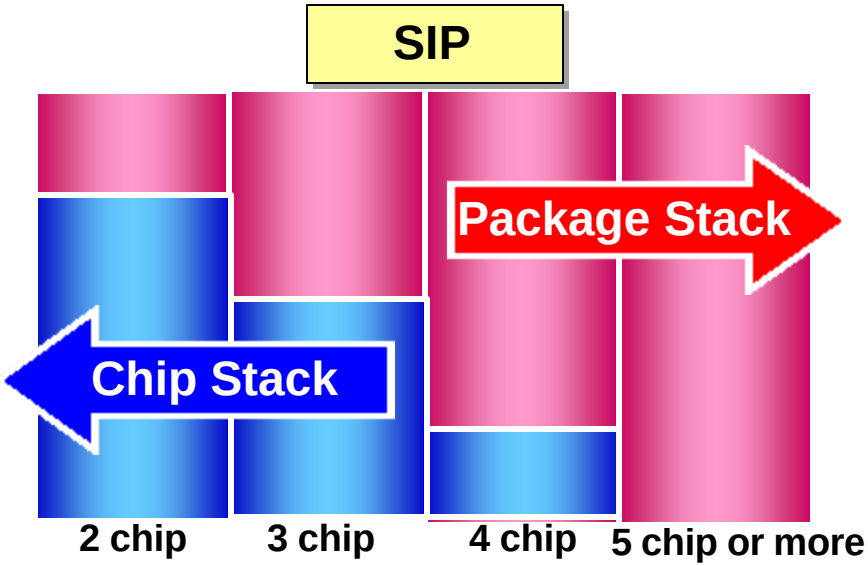


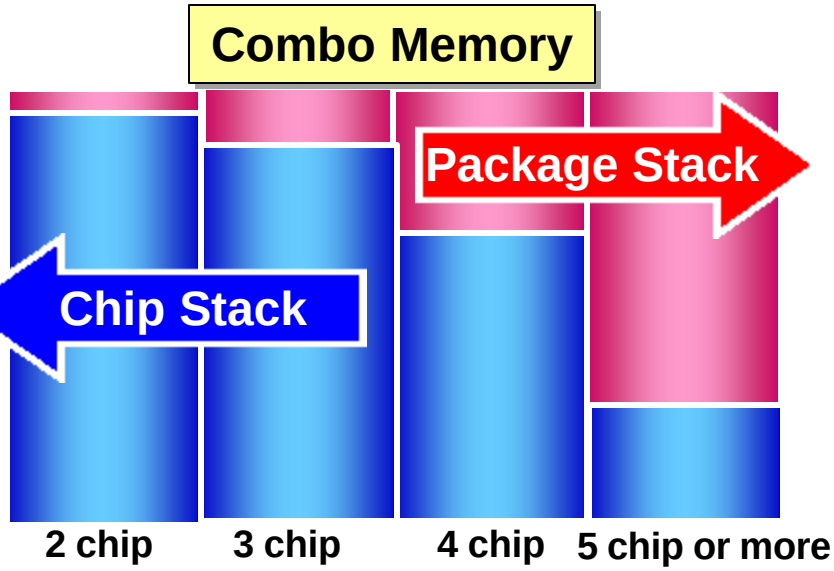
Wafer level	Chip level	Package level
Integration density		
Electrical performance		
Process easiness		
Ease of Design or Flexibility,TTM		

Chip Stacking or Package Stacking ?

*Small package size
*Current assy equipment usable
*Advantage on assy cost

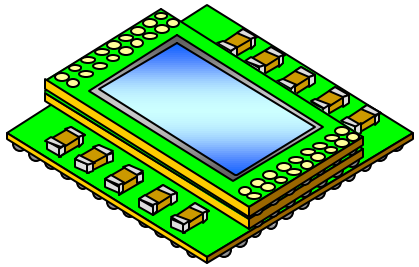






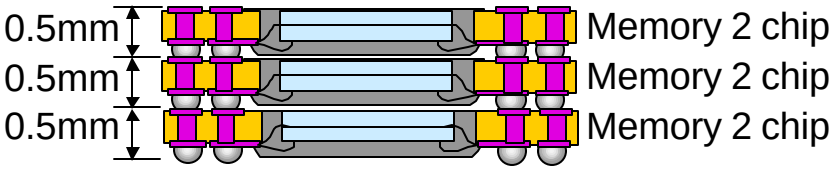
Advantage

*No stack qty limitation
*Any type of chip stackable including ASIC
*Passive device stackable
*Flexible for different memory capa.requirement
*Enable SIP with other LSI manufacturer
*Better stack yield

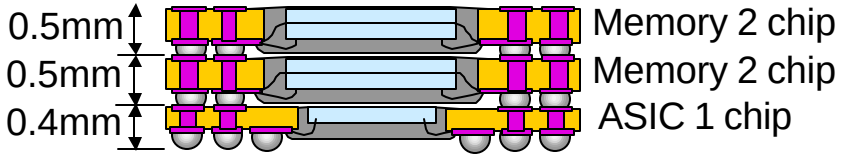


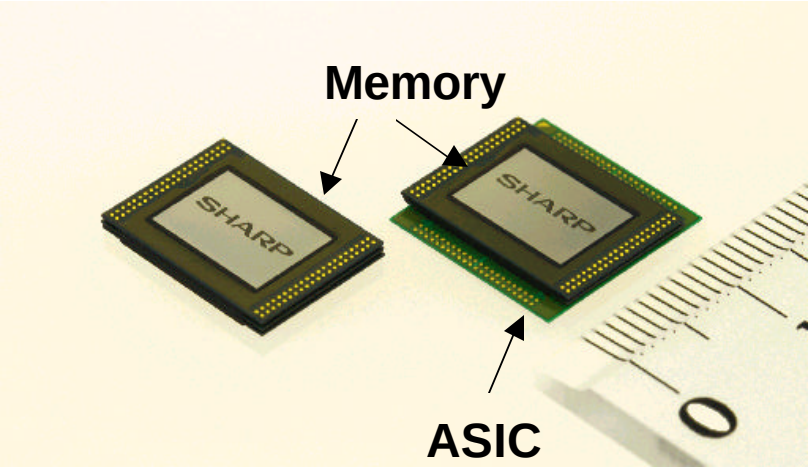
3D-System in Package (SIP) Technology
-Package Stack Technology

Large Capacity Combo Memory
(Memory 4-6 chip)

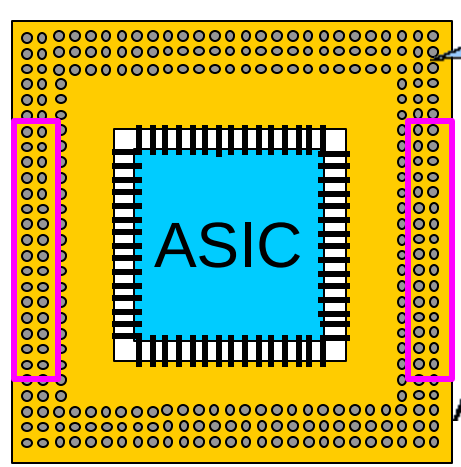


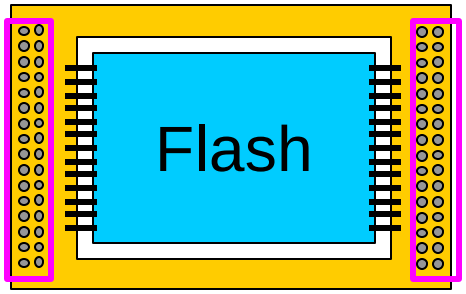
System LSI
(ASIC:1 chip + Memory 4 chip)

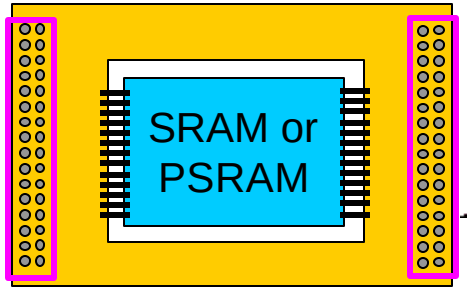




Standard Proposal on Pin Layout of SIP Device







Custom spec on ASIC pin

(ex:240pin by 14x14mm/0.5mm pitch,
72 pin for memory

SIP (System in Package)

5.	SRAM2
4.	SRAM1
3.	Flash2
2.	Flash1
1.	ASIC

1.4mmt Max

Large Capa Combo memory

8.	Flash8
7.	Flash7
6.	Flash6
5.	Flash5
4.	Flash4
3.	Flash3
2.	Flash2
1.	Flash1

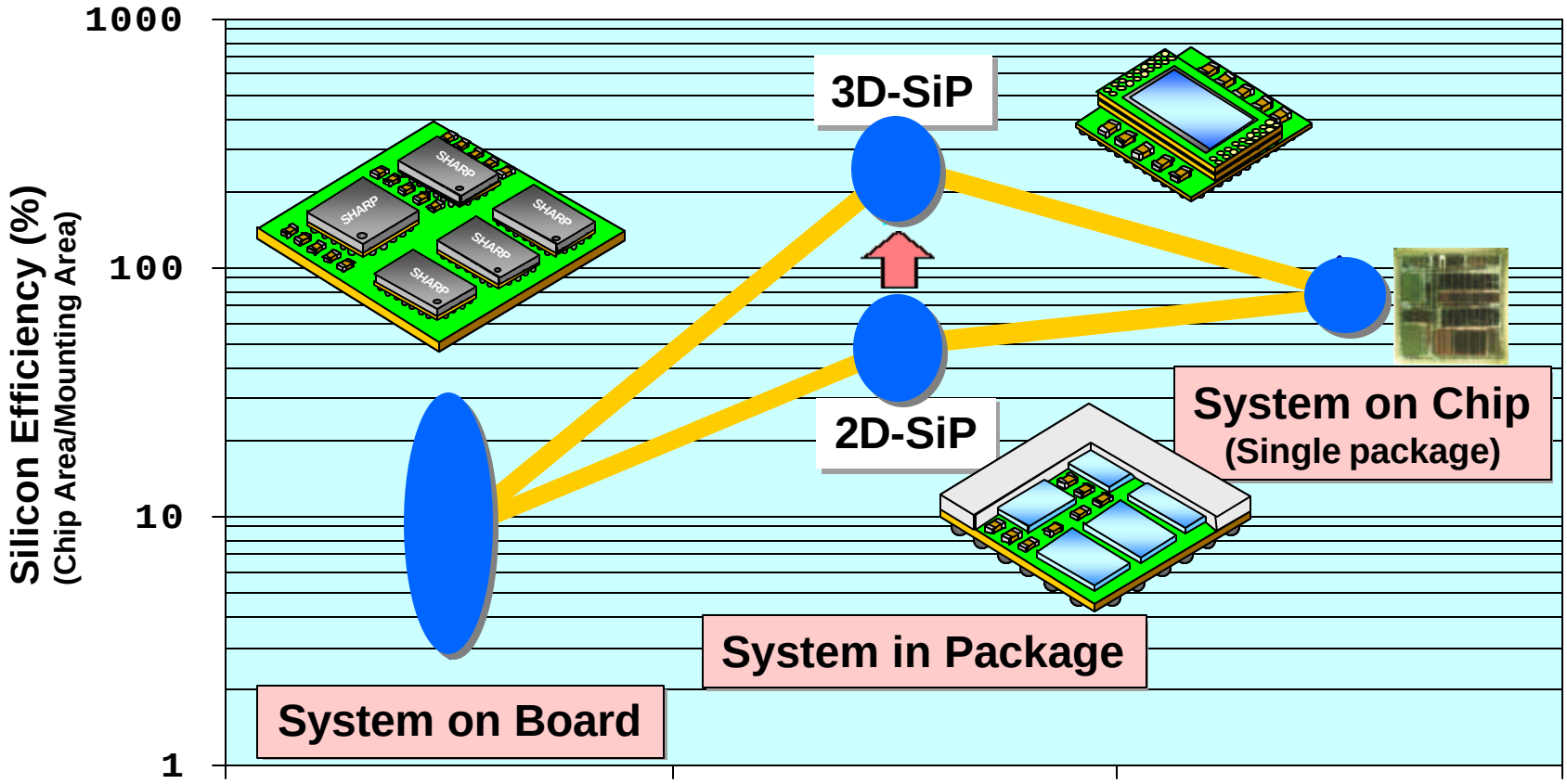
512M Flash (64Mx8)
1G Flash (128Mx8)

2.0mmt Max

Standard on memory pin layout

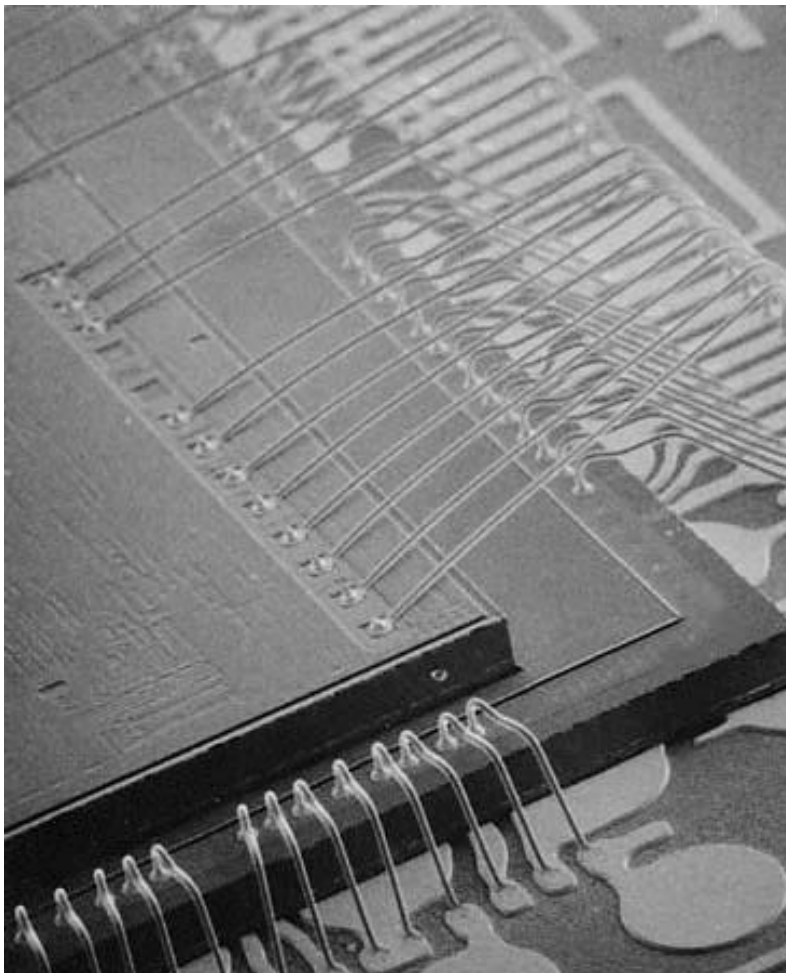
- 3D-System In Package(SIP) Era

Purpose of 3D-SIP Technology
-System Solution Which Surpass SoC-



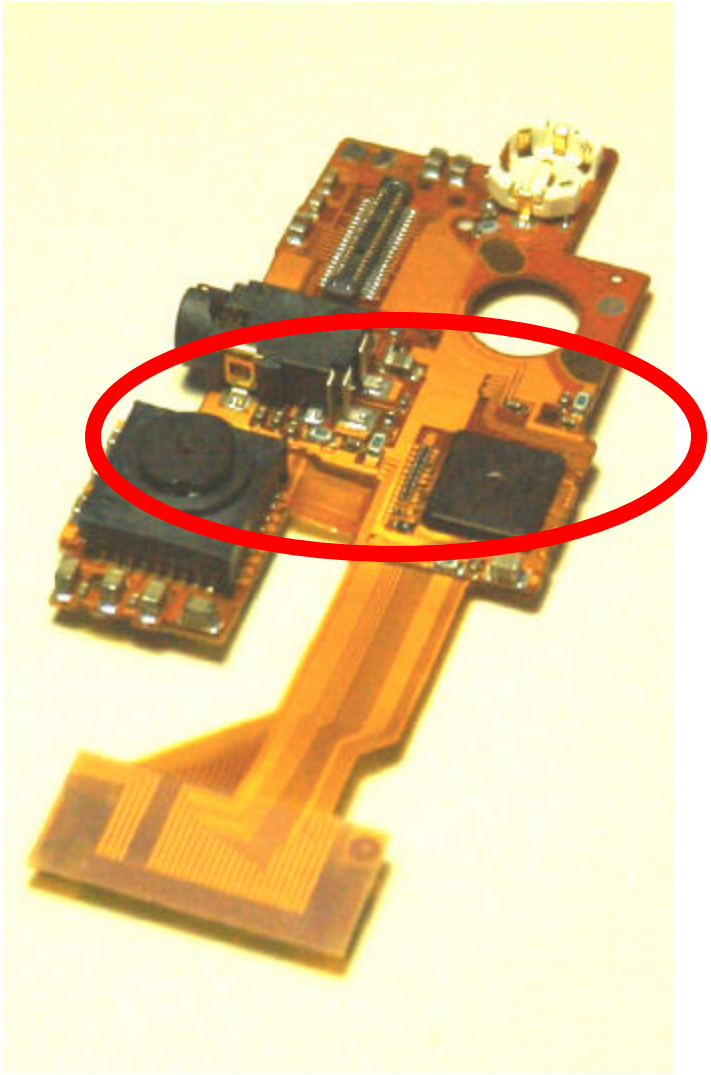
Development Time	Short	⟷	Short	Long
Development Cost	Low	⟷	Low	High
System Speed	Slow	⟷		Fast
System Reliability	Low	⟷		High

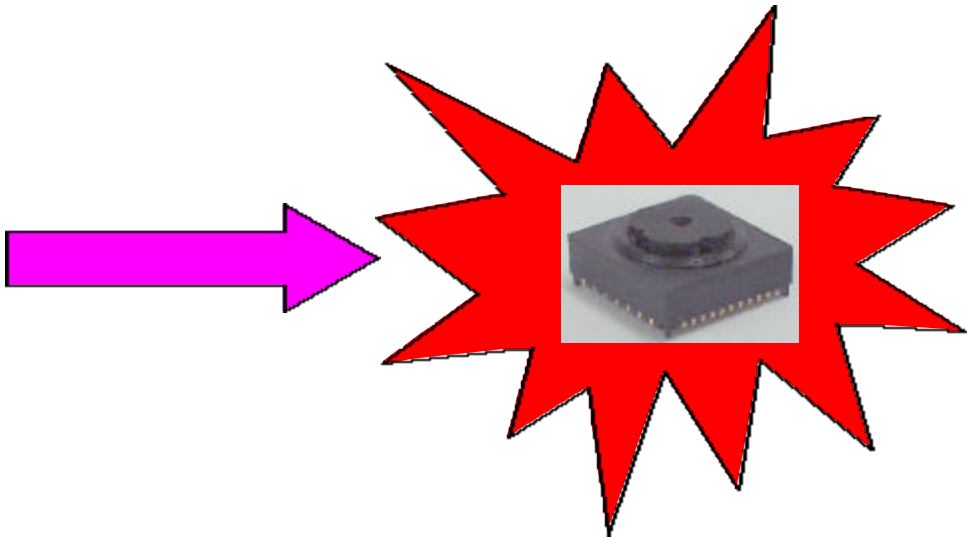
Various Combinations of ICs



- Controller IC+ Flash Memory
- DSP+ASIC
- Base Band IC+ Flash Memory
- Base Band IC+SRAM
- Micro Cntroller+E2PROM
- DSP+ Image Sensor

Latest CMOS Camera Module





Sensor + DSP

The Era of the New Package "3D-SIP"