THE PRESENT AND FUTURE DEVELOPMENT OF ALIVH

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Panasonic

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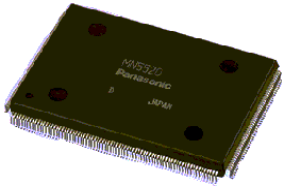
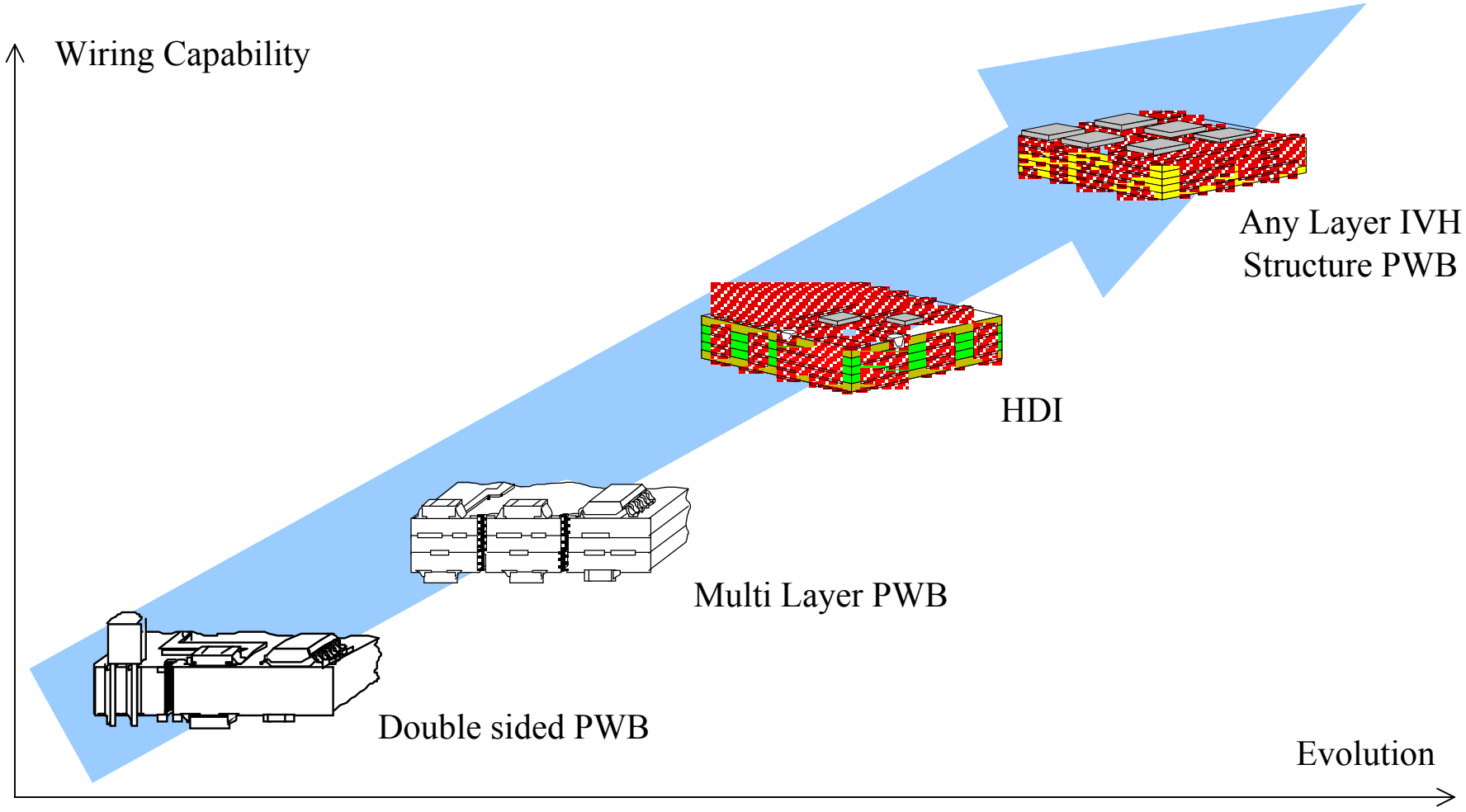
INTRODUCTION

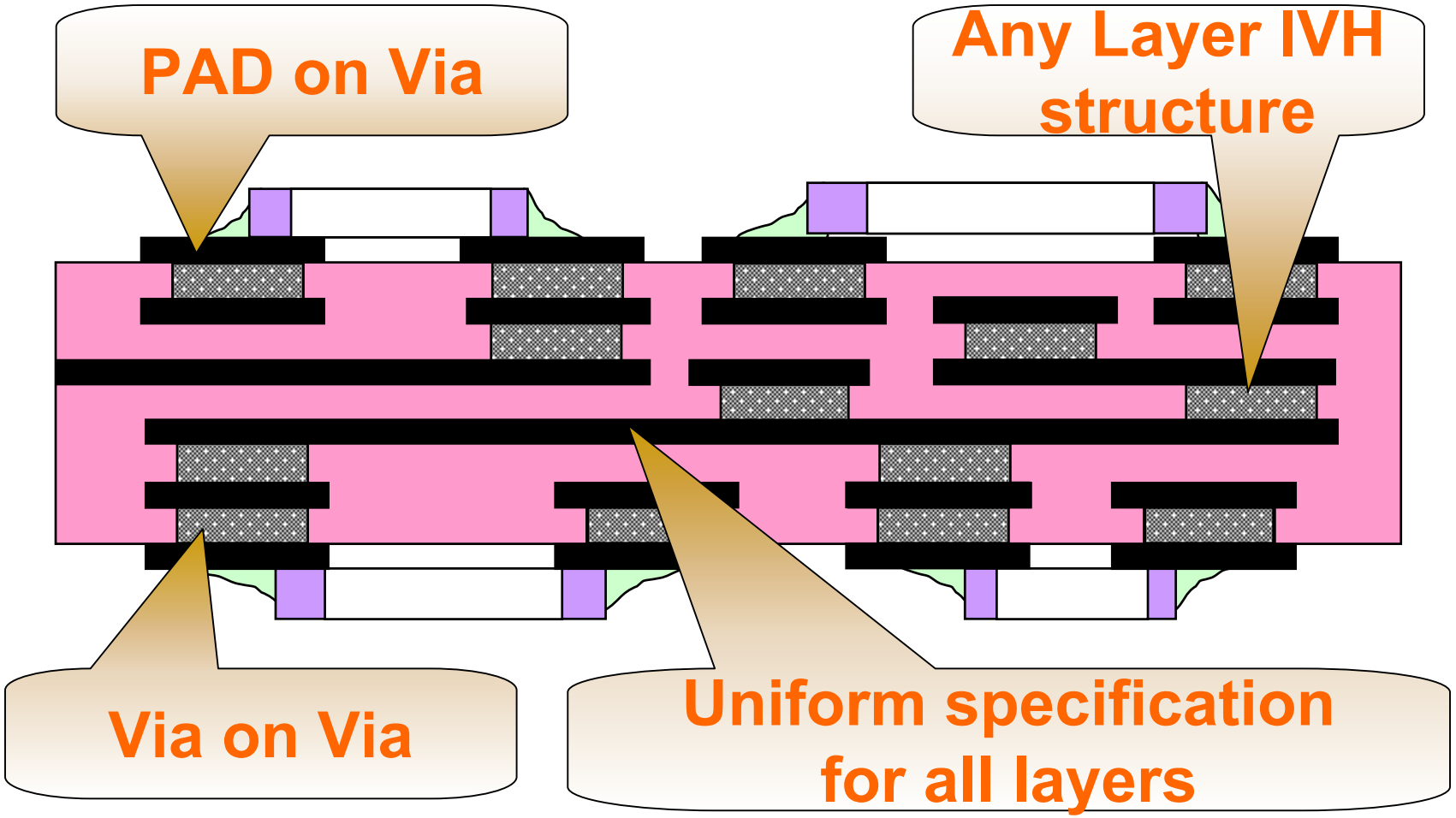
DOWNSIZING & WEIGHT REDUCTION FOR SEMICONDUCTORS

	1990	2000	2005
Semiconductor	100MHz/100pin	1GHz/600pin	5GHz/1200pin
Semiconductor Package	 QFP	Finer-Multiple Pin  0.5CSP	 0.25CSP	 SIP
Structure	Wire-Bonding  Lead Frame	Flip-Chip  Solder Ball	Substrate	Flip-Chip  DCA(Chip on Chip)

THE EVOLUTION OF PWB

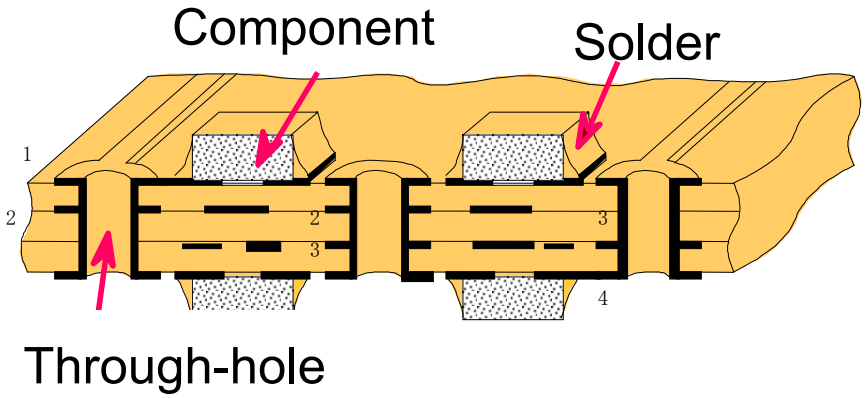


FEATURES OF ANY LAYER IVH STRUCTURE PWB



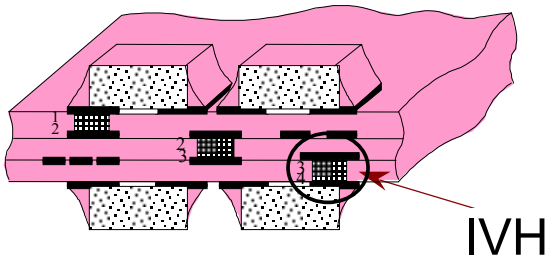
COMPARISON WITH THE MULTI-LAYER STRUCTURE

Conventional PWB (Through-hole)



(Cannot be mounted on hole)

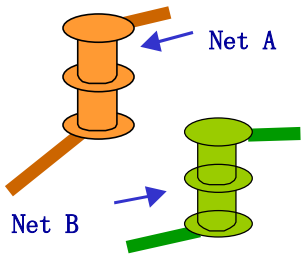
Any layer IVH structure PWB

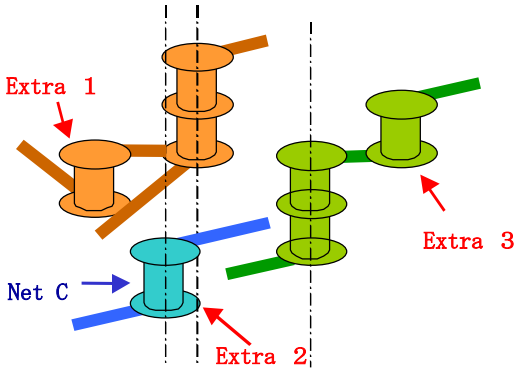


(Surface can be fully utilized)

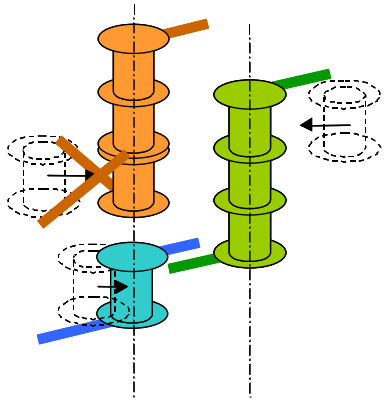
- **Downsizing & High density mounting**
- **Easily Designed**
- **Ideal for high-speeded applications**

DESIGN FREEDOM WITH ANY LAYER IVH STRUCTURE PWB

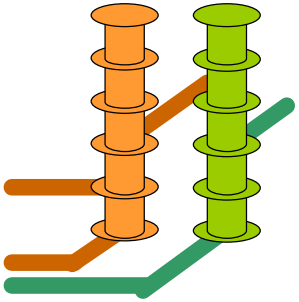




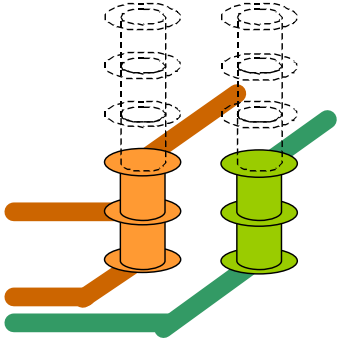
HDI



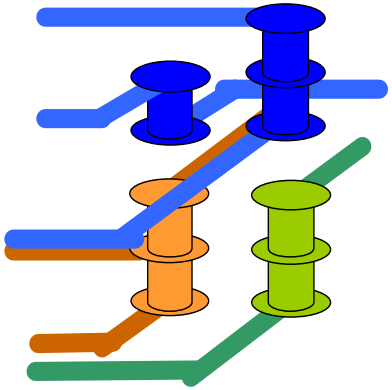
Any Layer IVH Structure



Conventional Through Hole Structure



Any Layer IVH Structure

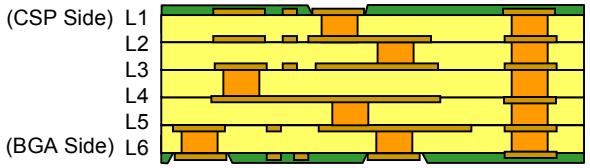


Any Layer IVH Structure

DESIGN SIMULATION EXCERCISE

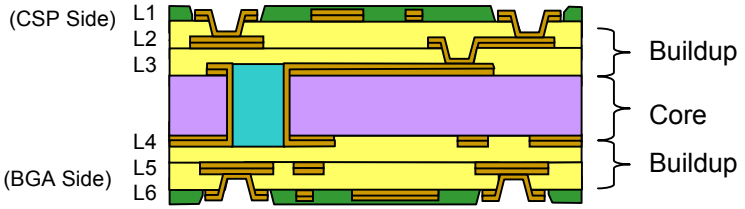
OBJECTIVE: To compare the wiring capabilities of **Any Layer IVH structure PWB** with **HDI** for connecting between 2 0.5mm pitch CSPs.
SIMULATION TOOL: Auto-router SPECTRA Ver.9

Any Layer IVH structure

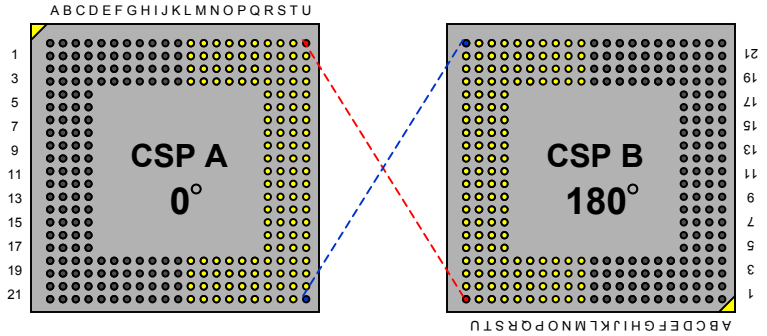


All layer - L/S: 60/70µm Land: Ø300µm

2+2+2 HDI



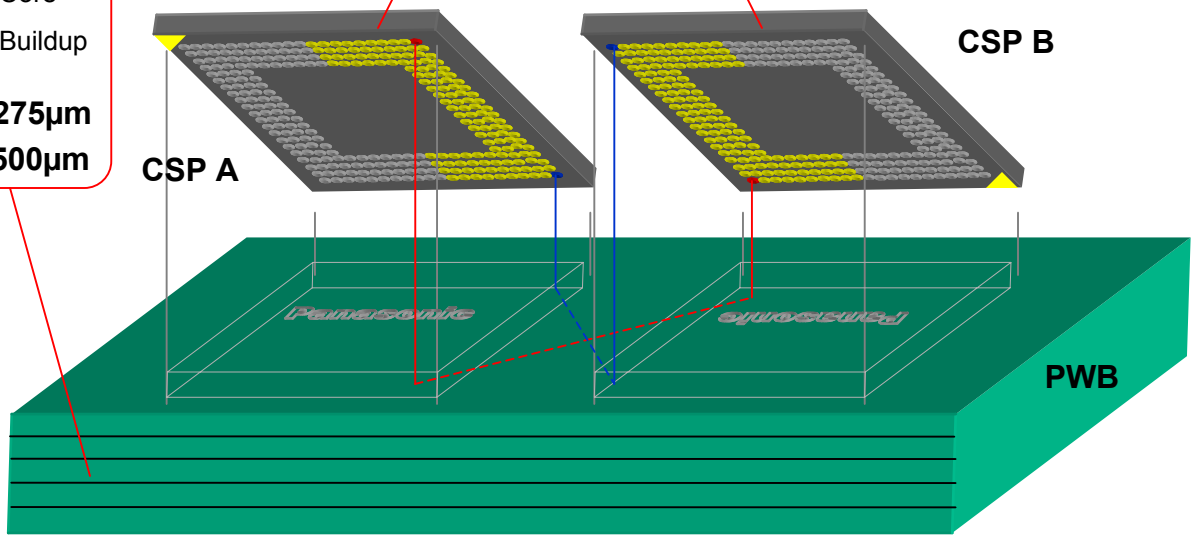
Buildup layer - L/S: 75/75µm Land: Ø275µm
Core layer - L/S: 75/75µm Land: Ø500µm



CSP A = CSP B

Package Size: 11×11mm **Pin Count:** 272 pins

Pin Configuration: 21×21 (4-row peripheral)



Routing Condition:

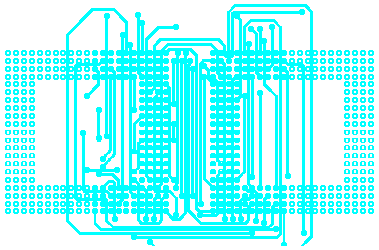
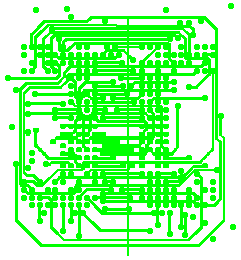
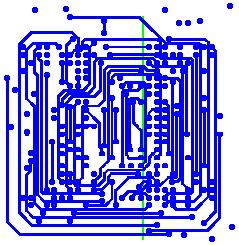
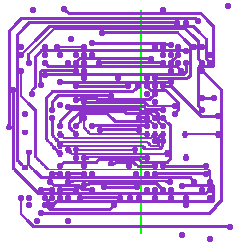
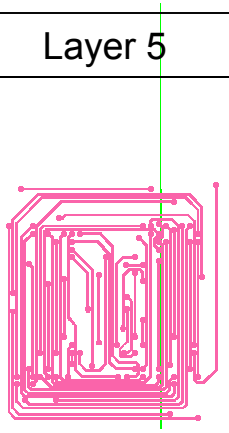
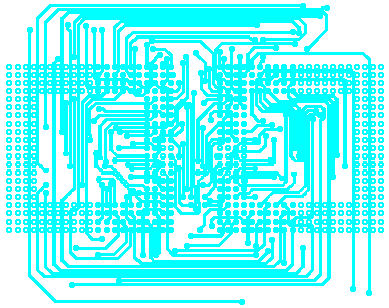
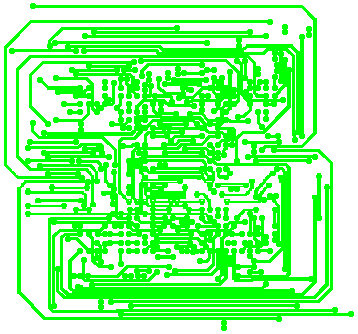
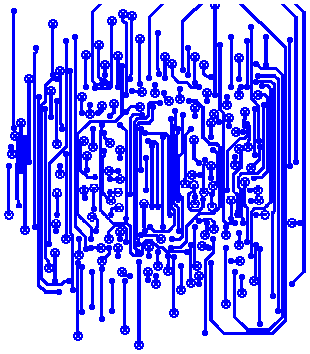
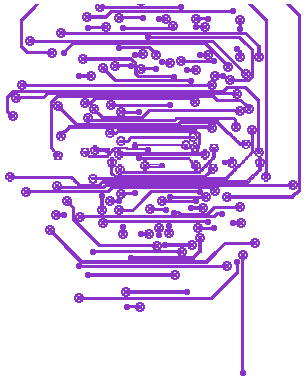
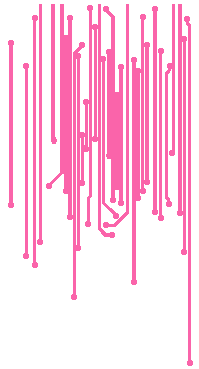
Same location pad connection (eg between Pad U-21 of CSP A & B)

CSP B shall be inverted at 180° of CSP A.

50% of pad connection (Gold pads only)

No routings on L6 (BGA Side)

SIMULATED LAYER TRACES

	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5
Any Layer IVH structure					
HDI (2+2+2)					

COMPARISON RESULTS

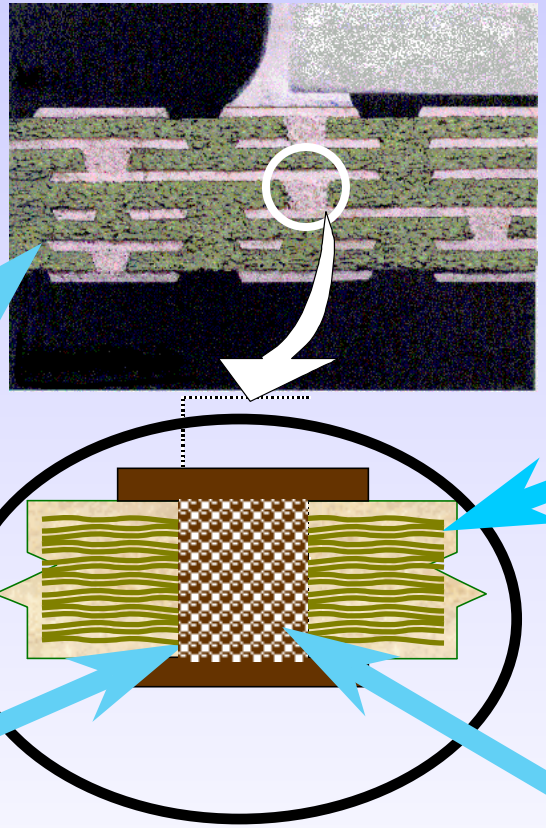
Any Layer IVH structure PWB Performance

	Wiring Area	Wiring Length	Wiring Time
HDI	100	100	100
Any Layer IVH structure	58	68	11

*All values calculated based on the overall layers.

KEY TECHNOLOGY AND FEATURES

ALIVH CONCEPT AND KEY TECHNOLOGY



Stacking

Hot Press

Material

Non-woven Aramid

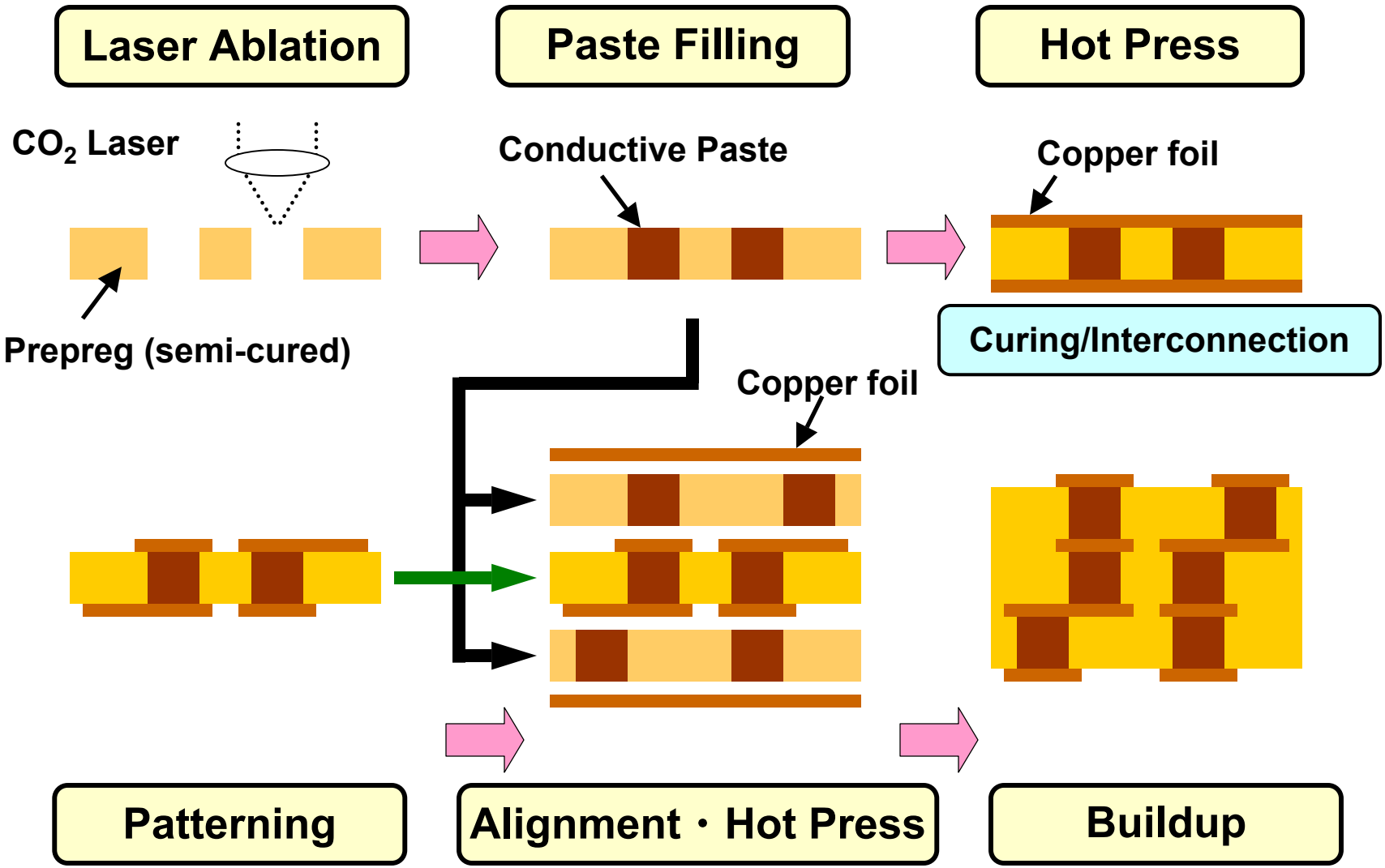
Microvia holes

Laser Ablation

Interconnection

Conductive Paste

ALIVH MANUFACTURING PROCESS



SPECIFICATIONS & CHARACTERISTICS OF ALIVH

Base material	—	Non-woven aramid fabric-epoxy
No. of layers	Layer	max. 10
Thickness	mm	6-layer: 0.75(min.0.60)　8-layer: 0.95(min.0.80)
Copper foil	μm	18(min 12): internal layer 18(35: in case of copper plating): external layer
Conductor width / Conductor space	μm	Standard 100/100(min 60/70)
Via diameter	μm	200 (min 150)
Land diameter	μm	400 (min 300)

	Unit	ALIVH	FR-4
Density	g/ml	1.4	1.9
Dielectric constant (at 1GHz)		3.7	4.4
Tg (DMA method)	℃	198	130
Coefficient of thermal expansion	$x10^{-6}K^{-1}$	6 to 10	15

EXPANSION TO A PACKAGE SUBSTRATE

SPECIFICATIONS OF ALIVH FOR BARE CHIP MOUNTING

High Packing and Wiring Density

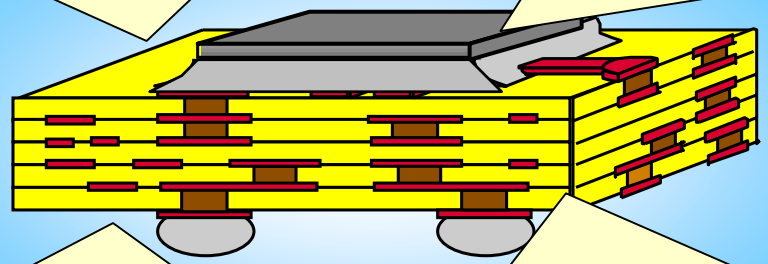
Any layer IVH Structure and fine pattern for fine pitch and multiple pin compatibility

**L/S = 40/40 um*
**V/L = 100/200 um*
**Via-on-via, Pad-on-Via structure*

Superior Mountability for Bare Chip

All layers strengthened Aramid for superior substrate performance

**Low CTE α = 9 ppm/°C*
**High Heat Resistance T_g = 198°C (DMA)*
**High coplanarity <10 um/ 10*10mm sq.*
**High Hardness 50 (Barcall) /180°C*



High Reliability at Package Level

High connection reliability for bare chip mounting

- *JEDEC > Level II*
- *Thermal Cycle (–65/150°C) 2000cyc passed*
- *PCT (121°C, 2atm) 500hrs passed*

Ideal for High Speed

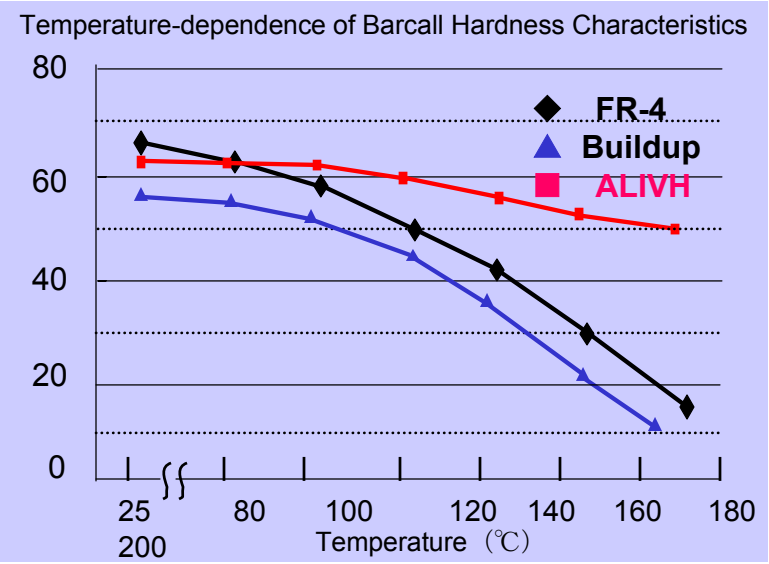
Uniform specification throughout all layers for better impedance control

- *Dielectric Constant 3.7(1GHz) to 3.6(10GHz)*
- *High Thickness Accuracy 3σ = 6.6 /100 um layer thickness*
- *Short wiring length, strengthened ground and power plane*

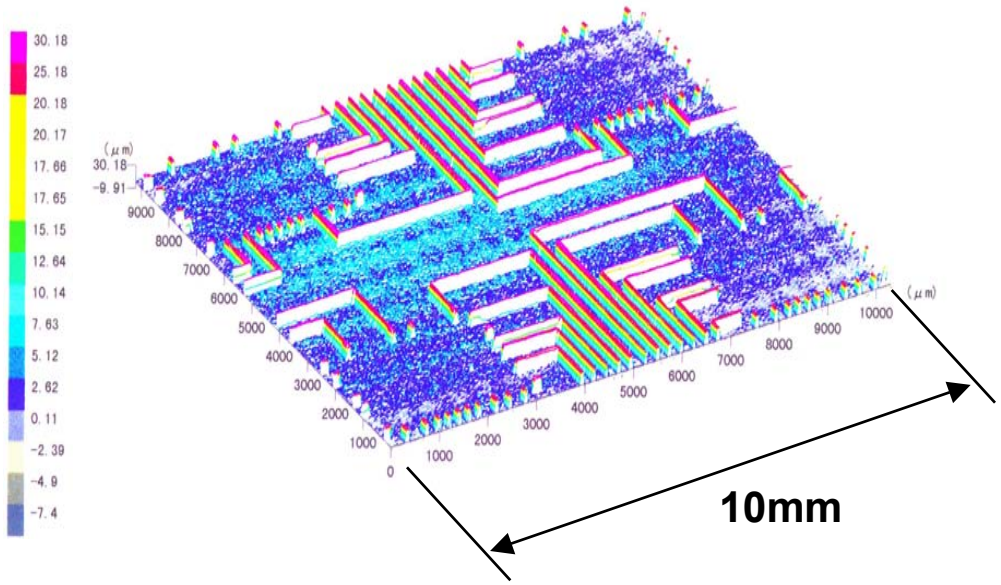
due to Any Layer IVH Structure

BARE BOARD RELIABILITY : HARDNESS & CO-PLANARITY OF ALIVH

Barcall Hardness



Surface Co-planarity



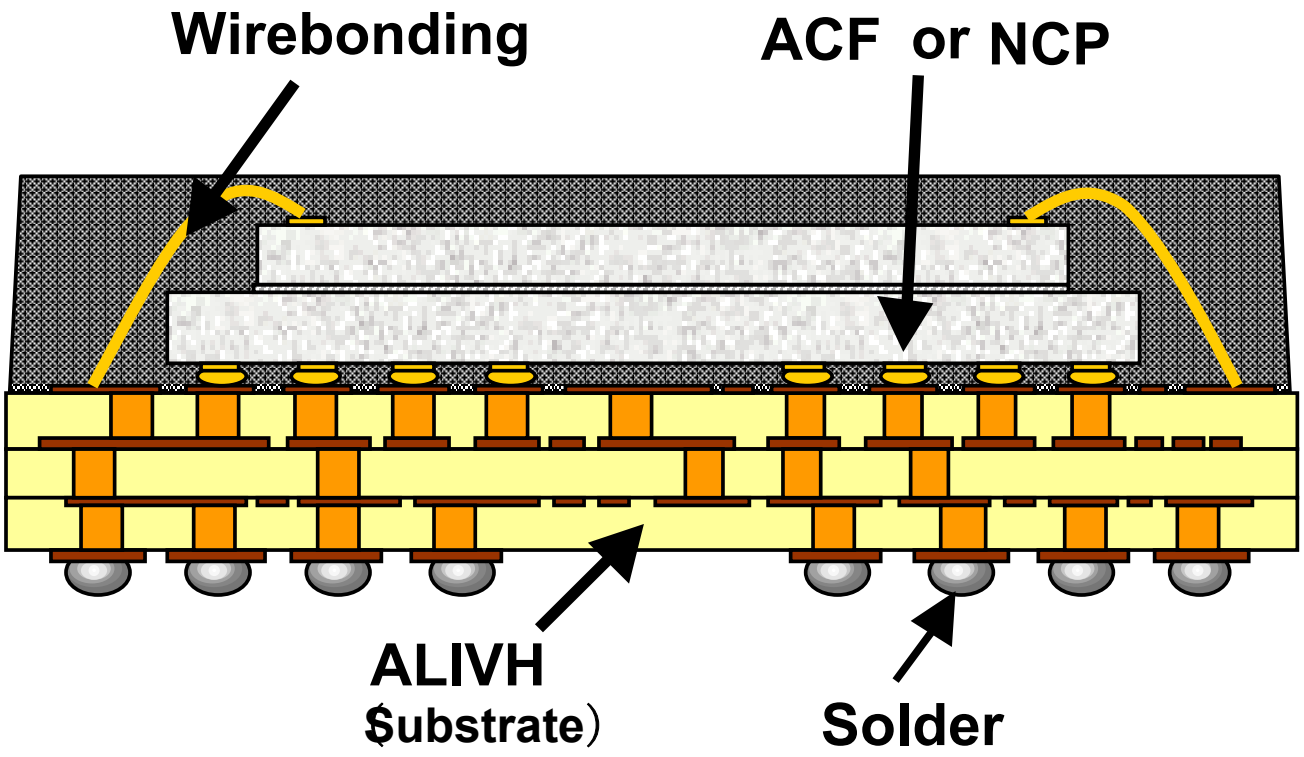
High Hardness at High Temperature

- **Low power loss when heat and ultrasonic are applied**
- **No dimensional changes**

Co-planarity < 10um/10x10mm sq.

- **Provide a smaller height disparity between connection planes so that the pressure applied during flip chip mounting can be smaller**

EXAMPLE OF THE SEMICONDUCTOR PACKAGE STRUCTURE



WIREBONDING PULL TEST METHOD

WIREBONDER: Shinkawa UTC-245BI-C2-07

Test Parameters:

2 different test wire length:

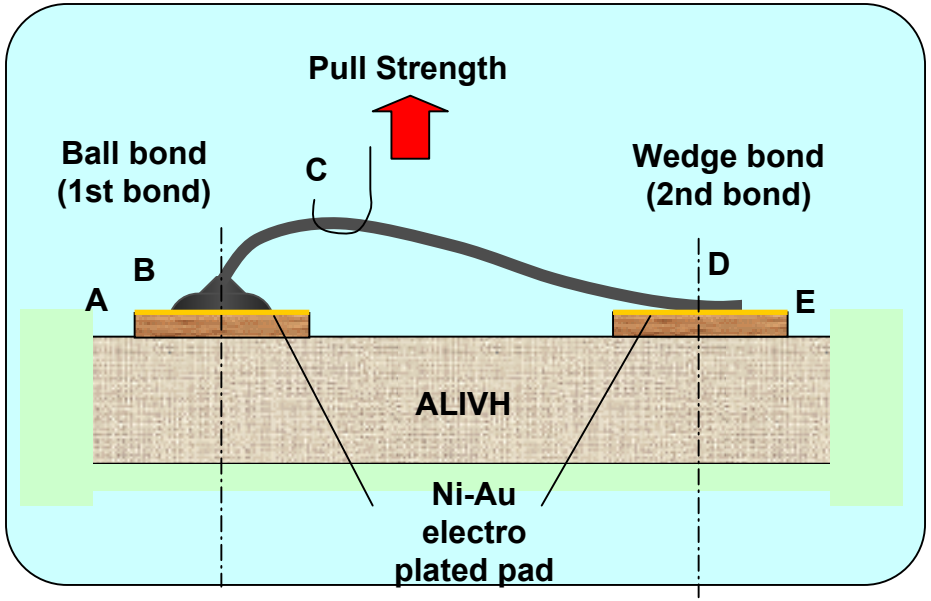
- x = 1.0mm, 1.5mm

Pull Test Condition:

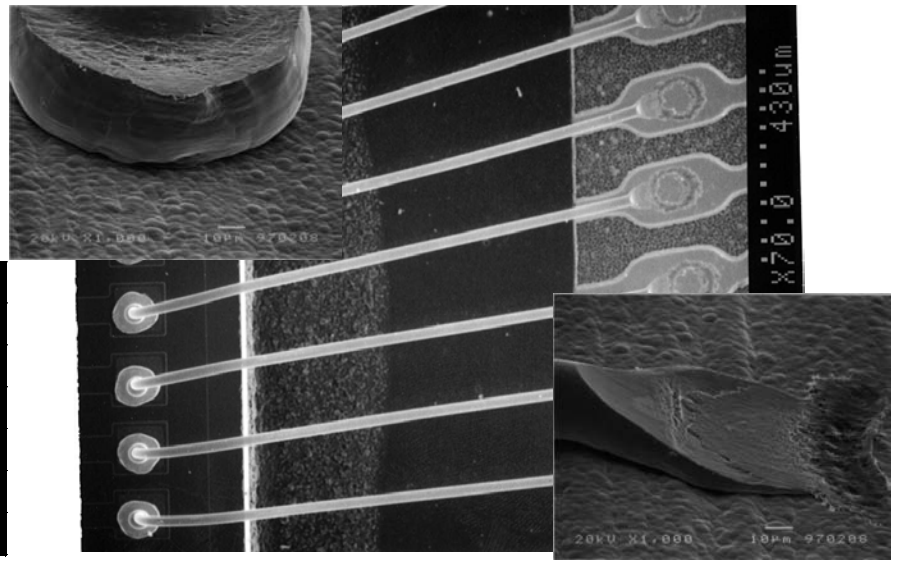
- Pull force shall be applied at the wire's centre at point C.
- Pull speed shall be at approx. 0.5mm/s

Passing Criteria:

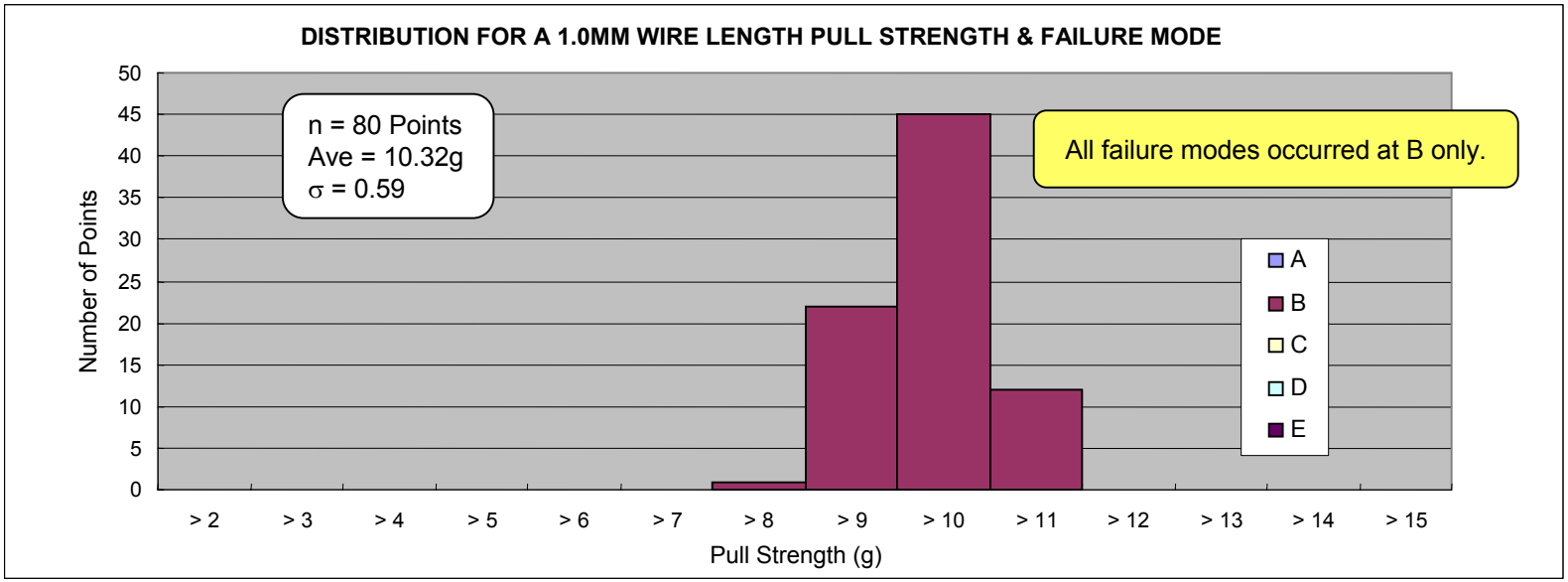
- Pull strength shall not be less than 3-gram.
- Failure mode shall not occur on the joint interface at points A or E.

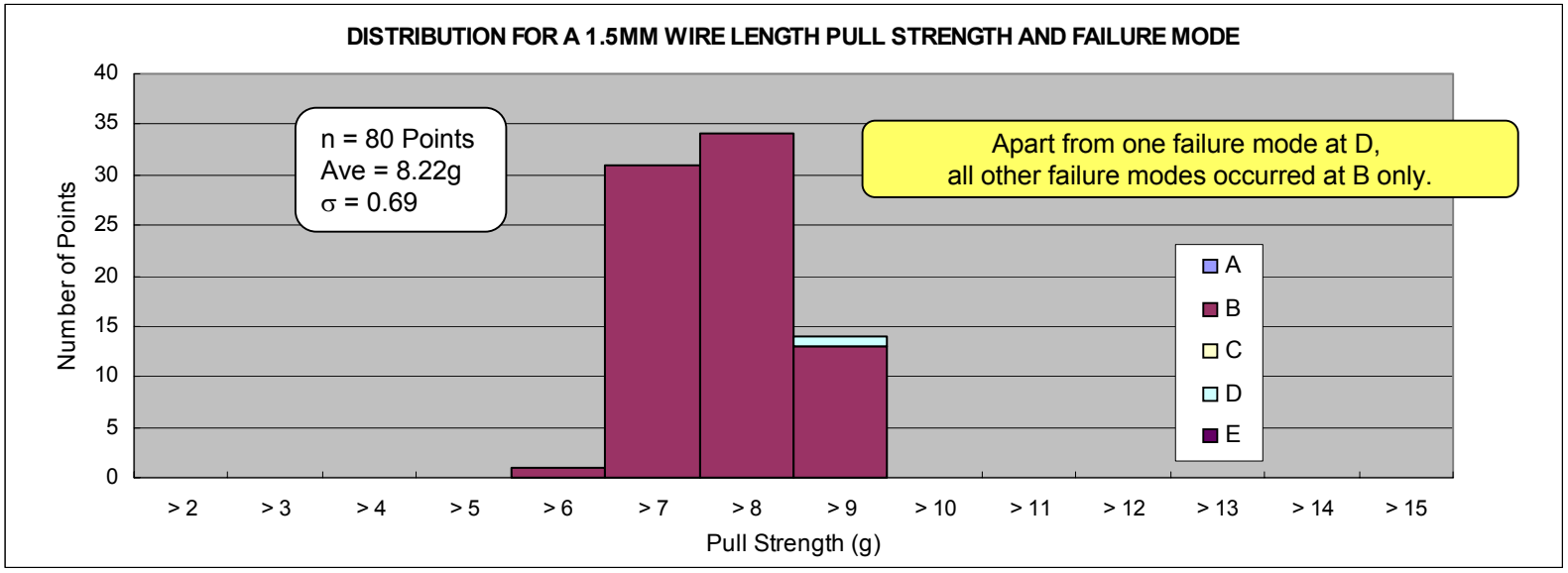


ITEM	UNIT	1st Bond	2nd Bond
Application time	ms	20	50
Ultrasonic Power	W	100	180
Force	gf	70	120
Table Temperature	degC	150	
Au Wire Diameter	um	25	
Capillary	ADAMANT AD-2N-43L		



WIREBONDING PULL TEST RESULTS OF ALIVH

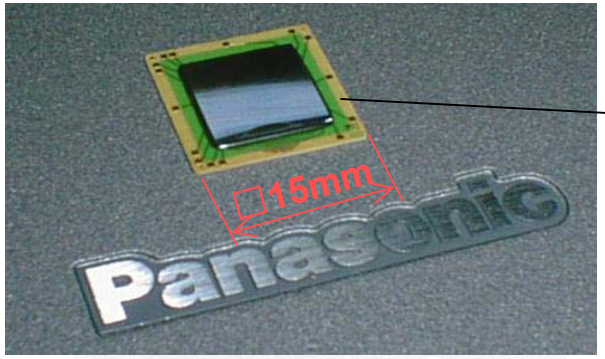




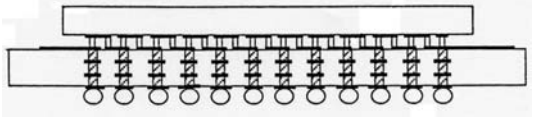
PACKAGE RELIABILITY : SCOPE OF EVALUATION

Sample for Evaluation With Solder FC Mounting

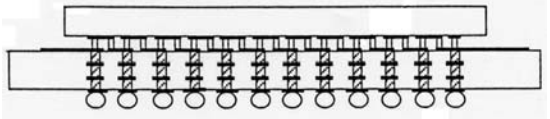
Test Sample for Evaluation with ACF Mounting

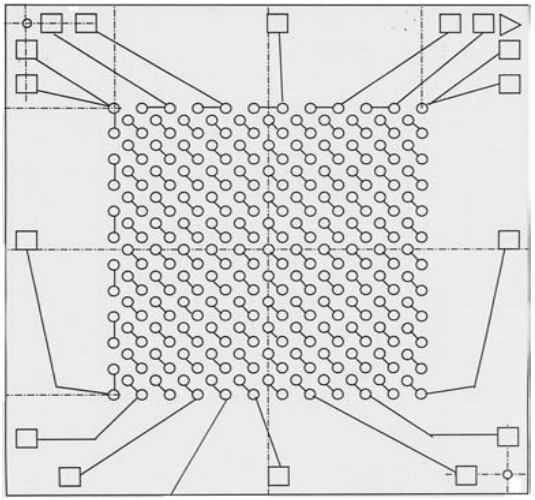


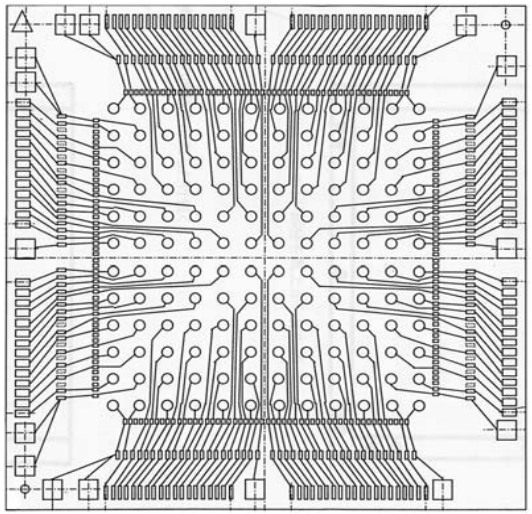
ALIVH



Circuit Pattern Design







PACKAGE RELIABILITY : EVALUATION CONDITION

SOLDER FLIP CHIP

SOLDER BUMP	90%Pb; 8%Sn; 2%Au (High temp solder) 96.2%Sn; 2.5%Ag; 0.8%Cu (Pb-free solder)
PWB	□15mm ALIVH-B (4 and 6-layer)
IC CHIP	□10mm Area Array TEG Chip (400um pitch×265 pads)
UNDERFILL RESIN	2 types (see below)

UNDERFILL RESIN		Units	A	B
Curing Condition		°C	150 (20mins)	100(1hr) +150(1hr)
Adhesiveness		Pas/25°C	40	10
Gel Time		Pas/25°C	40	120
T_g (TMA)		°C	137	130
CTE	α1	ppm	32	32
	α2	ppm	120	-
Modulus of Elasticity		GPa	9	9
Bending Strength		MPa	140	130
Moisture Absorption		wt%	1.2	-

ACF

ACF RESIN	2 types (see below)
PWB	□15mm ALIVH-B (4 and 6-layer)
IC CHIP	□10mm Peripheral TEG Chip (160um pitch×208 pads)

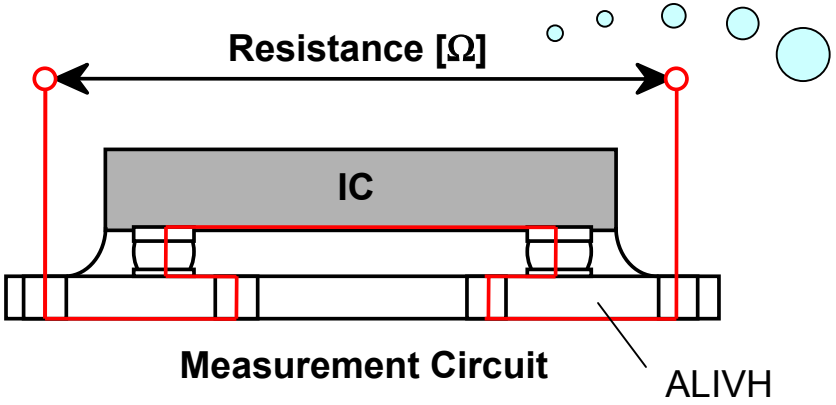
ACF		Company S	Company H
Filler Content (wt%)		50	20
T_g (°C)		170	173
E1 (Mpa)	40°C	4	2.4
E2 (Mpa)	150°C	1.7	0.7
α1 (ppm/°C)	40 - 100°C	27	59
α2 (ppm/°C)	120 - 140°C	64	95
Moisture Absorption		1.3	1

PACKAGE RELIABILITY : ITEMS TO BE EVALUATED

ITEMS FOR RELIABILITY TESTS

ITEM TO BE EVALUATED	PCT	THERMAL CYCLE	Temperature & Humidity
Pre-Treatment	JEDEC Level III	JEDEC Level III	JEDEC Level III
Condition	(121°C, 2atm, 100%) × 300hrs	(-65°C for 30mins/ 150°C for 30mins) × 1000hrs	(85°C/85%RH) × 2000hrs

*JEDEC Level III: 30℃, 60%×192hrs → 3 times reflow (Peak temp: 220℃)

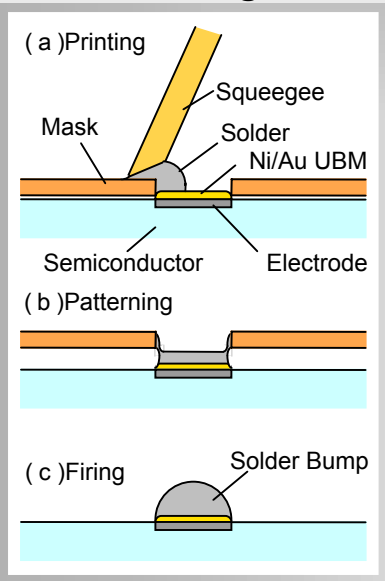


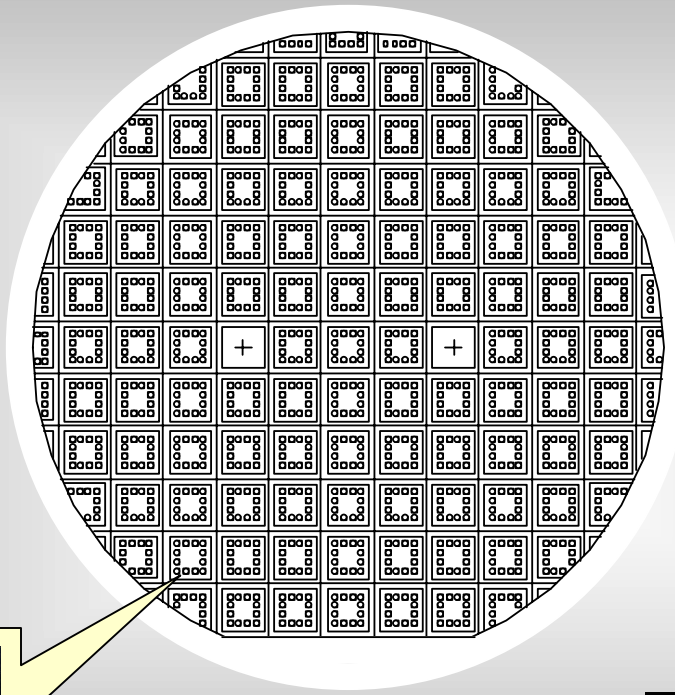
Measured resistance includes wiring resistance of PWB, via resistance of all layers, resistance of bonding connection, and wiring resistance of IC.

PACKAGE RELIABILITY : SOLDER FLIP CHIP MOUNTING

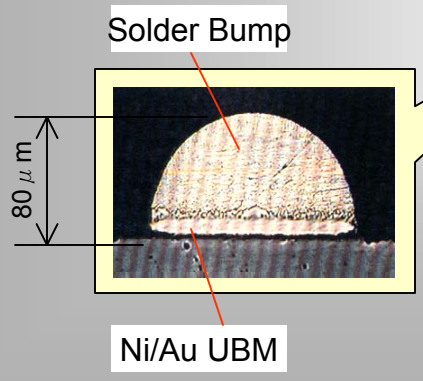
Step 1: Solder Bump Formation

Screen Printing Process

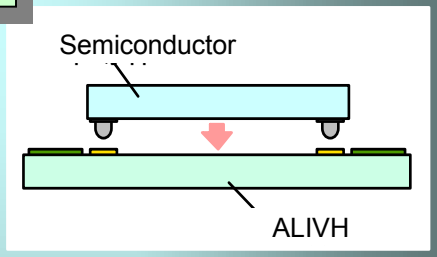




Semiconductor Wafer

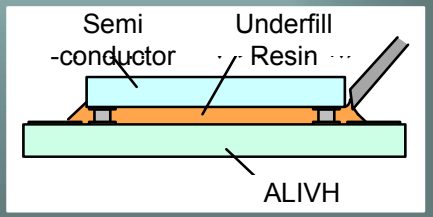


Step 2: Mounting

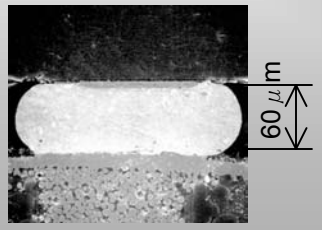


Alignment & Reflow

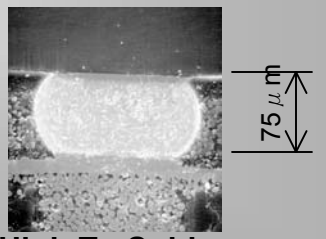
Direct Pass Cleaning



Underfill Resin Injection



Pb-free Solder



High Tg Solder

PACKAGE RELIABILITY : SOLDER FLIP CHIP MOUNTING PROCESS

Semiconductor

Wafer

- Electroless Ni-Au Plating
- Dicing（Die Separation）
- Solder Screen Printing
- Soldering Reflow
- Cleaning Flux
- Inspection
- Storage（Moisture absorption and Oxidization proof）

PWB

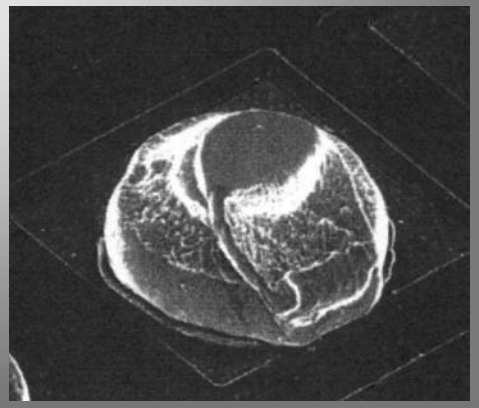
ALIVH

- Cutting（Unit Separation）
- Cleaning
- Drying（125℃，2hr）
- Storage（Moisture absorption and Oxidization proof）
- Solder Printing, Flux Coating

- Chip Alignment（20gf/bump）
- N_2 Reflow
- Cleaning Flux
- Drying (125℃，2hr)
- Underfill filling
- Curing
- Inspection
- Storage（Moisture absorption and Oxidization proof）

PACKAGE RELIABILITY : ACF MOUNTING

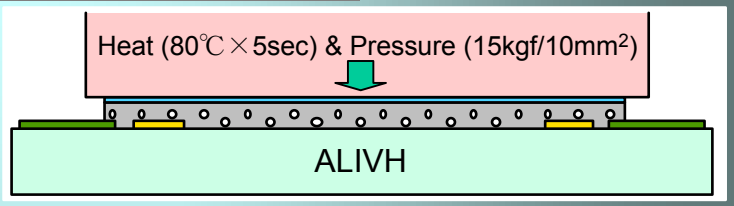
Step 1: Bump Formation



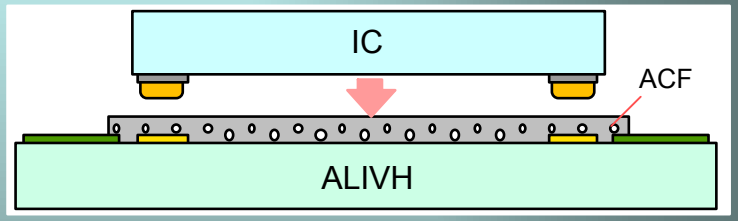
Stud Bump (Au)

Mounting Connection

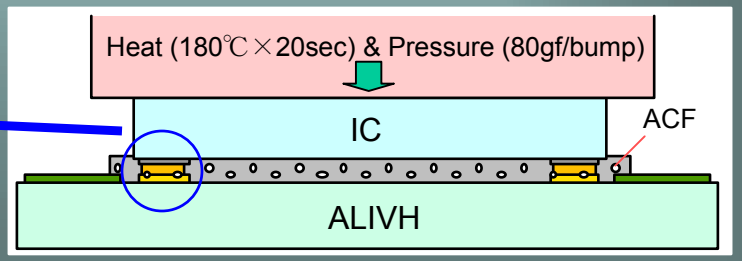
Step 2: Mounting



Adhesion



Alignment



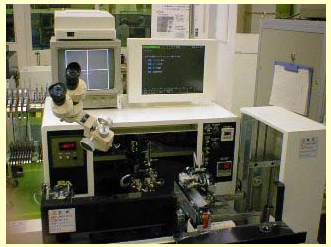
Bonding

PACKAGE RELIABILITY : ACF MOUNTING PROCESS

Semiconductor

Wafer

- Dicing（Die Separation）
- Au Bump Forming
- Inspection
- Storage（Moisture absorption and Oxidization proof）

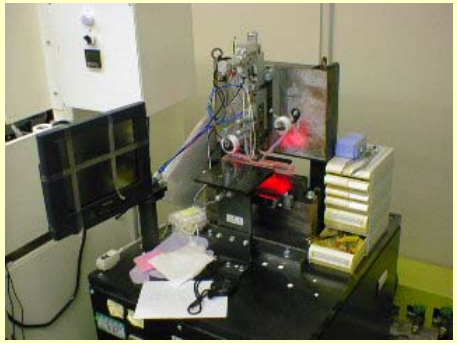


PWB

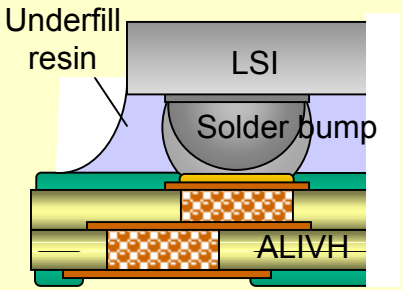
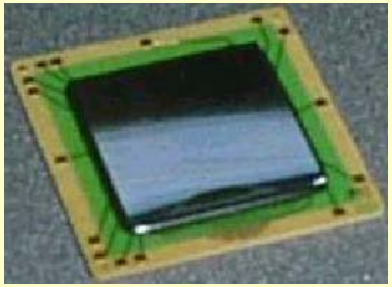
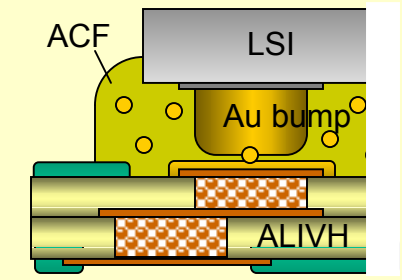
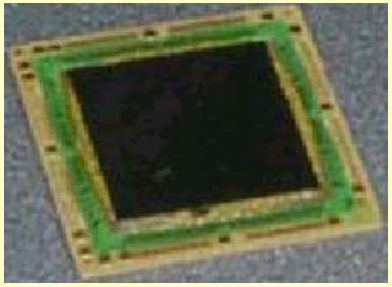
ALIVH

- Cutting（Unit Separation）
- Cleaning
- Drying（125℃，2hr）
- ACF Pre-sealing（80℃，5sec）

- Chip Alignment（10gf/bump）
- Sealing（180℃，20sec）
- Inspection
- Storage（Moisture absorption and Oxidization proof）

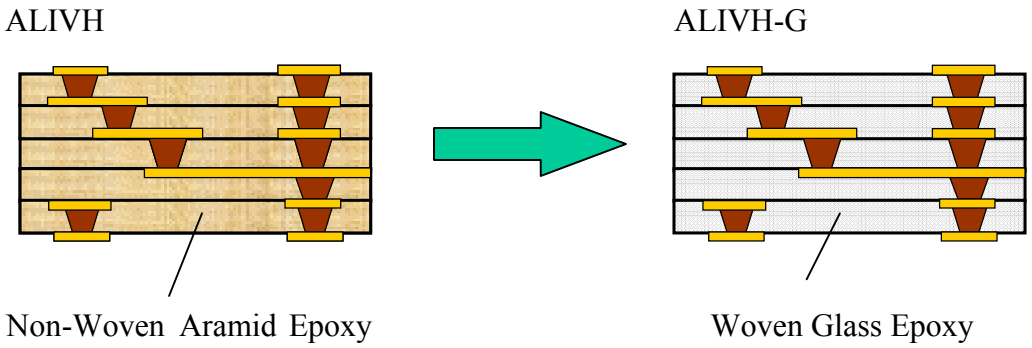


PACKAGE RELIABILITY : EVALUATION RESULTS

Method	Structure	Sample	Reliability Test Results			
			Layers Count		6	4
Solder FC			Moisture Absorbed Reflow Test JEDEC Level III	HT	Pass	Pass
				LF	Pass	Pass
			PCT : 121℃, 2atm, 100%, 240hrs	HT	Pass	Pass
				LF	Pass	Pass
			T/C : -65 to 150℃, Dry, 1000cycles	HT	Pass	Pass
				LF	Pass	Pass
	10mm^2 Area Array TEG Chips (400um Pitch × 265 pads) High Temp Solder(HT) / Lead Free Solder (LF) Bump		TH : 85℃, 85%, 2000hrs	HT	Pass	Pass
				LF	Pass	Pass
ACF			Moisture Absorbed Reflow Test JEDEC Level II × 5 times		Pass	Pass
			PCT : 121℃, 2atm, 100%, 168hrs		Pass	Pass
			T/C : -65 to 150℃, Dry, 1000cycles		Pass	Pass
	10mm^2 Peripheral TEG Chip, (160um Pitch × 208 pads)		TH : 85℃, 85%, 2000hrs		Pass	Pass

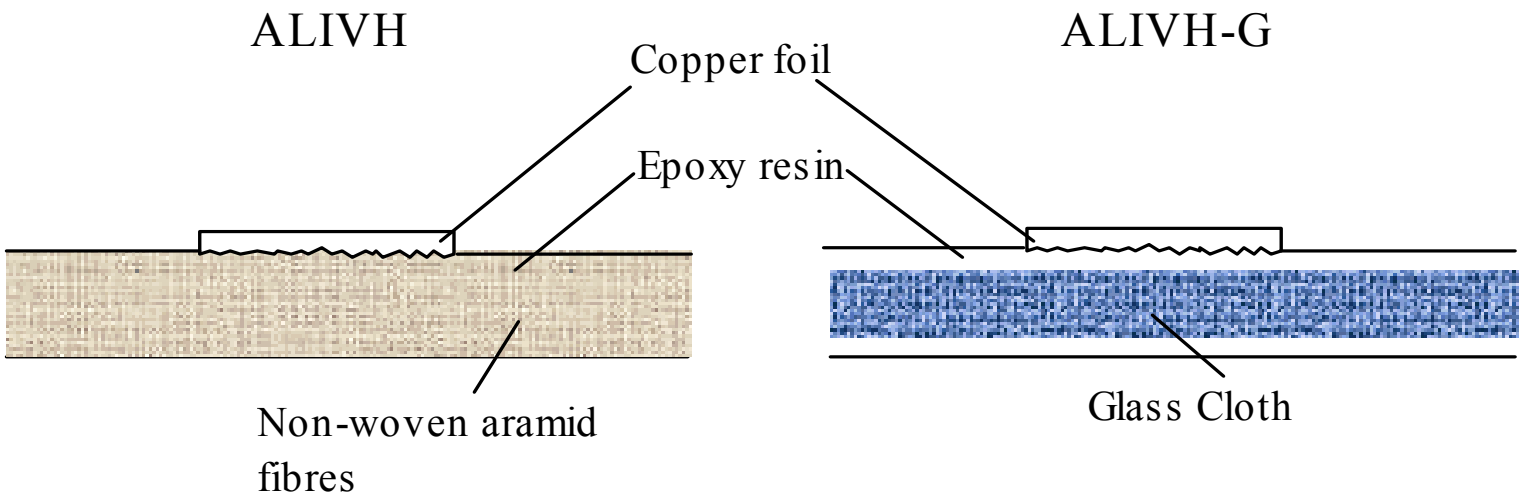
NEW ANY LAYER IVH STRUCTURE PWB

DEVELOPMENT CONCEPT WITH FR-4 MATERIAL

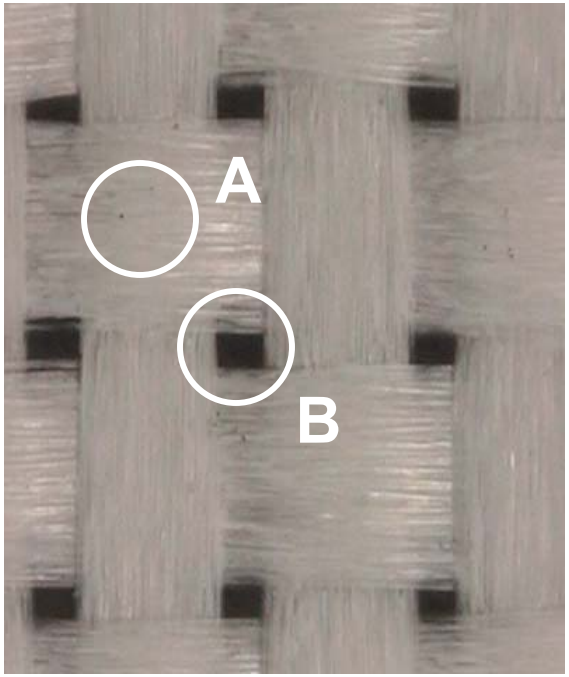


	Aramid (ALIVH)	FR-4 (ALIVH-G)
Tg (Heat Resistant)	◎	○
Dielectric Constant	◎	○
Weight (Density)	◎	△
Surface Mechanical Strength	△	◎
Rigidity	△	◎
Halogen Free	△	◎
Moisture Absorption	△	◎
Cost	△	◎

LAYER STRUCTURE COMPARISON

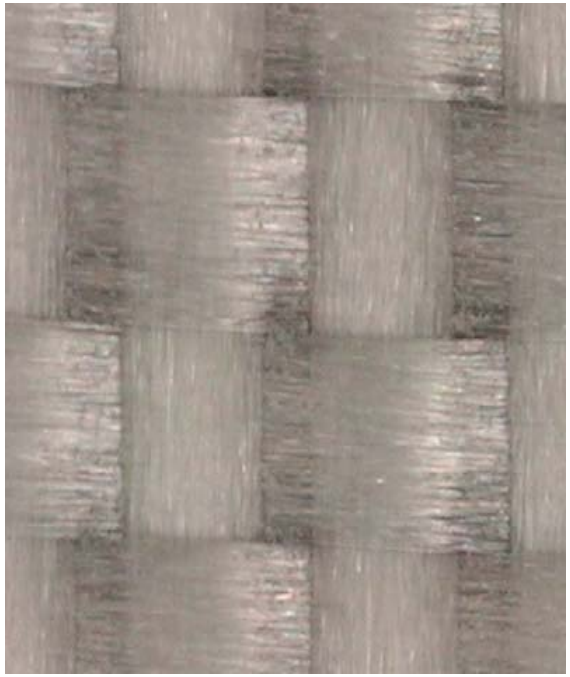


WOVEN GLASS CLOTH FOR NEW ANY LAYER IVH STRUCTURE PWB



A・・・Glass rich

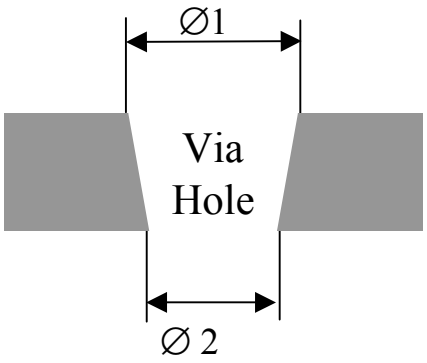
B・・・Epoxy rich



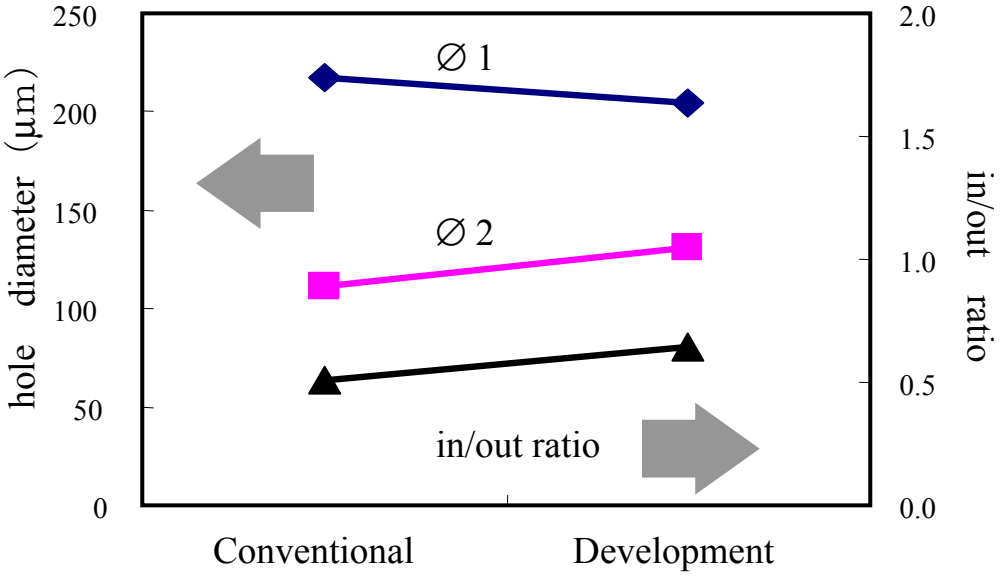
Conventional Type
（Opening Filament Fabrics）

Development Type
（Flatten Cloth）

IMPROVEMENT OF LASER DRILLING CONDITION

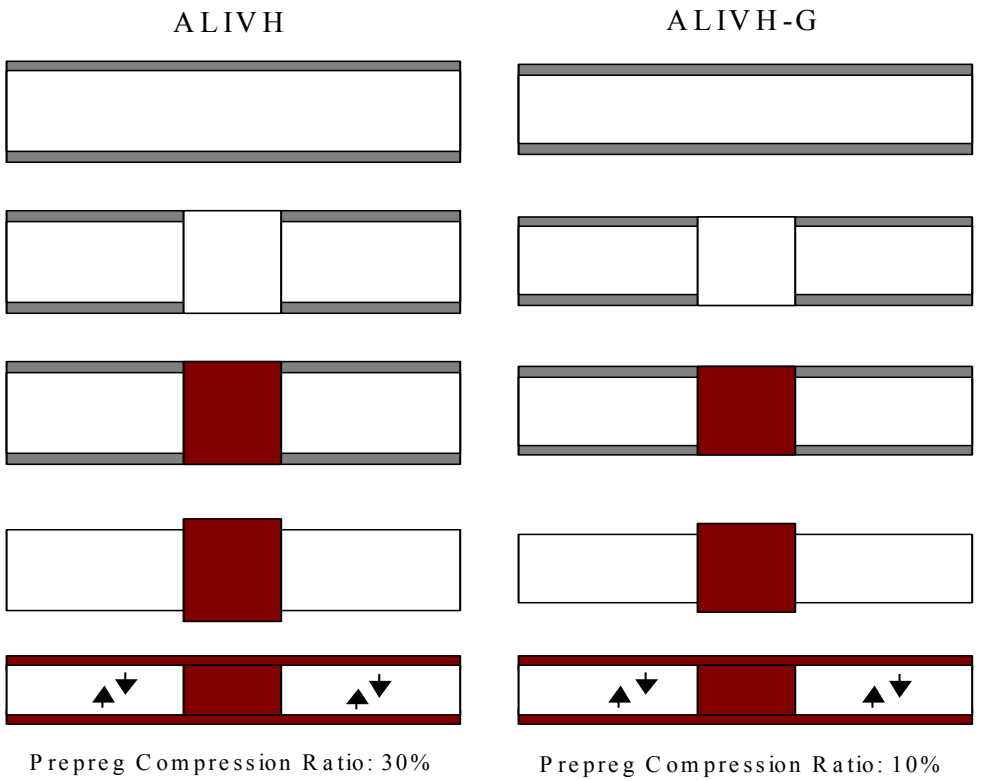


in/out ratio
= ∅ 2/ ∅ 1



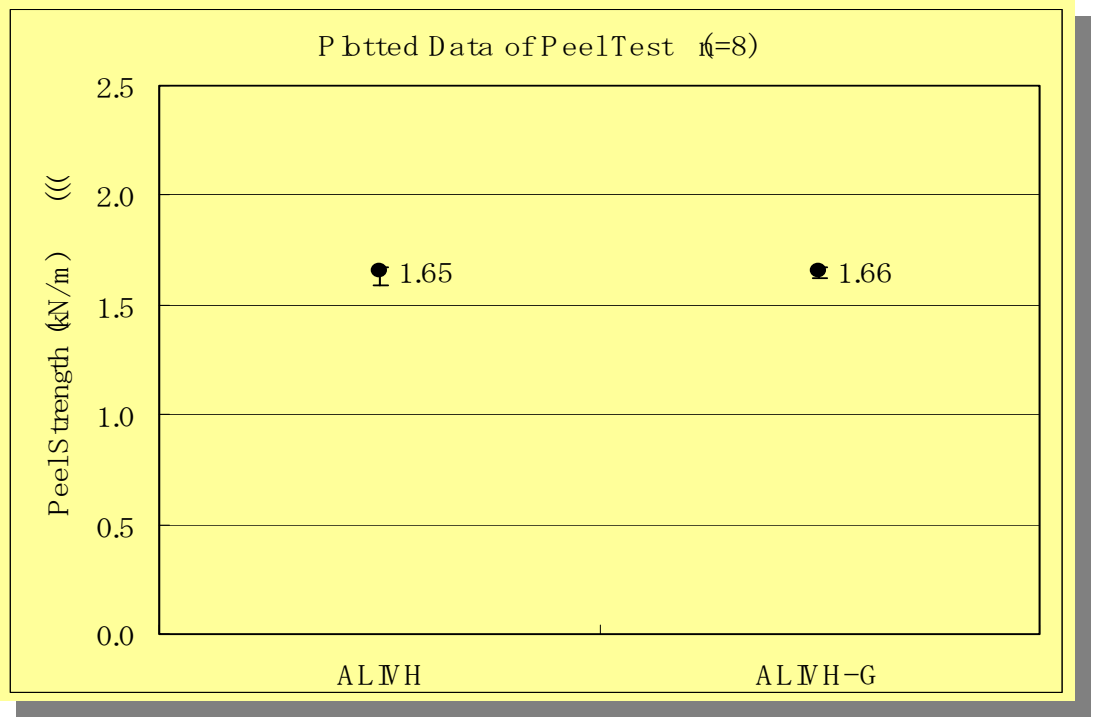
Laser Drilling Condition

COMPARISON OF CONNECTION MECHANISM



C.T.E. for Z-direction (ppm/degC)		
25 to 125 degC	90	45
200 to 250 degC	293	200

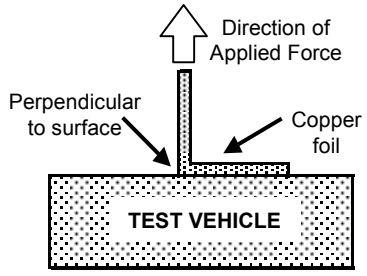
COMPARISON OF PEEL STRENGTH



- **TEST METHOD**

- Peel a pre-determined width of the copper conductor perpendicularly to the surface of the test vehicle.
- Measure and record the peel strength of the copper conductor along the peeling edges.

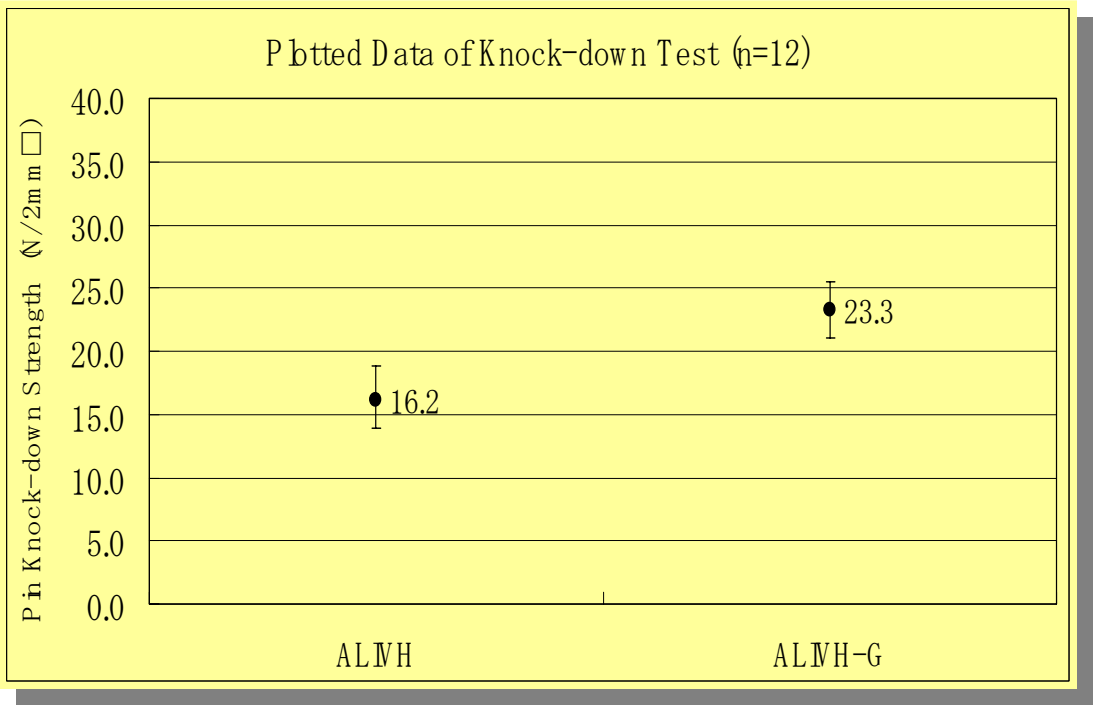
- **SCHEMATIC OF TEST SETUP**



- **SPECIFICATIONS OF TEST VEHICLE**

- LAYER COUNT: 6 Layers
- CONDUCTOR THICKNESS: 35um (18um Cu foil + Cu plating)
- BUILD-UP: HALOGEN FREE TYPE

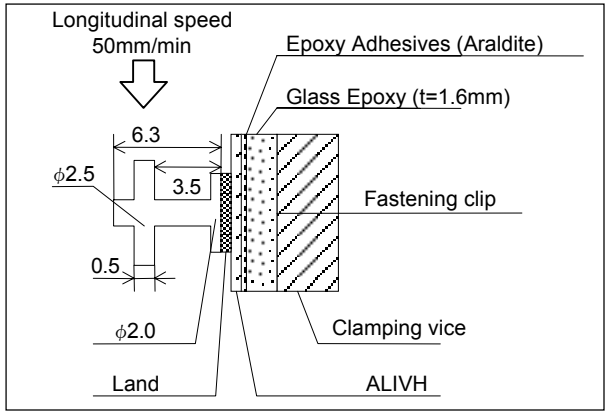
COMPARISON OF PIN KNOCK-DOWN STRENGTH



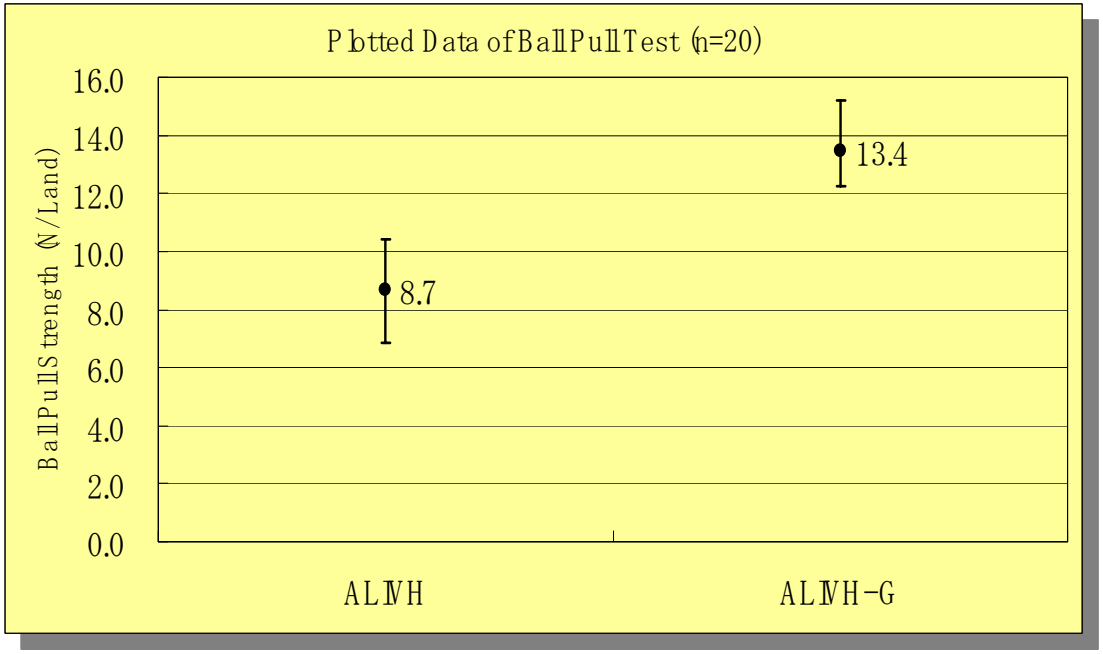
- **SPECIFICATIONS OF TEST VEHICLE**
  - **LAYER COUNT: 6 Layers**
  - **SURFACE TREATMENT: Electroless Au Plating**
  - **LAND GEOMETRY: 2mm sq.**
  - **BUILD-UP: HALOGEN FREE TYPE**

- **TEST METHOD**
  - **Solder the pin to a pre-determined land on the test vehicle.**
  - **Set the test vehicle with the soldered pin on the clamping vice of the test machine.**
  - **Set the longitudinal speed to 50mm/min on the pin and measure and record its strength after the pin is knocked down.**

- **SCHEMATIC OF TEST SETUP**

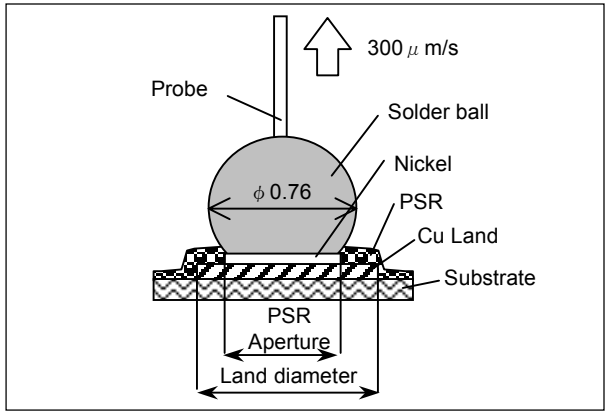


COMPARISON OF BALL PULL STRENGTH



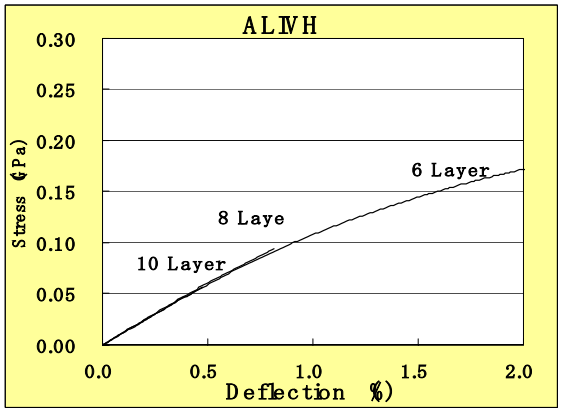
- **SPECIFICATIONS OF TEST VEHICLE**
  - **LAYER COUNT: 6 Layers**
  - **SURFACE TREATMENT: Electroless Au Plating**
  - **LAND GEOMETRY: 0.55mm sq.**
  - **PSR APERTURE: 0.45mm dia.**
  - **BUILD-UP: HALOGEN FREE TYPE**

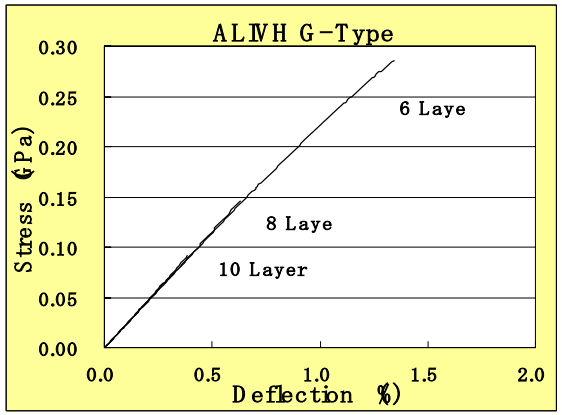
- **TEST METHOD**
  - **Place a solder ball (0.76mm dia) on a pre-determined land and reflow solder test vehicle with a solder ball (at peak temp. 240degC).**
  - **Heat the attached solder ball before puncturing it with the probe. Under cool air, lift the probe upwards at a longitudinal speed of 300um/s.**
  - **Measure and record the pull strength and its failure mode after separation.**
- **SCHEMATIC OF TEST SETUP**



COMPARISON OF BENDING STRENGTH

PLOTTED DATA OF STRESS vs DEFLECTION





- **ELASTIC MODULUS (GPa)**

(n=5 each)

	6 Layer	8 Layer	10 Layer
ALIVH	12.0	12.4	12.1
ALIVH-G	23.7	23.1	23.7

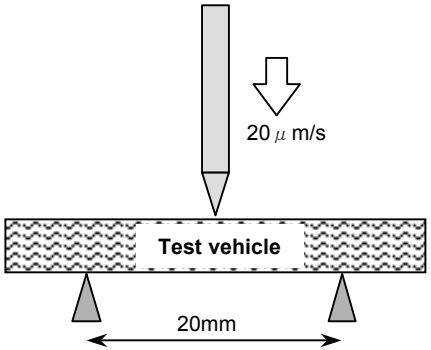
- **SPECIFICATIONS OF TEST VEHICLE**

- **LAYER COUNT: 6, 8, 10 Layers**
- **STRUCTURE: Base Material only (No copper foil layers)**
- **BUILD-UP: HALOGEN FREE TYPE**

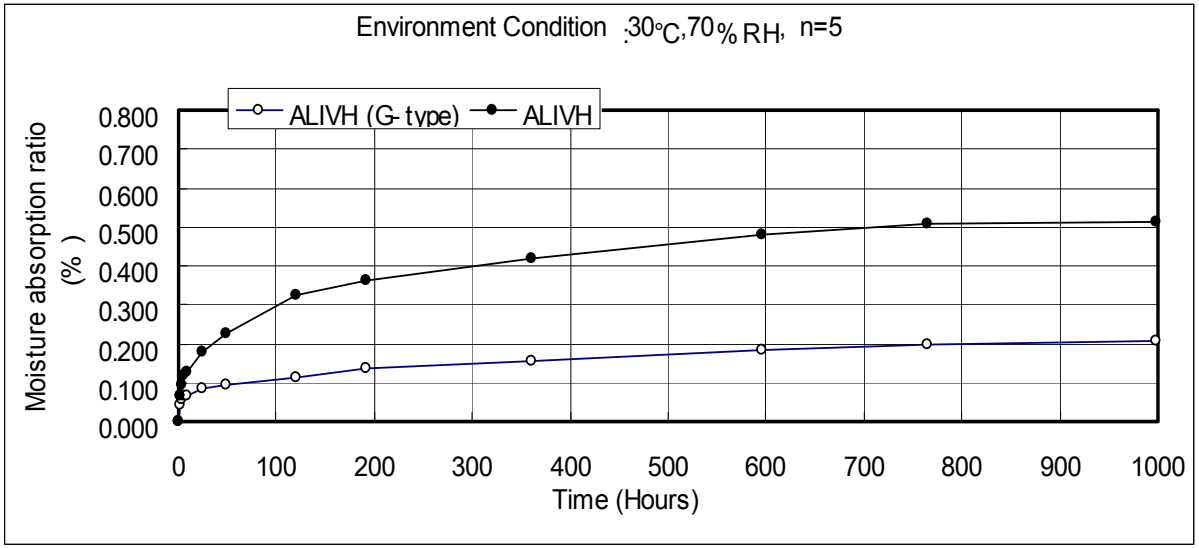
- **TEST METHOD**

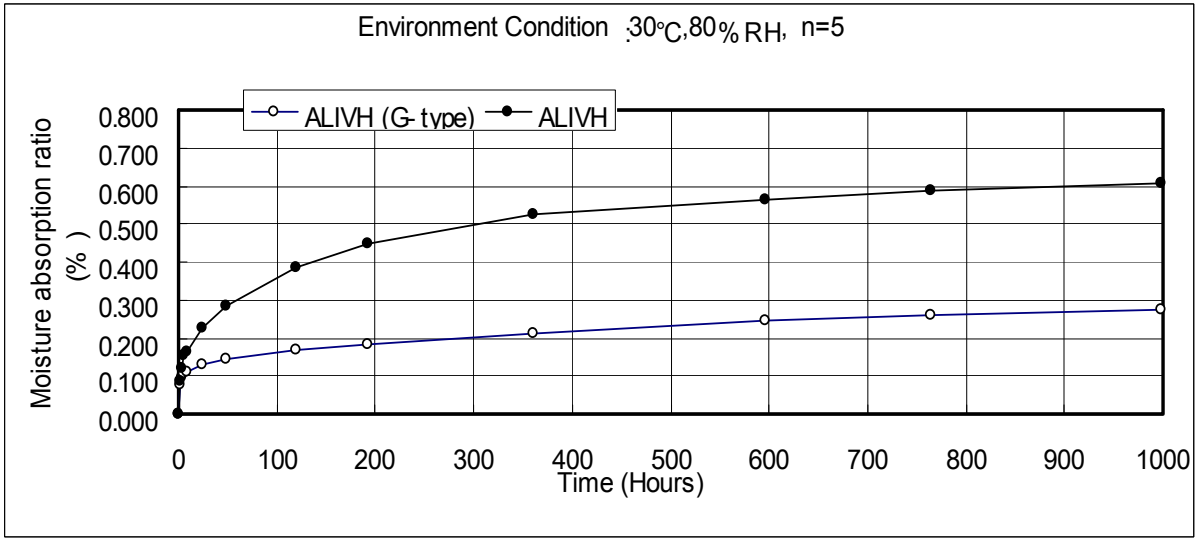
- **Set the test vehicle 20mm apart between the supports.**
- **Set the longitudinal speed of 20um/s at the centre of the test vehicle between the supports. Measure and record the corresponding stress and deflection.**
- **Determine the Elastic Modulus at 0.3% deflection using its corresponding stress.**

- **SCHEMATIC OF TEST SETUP**



MOISTURE ABSORPTION RATIO

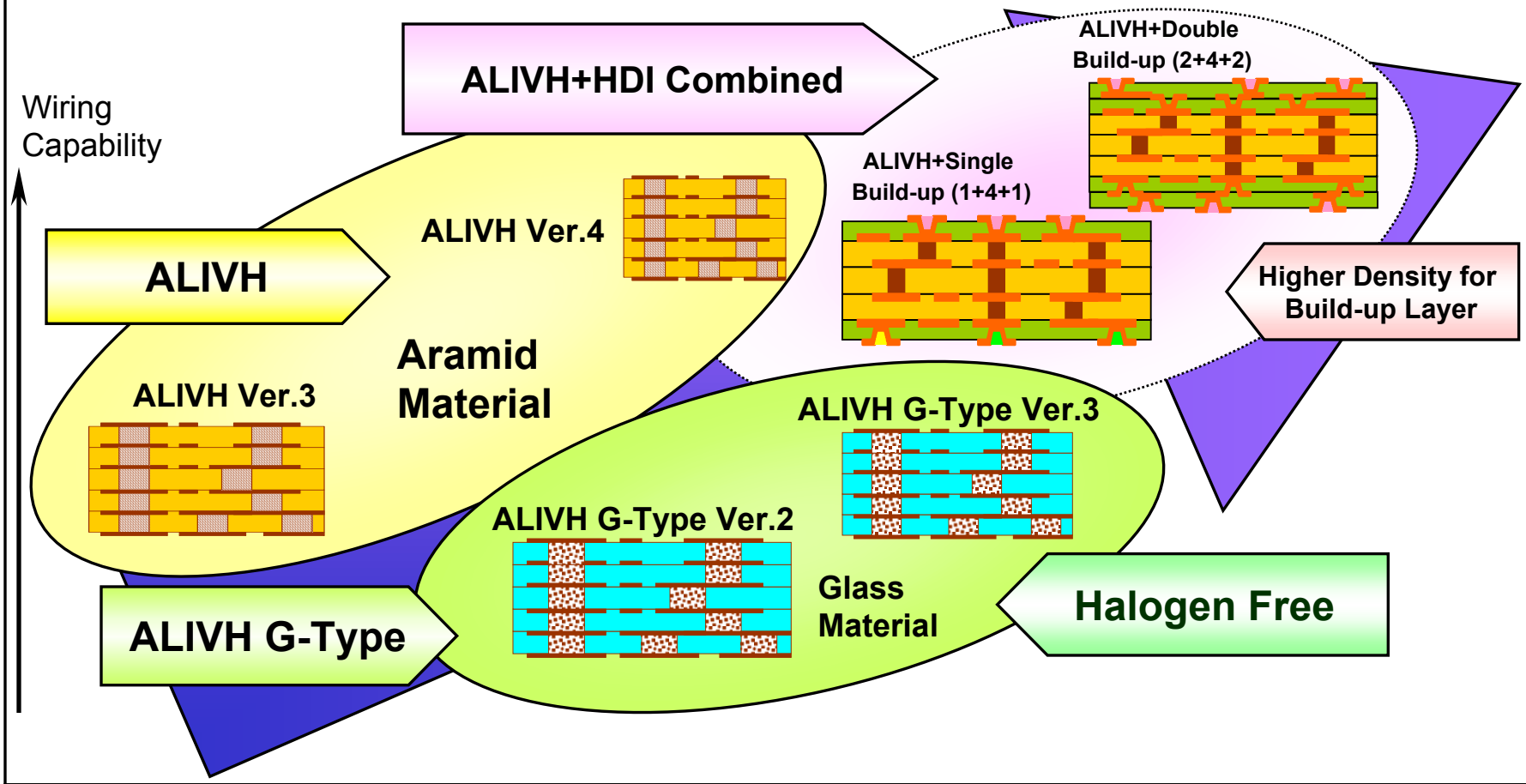




DEVELOPMENT ROADMAP

ALIVH DEVELOPMENT ROADMAP

Component		0.8CSP	0.5CSP	0.4/0.3CSP	0.25CSP	FC&DCA
PWB	V/L	200/400	150/300	100/200	80/150	50/80
	L/S	60/90	60/70	50/50	35/35	25/25
Version		Ver.2	Ver.3	Ver.4	HDI Combined	



Year 2001 2002 2003 2004