Roadmap Technology Verification (Section A-5)

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Purpose

- Compare the current RCG and SoA rigid board manufacturing data presented in **Section E** to the **IPC PCQR² Database**
- Validate the technology roadmap data, comment on inconsistencies, and expand on the roadmap information to include additional attributes

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IPC PCQR² Database

- Capabilities demonstrated by PCB manufacturers based on industry standard test vehicles
- Applications
  - Statistically **benchmark** board suppliers' capabilities
  - Perform **intelligent sourcing**
  - Select **new suppliers**
  - Ensure **design for manufacturability**
  - Establish realistic **design rules**

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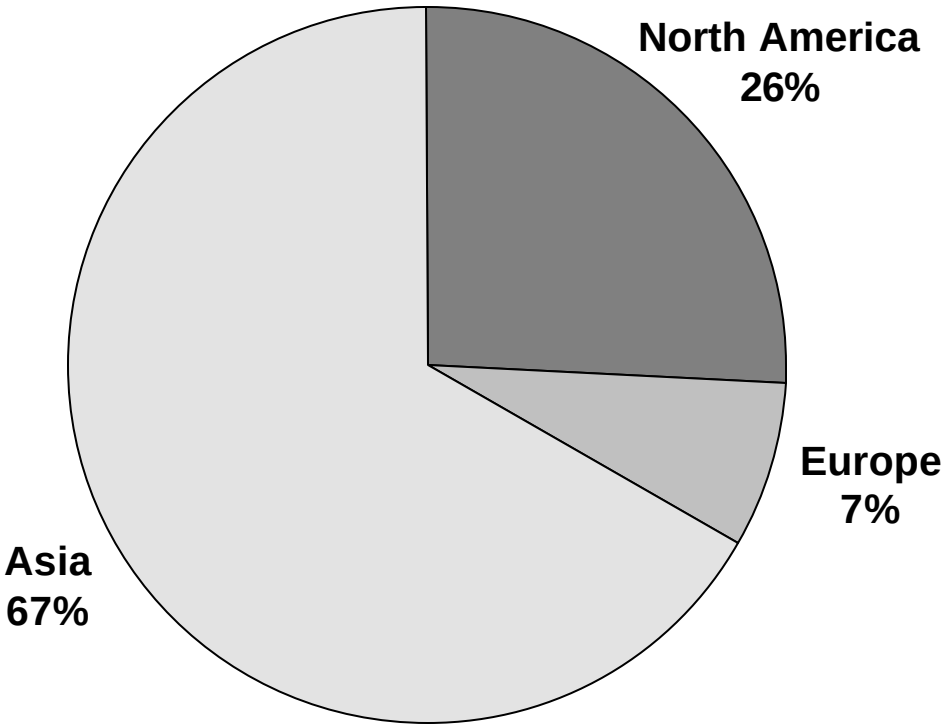
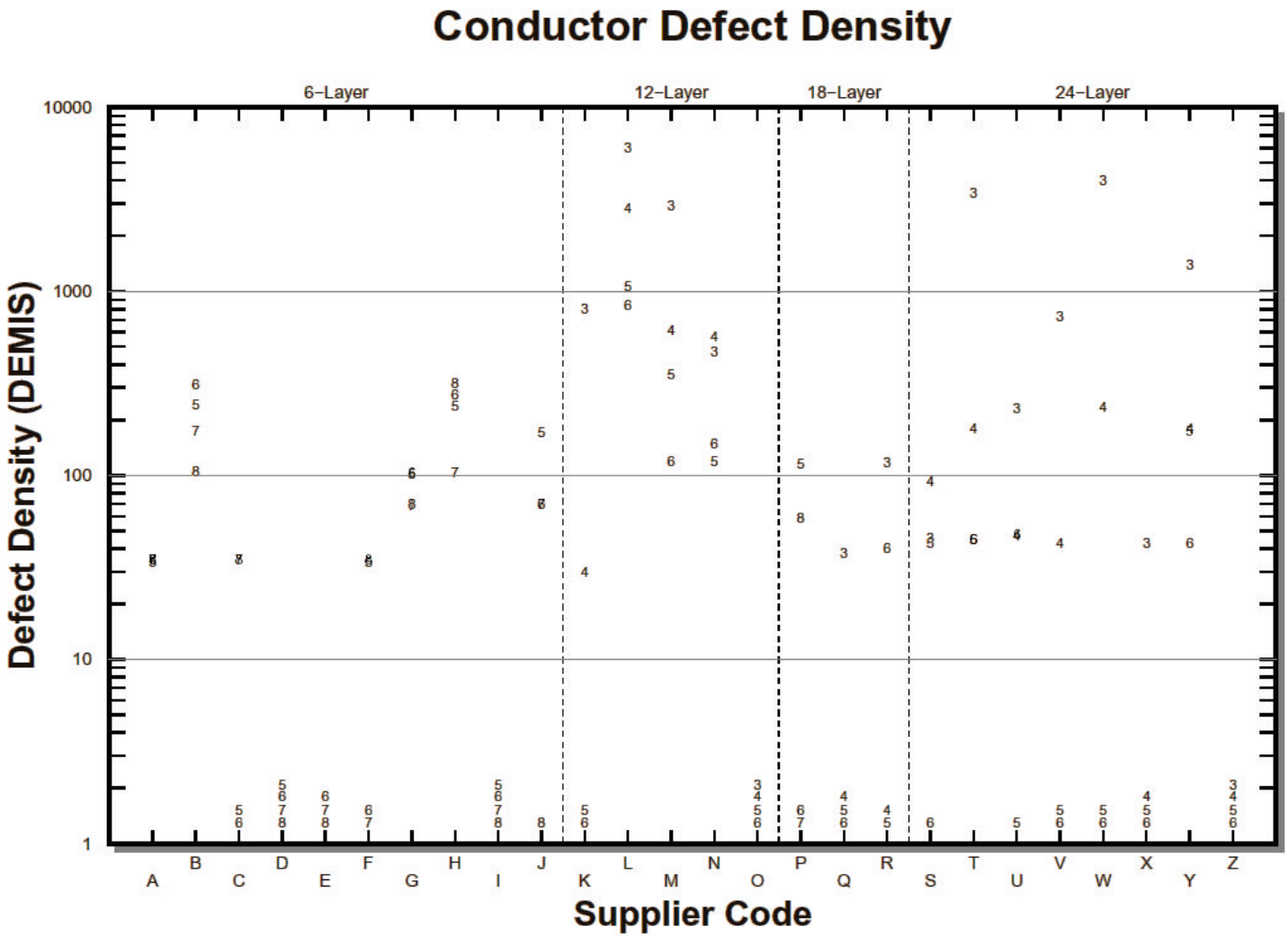
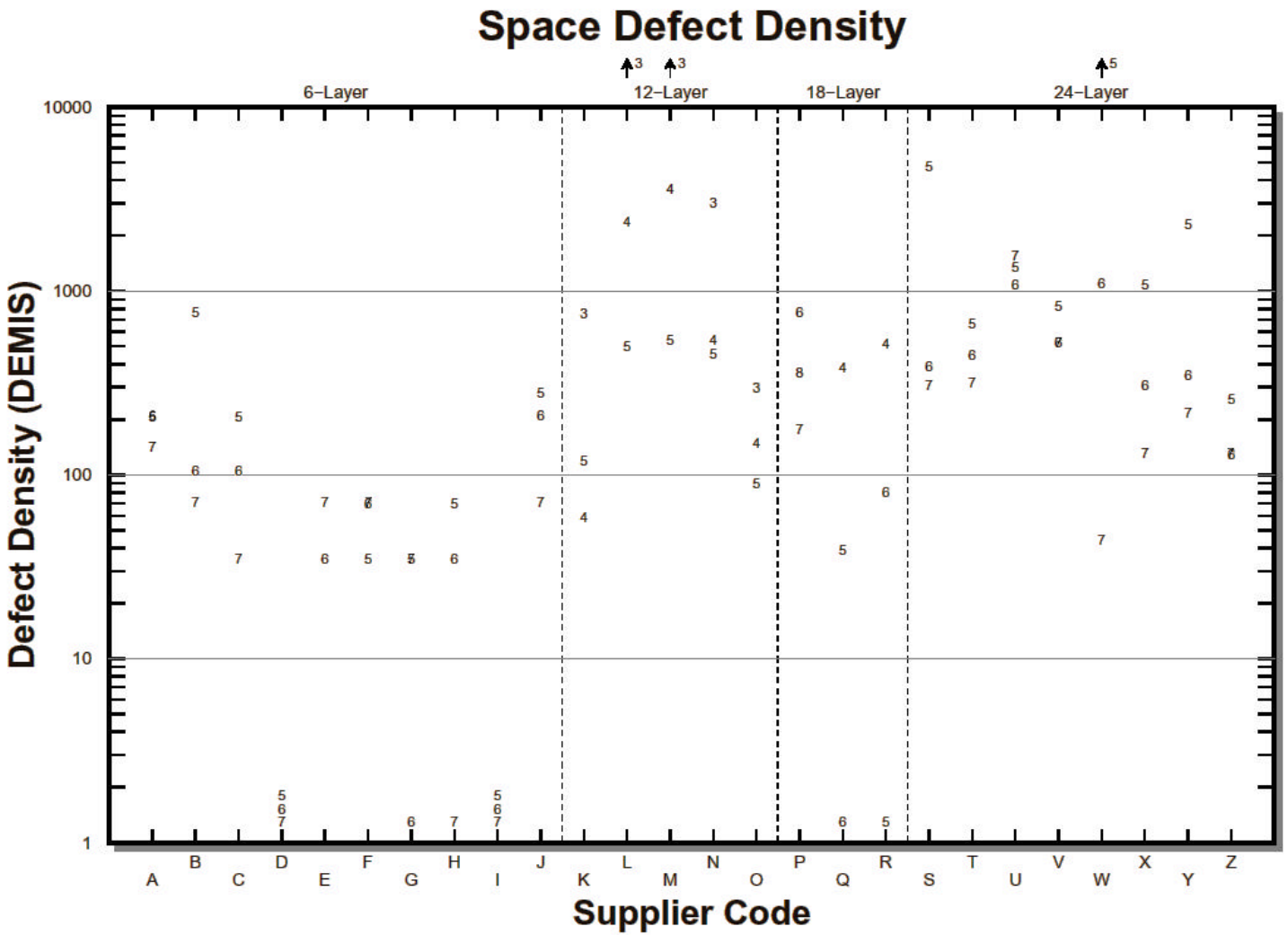


As of September 2002

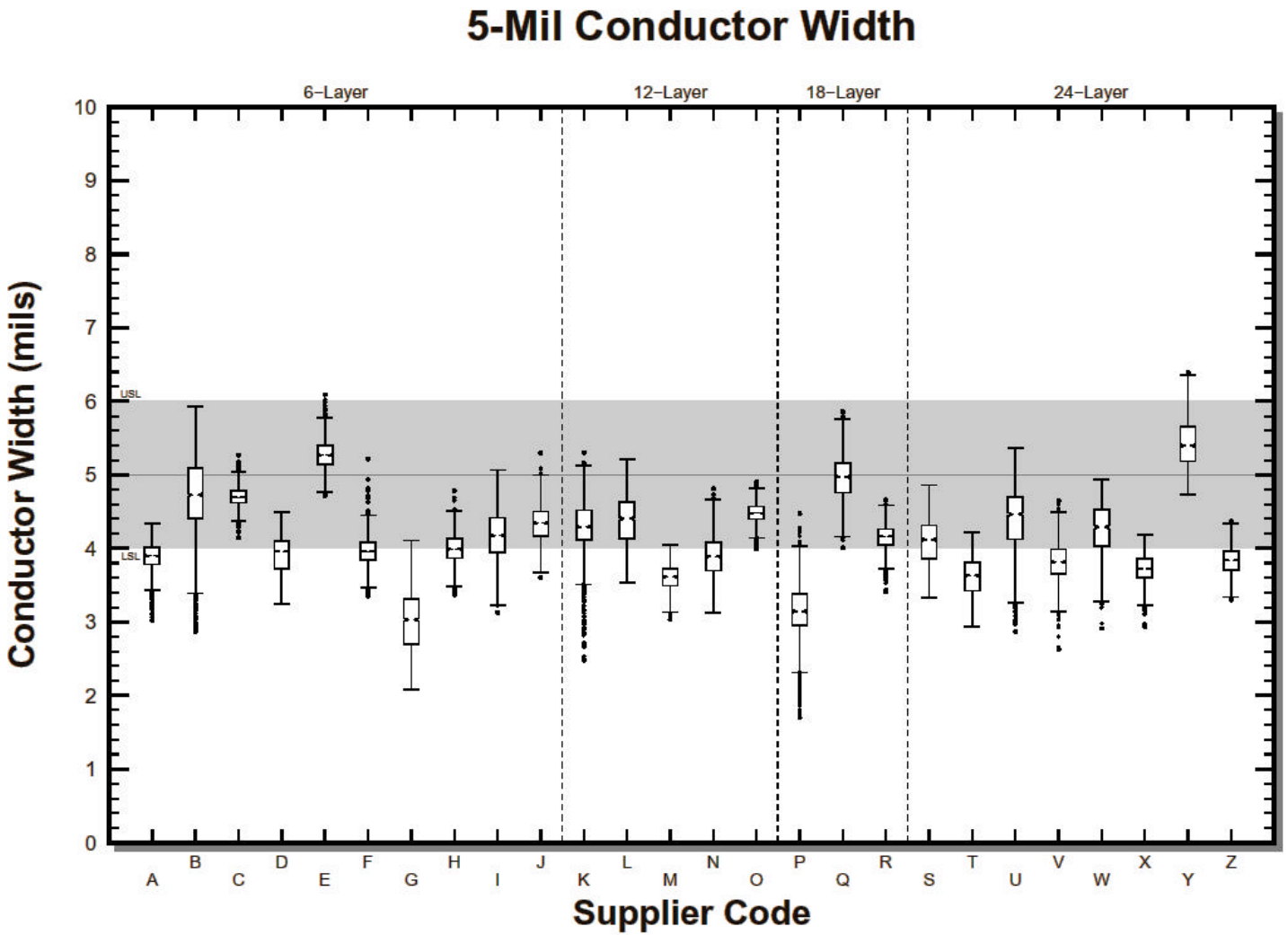
Outerlayer


Conductor Defect Density
6–Layer
12–Layer
18–Layer
24–Layer
Defect Density (DEMIS)
10000
1000
100
10
1
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z
Supplier Code

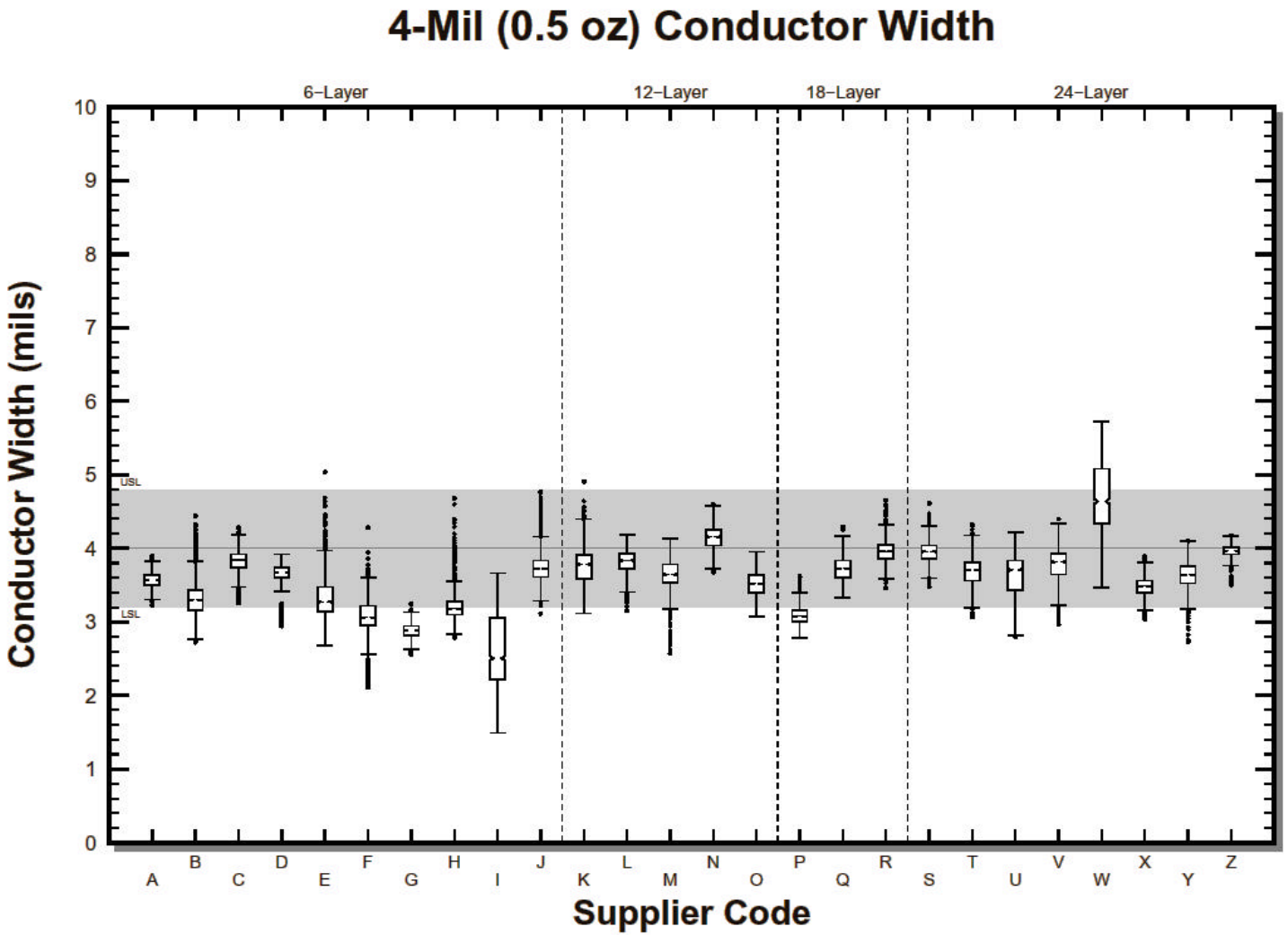
Outerlayer


Space Defect Density
6–Layer
12–Layer
18–Layer
24–Layer
Defect Density (DEMIS)
10000
1000
100
10
1
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z
Supplier Code

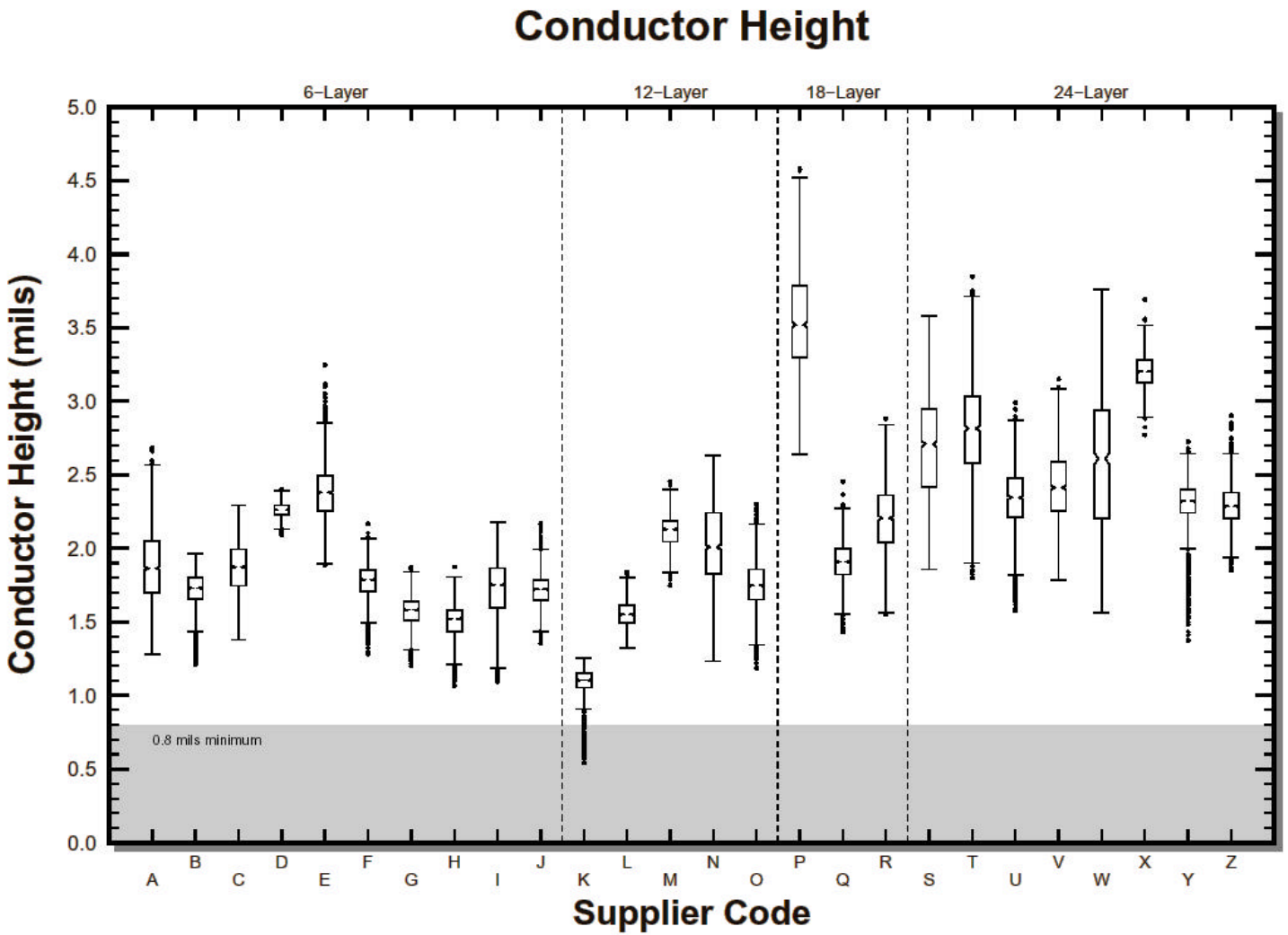
Outerlayer


5-Mil Conductor Width
6–Layer
12–Layer
18–Layer
24–Layer
Conductor Width (mils)
USL
LSL
0
1
2
3
4
5
6
7
8
9
10
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z
Supplier Code

Innerlayer


4-Mil (0.5 oz) Conductor Width
6–Layer
12–Layer
18–Layer
24–Layer
Conductor Width (mils)
USL
LSL
0
1
2
3
4
5
6
7
8
9
10
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z
Supplier Code

Outerlayer


Conductor Height
6–Layer
12–Layer
18–Layer
24–Layer
Conductor Height (mils)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.8 mils minimum
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z
Supplier Code

Outerlayer Conductor and Space

Table A5-1. Outerlayer Conductor and Space Formation (1.5mm Board Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Conductor Size (µm)	150	60	150	75
Space Size (µm)	150	60	150	75
Conductor Width Tolerance (µm)	40	15	46	24

Table A5-2. Outerlayer Conductor and Space Formation (3.0mm Board Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Conductor Size (µm)	-	-	100	75
Space Size (µm)	-	-	175	150
Conductor Width Tolerance (µm)	-	-	50	30

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Innerlayer Conductor and Space

Table A5-3. Innerlayer Conductor and Space Formation

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Conductor Size (µm)	125	50	75	50
Space Size (µm)	125	50	100	75
0.5-oz. Width Tolerance (µm)	35	10	36	16
1.0-oz. Width Tolerance (µm)	-	-	48	24

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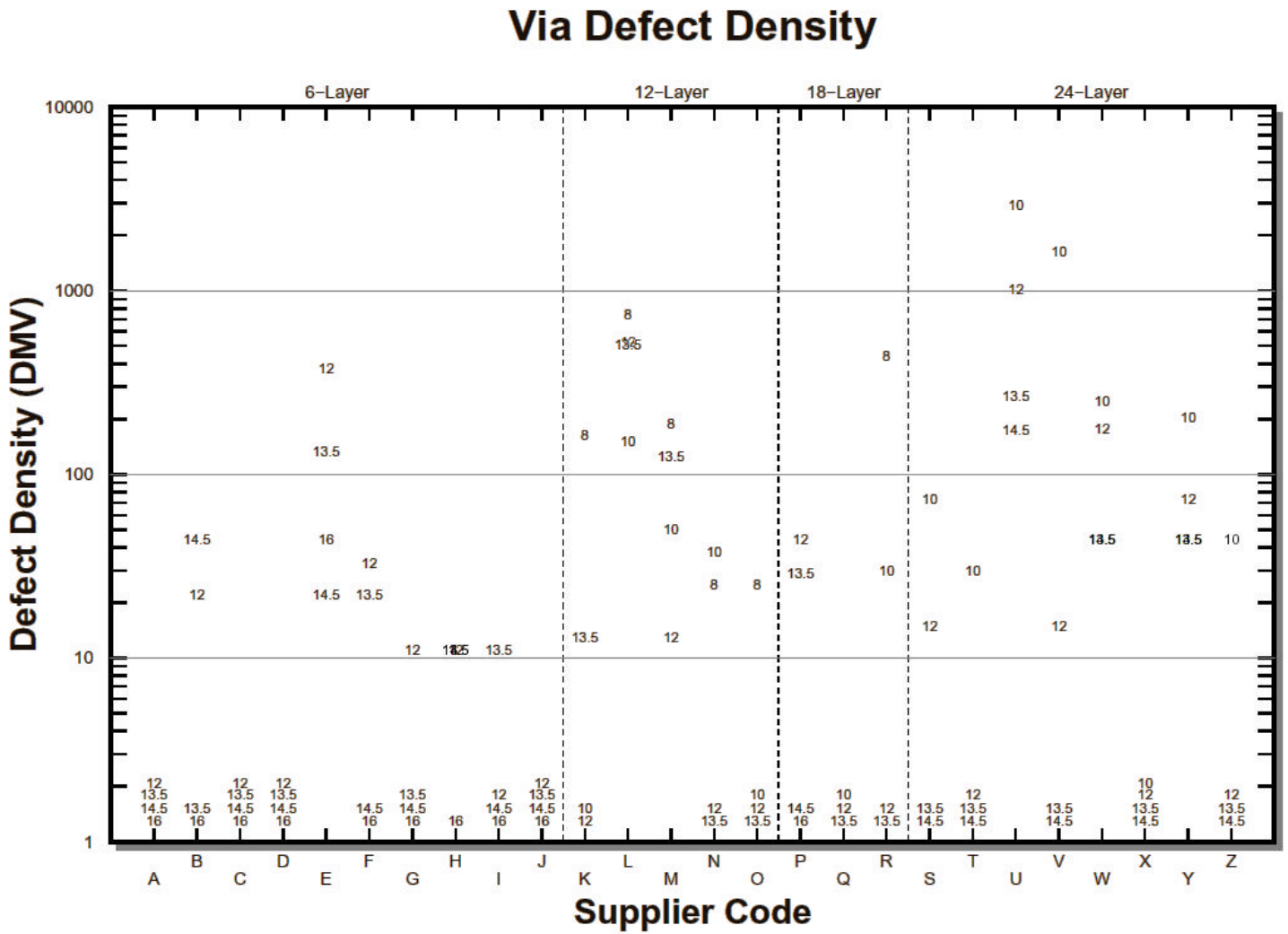
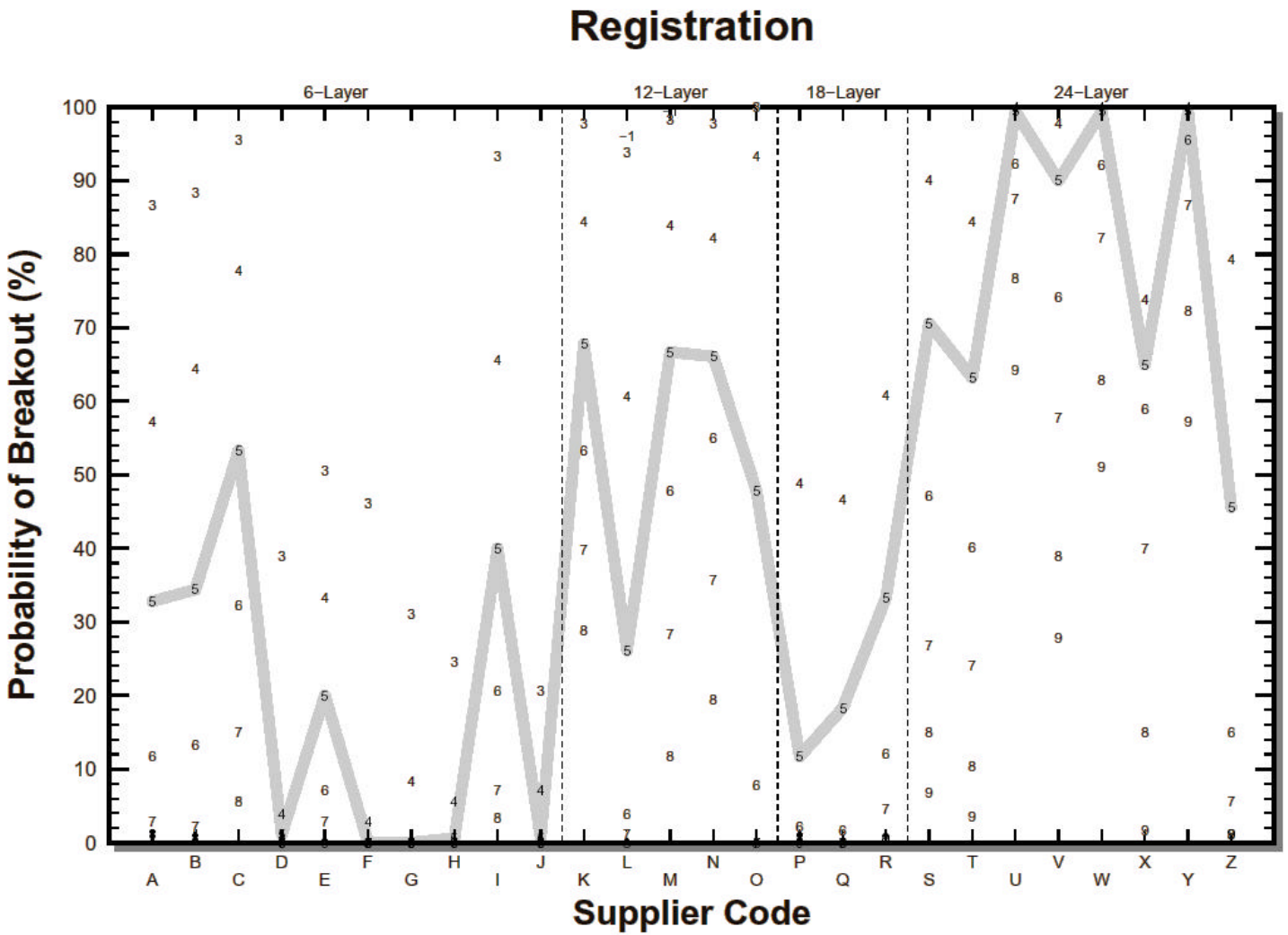
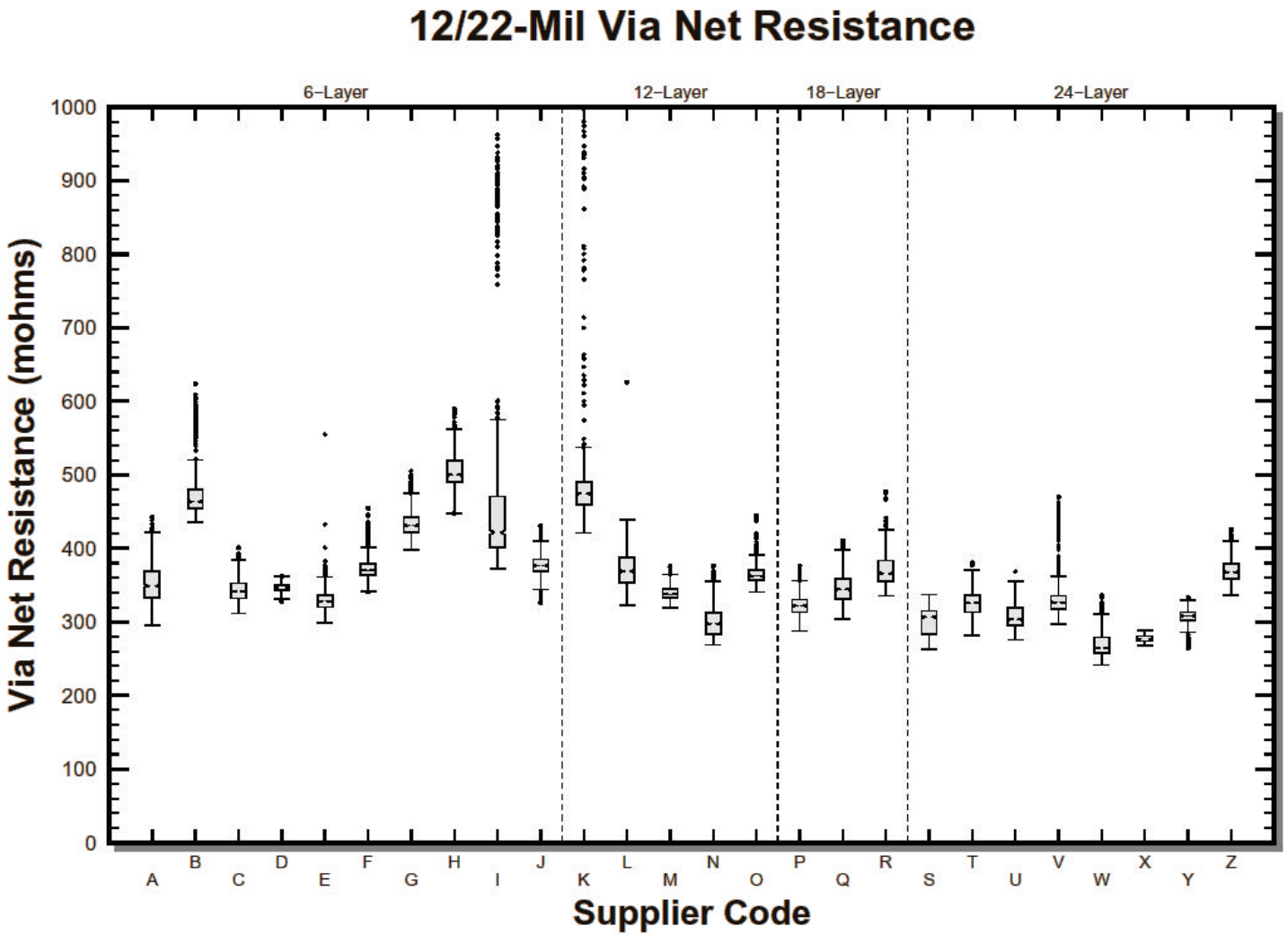
Through Via


Via Defect Density
6–Layer
12–Layer
18–Layer
24–Layer
Defect Density (DMV)
10000
1000
100
10
1
Supplier Code
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z

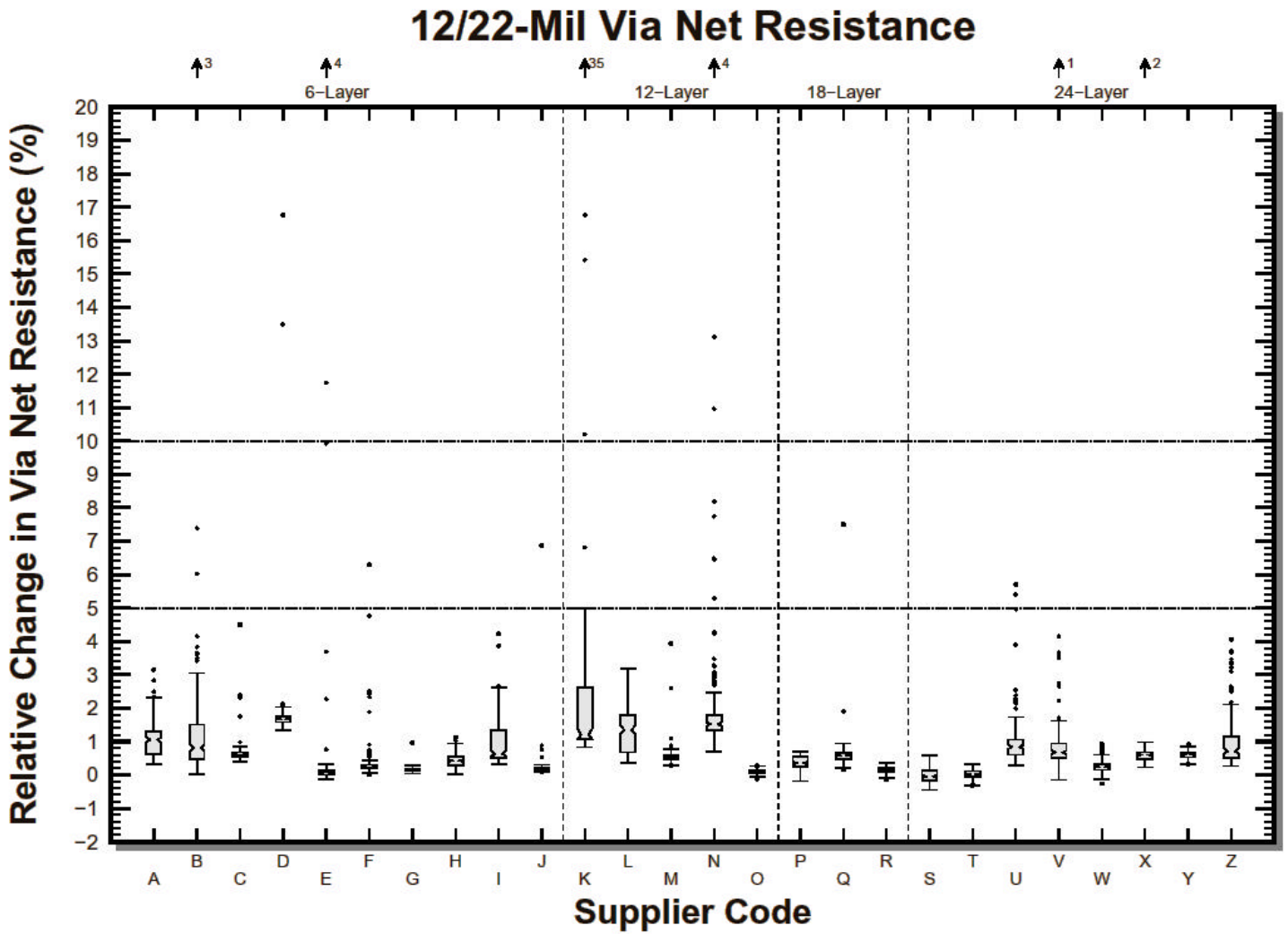
Through Via


Registration
6–Layer
12–Layer
18–Layer
24–Layer
Probability of Breakout (%)
100
90
80
70
60
50
40
30
20
10
0
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z
Supplier Code

Through Via


12/22-Mil Via Net Resistance
6–Layer
12–Layer
18–Layer
24–Layer
Via Net Resistance (mohms)
1000
900
800
700
600
500
400
300
200
100
0
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z
Supplier Code

Through Via


12/22-Mil Via Net Resistance
6–Layer
12–Layer
18–Layer
24–Layer
Relative Change in Via Net Resistance (%)
Supplier Code
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

Through Via

Table A5-4. Through Via Formation (1.5mm Board Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	300	200	300	200
Annular Ring (µm)	-	-	200	100

Table A5-5. Through Via Formation (3.0mm Board Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	-	-	300	250
Annular Ring (µm)	-	-	300	200

Blind Via

Table A5-6. PCQR^2 Database Blind Via Structures

Description	Formation Method	Interconnect
1-Deep Blind	Laser (typical)	1 to 2 and n to n-1
2-Deep Blind	Laser (typical)	1 to 3 and n to n-2
3-Deep Controlled Depth Drill	Mechanical	1 to 4

Table A5-7. 1-Deep Blind Via Formation (75m Dielectric Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	-	75	150	75
Annular Ring (µm)	-	-	125	75

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Blind Via Cont.

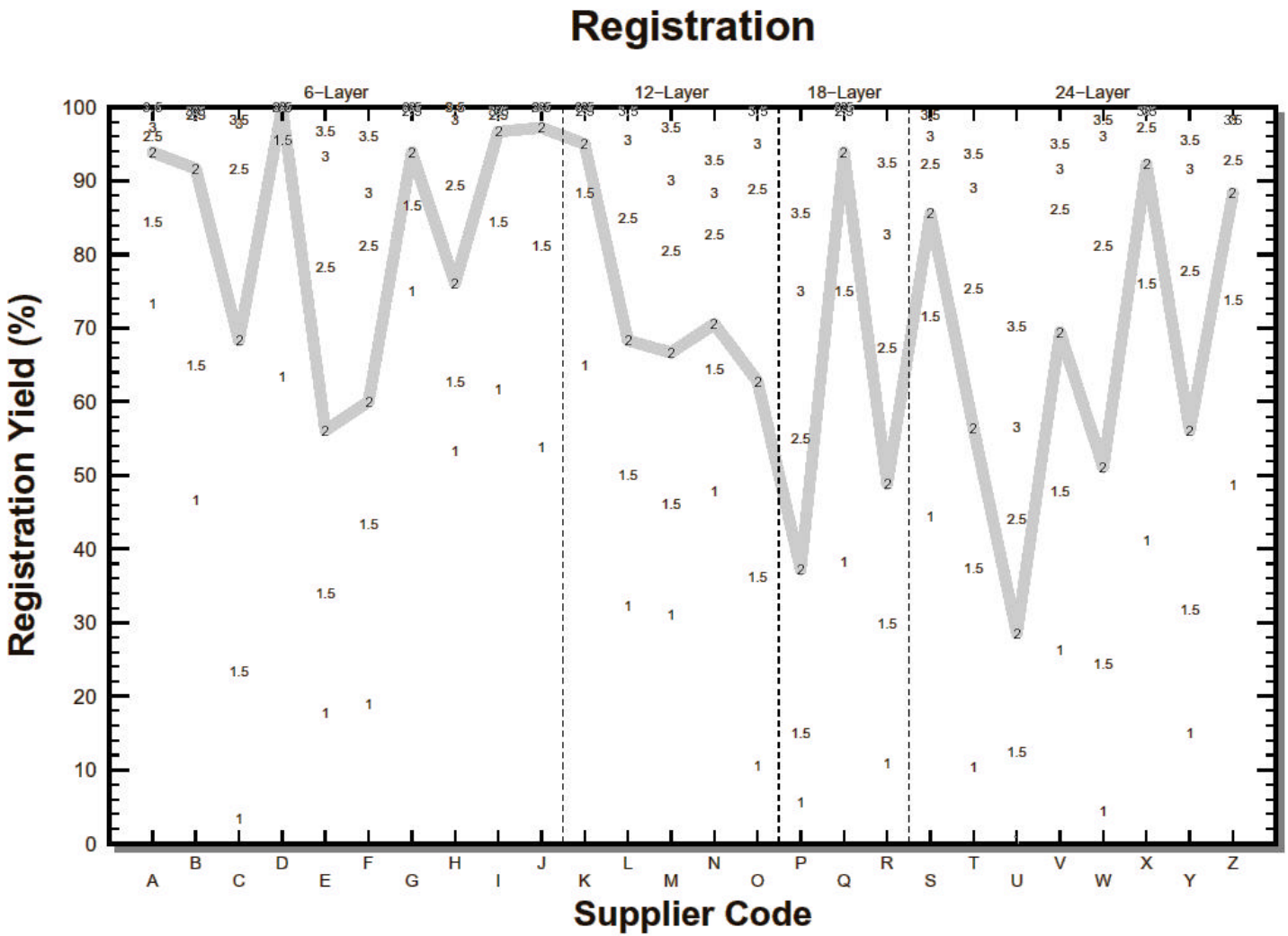
Table A5-8. 2-Deep Blind Via Formation (175㎛ Dielectric Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR² DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	-	-	250	175
Annular Ring (µm)	-	-	125	75

Table A5-9. 3-Deep Controlled Depth Drill Via Formation (300㎛ Dielectric Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR² DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	-	-	450	350
Annular Ring (µm)	-	-	200	100

Soldermask Registration



Soldermask Registration

Table A5-10. Soldermask Registration

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Registration (µm)	75	50	88	63

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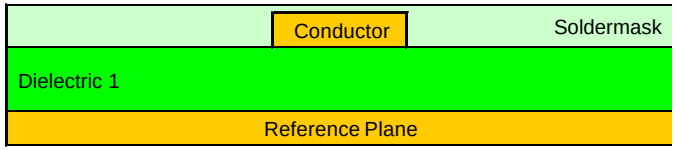
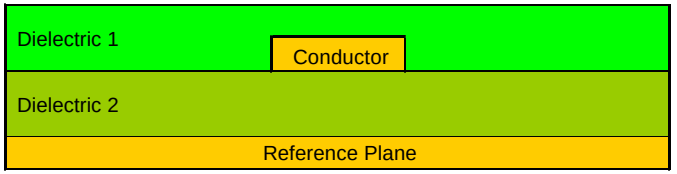
Controlled Impedance Structures

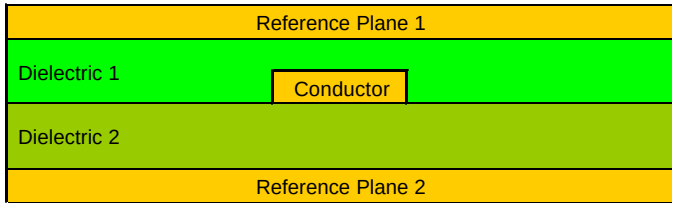
Figure A5-2. PCQR^2 Controlled Impedance Structures



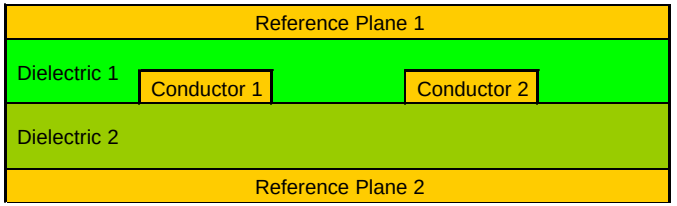
(a) Surface Microstrip



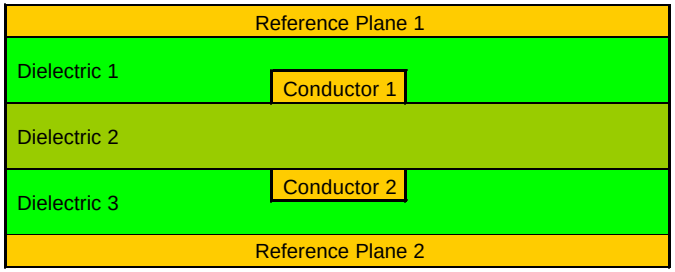
(b) Embedded Microstrip



(c) Stripline

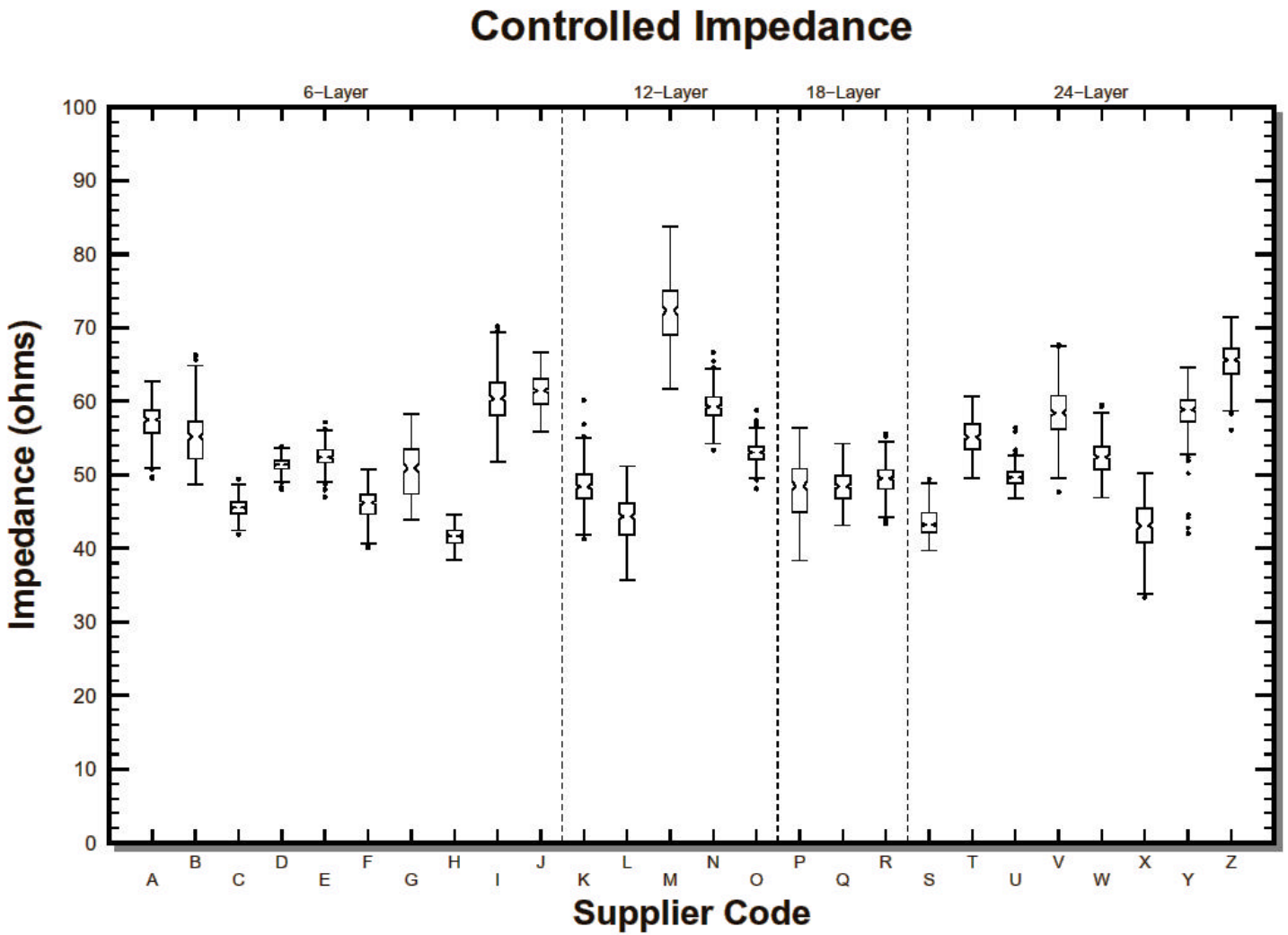


(d) Edge-Coupled Differential Stripline



(e) Broadside-Coupled Differential Stripline

Surface Microstrip



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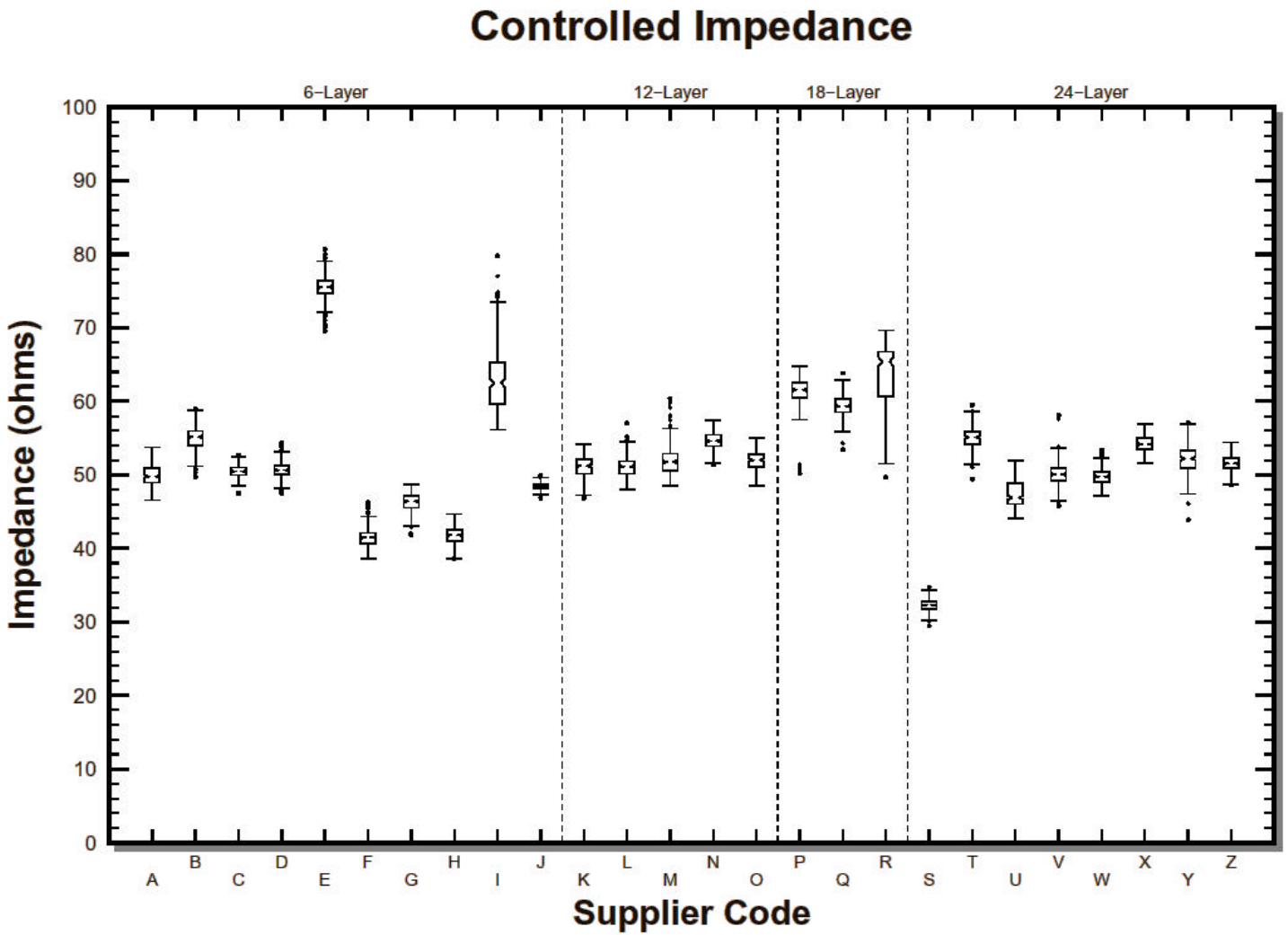
Embedded Microstrip



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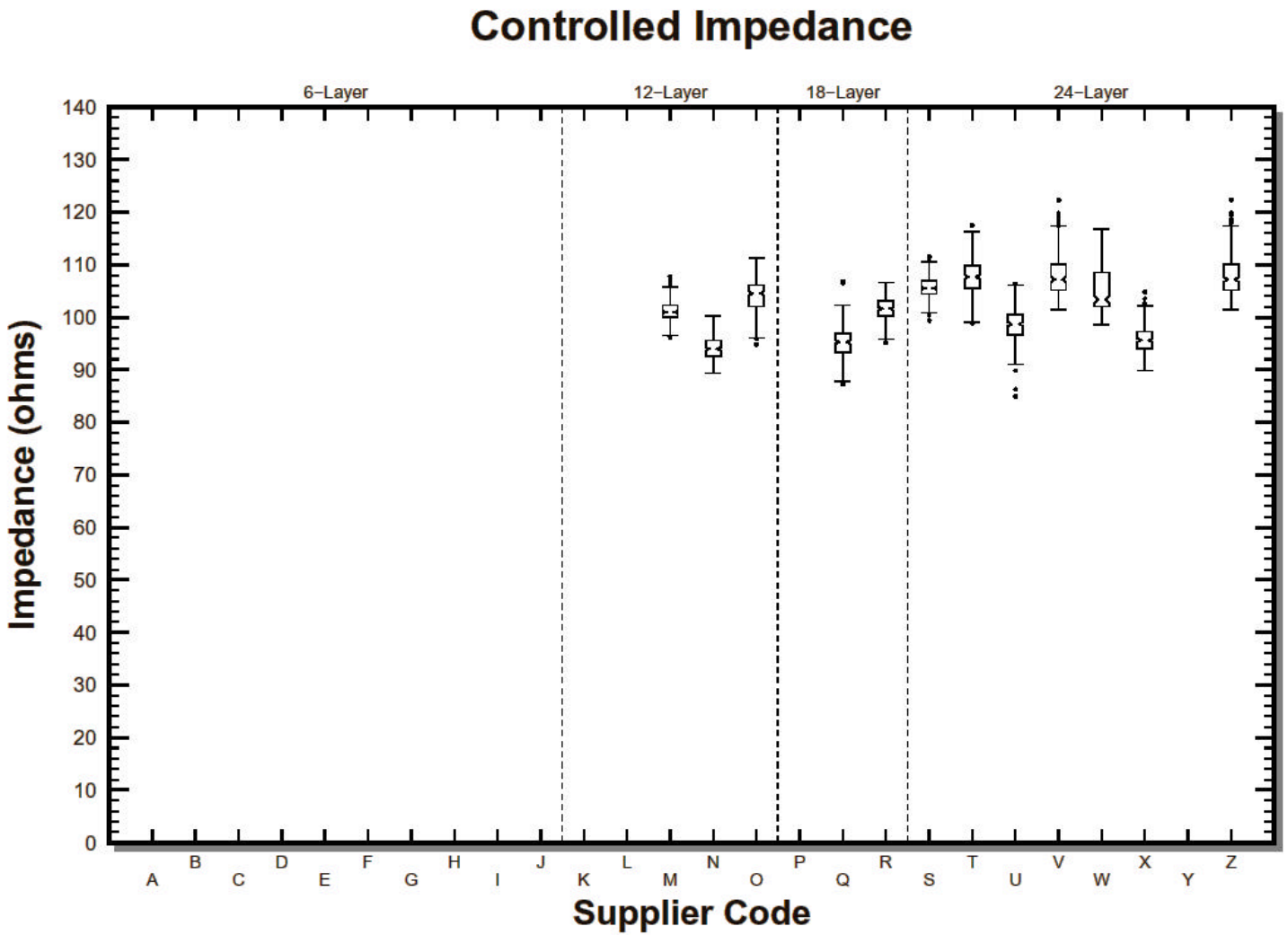
Edge Coupled Differential Stripline



Controlled Impedance

Table A5-11. Controlled Impedance Formation (125㎛ Conductor)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Surface Microstrip C_p	-	-	0.8	1.4
Embedded Microstrip C_p	-	-	1.3	2.4
Stripline C_p	-	-	1.3	1.8
Edge-Coupled Differential Stripline C_p	-	-	1.3	2.0
Broadside-Coupled Differential Stripline C_p	-	-	1.1	1.6