Investigation into Challenges of using .BSDL Files: iNEMI Survey Results and Conclusions

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Abstract
The number one issue identified by the 2009 International Electronics Manufacturing Initiative (iNEMI) Boundary-Scan survey was problems with obtaining correct and compliant boundary-scan description language (.bsdl) files from the semiconductor industry for use in boundary-scan printed circuit board assembly (PCBA) test generation. The major conclusions from the survey were:

- The semiconductor industry needs to make a greater effort to produce correct and compliant BSDLs.
- A better job needs to be done verifying .bsdl file compliance to the implemented JTAG hardware.

Non-compliance is typically found when a test is generated and it doesn't work!

The consequences of not having correct and compliant .bsdl files to generate boundary-scan tests is the inability to generate boundary-scan based tests and if tests cannot be generated, the result is lower overall test coverage for PCBAs which results in higher manufacturing costs and lower overall product quality.

The work presented here by the iNEMI Boundary Scan Phase 3: Investigation into Challenges of Using .BSDL Files project group takes a more comprehensive view of the problem by surveying the industry to determine if issues associated with .bsdl files identified in the 2009 iNEMI Boundary-Scan survey still exist (and if so to what extent) and to identify new issues.

Introduction
iNEMI is a not-for-profit R&D consortium of approximately 100 leading electronics manufacturers, suppliers, associations, government agencies and universities. iNEMI roadmaps the future technology requirements of the global electronics industry, identifies and prioritizes technology and infrastructure gaps, and helps eliminate those gaps through timely, high-impact deployment projects. These projects support members' businesses by accelerating deployment of new technologies, developing industry infrastructure, stimulating standards development, and disseminating efficient business practices. iNEMI is based in Herndon, Virginia (near Washington, D.C.), with regional offices in Asia (Shanghai and Tokyo) and Europe (Limerick, Ireland). For additional information about iNEMI, visit http://www.inemi.org.

The iNEMI Boundary-Scan Adoption Phase 3 Project was organized under the Board and Systems Manufacturing Test Technology Integration Group (TIG). The project's overall goal is to promote wider adoption of boundary-scan (JTAG/IEEE 1149.x) throughout the electronics industry, encourage semiconductor suppliers to include the technology in their products, and promote the development of tools by ATE (automated test equipment) suppliers to support boundary-scan based board test.

The Phase 3 project team developed an online survey covering .bsdl file usage, issues, generation, and validation and solicited participation from the iNEMI membership and team member contacts. It also promoted the survey at trade shows and on the iNEMI website.

In this paper, we will provide a brief description of the survey methodology, along with a review and analysis of the data obtained in the survey. Current and best practices for .bsdl file creation and validation will be identified and documented and results will be used to raise industry awareness of the issues and potential solutions.

Survey Methodology
It was determined that the survey should focus on three groups; Board/System Engineering, and Integrated Circuit (IC) Design and Development Engineering, and Integrated Circuit Manufacturing Engineering. Each group brings its own unique perspective to .bsdl file usage, issues, generation, and validation.

The first section of the survey consisted of general information, such as name, company name and primary business sector, company's annual sales, and respondent's primary area of responsibility (Board/System Engineering or Integrated Circuit Engineering). Depending on their answers, the respondents were then directed to either a Board/System Engineering survey or an Integrated Circuit Engineering survey. The IC Engineering section was further divided into IC

Design and Development Engineers and IC Manufacturing Engineers sections.

The Board/System Engineering section consisted of 15 questions that covered topics such as:

- job function
- industry (product) sector the respondent works in
- how .bsdl files are obtained
- .bsdl file usage information and issues associated with usage
- .bsdl file issue resolution
- .bsdl file issue impact
- .bsdl file quality status over the last few years
- knowledge and use of current and future boundary-scan standards

All IC Engineering respondents were asked nine questions that covered the following topics:

- Job function
- Industry (product) sector the respondent works in
- Role in creating .bsdl files
- How .bsdl files are created
- Issues associated with .bsdl file creation
- Knowledge and use of current and future boundary-scan standards
- Area of engineering responsibility (IC Design or IC Manufacturing)

The IC Design and Development Engineering section consisted of 22 questions that covered such topics as:

- .bsdl file generation
- .bsdl file verification
- .bsdl file usage and issues associated with usage
- Processes to update .bsdl files
- How IC test modes are accessed in development

The IC Manufacturing Engineering section consisted of 22 questions that covered such topics as:

- How .bsdl files are obtained
- .bsdl file verification
- .bsdl file usage and issues associated with usage
- Processes to update .bsdl files
- How IC test modes are accessed in manufacturing

Overall Respondent Statistics

A total of 86 people, from 37 companies in 10 countries responded to the survey. Of the respondents, 73 (85%) classified themselves as Board/System Engineering and 13 (15%) classified themselves as Integrated Circuit Engineering. Of the Integrated Circuit Engineers, 9 were IC Design Engineers and 4 were IC Manufacturing Engineers.

The majority of respondents work for original equipment manufacturers (OEMs) (37.8%), test equipment providers (30.5%), and third party test developers (12.2%). Table 1 shows the overall breakdown of the business of the respondent's company.

Table 1 – Primary Business of the Respondent's Company or Division

Primary Business	Response
OEM (Original Equipment Manufacturer)	37.8%
Test Equipment Provider (Manufactures Test Equipment)	30.5%
Third Party Test Developer	12.2%
IC Designer (IC Design or Layout)	7.3%
EMS/CM (Electronics Manufacturing Services/Contract Manufacturer)	3.7%
ODM (Original Design Manufacturer – manufactures products for rebranding)	3.7%
IC Fabricator (Manufacturer)	3.7%
Other (Sales/Marketing, DFT Services, Supplier Management)	1.2%

54.7% of the respondents work for companies with greater than $500 million in annual sales. 26.7% work for companies with sales in the $10 million to $500 million range, and 18.6% work for companies with less than $10 million range.

Board/System Engineering Respondent Demographics
Table 2 shows the overall job function breakdown for the Board/System Engineers.

Table 2 – Board/System Engineer Job Functions

Job Function	Response
Test/Measurement Equipment Engineer	31.3%
PCBA Structural Test Engineer (MDA/ICT/Boundary-scan)	17.2%
Design For Test (DFT) Consultant	14%
3rd Party Test Development Service	11%
Electrical Design Engineer	9.4%
PCBA Functional Test Engineer	7.8%
Test Engineering Manager	4.7%
Field Service Engineer	1.6%
Service and Support (service center or repair depot)	1.6%
Other	1.6%
Development Engineering Manager	0.0%
Manufacturing Manager	0.0%
PCBA CAD Designer	0.0%

The majority of Board/System Engineer respondents (31.3%) work as test/measurement equipment engineers for companies that design and sell test equipment. The next three largest groups are PCBA Structural Test Engineers (17.2%), DFT Consultants (14%), and 3rd Party Test Development Engineers (11%). 9.4% of the respondents were Electrical Design Engineers.

Figure 1 shows the overall industry sector break-down for the Board/System Engineering respondents. All industry sectors are fairly evenly represented in the survey.

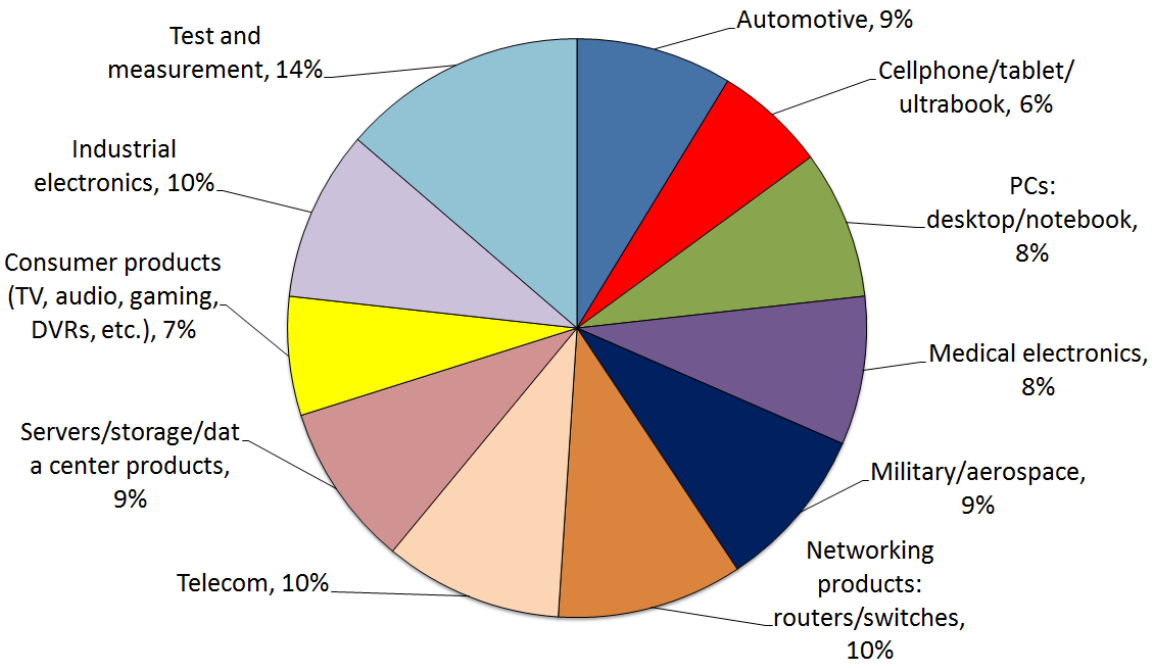

Figure 1 – Board/System Engineer Industry Sectors

IC Engineering Respondent Demographics

It should be noted that only 13 respondents classified themselves as IC Engineers. That sample size is too small to draw any conclusions from.

The top three respondent job functions for IC Engineering were DFX Engineer (43%), IC ATE Test Engineer (19%), and IC Design Designer (14%).

Table 3 shows overall job function break-down for the IC Engineering respondents.

Table 3 – IC Engineer Job Functions

Job Function	Response
DFx engineer (DFT, DFM, design for debug)	43%
Test engineer (IC ATE test development engineer)	19%
IC Design engineer - responsible for the design of integrated circuits	14%
Verification/validation engineer (IC design simulation/validation)	10%
Other (Marketing Manager, Design for Security)	10%
System test engineer (IC "functional test" engineer)	5%
IC engineering manager	0%
Physical design engineer (IC layout engineer)	0%
Product engineer (IC package type engineer)	0%

Figure 2 shows the overall industry sector break-down for the IC Engineering respondents. The top three represented sectors are Computing, NetCom, and Consumer. All segments were represented by at least one respondent.

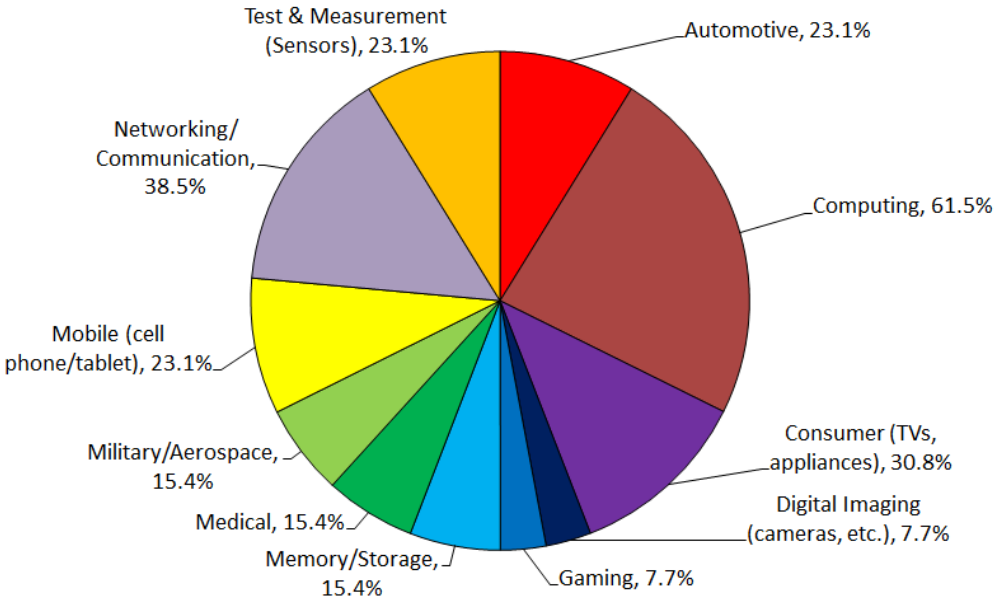

Figure 2 – IC Engineer Industry Sectors

Board/System Engineering .bsdl File Usage Review and Analysis

Board/System Engineer respondents were asked several questions dealing with .bsdl file usage so the team could gauge how many .bsdl files are used, what types of devices they were for, what processes .bsdl files were used in, and where .bsdl files were obtained from.

As shown in Figure 3, the majority of respondents use more than 10 .bsdl files per year. 31% use between 11-20, 27% use 21-50, and 19% use greater than 50 per year.

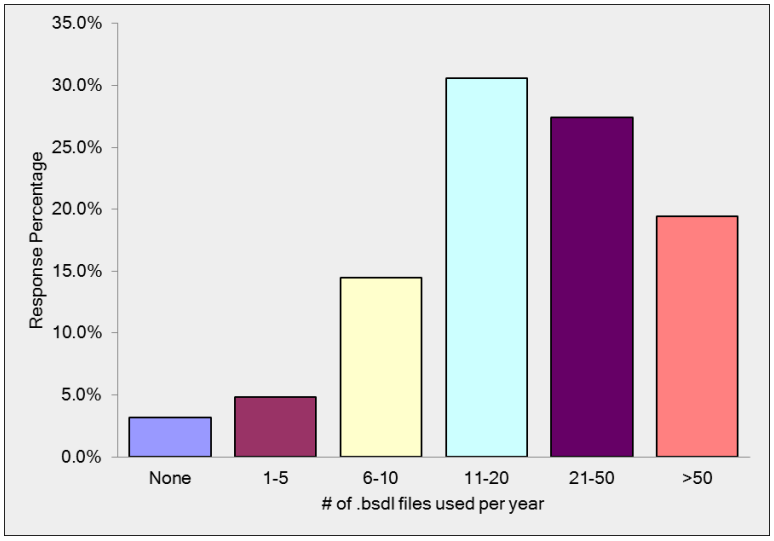

Figure 3 – # of .bsdl Files Used per Year

When queried about the types of devices that the .bsdl files were for, programmable devices (CPLDs, FPGAs, etc.) were the majority, followed by processors, network controllers, ASICs, and computer chipsets. Since the distribution between devices types only varied about 8% between lowest and highest, it appears that all device types are adequately represented in the data. Complete data is in Table 4 below.

Table 4 – .bsdl Device Types

Device Type	Response
Programmable devices (CPLDs, FPGAs, etc.)	18.5%
Processors	17.5%
Network Controllers	15%
ASICs	14.6%
Computer Chipset	13.7%
Other	10.8%
Storage Controllers	9.9%

.bsdl files can be used to generate boundary-scan tests in many places in the product development and/or manufacturing process. The Board/System engineer respondents reported using .bsdl files for the processes shown in table 5.

Table 5 – Processes where .bsdl Files Are Used

Process	Response
Structural test – single device or scan chain test, virtual nails, device id.	28.3%
Device programming (in-system programming)	25.7%
Product development – debug and verification of prototype designs	18.7%
Functional test – board level, system level	18.2%
Field service – test of systems/boards in the field	7.5%
Other (ESS, “testing” Built-in-self-test)	1.6%

Over 60% of the respondents said they obtain .bsdl files from IC supplier websites. Product development engineers and OEMs were that next two highest cited sources with 13.1% each. The remainder obtained them from IC applications engineers, IC sales engineers and online repositories. Complete data is shown in Table 6.

Table 6 – Sources of .bsdl Files

.bsdl File Source	Response
IC supplier website	62.3%
Product development engineers	13.1%
OEM	13.1%
IC apps engineers	4.9%
IC sales engineers	3.3%
Online repository - please provide the URL	3.3%

Almost all Board/System engineers reported difficulties in getting some .bsdl files. The biggest difficulty is when non-disclosure agreements are required to obtain the .bsdl file. The next highest reported obstacle is obtaining pre-release device .bsdl files to use for product development test process before the IC is formally released. Complete data is shown in Table 7. The most common "Other" response was a variation on this theme: not being able to find where or from who to obtain the .bsdl file.

Table 7 – Difficulties in Obtaining .bsdl Files

	Response
NDAs are required to obtain .bsdl for new/custom/unreleased devices	66.7%
Pre-release device .bsdl's difficult to obtain in a timely manner	63.3%
Wrong .bsdl (revision or device type) delivered	51.7%
All .bsdl files in the file set not delivered	23.3%
Other (please specify)	18.3%

Board/System Engineering .bsdl File Issue Review and Analysis

Issues that Board/System engineers have with using .bsdl files, along with the frequency of those issues, type of issues, impact of issues, and resolution of issues is a one of the primary sets of data the team wanted to obtain in order to determine the root cause of the issues. Once a root cause is identified, corrective actions to reduce or eliminated that root cause can be determined.

Over 50% of Board/System engineers reported issues with 1-20% of the .bsdl files they use. 22% reported the 21-40% of .bsdls had issues. Complete data is shown in Table 8. It is clear from the data that almost everyone experiences issues with .bsdl files a significant amount of the time.

Table 8 – Percentage of .bsdl Files with Usage Issues

% of .bsdl files with issues encountered	**Response**
None	6.3%
1-20%	52.4%
21-40%	22.2%
41-60%	14.3%
61-80%	3.2%
81-99%%	1.6%
100%	0.0%

Table 9 shows what percentage of respondents had each particular type of issue listed when trying to use .bsdl files. The number one issue was syntax errors. "Other" issues specified by 23% of respondents were functional issues with the content of the .bsdl file not specifically in Table 9, i.e. not syntax issues.

Table 9 – .bsdl Usage Issues Encountered

Issue Encountered	Response
Syntax errors	65.6%
Differential pins not described correctly	47.5%
No compliance pins listed	44.3%
Incorrect cell types (i.e. standard pins described as self-monitoring pins or vice versa)	39.3%
.bsdl is for a down revision device	37.7%
Incorrect device identification code	37.7%
Device pin mapping incorrect (wrong package)	32.8%
Device cell mapping incorrect	29.5%
Length of boundary-scan register is incorrect	27.9%
Complete file set not provided from source (i.e. package file missing)	27.9%
Device pin mapping incorrect (for die, not package)	24.6%
Other	23.0%
Commands in wrong order for version of IEEE1149.1 used on the device	19.7%
Incorrect instruction codes	14.8%
.bsdl incompatible for 2nd source IC	14.8%
Multi-vendor .bsdl issues (SoCs)	11.5%
I don't have issues.	9.8%
Embedded taps not properly defined	9.8%
Issues with the file set (i.e. mixed or down revision files)	6.6%

When asked how they fix .bsdl files that have issues, 83% of Board/System engineers said they manually edit the file, 62% said they get an updated .bsdl from the IC supplier website, 57% report it to the device supplier and get them to fix it, 26% contact 3rd party boundary-scan test suppliers for help and 6.6% said they don't have any issues to fix. The 6.6% that specified other answers not listed were just minor variations of the previous solutions. Figure 4 is a graphical representation of this data.

Figure 4 – Solutions for fixing .bsdl Files That Have Issues

The impact of having a .bsdl with issues is typically delay of test development and/or test coverage loss. Respondents were asked what impacts they see when they have issues. 89% reported test development delays. About 55% reported partial test coverage loss in boundary-scan tests and 23%-25% reported full test coverage loss in single and multi-device boundary-scan tests. Almost 28% reported product development delays. Figure 5 shows the respondent data.

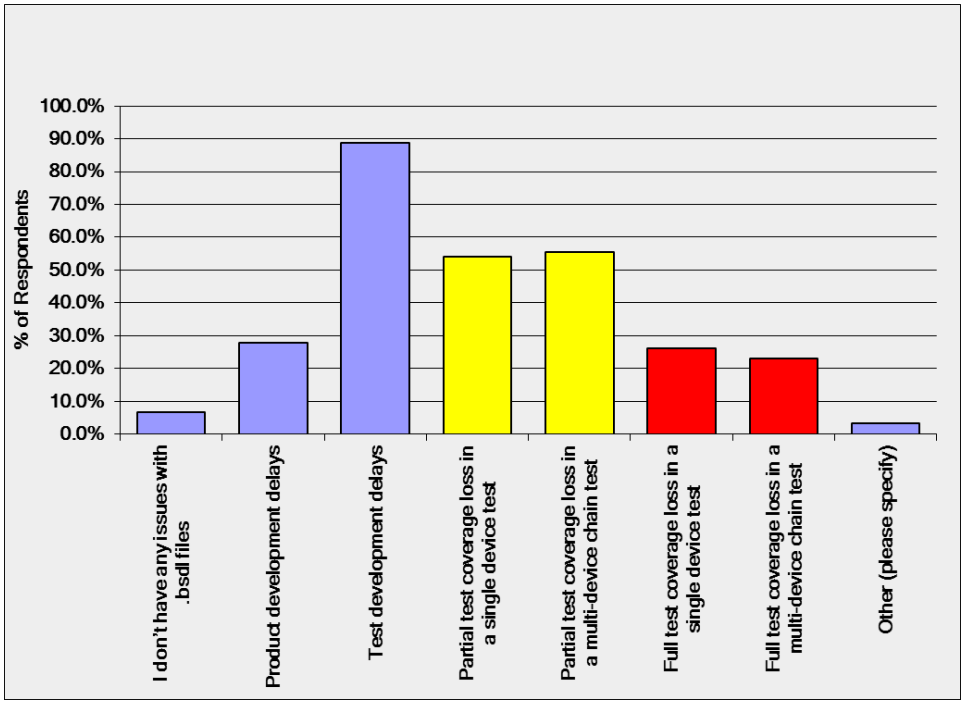

Figure 5 – Impact of Issues With .bsdl Files

The respondents were asked if .bsdl file quality has changed over the last few years. Almost 55% said .bsdl file quality had improved and about 31% said it had stayed the same. Almost 5% said it had gotten worse and about 9% said they were too new to using .bsdls to make a determination. This data is shown in Figure 6.

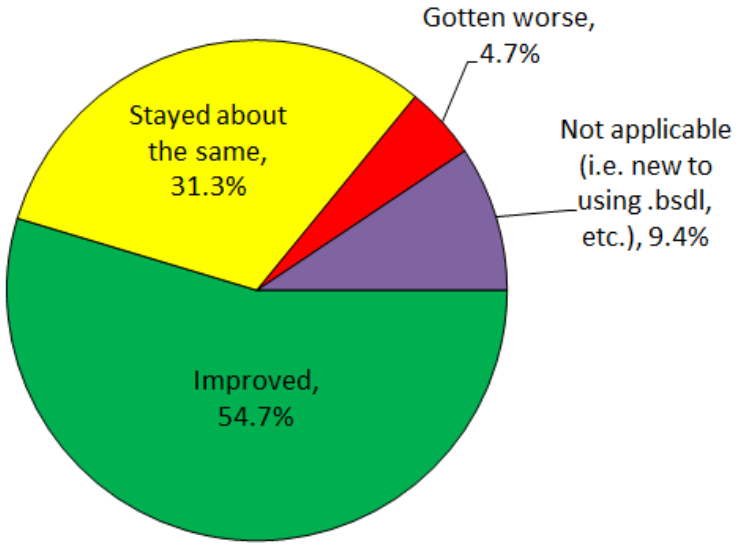

Figure 6 – .bsdl File Quality Change over the Last Few Years

IC Engineering Data Analysis and Review

The primary goals of the survey regarding IC engineers were to find out how they use .bsdl files, what issues they have using them, how .bsdl files are generated, and how they are validated for syntax and accuracy to the physical scan design. From that data and the data Board/System engineers gave us regarding .bsdl issues, our goal was to develop a recommendation for best practices for .bsdl file generation and validation.

There were 13 respondents that classified themselves as Integrated Circuit Engineers. 9 were IC Design Engineers and 4 were IC Manufacturing Engineers. With that few respondents, no trends in the IC industry can be derived from the data and no best practices for .bsdl file creation and validation can be determined. This section will simply present the responses received from the IC engineers.

The IC Development engineers were asked to estimate how many devices they designed with boundary scan cells in the last 12 months. 7 answered 1-5 devices and 1 answered 6-10 devices.

8 IC engineers responded that their organization created .bsdl files, but only 5 IC Development engineers stated that they personally created them. No IC Manufacturing engineers stated that they personally create .bsdl files. Methods used to generate .bsdl files were reported as;

- Using EDA Tools (3 responses)
- Hybrid (Manual + EDA Tools) (3 responses)
- Manual (1 response)
- Don't know (1 response)

When asked what issues were encountered generating .bsdl files, half (4) of the IC engineers reported no issues and half reported they had problems with the .bsdl file generation tool.

The types of devices that the respondents' generated .bsdl files for were reported to be;

- Processors (2 respondents)
- ASICs (2 respondents)
- Programmable devices (CPLDs, FPGAs, etc.) (1 respondent)
- Network Controllers (1 respondent)
- Storage Controllers (1 respondent)

Table 10 shows the IC Engineer responses when asked who in their organization created .bsdl files.

Table 10 – Who in the IC Organization Creates .bsdl Files

	IC Development Responses	**IC Manufacturing Responses**
Design engineer	3	1
DFT engineer	5	0
Applications engineer	0	0
Product sustaining engineer	0	0
Marketing	0	0
3rd party provider (outsourced)	0	1
Don't know	1	1
Other (FPGA Programmer)	1	n/a
Other (Physical Design Engineer)	1	n/a
Other (Customers)	n/a	1

7 of the 8 IC Development engineers responded that they use .bsdl files during the IC design verification or silicon evaluation process. When asked what they specifically used them for, they replied;

- Product Development – debug and verification of prototype designs (5 respondents)
- Structural test – single component test, scan chain test, virtual nails, device identification (4 respondents)
- Functional test – IC wafer level, IC package level, system level (5 respondents)
- Boot verification (1 respondent)
- Device programming (in-system programming) (2 respondents)
- Other (DC Characterization of I/O pins) (1 respondent)
- Other (Operation of verification JTAG based tool) (1 respondent)

Half (4) of the IC Development engineers stated they never have to fix .bsdl files to make them work and the other half reported that they so need to fix them, one reporting that 100% of the .bsdl files seen need to be fixed before they can be used.

Three IC Manufacturing engineers reported using .bsdl files for the IC test and verification process. One did not. Two reported that 1-24% and one reported 50-57% of the .bsdl files they see require fixing before they can use them.

Table 11 shows the IC Engineer responses when asked how they verified the .bsdl for syntax/semantics.

Table 11– How .bsdl Files are Verified for Syntax/Semantics

	IC Development Responses	IC Manufacturing Responses
We do not verify it	0	0
By use (boundary-scan test system, ATE, etc.)	2	3
Assume it is correct from construction by test synthesis tool	1	n/a
Manually	0	0
Simulation tool	2	1
Other (.bsdl verification tool)	1	n/a
Other (.bsdl compliance tool)	1	n/a

Table 12 shows the IC Engineer responses when asked how they verified that the .bsdl matched the physical design of the IC.

Table 12– How .bsdl Files are Verified Against Physical IC Design

	IC Development Responses	IC Manufacturing Responses
We do not verify it	0	0
By use (boundary-scan test system, ATE, etc.)	3	3
Assume it is correct from construction by test synthesis tool	1	1
Manually	0	0
Simulation tool	3	0

Table 13 shows IC Engineer responses when asked who fixes .bsdl files if they are found to be incorrect.

Table 13 – Who in the IC Organization Fixes .bsdl Files

	IC Development Responses	IC Manufacturing Responses
Design engineer	1	1
DFT engineer	5	0
Applications Engineer	0	1
Product Sustaining Engineer	0	0
Marketing	0	0
3rd party provider (outsourced)	0	0
Don't know	1	2
Other (Design or DFT depending on bug)	1	0

When asked if there is a documented process in place to update a released-to-customer .bsdl file with a corrected .bsdl file, three IC development engineers replied yes and five replied no. When asked the same question, one IC Manufacturing engineer replied yes, three said no.

Familiarity With Boundary-scan Standards

.bsdl files are used to define boundary-scan circuitry architecture and control in integrated circuits and are used to automatically generate boundary-scan based tests. "Boundary-scan" is a generic term commonly used to describe several IEEE standards released since 1990, with IEEE 1149.1 and IEEE 1149.6 being most common. Several newer standards have been released in the last few years to enhance or extend the effectiveness of boundary-scan for newer technologies. This work continues with initiatives for additional new standards. A goal of the survey was to gauge Board/System engineer and IC engineer familiarity with existing and future boundary-scan related IEEE specifications and the extent they are using , or plan to use them. Table 14 lists the standards asked about and has a brief description of what each one is.

Table 14 – IEEE Boundary-Scan Related Standards

IEEE Standard	Revision	Test Type	Application
1149.1-2001 (BSDL added 1994)	General Update (1st Release 1990)	Digital BSCAN	Connectivity (DC)
1149.1-2013	Update to 1149.1-2001 New BSDL support for "Clause 9" design specific test data registers. Adds PDL (Procedure Definition Language) for accessing those on-chip registers. Adds new IC level instructions.	Digital BSCAN	Connectivity (DC) Access and control of embedded instrumentation
1149.4-2010	1st Release 1999 Updated 2010	Analog BSCAN	Connectivity (Mixed signal)
1149.6-2003	1st Release 2003	Advanced I/O BSCAN	Connectivity (AC-coupled) Differential, Serial Bus, High-Speed I/O, SerDes.
1149.7-2009 (cJTAG)	1st Release 2009	Compact JTAG. BSCAN with reduced TAP pin count (2 rather than 4 pins) total. Superset of 1149.1.	Connectivity (DC). Extended functionality of device integration, power management, application debug, and device programming. SoC and SiP test.
1149.8.1-2012	1st Release 2012	Adds new operational modes to extend BSCAN testing of connections to passive and active components. Augments 1149.1	Connectivity (DC). Connector & Non-BSCAN Device Test. Powered OPENs Test.
1500-2005	1st Release 2005	Embedded Core BSCAN	Multi-core ASIC digital Test
1532-2002	1st Release 2002	In-System Configuration with 1149.1 BSCAN	In-system access & configuration of Programmable Devices. FPGA, ePLD, cPLD, FlashRAM, PAL, EEPROM
1581-2011	1st Release 2011	Interconnect test mode (no added pins). Augments 1149.1	Connectivity (DC) for non-BSCAN Memory Device Test (DDR,SRAM,FLASH)
1687-2014 (IJTAG)	1st Release 2014	Internal JTAG. Embedded Instrument Gateway access through 1149.1 BSCAN TAP	Embedded Instrumentation access and control
P1838 – Test Access Architecture for 3-D Stacked Integrated Circuits	IEEE PAR approved 2011	Digital BSCAN and access/control of embedded instrumentation in 3-D ICs.	3-D die stack structural and functional tests through a package level TAP.
SJTAG Proposed Initiative (IEEE has not assigned an initiative number yet)	PAR in development	Named System JTAG. Inter-module and Backplane BSCAN	System-based Connectivity (DC)

When asked about familiarity and usage of boundary-scan standards, Board/System engineers replied as shown in Figure7. The standards most used and familiar to the respondents are 1149.1 (including the 2013 update), 1149.6, and 1149.4. IEEE 1532, which allows configuration of programmable parts through the boundary-scan TAP is also well used and familiar. Few respondents use or are familiar with 1149.8.1, 1581, and P1687 (now approved), but they are all relatively new specifications. No respondents are currently using 1149.7 or 1581, but they have plans to use them and are familiar with them.

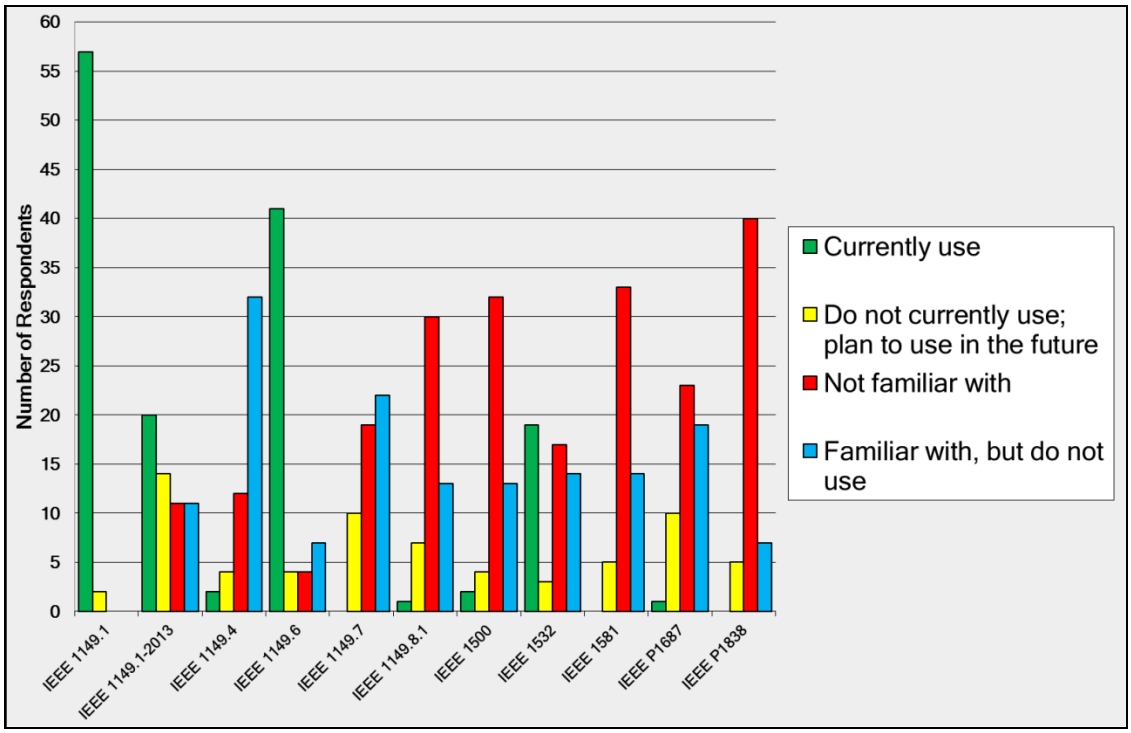

Figure 7 – Board/System Engineer Familiarity with Boundary-Scan Standards

When asked about familiarity and usage of boundary-scan standards, IC engineers replied as shown in Figure 8.

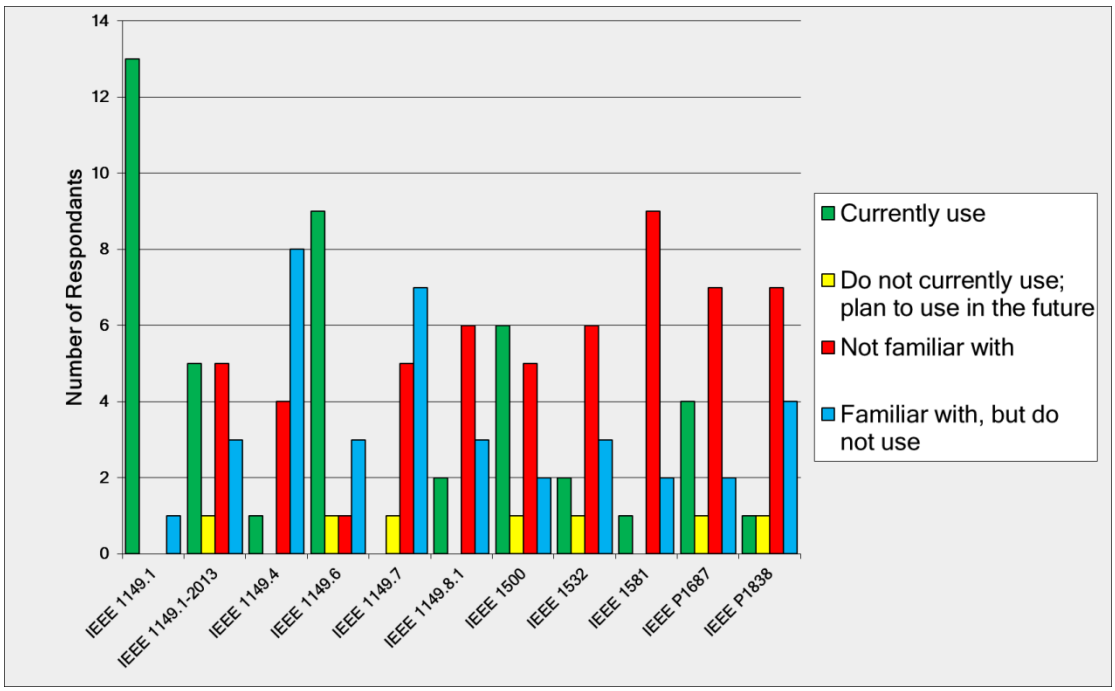

Figure 8 – IC Engineer Familiarity with Boundary-Scan Standards

Note that these results are for only 14 respondents, and that no conclusions about trends in the IC industry can be drawn from this data. The standards with which respondents have the most familiarity with and use the most are the oldest: 1149.1, 1149.6, and 1500. Newer standards 1149.1-2013 and P1687 (now approved) are represented well, showing a fair amount of familiarity and use. The rest of the standards are somewhat device type specific and show low usage and good to fair familiarity.

New standards IEEE 1149.1-2013 and 1687 introduce more than the traditional single .bsdl file to the files required to generate boundary-scan based tests. Instrument Connectivity Language (ICL) and Procedural Description Language (PDL) are additional files that need to be generated for complex devices like 3-D ICs and System on a Chip (SoC) that are 1149.1 and/or 1687 compatible. Because we now can have files sets instead of one file, and some of the known issues with .bsdl files are associated with file revision, both groups of engineers were asked if they would like to see naming conventions and file revision control standards developed for .bsdl file packages.88% of Board/System Engineers, 75% of the responding IC Manufacturing engineers, and 38% of the IC Design engineers would like to see naming conventions and file revision control standards. A few System/Board engineers commented that naming and revision standards would be nice to have, but not essential.

Conclusions

This survey was primarily focused on the following issues;

- .bsdl file implementation issues
- .bsdl file creation practices
- .bsdl file validation practices

In addition, the level of familiarity and use of existing and future boundary-scan standards was to be gauged.

Board/System engineers have a very good familiarity with the boundary-scan standards that are targeted toward board/system test and use them extensively in product development and manufacturing. They are less familiar with new specifications and specifications targeted toward IC development and test.

Over half the Board/System engineers reported that .bsdl file quality has improved over the last few years. Only 4.7% said it had become worse. Even with the perceived improvement in file quality, over 94% of them reported having issues using .bsdl files – 50% having issues with 1-20% of the .bsdl files and 22% having issues with 21-40% of them. Over 65% of the Board/System engineer respondents reported issues with syntax errors. All other issues reported related to the content or compliance of the .bsdl, not syntax. The top three content/compliance related issues were that almost 48% reported that differential pins were not described correctly, 44% reported no compliance pins were listed and 39% reported incorrect cell types. These types of issues are typically not found until trying to debug a test and that is far too late in the test development cycle to discover those issues!

Solutions that the Board/System engineers used to overcome issues with the .bsdl files were varied. Over 80% reported they edit the .bsdl to fix issues, which can be a fast and simple fix for minor syntax issues. The other top solutions were to get an updated .bsdl, get the device supplier to fix the .bsdl, or contact a 3rd party boundary-scan test supplier for help.

The most reported impact of the .bsdl issues was that 89% of Board/System engineering respondents reported test development delays. Test coverage was significantly impacted, also. About 55% reported partial test coverage loss in boundary scan test and about 24% reported full test coverage loss. Test coverage loss can be a significant cost adder to a product.

There is certainly much improvement that can be made in .bsdl file quality that will result in more comprehensive tests being deployed faster.

Obtaining .bsdl files that were for the target IC in a timely manner was also a major concern for the Board/System engineers. The top three difficulties reported were needing NDAs (67%), obtaining pre-release device .bsdl files (63%) and receiving the wrong .bsdl file (52%). The last two difficulties factor into the issues of .bsdl file quality Board/ System engineers reported.

What can the IC industry do to improve this?

1. Every .bsdl file should be checked for syntax before releasing it to internal to external customers.
   There are several free .bsdl syntax checkers available from boundary-scan tool providers and it's recommended that each .bsdl file be processed through two or three to ensure syntax compatibility as some syntax checkers may not check 100% of the syntax.

2. Verify the functionality of a .bsdl file by using it to generate boundary-scan tests. Run those tests against the actual silicon device. Simulation, while useful, can be incomplete or not represent the latest version of silicon correctly.

3. Implement .bsdl file release processes that will ensure customers can get access to the correct revision of .bsdl file for the device they are using, for both pre-release and released devices.

The very small number of respondents from the IC Engineering sector makes it impossible to draw any conclusions from the IC Engineer data. It appears from the small amount of data collected that the IC engineering community experiences many of the same issues using .bsdl files that Board/System engineers do, but in IC development and manufacturing processes instead of board/system test processes. The project team recommends that iNEMI perform another survey targeted toward the IC Engineering sector and do a more thorough job of publicizing the survey in order to get a large enough response that conclusions can be drawn from and best practices for .bsdl file generation and validation can be determined.

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Boundary-Scan Project Phase 3: Investigation into Challenges of Using .BSDL Files

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Presentation Outline

- iNEMI's Boundary-Scan Adoption Project
- Boundary-Scan Phase 3 Project Background
- Boundary-Scan Phase 3 .bsdl Survey Methodology
- Summary

iNEMI's Boundary-Scan Adoption Project

- Organized under the iNEMI Board and Systems Manufacturing Test Technology Integration Group (TIG)
- Goals of the Boundary-Scan Adoption Project:
  - Gauge the adoption level of boundary-scan
  - Promote wider adoption of boundary-scan (IEEE 1149.x) and associated standards (i.e. IEEE 1581, P1687)
  - Encourage semiconductor suppliers to include the technology in their products

BScan Phase 3 Project Background

- The 2012 iNEMI roadmap gap analysis determined that one of the greater risks to High Volume Manufacturing (HVM) board test was the continuous erosion of test point access due to:
  - increasing bus signal speeds
  - higher component densities
  - shrinking PCB and component form factors
- A significant solution to the test point erosion issue is to use boundary-scan based testing to test areas where test point access has been eroded
- In order to generate boundary-scan tests, a required input is a correct, compliant Boundary-scan Description Language .bsdl file

BScan Phase 3 Project Background

- The number one issue in generating boundary-scan tests identified by the 2009 iNEMI Boundary-Scan survey:
  - Problems obtaining correct and compliant boundary-scan description language (.bsdl) files from the semiconductor industry for use in printed circuit board assembly (PCBA) boundary-scan test generation.
- The major conclusions from the survey were:
  - The semiconductor industry needs to make a greater effort to produce correct and compliant BSDLs.
  - A better job needs to be done verifying semiconductor JTAG implementation compliance to .bsdl files.
    - Non-compliance is typically found when a test is generated and it doesn't work!

BScan Phase 3 Project Background

- Consequences of not having correct and compliant .bsdl files:
  - inability to generate comprehensive boundary-scan tests
    - results in lower overall test coverage for PCBAs
    - resulting in higher manufacturing costs and lower overall product quality.
- .bsdl files are no longer the only output files specified by IEEE 1149.1 and other specifications.
  - IEEE 1149.1 2013 added .pdl (Procedure Definition Language)
  - New IEEE 1149.1 2013 .bsdl features further complicate the validation process
  - IEEE P1687 adds .pdl and .icl (Instrument Connectivity Language)

BScan Phase 3 Project Purpose

- Generate an industry survey that focuses on .bsdl file generation, validation, and industry usage
  - Focus on two groups
    - PCBA Board/System Engineering
    - Semiconductor (IC) Engineering
- Analyze and evaluate the survey results
- Determine Best Practices for .bsdl file generation and validation
- Increase industry awareness of the issues and potential solutions

Survey Methodology

- 15-20 minute survey
- Target respondents:
  - PCBA Design and Development Engineers/Managers
  - PCBA Test Engineers/Managers
  - IC Design Engineers/Managers
  - IC Manufacturing Engineers/Managers

Survey Methodology

- Question Categories
  - General demographic information
    - Name, Company info, area of responsibility
  - Board/System Engineering Questions
    - PCBA Design and Test Engineers
  - Semiconductor Engineering Questions
    - IC Design Engineers
    - IC Manufacturing Engineers

Survey Methodology

- PCBA Board/System Engineering Questions
  - PCBA Engineering specific demographics
  - BSDL usage
  - Issues seen with .bsdl files
  - Impact of issues
  - Methods of obtaining .bsdl files
  - Awareness of .bsdl file set evolution

Survey Methodology

- Semiconductor (IC) Engineering Questions
  - Semiconductor Engineering specific demographics
  - Does respondent create/make .bsdl files
    - If so, how are they generated?
    - What issues are there in generating .bsdl files?
  - Awareness of .bsdl file set evolution
  - Is respondent in IC design or IC manufacturing?
    - Some questions vary based on the respondent's job function.

Survey Methodology

- Semiconductor (IC) Engineering Questions
  - BSDL usage
    - Quantity of .bsdl files used per year
    - What are they used for?
  - Issues seen with using .bsdl files
  - Impact of issues
  - Methods of validating .bsdl files
  - Issues seen with validating .bsdl files

Summary

- #1 issue reported in 2009 iNEMI Boundary-scan survey for generating boundary-scan tests was obtaining correct and compliant .bsdl files
- There has been no indication of any significant improvement since 2009 and .bsdl file sets are becoming more complex
- iNEMI is conducting a new survey focused on
  - .bsdl file implementation issues
  - .bsdl file creation practices
  - .bsdl file validation practices
- Outcomes of the .bsdl survey project:
  - Updated analysis of issues using/generating/validating .bsdl files
  - Best Practices Guidelines for .bsdl file generation and validation

Summary

- If you are in the PCBA or Semiconductor engineering fields and you create or use .bsdl files, please go take the iNEMI survey.

- You can find a link to the survey at

  www.inemi.org