New Approaches to Develop a Scalable 3D IC Assembly Method

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ABSTRACT
The challenge for 3D IC assembly is how to manage warpage and thin wafer handling in order to achieve a high assembly yield and to ensure that the final structure can pass the specified reliability requirements. Our test vehicles have micro-bumped die having pitches ranging from 60um down to 30um. The high density of pads and the large die size, make it extremely challenging to ensure that all of the micro-bump interconnects are attached to a thin Si-interposer. In addition, the low standoff between the die and interposer make it difficult to underfill. A likely approach is to first attach the die to the interposer and then the die/interposer sub-assembly to the substrate. In this scenario, the die/interposer sub-assembly is comparable to a monolithic silicon die that can be flip chip attached to the substrate. In this paper, we will discuss various assembly options and the challenges posed by each. In this investigation, we will propose the best method to do 2.5D assembly in an OSAT(Outsourced Assembly and Test) facility.

Key words: 2.5D, 3D IC, TSV, Micro-bumped die, Si-interposer, CTE, warpage, JEDEC reliability specifications, chip stacking.

INTRODUCTION
The next generation of 3D packaging is the use of through silicon vias (TSVs) to produce a three dimensional stacked semiconductor chip structure. The ability to create a three dimensional heterogeneous integrated semiconductor structure offers numerous benefits, such as power reduction, performance improvement and miniaturization. The viability of the semiconductor technology to create these TSVs has been achieved. However, the next stage of packaging a three dimensional semiconductor structure is where the focus needs to be in order to make this a cost effective technology for high volume manufacturing [1-3].

Another major topic of discussion is who will do the 3D IC assembly. In the past, the semiconductor fabricator designed and manufactured the die and then handed it over to the packaging facility for assembly and test. As flip chip technology developed, a new sector developed called the "middle end" which included RDL, wafer bumping and test. This middle region has further evolved to include micro-bumping, wafer thinning and backside reveal, interposer fabrication, wafer level assembly and 3D wafer level test. Figure 1 schematically shows how this middle region evolved with time. Also, this is the largest growth segment. As we develop this technology we realize that the packaging solution for the foundry is likely to be different from that of the OSAT. In this paper we will discuss four different assembly flows and how they fit with either a foundry centric process flow or an OSAT centric process flow.

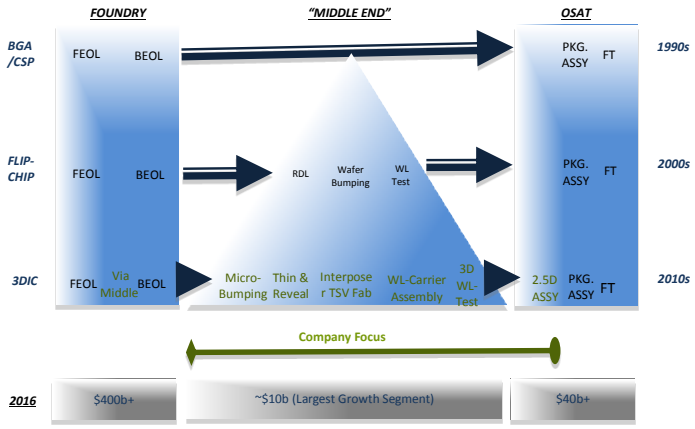

Figure 1. A schematic illustration of the location of the "middle end" region located between the foundry and the OSAT. Note how the middle region has grown and is the largest growth segment.

In this paper, we will discuss our experience with different assembly flows for a standard type of 2.5D test vehicle, as schematically illustrated in Figure 2.

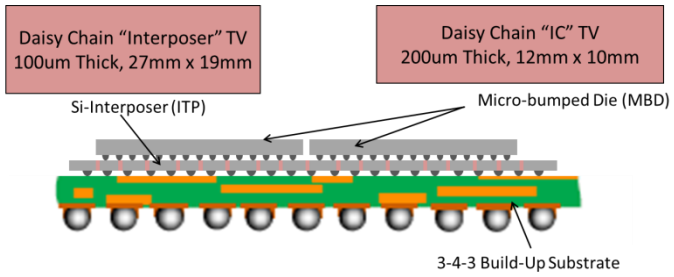

Figure 2. A schematic illustration of a typical 2.5D assembly having two micro-bumped die attached to a Si-interposer, which is then attached to a buildup substrate.

In Figure 2, two micro-bumped die (MBD) are attached to a Si-interposer (ITP), which is then attached to a standard buildup substrate.

In developing a package solution, one must engineer this package to be able to pass the JEDEC standard module and board level reliability tests, which are temperature cycling, high temperature storage, temperature and humidity testing, unbiased high accelerated stress testing (HAST), and pressure cooker testing. Based on our experience in developing reliable packages, we know that understanding stress and its impact through the assembly process can have a dramatic effect on the final warpage of the assembled package. Much research has been done to investigate the effect of warpage on reliability of organic flip chip packages and substrates, and this knowledge can be applied to current 3D IC packaging designs [4-7]. This warpage will affect the final reliability of the package, which is why it is paramount to properly engineer the package & assembly process in order to minimize the ITP and substrate warpage.

Table 1. Test vehicle description.

Dimensions		TV3
Mold	Cap (mm)	1.1
	Gap (mm)	0.680
Die	Overall dimensions (mm)	10 x 12 x 0.2
	uBump dimensions (um)	H: 20 (Cu)+15(SnAg) = 35, D: 35
	uBump pitch (um)	60 / 120
	# of bumps	7744
	Bump layout	Full array - staggered
Interposer	Overall dimensions (mm)	27.05 x 19.25 x 0.10
	TSV dimensions (um)	10 x 100
	FC Bump (mm)	0.095 (including UBM) x 0.120
	FC pitch (mm)	0.18
	uBump Die to Die gap on ITP (mm)	2.0
Substrate	Overall dimensions (mm)	40 x 40 x 1.47
	Build up	3-4-3
	Core thickness (mm)	0.8 + 0.2PP = 1.0
	BGA ball (mm)	0.56 x 0.45
	BGA pitch (mm)	1.0
Total thickness	Without BGA (mm)	2.47
	With BGA (mm)	2.92

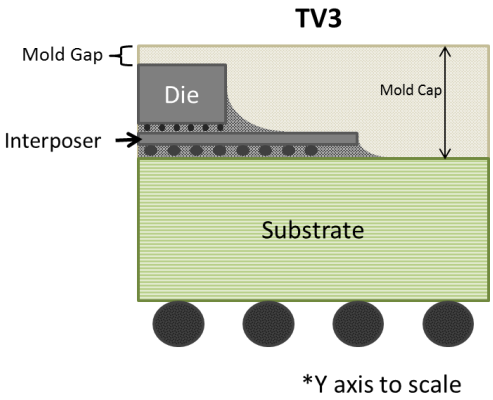

Figure 3. A schematic illustration of the TV3 test vehicle design.

TEST VEHICLE DESIGN

Figure 3 is a schematic of the overmolded TV3 test vehicle design used in this analysis, which shows the details of the die thickness relative to the ITP and substrate. The detailed description of this test vehicle is shown in Table 1. In this test vehicle, the ITP with dimensions of 19.25mm x 27.05mm and a thickness of 0.100mm is attached to a 3-4-3 buildup substrate having a total thickness of 1.47mm. On the surface of the ITP are two MBD with dimensions of 10mm x 12mm and a thickness denoted by X, and a mold gap thickness denoted by Y. Both MBD are spaced 2mm apart. A solder capped pillar is used to attach the MBD to the ITP with a 35 um standoff and a 60um perimeter pitch with a 120um pitch inner array. The ITP is attached to the 3-4-3 buildup substrate. Solder balls are attached to the substrate and a standard flip chip- pick and place followed by reflow are used during the ITP attach. Both the MBD and the ITP are underfilled using commercially available capillary underfill materials. Following underfill cure, the entire strip is molded with a transfer mold process using qualified HVM mold materials.

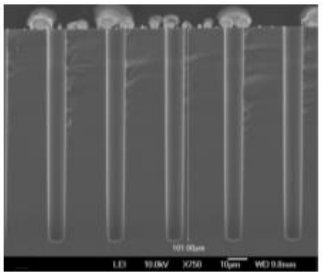

Figure 4. Cross-section of a via hole after DRIE etch .

FABRICATION OF Si-INTERPOSER (ITP) AND MICRO-BUMPED DIE (MBD)

The ITP is made from a 300mm wafer using a via first process. The TSVs have a 10um diameter and are 100um deep. A standard DRIE dry etch process was used to form via holes in the wafer. Figure 4 shows an SEM image of the drilled via holes. A standard PECVD TEOS process was used to deposit the SiO2 isolation layer. A Ti-Cu barrier/seed layer was deposited and the vias were filled using a Cu-electroplating process. Figure 5 shows an X-ray image of the Cu-filled TSV after plating. Note that there is complete hole fill and no voids. A standard oxide BEOL process was used to create the top surface metallization layer. In this design only a single metal layer was used. The unrevealed thick wafer is then attached to a temporary carrier wafer in order to thin and reveal the TSVs on the backside of the wafer.

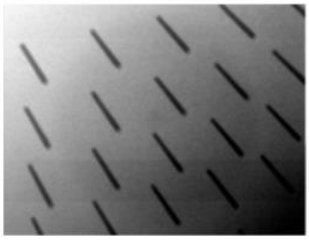

Figure 5. Photograph of an X-ray image of a Cu-electroplated filled TSV in the Si-interposer.

Then an RDL and backside solder bumping was done. Next, the carrier wafer is removed and the wafer is diced to produce singulated ITP die which may then be used for assembly.

The MBD is made from a 300mm wafer. First a standard metallization is produced on the wafer in order to create the proper daisy chained structure used for reliability testing. A surface oxide is then deposited over the entire wafer and removed at sites where Cu pillars will be plated. Then a 35um diameter Cu pillar is plated on each respective site, followed by plating a Pb-free solder and then reflowed. Figure 6 shows a SEM image of the solder capped Cu-pillars on the MBD.

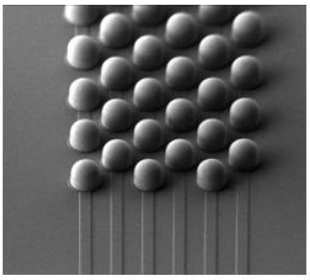

Figure 6. An SEM image of the reflowed solder caps on the Cu-pillars of the micro-bumped die. Bump height total thickness variation (TTV) was 5um.

ASSEMBLY PROCESS FLOW

Four different types of assembly flows are being evaluated. Each flow can be divided into 3 steps, which are shown in Table 2, and the details of each process are outlined as follows:

Table 2. Four different types of 3D IC assembly flows evaluated

Assembly Process Flow		First Step	Second Step	Third Step
Process Flow 1 – Substrate First Approach	PF1(a)	ITP → Substrate	uBD → ITP	
	PF1(b)	ITP → Substrate	uBD → ITP	Molding
Process Flow 2 – Molded Substrate Approach	PF2	uBD → ITP	Molding	Molded ITP →Substrate
Process Flow 3 – Substrate Last Approach	PF3(a)	uBD → ITP	ITP → Substrate	
	PF3(b)	uBD → ITP	ITP → Substrate	Molding
Process Flow 4 – Permanent Carrier Approach	PF4(a)	uBD → ITP Wafer→ Handle Wafer Attach	TSV Reveal & Backside RDL/Bumping & Singulate→Substrate	Molding
	PF4(b)	uBD → ITP Wafer→Modified Handle Wafer Attach	TSV Reveal & Backside RDL/Bumping & Singulate→Substrate	Molding

- Process Flow 1 (PF1) – Substrate First Approach: In process flow PF1(a), the ITP if first attached to the substrate, and then the MBD are attached to the topside of the singulated ITP. In PF1(b), the assembly is then overmolded to further improve the package warpage, which will improve the overall reliability of the final 2.5 structure.
- Process Flow 2 (PF2) – Molded Substrate Approach : The second process flow is a variation of process flow PF1, where a 2x4 ITP block is held on a vacuum chuck and the MBD are first attached to the ITP block, then the topside is overmolded, and the backside is solder bumped. This molded assembly is then attached to the substrate using a conventional mass reflow solder attach method.
- Process Flow 3 (PF3) – Substrate Last Approach: In PF3(a), a singulated ITP, either with or without backside solder bumps is held in place with a vacuum fixture. The two MBD are then attached to the ITP, and the assembled ITP is attached to the substrate. For PF3(b) assembly flow, the MBD/ITP/substrate assembly is molded to reduce overall warpage.
- Process Flow 4 (PF4) – Permanent Carrier Approach: For the PF4(a) flow, the MBD are attached to a thick ITP wafer. A handle wafer is attached to the top die, and then the wafer is thinned and the TSVs revealed. The wafer is singulated and then the MBD/ITP assembly is attached to the substrate. In process flow PF4(b) a modified handle wafer design is used to reduce final package warpage. The details of this process flow will be the subject of future papers.

More details on these process flows are outlined in a recent publication [8]. The focus of this paper will be the process assembly development related to Process Flow 3 – Substrate Last Approach Process (PF3). In this work the effect of process conditions, materials selection and package dimensions will be discussed in order to design a package to meet reliability requirements.

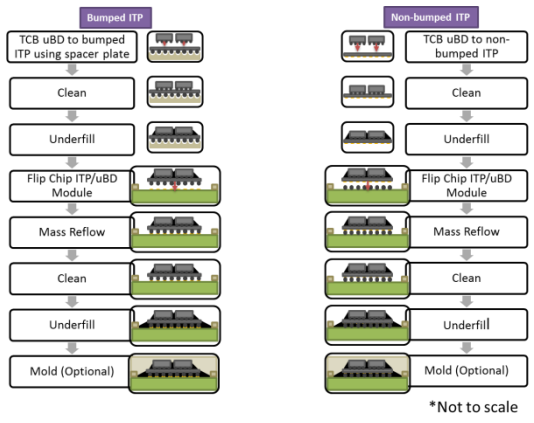

Figure 7. Process flow PF3, Substrate Last Approach, using a solder bumped interposer (left side) and a non-solder bumped interposer (right side).

The details of this process flow are shown in Figure 7. In this process there are two different assembly flows. In the first one, PF3(a) the solder bumped ITP is held in place by a fixture. Here a precision fixture holds the solder bumped ITP in place using vacuum during the MBD attach. In the second flow, PF3(b), a non-bumped ITP is firmly held in place using vacuum. The two MBD are then attached to the ITP. In this flow the solder balls are placed on the substrate, and then the substrate is attached to the ITP using mass reflow.

In this paper we will focus on the MBD to ITP attach step of the PF3 assembly method that uses a non-bumped interposer (right-hand side of the process flow in Figure 7).

ASSEMBLY PROCESS DEVELOPMENT

In this work, design of experiments (DOEs) were used to achieve a high yielding MBD attach to the Si-ITP. When the initial set of hardware was built it was determined that the primary failure mode was soldering bridging of the MBD to the IPT. Figure 8 shows an X-ray image of these bridges in the 60um pitch periphery array of the TV3 MBD after assembly to the ITP. To achieve the final acceptable process window, three different DOEs were performed. In the following write up, we will discuss each of these experimental DOEs in more details.

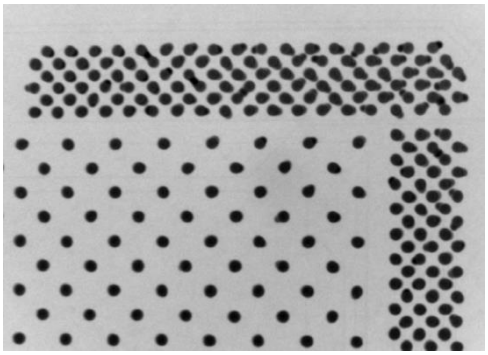

Figure 8: X-ray image showing solder bridging of the TV3 MBD after assembly to the ITP in the periphery array.

Table 3: DOE1 – Process to eliminate MBD shorts.

DOE Leg	Stage Temp (C)	Time at 305C (sec)	Cooldown Temp(C)	Yield
1	100	5	80	1 Open
2	130	5	80	1 Open each on 2 Die
3a	130	1	80	2 Opens on 1 Die
3b	130	1	130	

DOE1: PROCESS TO ELIMINATE SHORTS

In this first DOE the three variables to evaluate were stage temperatures, time at peak temperature of the thermode, and cool down temperature. The peak temperature of the thermode head was 305C. From this experiments, the nominal MBD interconnect height was 43.2 um. The target height that we wanted to achieve was 35um, which was based on finite element analysis. Figure 9 shows a SEM of the resulting solder interconnect from this build. The results of this DOE have shifted the failure mode to solder opens. For all four legs of the DOE there were solder opens as shown in Table 3.

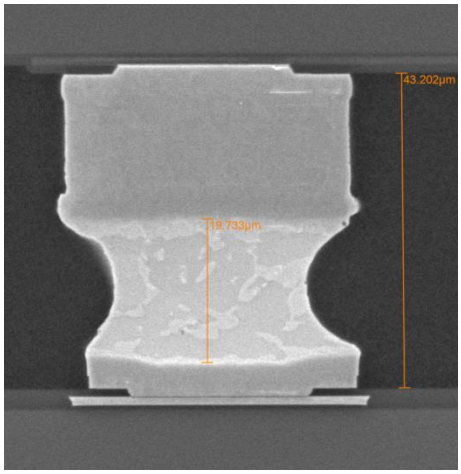

Figure 9: The nominal MBD solder interconnect height of 43.2um from DOE1.

Table 4: DOE2 – Process to eliminate MBD opens

Stage Temp (C)	Contact Temp(C)	Peak Temp	Release Temp(C)	Contact Force(N)	Melting Setting (um)
130	130	305C for 5sec	130	2.8	6
					8
					10

DOE2: PROCESS TO ELIMINATE SOLDER OPENS

The process conditions to eliminate solder opens are shown in Table 4. During bonding one must account for the collapse of the solder capped Cu-pillar due to the melting of the solder. In order to prevent total collapse, there is a z-displacement setting on the machine to control the amount of z-displacement of the head. This amount of controlled z-displacement after solder reflow is called the "Melt Setting." Here the major variable was to control the melt setting height ranging from 6-10um. From this work the electrical testing confirmed no solder opens and no shorts when using a melt setting height of 10um. Electrical testing and X-ray was also used to verify no short failures. The thermal bonder conditions used for this build are shown in Figure 10, which shows the locations for the 6um, 8um and 10um melt setting conditions.

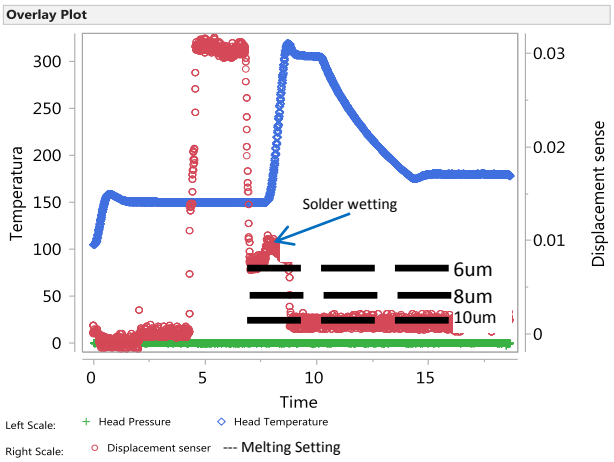

Figure 10: DOE2 thermal bonder conditions

From this build cross-sectioning of the MBD solder interconnects was done and it was found that there was a slight bow of the die. It is believed that this bow is due to a temperature gradient across the MBD that causes an uneven gap height. Figure 11 shows the edge MBD solder joints having a height of 40um and the center die solder joints having a height of 42um.

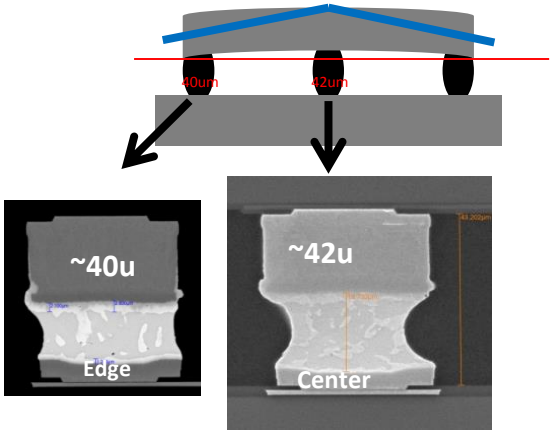

Figure 11: Comparison of edge and center MBD interconnect height using DOE2 bonding conditions.

Also, it was found that the intermetallic compound (IMC) thicknesses varied on the MBD interconnect. Figure 12 shows a 2.1-2.8um IMC thickness range at the Cu pillar interface whereas only a 1.2um IMC thickness at the ITP pad interface. This can be explained by the fact that the solder capped Cu-pillar saw two reflows whereas the ITP pad saw just one solder reflow. The amount of IMC on the die side prior to assembly is approximately 1um.

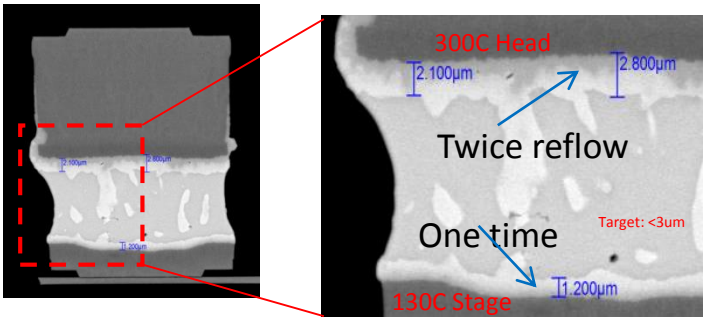

Figure 12: IMC thickness variation on the top and bottom of the MBD interconnection.

DOE3: PROCESS WINDOW DEFINITION

As mentioned previously the goal is to develop a process having a MBD interconnect nominal height of around 35um and having no solder bridges or opens. In the final DOE3, the stage temperature, hold time and melting setting were evaluated to arrive at the final process window. Figure 13 shows the details of DOE3. In this build, melt settings of 6um and 8um both yielded solder opens.

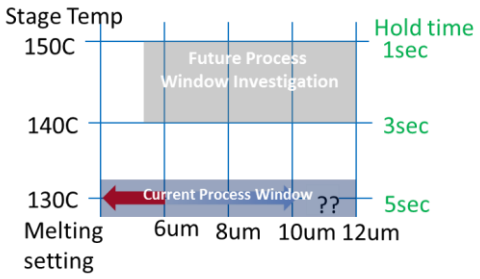

Figure 13: DOE3 – Process window definition

A melt setting of 12um resulted in solder bridging. Only a melt setting of 10um yielded a nominal joint height of about 32um without any opens or bridges. Figure 14 shows a comparison of the nominal MBD interconnect heights when a melt setting of 6um and 10um was used. For the 6um melt setting a nominal joint height of 42.6um was achieved, and for a 10um melt setting a nominal joint height of 31.8um was achieved.

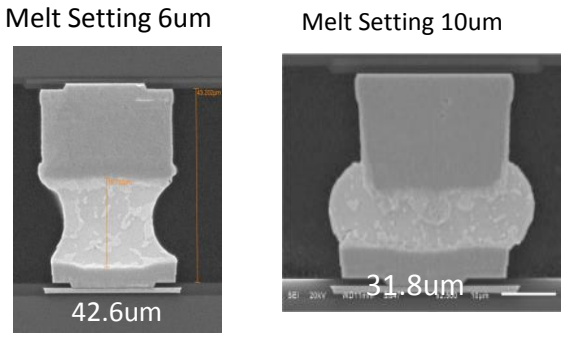

Figure 14: Comparison of MBD nominal joint heights, melt settings of 6um and 10um using DOE3.

In order to validate the best process window conditions a set of 36 interposers were assembled using the process conditions shown in Table 5. From this build 33/36 parts passed electrical test with no solder defects.

Table 5: Build conditions to validate DOE3 process window.

Bonding Conditions:

- Gap Control = -10um
- Flux Type/Dip = ABC / 5um
- Force = 2.8N
- Stage Temp = 130C
- Contact Temp = 130C
- Peak Temp/Time = 305C / 5sec
- Release Temp = 130C

91.7% MBD Yield: 33/36 MBD Passed e-test "Good" ITP

However, after careful failure analysis of the 3 parts showing electrical test open failures, it was determined that all three were due to opens in the trace on the stitched MBD hardware. Figure 15 shows an SEM image of the open in the trace on the MBD side. When this open defect was compared with a good interconnect, it was found that the good interconnect had no metallization defects. Thus, explaining why these 3 assemblies failed. Current builds are underway to revalidate this process.

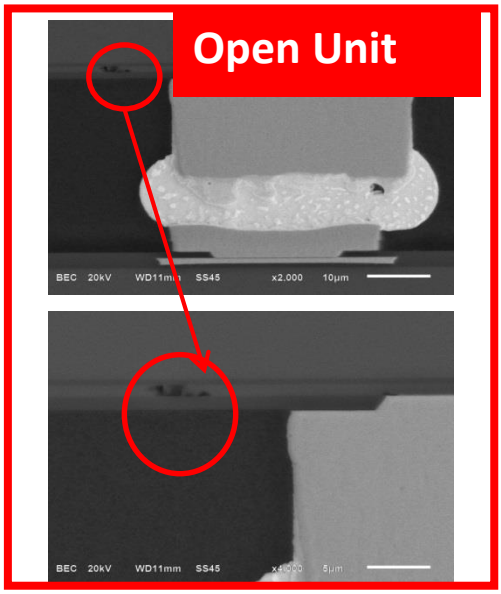

Figure 15: SEM image showing open defect in the trace.

DISCUSSION

The main focus of this assembly process development is to establish an assembly process window that is compatible with OSAT assembly facility. In this approach a Si-to-Si bonding of the solder capped Cu-pillars on the MBD is done to a non-bumped Si-ITP using thermal compression bonding. The challenge is to create the right process conditions that can produce a high yield with no solder bridges or opens.

As can be seen from the experimental flow, first we experienced solder bridging. Once the solder bridging was eliminated using the conditions of DOE1, the next goal was to eliminate the solder opens, which was the objective of DOE2. From DOE2 solder opens where eliminated, however, the nominal solder interconnect height was about 43um, which was higher than the nominal goal of around 35um.

In DOE2, the melt setting was varied and it was determined that a value of 10um produced no solder opens. This is based on bonding 70 die in which we achieved a 90% assembly yield, in which the remaining 10% failures were due to cracked traces on the micro bumped die (as shown in Figure 15). Also, from this work, we were able to plot the gap height versus melt setting and determine the best condition to achieve a nominal interconnect height of 35um. Figure 16 shows a linear regression plot of the gap height versus melting setting from this particular build. These are single measurement points made at the same location, which is the center of the micro bumped die.

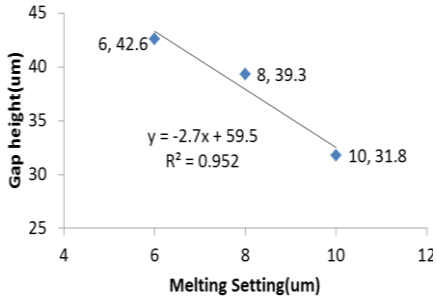

Figure 16: MBD gap height versus melt setting linear regression from DOE2 build.

The goal of DOE3, was to determine the best process window. Here the goal was to achieve a nominal interconnect height of about 35um without defects. As shown from Table 5 there were 3/36 assemblies with opens which were due to defects in the MBD metallization. Based on this work we are very confident in achieving a process window that can produce a high yield MBD to Si-ITP assembly yield.

CONCLUSIONS

1. The semiconductor fabs can produce robust and reliable devices with TSVs.
2. A PF3 type of process, is compatible with an OSAT facility, and can produce 3D IC packages that can meet the challenges of JEDEC reliability specifications.
3. This work has shown that a high yielding MBD to Si-ITP process is achievable.
4. The manufacturing infrastructure exists to assembly in high volume these types of packages using existing OSAT manufacturing infrastructure.

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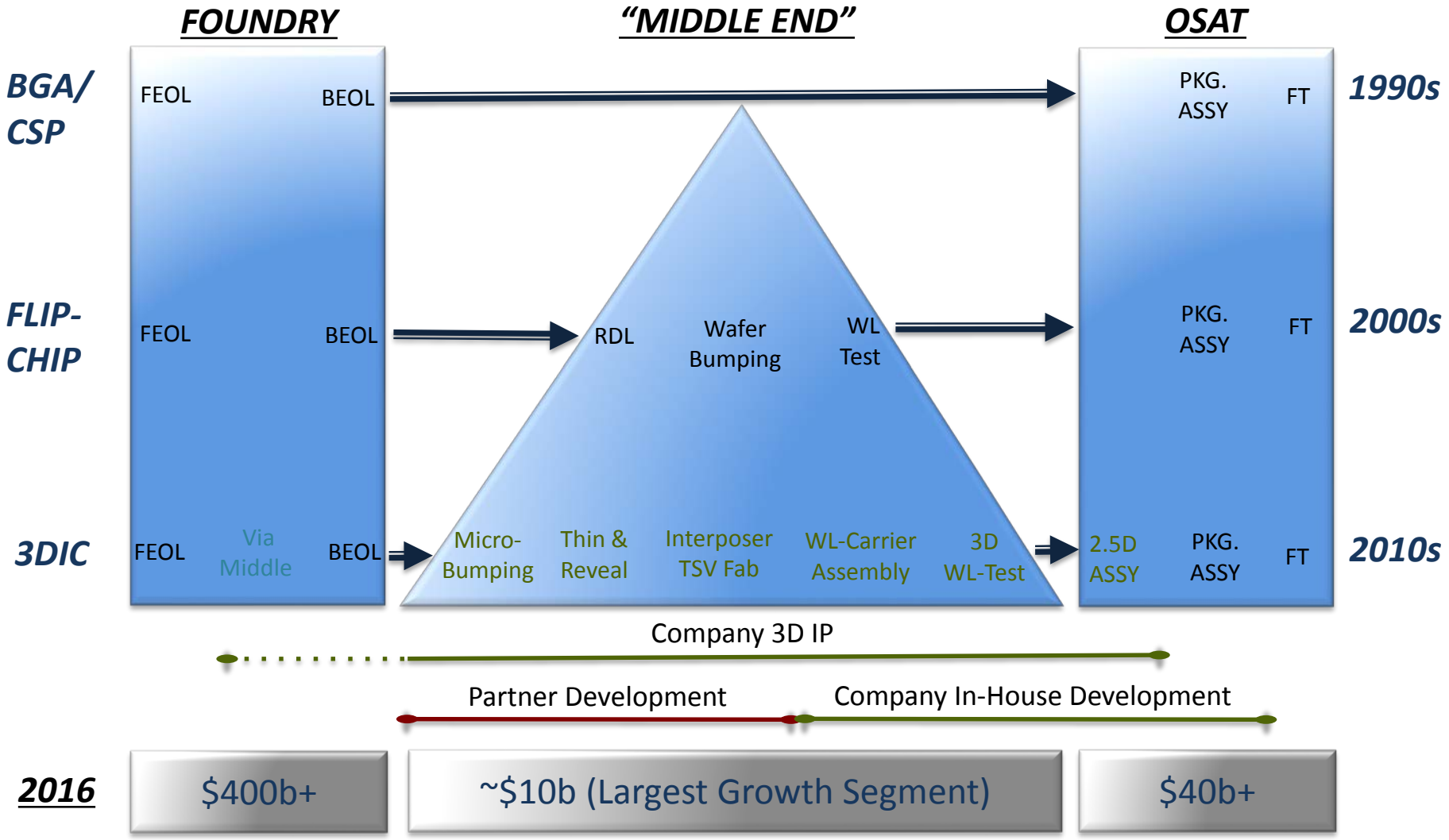
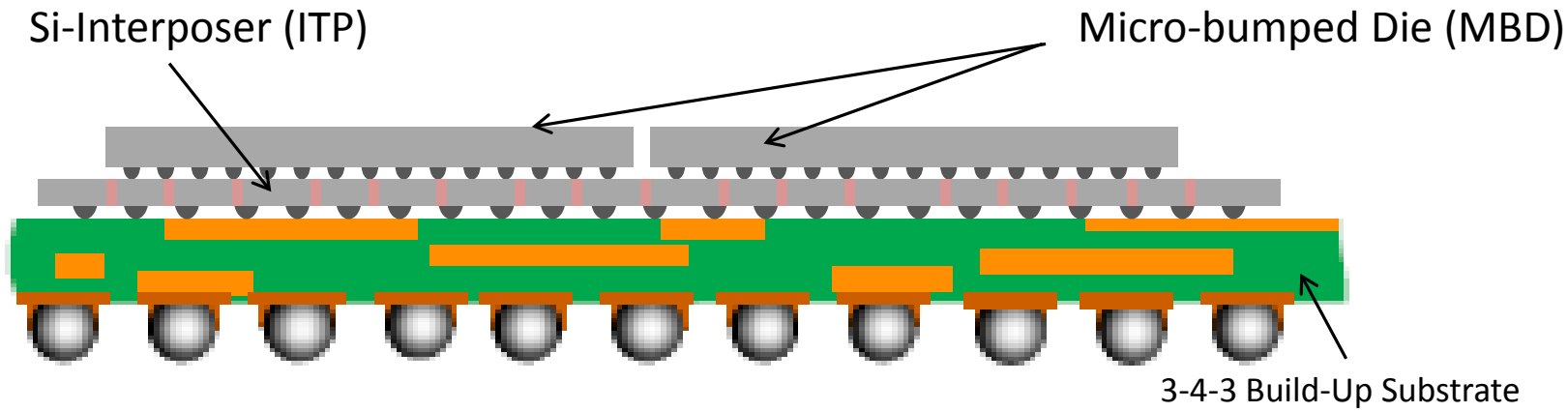
Outline

- Who will do the 3D IC assembly?
- Test vehicle description
- Si-Interposer processing capability
- Assembly flows
- Design of Experiments
- Summary

3DIC Strategy InfoGraphic

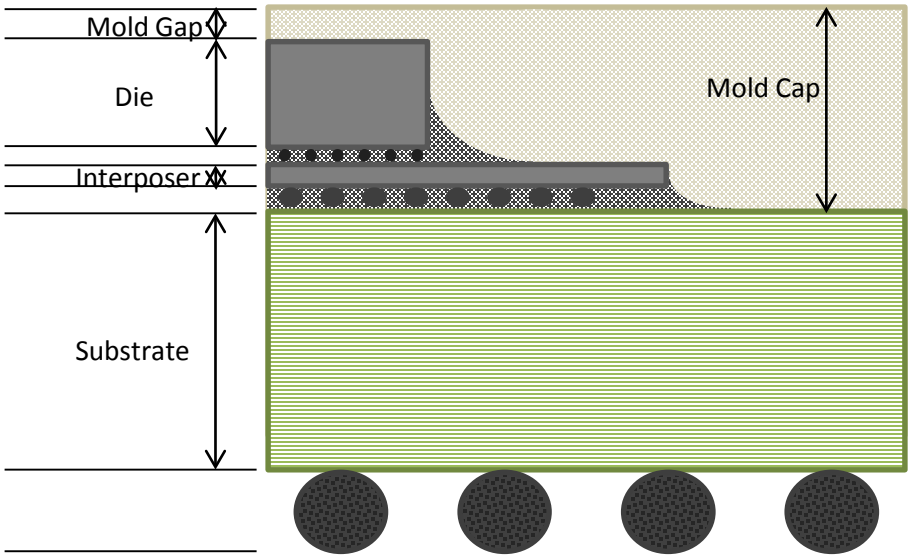


Typical 2.5D Assembly



Schematic of TV3 Design

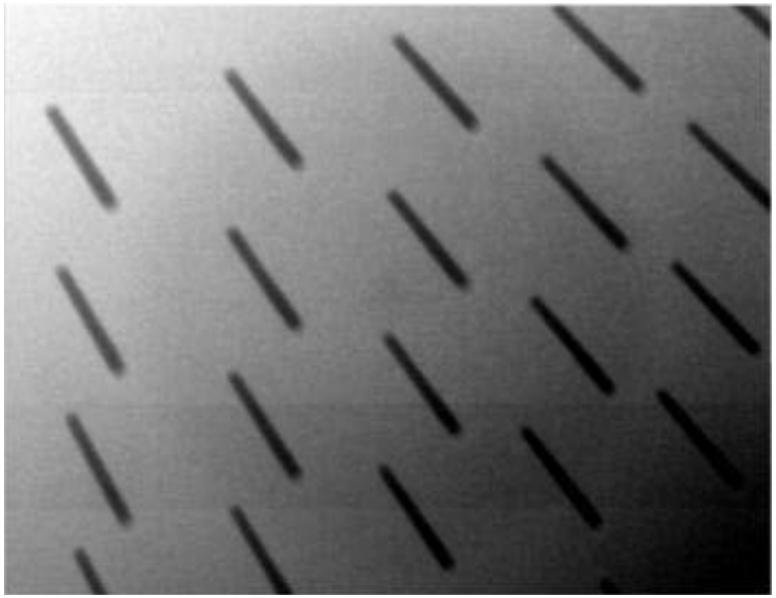
TV3



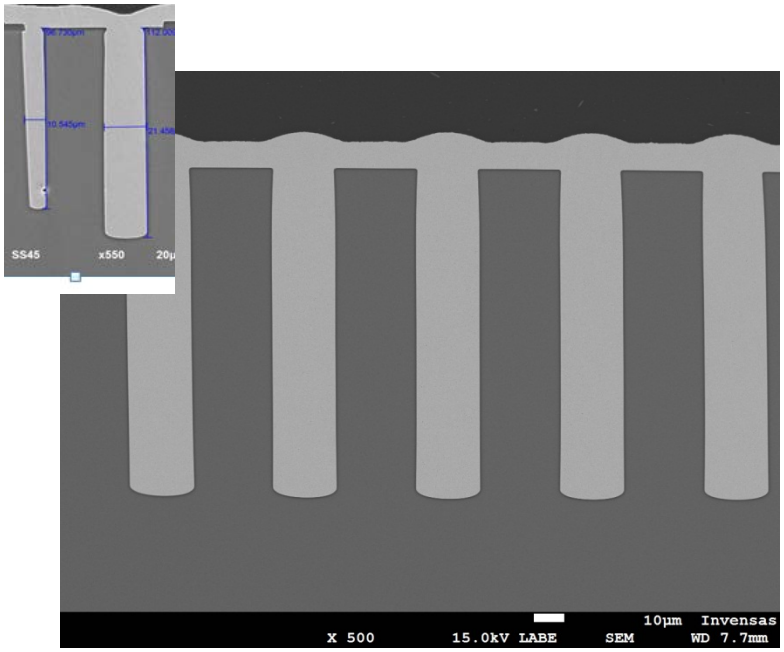
Dimensions		TV3
Mold	Cap (mm)	1.1
	Gap (mm)	0.680
Die	Overall dimensions (mm)	10 x 12 x 0.2
	uBump dimensions (um)	H: 20 (Cu)+15(SnAg) = 35, D: 35
	uBump pitch (um)	60 / 120
	# of bumps	7744
	Bump layout	Full array - staggered
Interposer	Overall dimensions (mm)	27.05 x 19.25 x 0.10
	TSV dimensions (um)	10 x 100
	FC Bump (mm)	0.095 (including UBM) x 0.120
	FC pitch (mm)	0.18
	uBump Die to Die gap on ITP (mm)	2.0
Substrate	Overall dimensions (mm)	40 x 40 x 1.47
	Build up	3-4-3
	Core thickness (mm)	0.8 + 0.2PP = 1.0
	BGA ball (mm)	0.56 x 0.45
	BGA pitch (mm)	1.0
Total thickness	Without BGA (mm)	2.47
	With BGA (mm)	2.92

*Y axis to scale

Filled TSV in Si-Interposer



X-ray image showing complete fill of a 20um x 100um TSV



Production bottom up fill chemistry

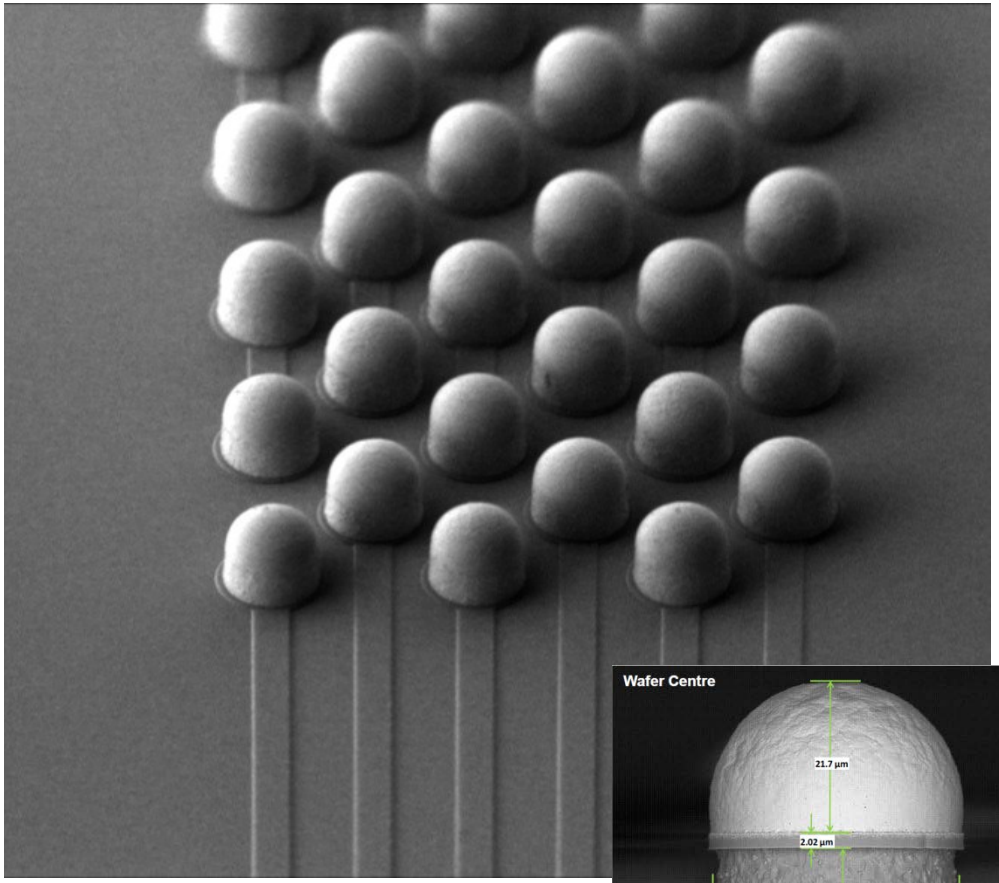
< 3 hour plating time (20x100 um TSV)

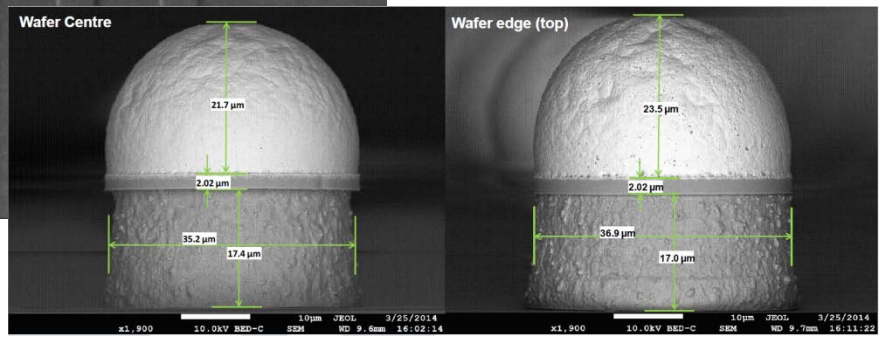
Void free, high aspect ratio fill

Low overburden

2 additive (vs 3) plating process developed

SEM image of Micro-Bumped Die

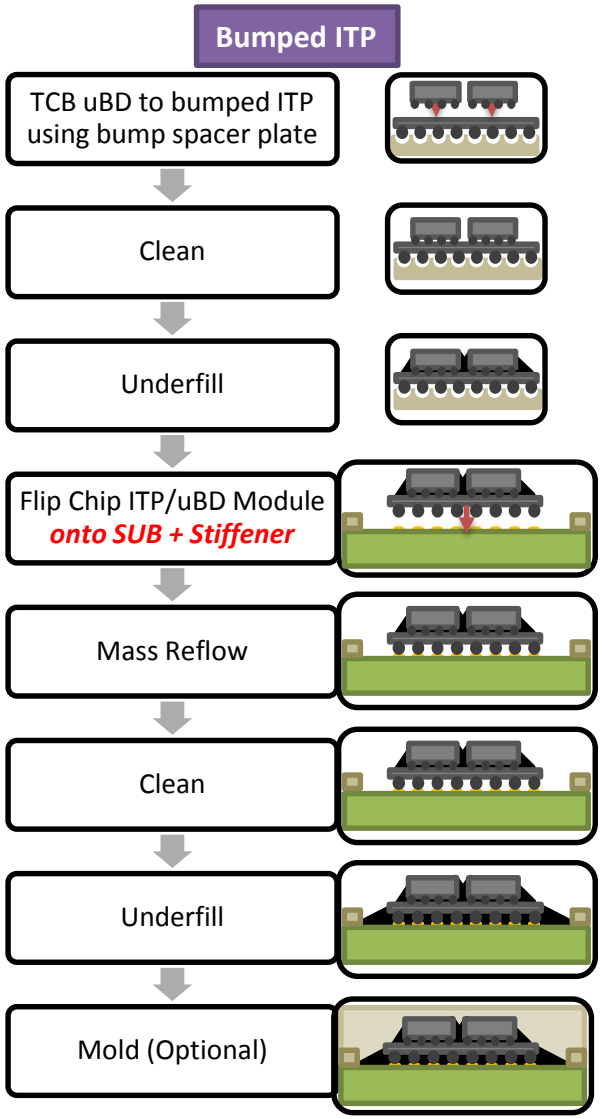


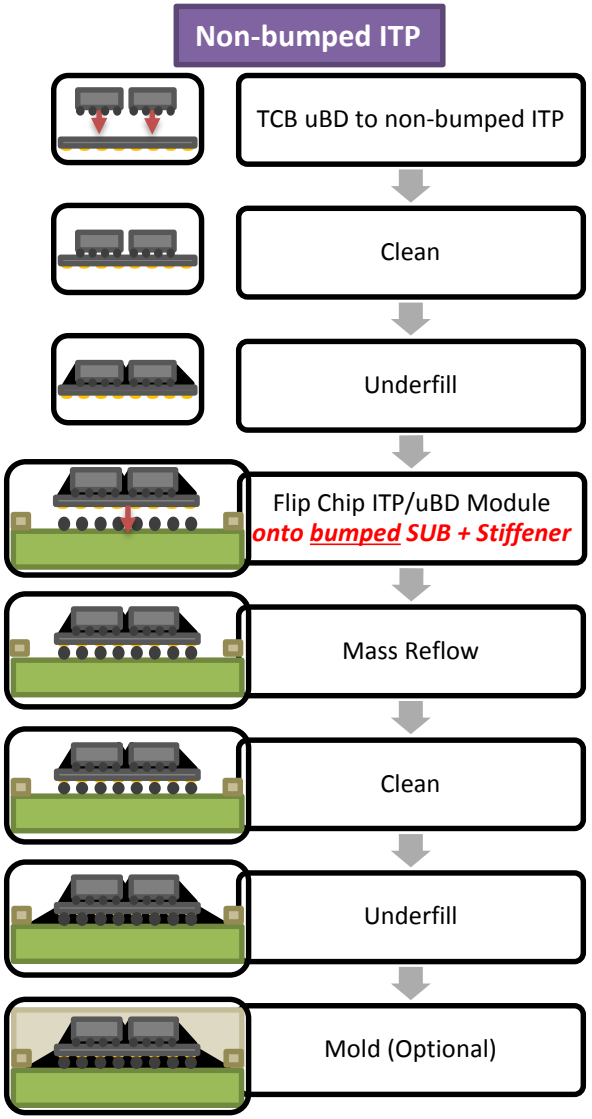


3D IC assembly flows evaluated at the company

Assembly Process Flow		First Step	Second Step	Third Step
Process Flow 1 – Substrate First Approach	PF1(a)	ITP → Substrate	uBD → ITP	
	PF1(b)	ITP → Substrate	uBD → ITP	Molding
Process Flow 2 – Molded Substrate Approach	PF2	uBD → ITP	Molding	Molded ITP →Substrate
Process Flow 3 – Substrate Last Approach	PF3(a)	uBD → ITP	ITP → Substrate	
	PF3(b)	uBD → ITP	ITP → Substrate	Molding
Process Flow 4 – Permanent Carrier Approach	PF4(a)	uBD → ITP Wafer→ Handle Wafer Attach	TSV Reveal & Backside RDL/Bumping & Singulate→Substrate	Molding
	PF4(b)	uBD → ITP Wafer→Modified Handle Wafer Attach	TSV Reveal & Backside RDL/Bumping & Singulate→Substrate	Molding

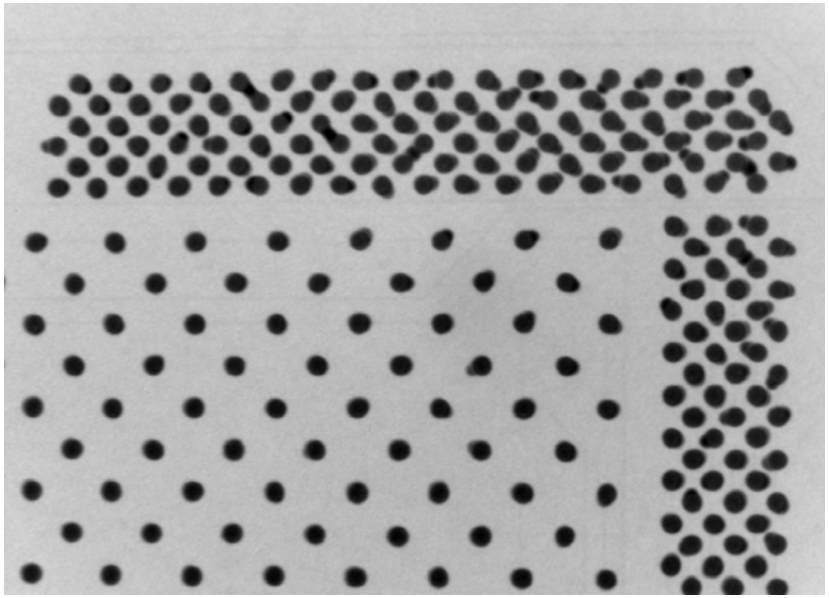
Process Flow 3 – Substrate Last Process Flow





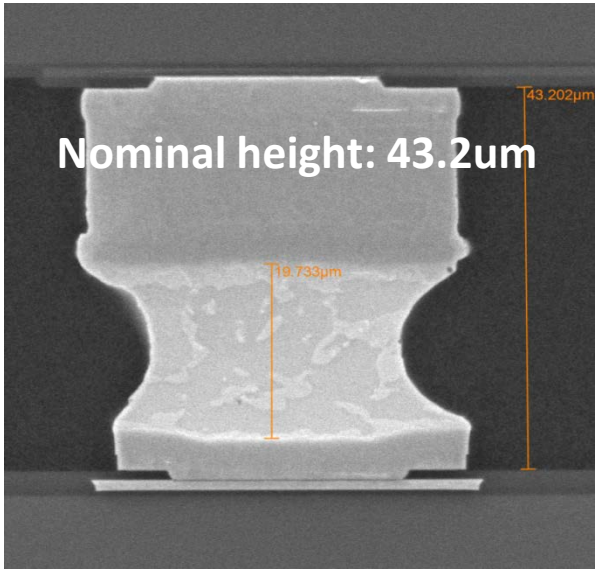
*Not to scale

X-ray image showing solder bridging of MBD on first set of assembly hardware



DOE 1 - Process to eliminate MBD shorts

DOE Leg	Stage Temp (C)	Time at 305C (sec)	Cool down Temp(C)	Yield
1	100	5	80	1 Open
2	130	5	80	1 Open each on 2 Die
3a	130	1	80	2 Opens on 1 Die
3b	130	1	130	



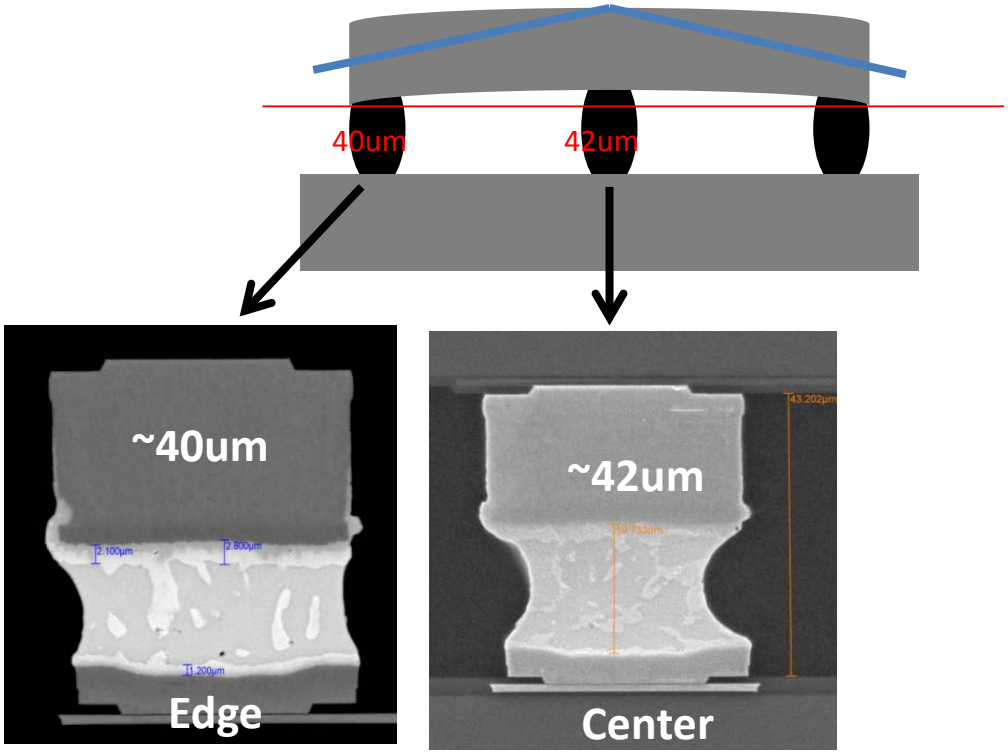
Nominal MBD Interconnect after DOE 1

DOE 2 - Process to eliminate open failures

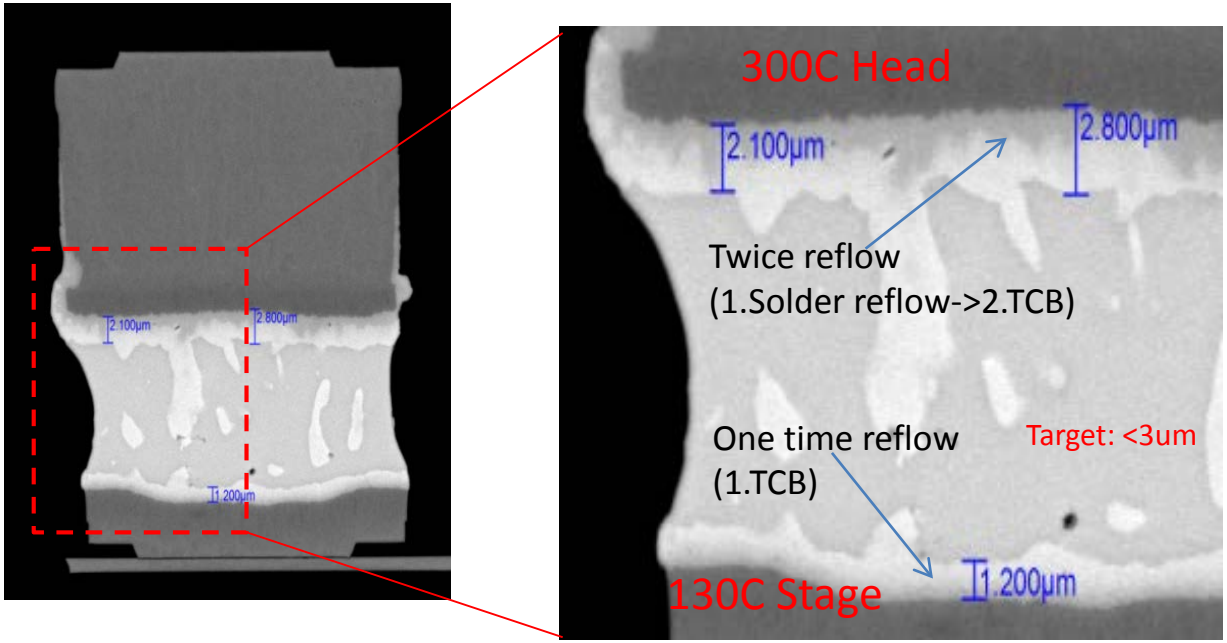
Stage Temp (C)	Contact Temp(C)	Peak Temp	Release Temp(C)	Contact Force(N)	Melting Setting (um)
130	130	305C for 5sec	130	2.8	6
					8
					10

DOE 2 thermal bonder conditions

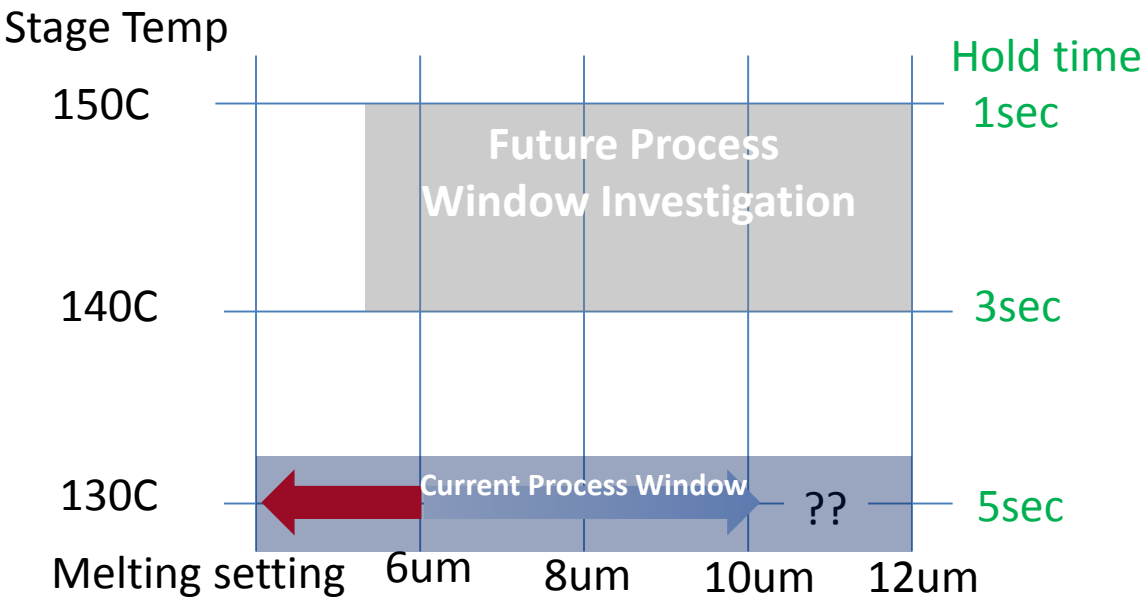
Temperature gradient causes uneven gap height



IMC thickness variation on top and bottom

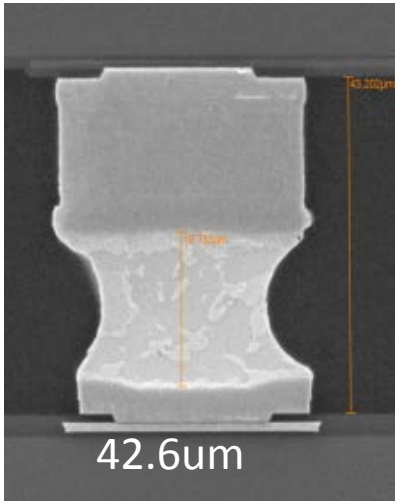


DOE 3 – Process window definition

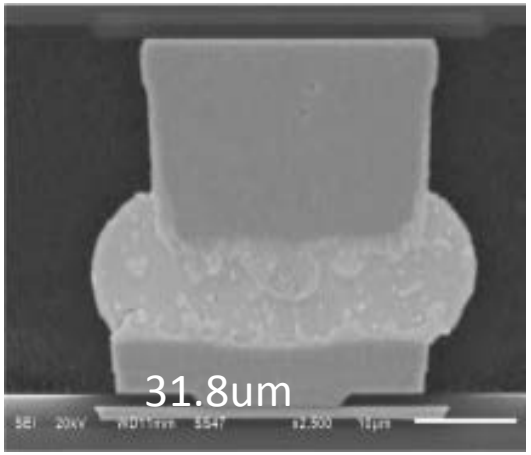


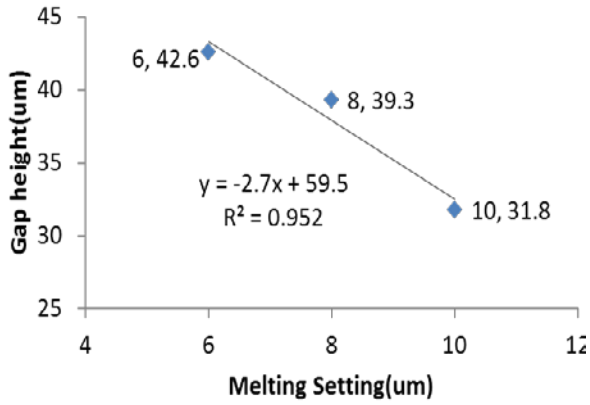
Gap height versus 6um and 10um melt setting

Melt Setting 6um



Melt Setting 10um





From this work, we were able to plot the gap height versus melt setting and determine the best condition to achieve a nominal interconnect height of 35um.

Build to validate DOE 3

Bonding Conditions:

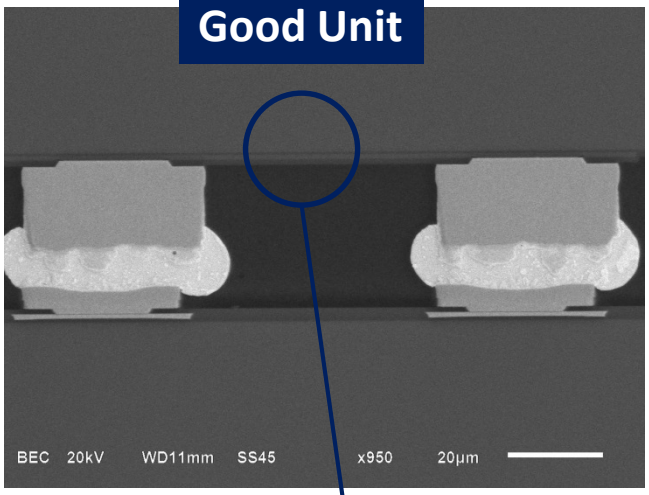
- Gap Control = -10um
- Flux Type/Dip = ABC / 5um
- Force = 2.8N
- Stage Temp = 130C
- Contact Temp = 130C
- Peak Temp/Time = 305C / 5sec
- Release Temp = 130C

91.7% MBD Yield: 33/36 MBD Pass on "Good" ITP
(OPEN failures. X-sec reveals trace defects in failing DC)

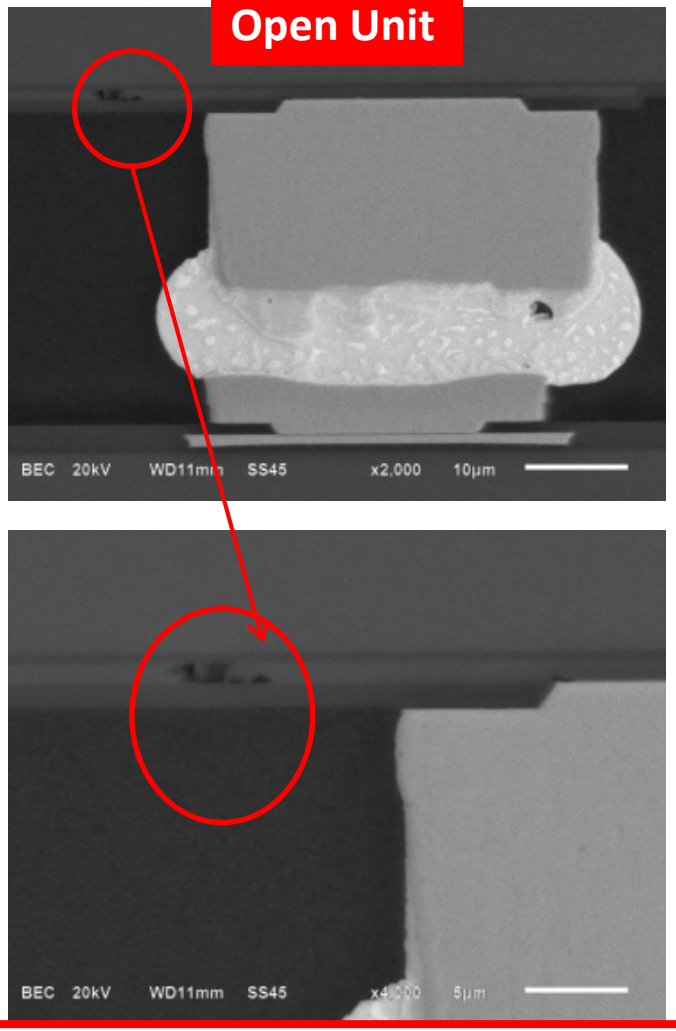
3/36 assemblies with opens which were due to defects in the MBD metallization.

Failure Analysis of Open Units from DOE 3

Good Unit



Open Unit



Summary

- The semiconductor fabs can produce robust and reliable devices with TSVs.
- A PF3 type of process, is compatible with an OSAT facility, and can produce 3D IC packages that can meet the challenges of JEDEC reliability specifications.
- This work has shown that a high yielding MBD to Si-ITP process is achievable.
- The manufacturing infrastructure exists to assembly in high volume these types of packages using existing OSAT manufacturing infrastructure.

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Gabe Guevara

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