Refining Stencil Design to Counter HIP Defects

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Abstract
Head-In-Pillow (HIP) defects, in which the BGA solder balls and paste deposit come in contact but do not coalesce, have proven to be a major problem since transitioning to RoHS soldering. Component warp can contribute significantly to HIP defects. While process engineers can make changes, such as reflow profile adjustment, to reduce the number of defects, component warp is generally dictated by component design. However, it is possible to counter the component warp by adjusting the stencil design. This paper outlines a method of refining the stencil design process to achieve the best results.

Introduction
Since transitioning to RoHS soldering several years ago, Analogic has found HIP defects to be a significant cause of failure. HIP defects can be especially damaging as they can escape electrical test, and therefore PCB's must be subjected to 100% x-ray inspection until it can be said with certainty that HIP defects are not present.

The author has found HIP defects to be uncommon, occurring on only a handful of over 1000 active assemblies we produce each year, but costly and difficult to eliminate. HIP defects have been found on a variety of board types, using both no-clean and water soluble pastes. Certain part numbers have been found to have more susceptibility to HIP defect.

This paper focuses on the case study of one particular PCB with a high incidence of HIP defects. Using the methodology outlined, process yield was improved from 0%, with 5-10 HIP defects per board, to 100% with no HIP defects.

Background
The focus of this study is a large (330x430 mm) PCB used in a medical imaging application. It is 3mm thick with good copper balance, and therefore the PCB warps very little during reflow. The solder paste used is a SAC305 water soluble, organic acid type paste. Reflow is done in an 8-zone convection reflow oven in a nitrogen environment, with O2 levels lower than 50ppm. Solder paste inspection (SPI) is done with a 3D solder paste inspection system.

The HIP defects occurred on only one part number, which is a small (10x10 mm) 144 I/O BGA located on both sides of the board. There are 24 BGAs of this part number per board. The ball pitch is 0.8 mm. The pads are 0.3 mm in diameter. Initial stencil design for this package was 0.125 mm thick foil with 0.36 mm square apertures.

The PCB also includes 5 other BGA part numbers, none of which suffered from HIP defects.

When the problem was first discovered in production, reflow profile changes were made in an attempt to eliminate HIP defects. It was found that a faster profile, with a minimum soak, did reduce the number of HIP defects from 5-10 per board to 0-3 per board but at the cost of increased in voiding on the BGA solder balls.

A change to a no clean solder paste was not allowed by design engineering due to electrical performance and reliability concerns.

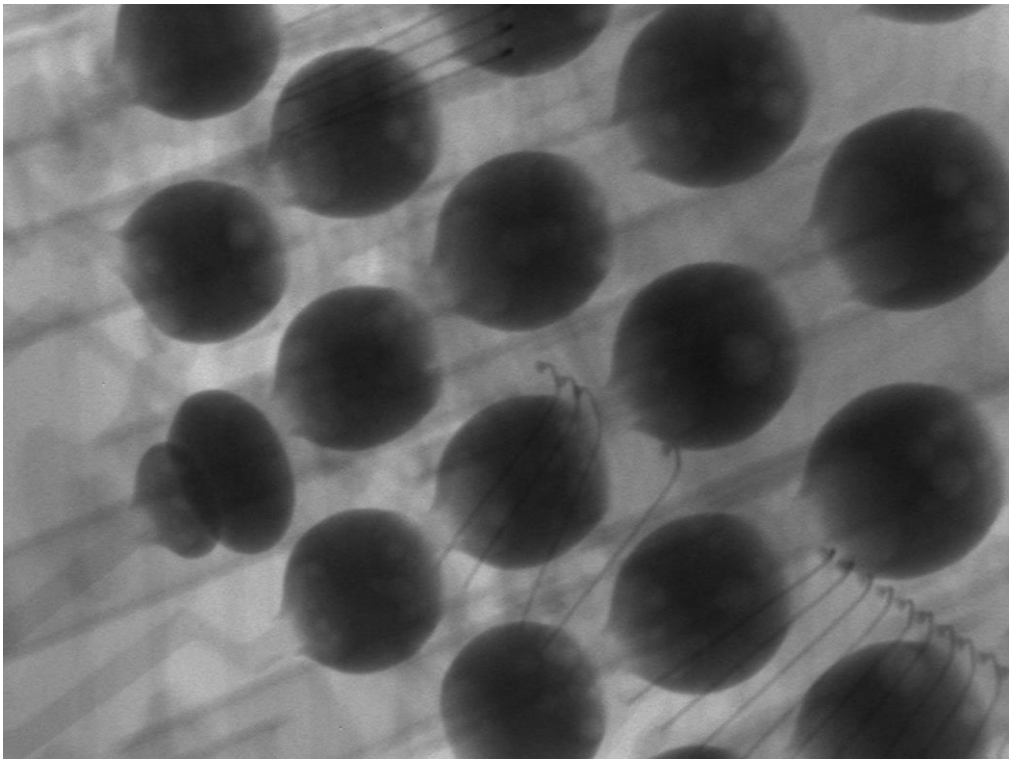


Figure 1- HIP Defect in Corner of BGA

The screen print process was examined, with extra attention paid to paste volume versus HIP defect location. Generally, transfer efficiency was found to be above minimal acceptable levels but with some room for improvements. No correlation was found between pads with lower paste volume and HIP defect locations.

Unable to eliminate defects with process changes, component warp was next examined as the root cause of the defects. Warp was suspected based on the pattern of the defects, with all HIP defects on the outer perimeter and the majority at the four corner balls. It was also known from previous experience that parts from this particular manufacturer were more likely to suffer from HIP defects.

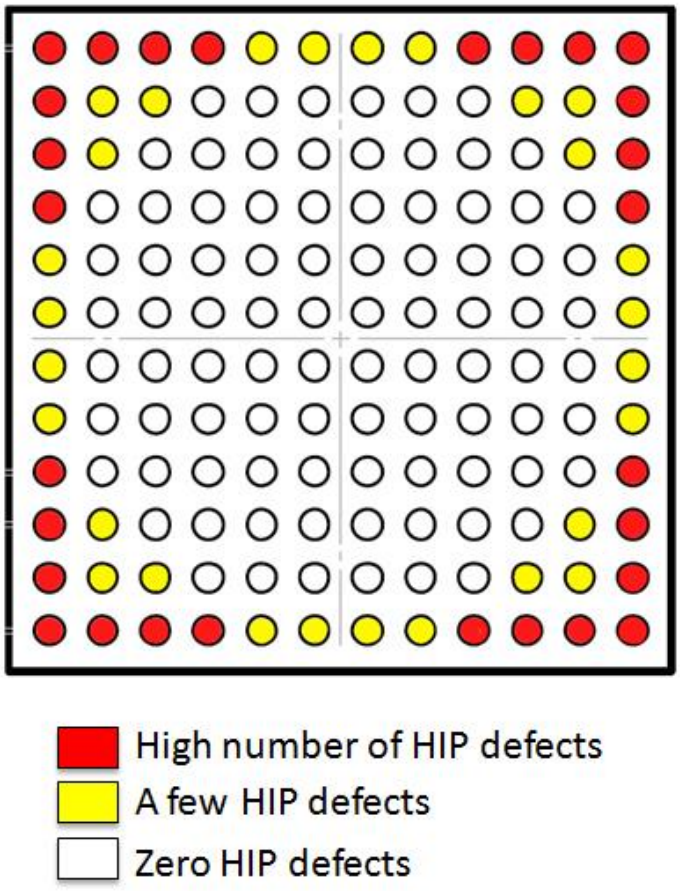


Figure 2- Initial Pattern of HIP Defects

First Attempt to Reduce Defects

It was decided to counter the package warp by adding more paste to the perimeter stencil apertures for this BGA. Using intuition, a "shot in the dark" guess was taken and enlarged the perimeter pads from 0.36 mm to 0.41 mm. This increased the paste volume by about 30% and completely eliminated the HIP defects on the perimeter. The average number of defects per board was also reduced.

The new stencil did not completely eliminate HIP defects. A new pattern to the defects was noted with all occurring on the second row in from the perimeter. It was speculated that the increased height of the perimeter solder bumps, raised the devices off the board slightly reducing the amount of BGA solder ball to pad solder bump contact on the second row.

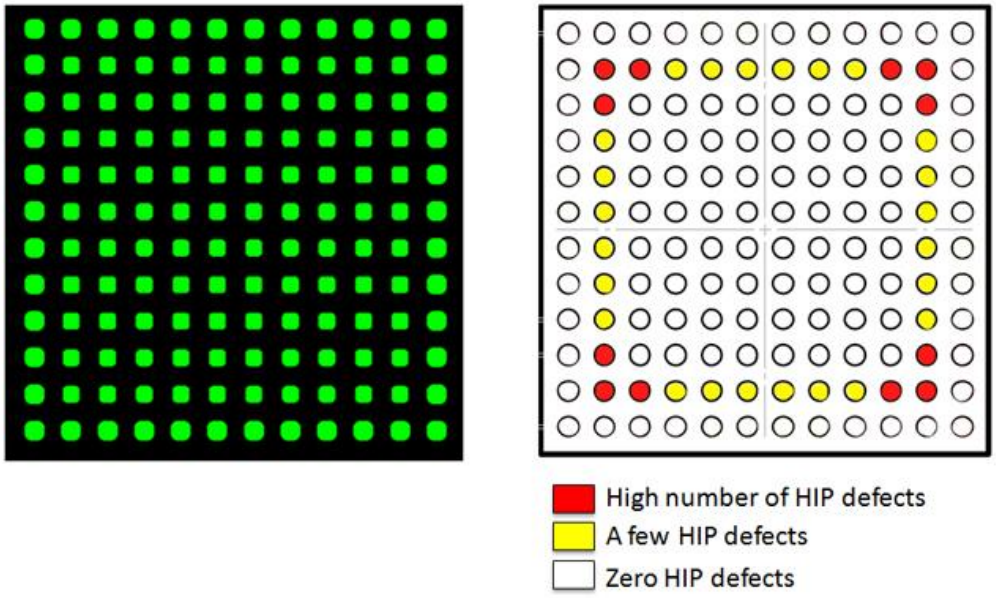


Figure 3- Revised Stencil Design (left) and resulting shift in HIP defect location (right)

Stencil Design Methodology

Based on the shift in defect location, it was decided that the stencil design process needed to be further refined. The approach taken was to attempt to match the warp of the component with variable solder volume on each pad; so that in reflow, the contact areas and wetting force between each solder ball and molten paste bump would be equal.

The first step was to measure the warp of the components. Using a non-contact profilometer, the warp of both soldered components and parts straight from the vender were measured. In both cases, a strong correlation between the location of HIP defects and areas of greatest warp was found. Unsoldered parts were found to have a warp of approximately 0.03mm from the vendor, increasing slightly (0.005-0.01 mm) after part was soldered to the board.

Because the warp of the individual components at room temperature is nearly equal to warp of the soldered component on the PCB, it is believed that the package flatness is relatively stable during the reflow process.

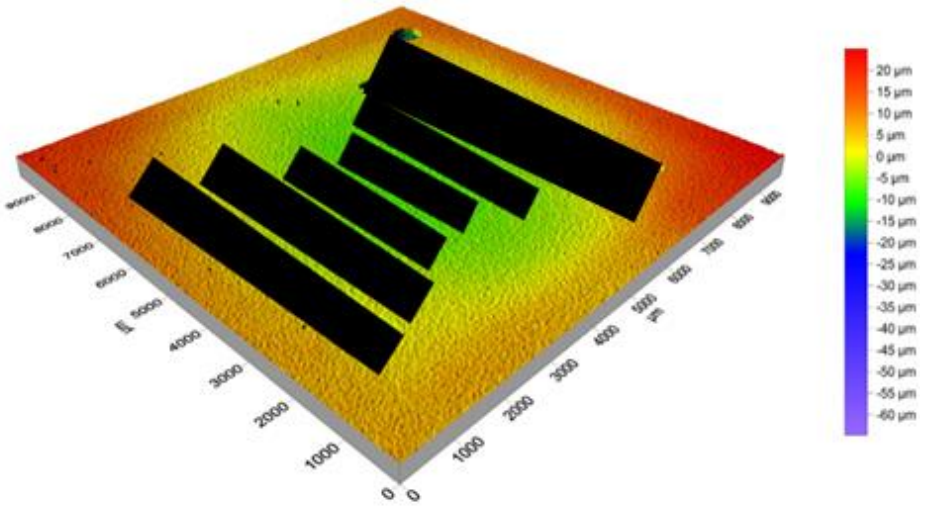


Figure 4- Warp of Component As Delivered

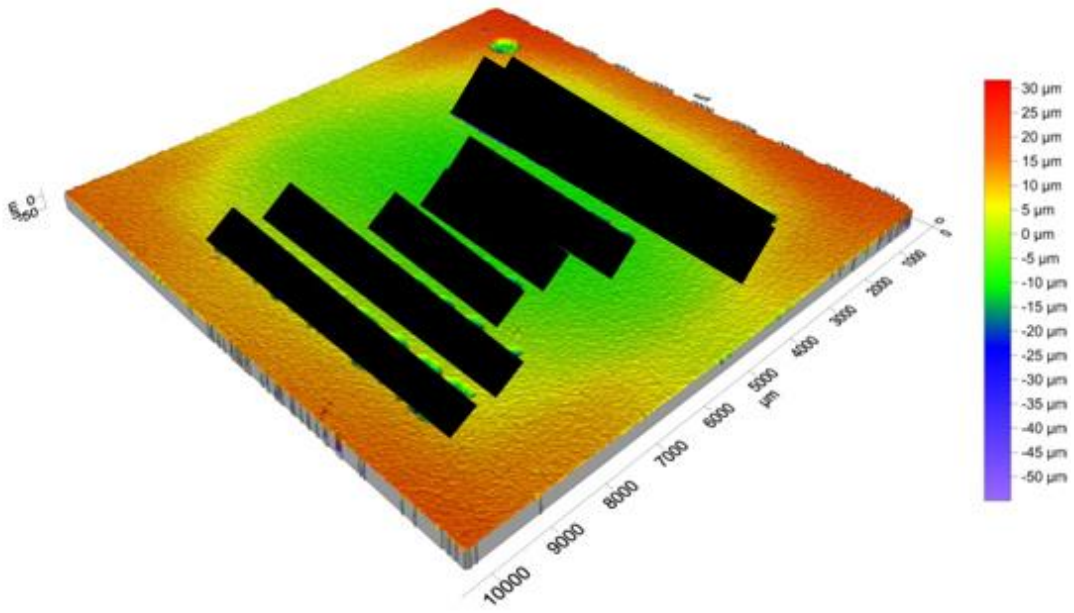


Figure 5- Warp of Component After Soldering

In order to gauge the impact of the warp on solder to bump contact, a 3D computer aided design (CAD) solid model was created as shown in Figure 6. In this view, the ball located closest to the center is on the left and the corner ball is on the right. It was assumed the distance between the board and bottom of BGA was 0.35 mm based on package specifications and x-ray images.

To quantify the solder mechanics reflow, the interference volume between BGA ball and solder bump was calculated, assuming this would be proportional to the wetting force. That is, the greater interference volume, the more the ball and bump are forced together and the greater the likelihood that they will wet/coalesce. The interference of the right most solder ball is highlight in red.

Solder balls were found to have a interference volume varying from 0.0014 mm^3 in the center to as little as 0.0005 mm^3 at the corners. The areas with the lowest interference volume matched the locations with increased HIP defects during production. This shows that even a relatively small warp of 0.030 mm can significantly impact the wetting forces in reflow.

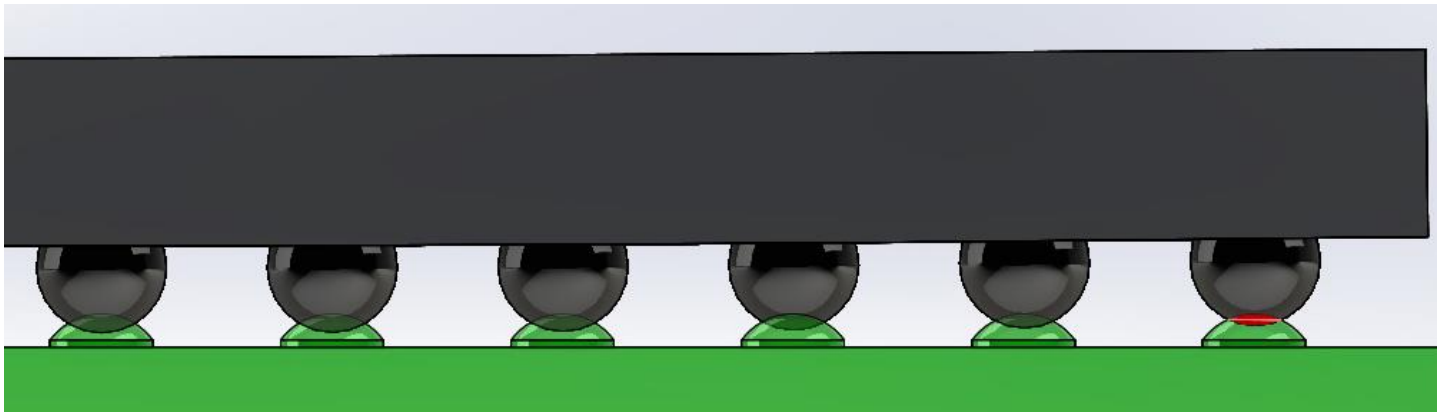
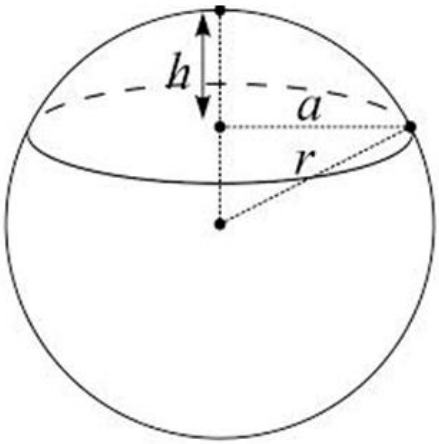


Figure 6- Modeled View of BGA Ball to Solder Bump Contact with Original Stencil

In order to calculate solder bump height in reflow, it was assumed the solder bumps would take the shape of a spherical cap. Using the formula $V=\pi*h(3a^2+h^2)/6$, where V is the volume of the paste deposited, a is the radius of the PCB pad, and h is the resulting height of the bump. A formula for h was then found as shown in Figure 7.



$$h = \frac{\sqrt[3]{\sqrt{\pi^2 a^6 + 9V^2} + 3V}}{\sqrt[3]{\pi}} - \frac{\sqrt[3]{\pi}\, a^2}{\sqrt[3]{\sqrt{\pi^2 a^6 + 9V^2} + 3V}}$$

$$V = \frac{\pi h}{6}(3a^2 + h^2)$$

Figure 7- Calculating Bump Height

The volume of the paste deposit was calculated using the formula $V=A_a * t_s * TE * \rho_p$, where A_a is the aperture area, t_s is the stencil thickness, TE is the transfer efficiency, and ρ_p is the paste density. The transfer efficiency was assumed to be 75% for all pads, though apertures with higher area ratios may be more efficient in reality. Paste density was assumed to be 50%.

A spreadsheet was created in which all of the variables discussed above, along with component warp, are input. The component warp is entered into a grid pattern representing ¼ of the part. This assumes each quarter of the part would have the same warp. The bump height required to match the component warp and the volume of paste needed to achieve that bump height were then calculated. Figure 8 shows the steps as laid out in the spreadsheet.

Part Warp Map					
30	27.5	23	18.5	14.4	10.8
27.5	25	18.5	14	10.3	7.19
23	18.5	12	9.5	6.5	4.13
18.5	14	9.5	7	3.5	1.75
14.4	10.3	6.5	3.5	0	0
10.8	7.19	4.13	1.75	0	0

Bump Height Requirement map					
120	118	113	109	104	101
118	115	109	104	100	97
113	109	102	100	97	94
109	104	100	97	94	92
104	100	97	94	90	90
101	97	94	92	90	90

Required volume					
419	408	389	370	353	339
408	398	370	352	336	324
389	370	343	333	322	312
370	352	333	324	310	303
353	336	322	310	296	296
339	324	312	303	296	296

Figure 8- Algorithm to Calculate Required Paste Volume

Finally, the aperture dimensions were determined. In order to simplify the area calculations, all apertures featured 0.05 mm rounded corners. Careful attention had to be paid to the edited stencil Gerber data received back from our supplier. Stencil fabricators are not accustomed to such exact requirements for aperture dimensions and tended to round up or down.

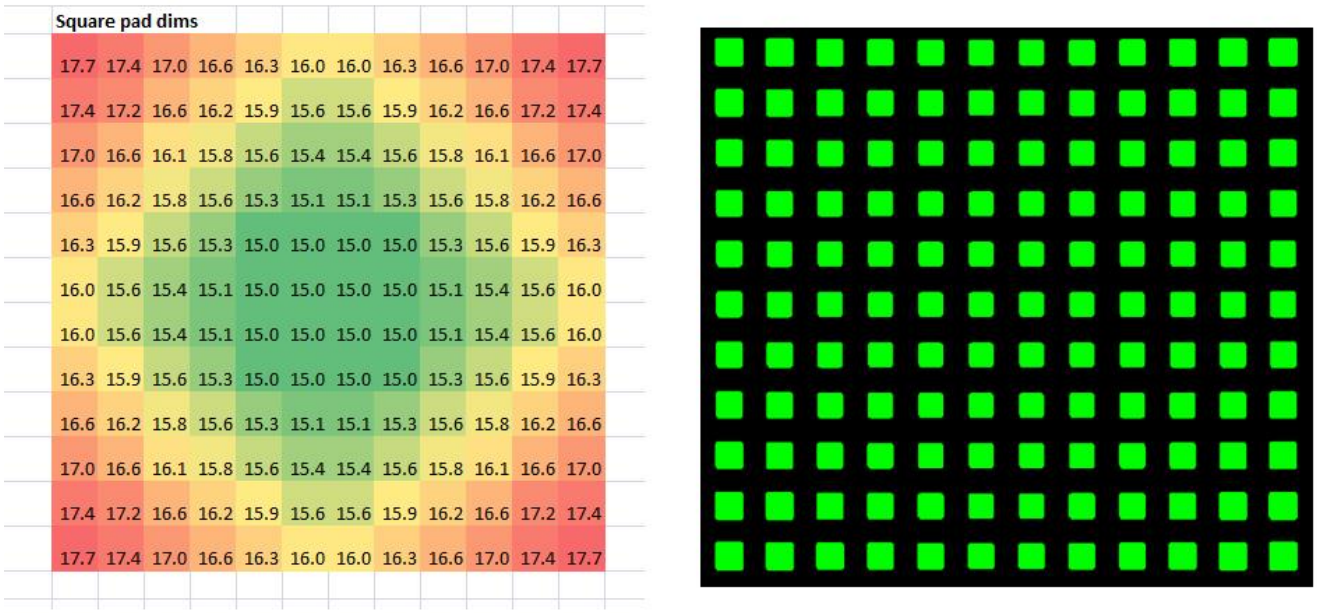


Figure 9- Final Calculated Aperture Dimensions (left) and Gerber Data for BGA (Right)

The bump heights calculated were then entered into the CAD model to determine the resulting interference volume. The model shows how the increasing bump heights compensate for the package warp (Figure 10). A comparison of interference volume using the initial and variable aperture stencils is shown in Table 1. Compared to the initial stencil design, the interference volumes calculated are much more uniform, and therefore it is believed the wetting forces should be relatively equal across the package.

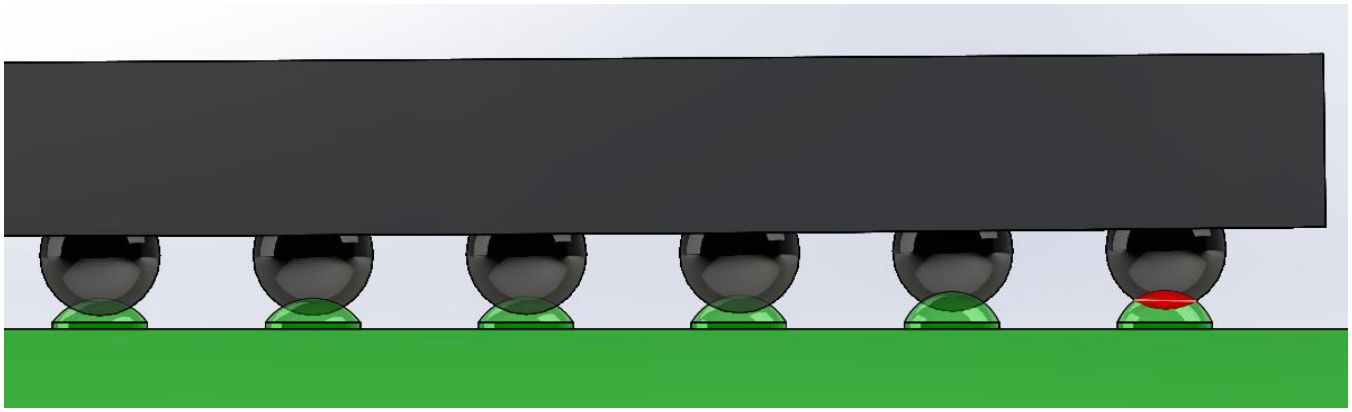


Figure 10- Modeled View of BGA Ball to Solder Bump Contact with Variable Aperture Stencil

Table 1- Interference Volume of Initial vs. Variable Aperture Stencils

Ball Distance From Center (mm)	Initial Stencil Interference Volume (mm^3)	Variable Aperture Stencil Interference Volume (mm^3)
0.6	0.0014	0.0014
1.7	0.0013	0.0013

2.8	**0.0012**	**0.0014**
4.0	**0.0010**	**0.0014**
5.1	**0.0008**	**0.0016**
6.2	**0.0005**	**0.0015**

Results

Using the new stencil design, HIP defects were completely eliminated.

Paste release data, measured in SPI, and reflowed bump height, measured on a profilometer on a reflowed bare board, show that the difference in volume and bump height is greater than expected. The predicted difference in bump height from center to corners was 0.03 mm. Actual difference was found to be about 0.05 mm. It is believed this was caused by differences in transfer efficiency between smaller and larger apertures, with larger apertures apparently having transfers efficiencies greater than the assumed 75%.

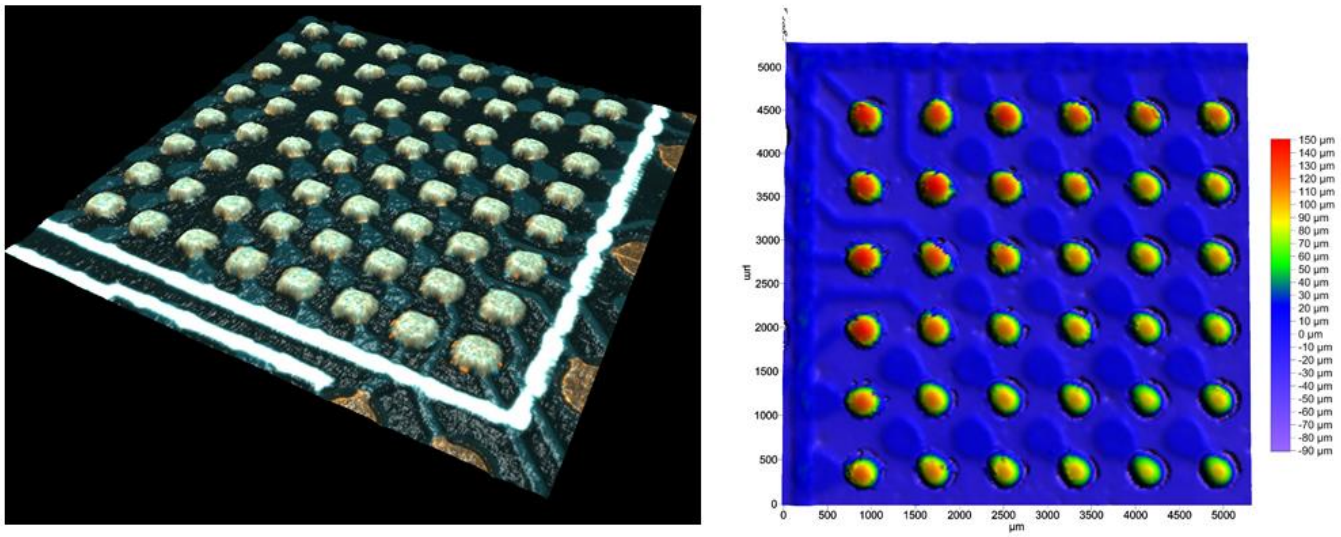


Figure 11- SPI Scan (left) and Bump Height Scan (right)

Conclusions and Future Work

A method for designing BGA stencil apertures was developed based on measured component warp. The results based on improvement in process yield show that this stencil design method provides an effective tool to counter HIP defects caused by BGA warp.

Based on the review of transfer efficiency and bump heights, further refinement is required. However, it is still believed this is still far superior to "shot in the dark" methods where stencil apertures are enlarged based on guesswork whenever HIP defects are found.

Future work will focus on refining the paste volume requirements to factor in differences in transfer efficiencies based on area ratio.

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Summary

•This presentation focuses on a novel approach to stencil design which reduces head in pillow defects caused by BGA component warp.

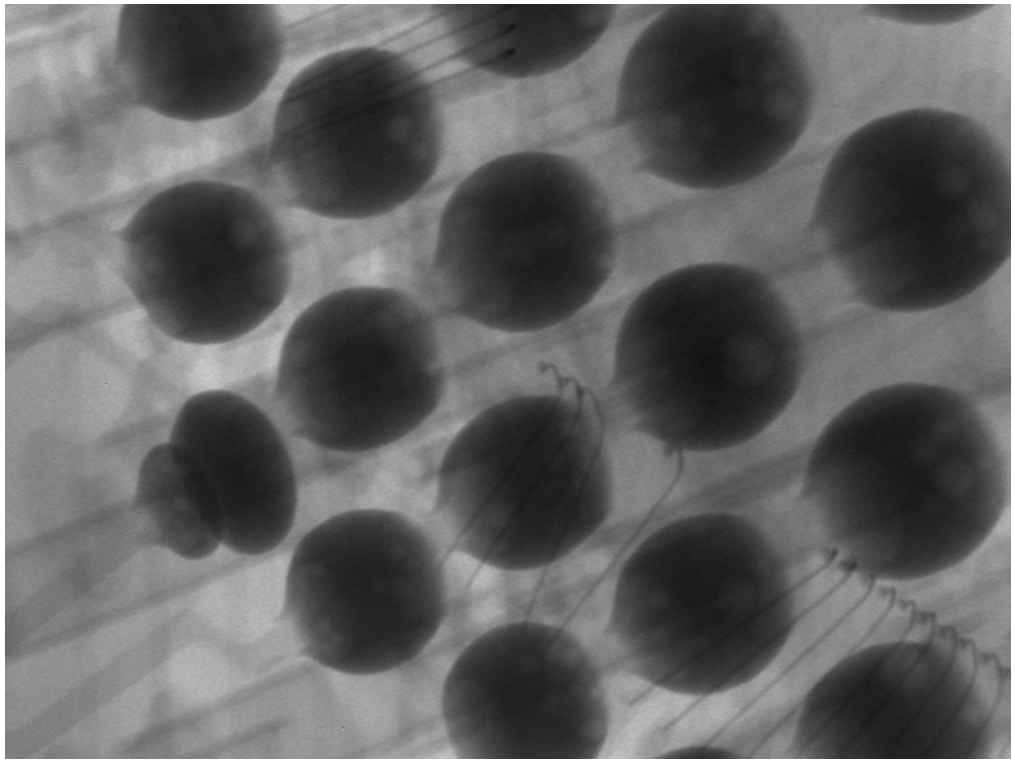
•Rather than guesstimate aperture dimensions required based on HIP defect location, we developed a method of calculating the ideal aperture dimensions to counter HIP defects caused by component warp.

•This presentation is based on our experience with a production PCB.

What Happened?

•During a production run of a large medical imaging PCB, we encounter a problem with HIP defects.

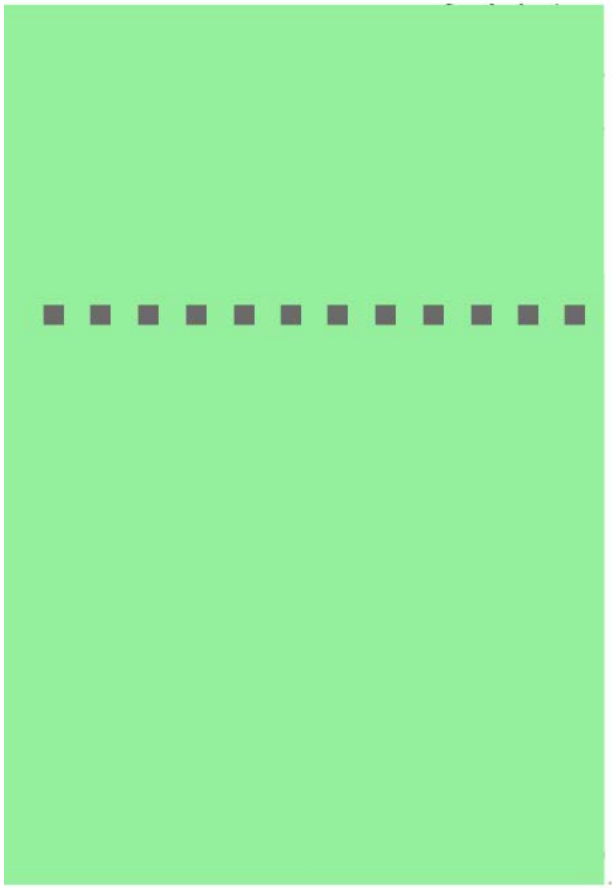
•Since changing to RoHS soldering, we have found this type of defect to be the most challenging.



X-ray image showing HIP defect in production.

Notes on Design

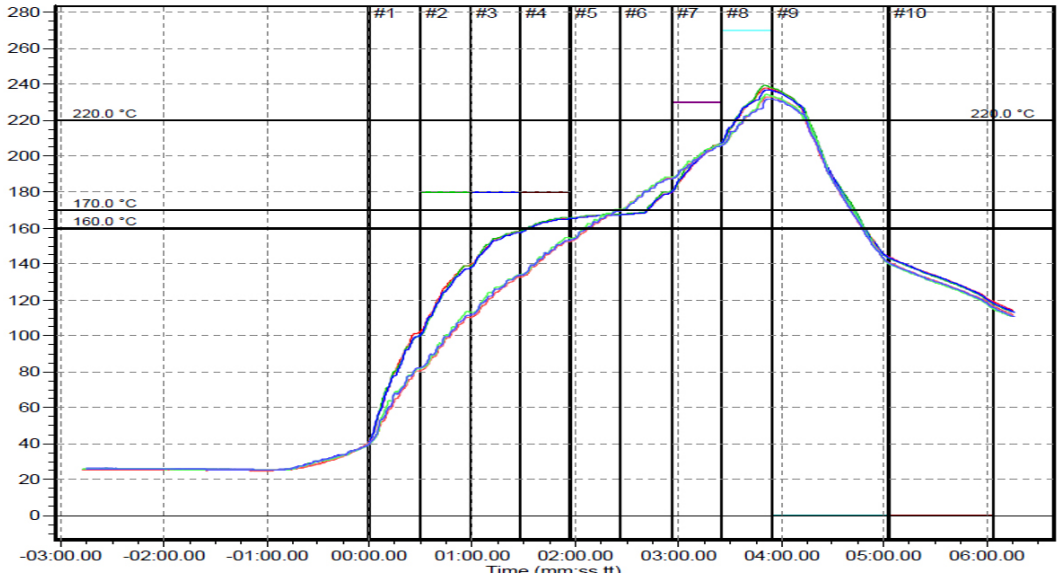
- Board is a large (330x432 mm), and about 3 mm thick.
- 20 layers with good copper balance
- BGA's with HIP problem arranged in row of 12 on each side of the board
- Pads are 14 mil diameter etch defined round
- The board also includes 5 other BGA types, which were free from HIP defects



Sketch of affected PCB, showing location of BGAs with HIP defects

Process Notes

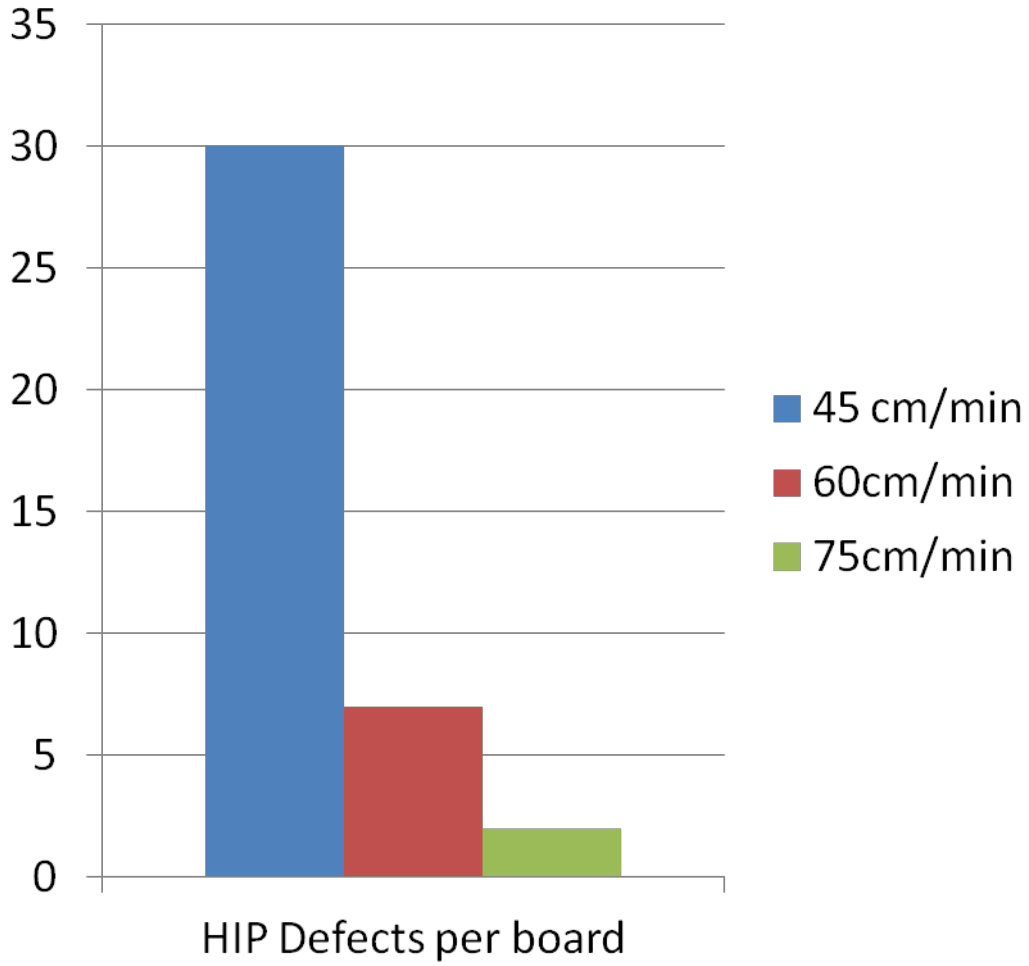
- SAC 305 OA solder paste.
- Profile with soak, to reduce voiding.
- 8 Zone convection reflow oven running with N2 (02 levels below 50ppm)
- Initial stencil with 5 mil thickness and square apertures, 14 mils with 3 mil rounded corners.
- Automated solder paste inspection.



View of both initial soak profile and predicted straight ramp profile.

Impact of oven speed

- In an effort to reduced defects we tried various oven speeds.
- Running faster reduced, but did not eliminate, defects, and with this paste leads to increased voiding.
- Ended up with a straight ramp 65 cm/min speed.



Impact of Paste Flux Type

- It is also worth noting that we have had good luck on other products changing to a no-clean (NC) flux with fairly high residue after reflow.

- We see significantly higher incidence of HIP using water soluble based chemistries or low-residue NC pastes.

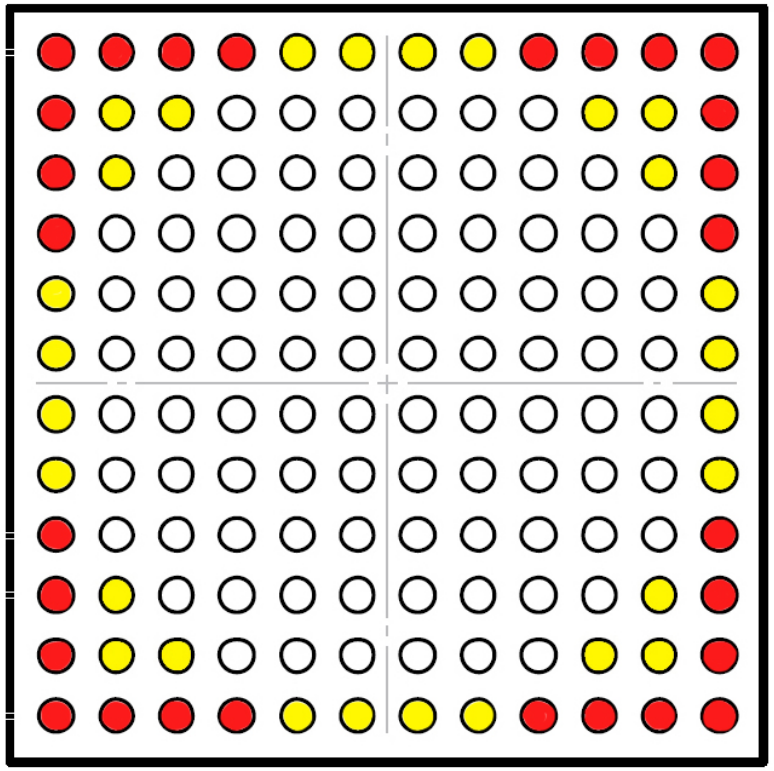
- In this case, electrical performance and reliability concerns would not allow the use of typical NC paste.

Defect Locations

Warp of part suspected as root cause based on:

- Location of defects on parts.

- Experience with HIP defects on another device from same vendor.



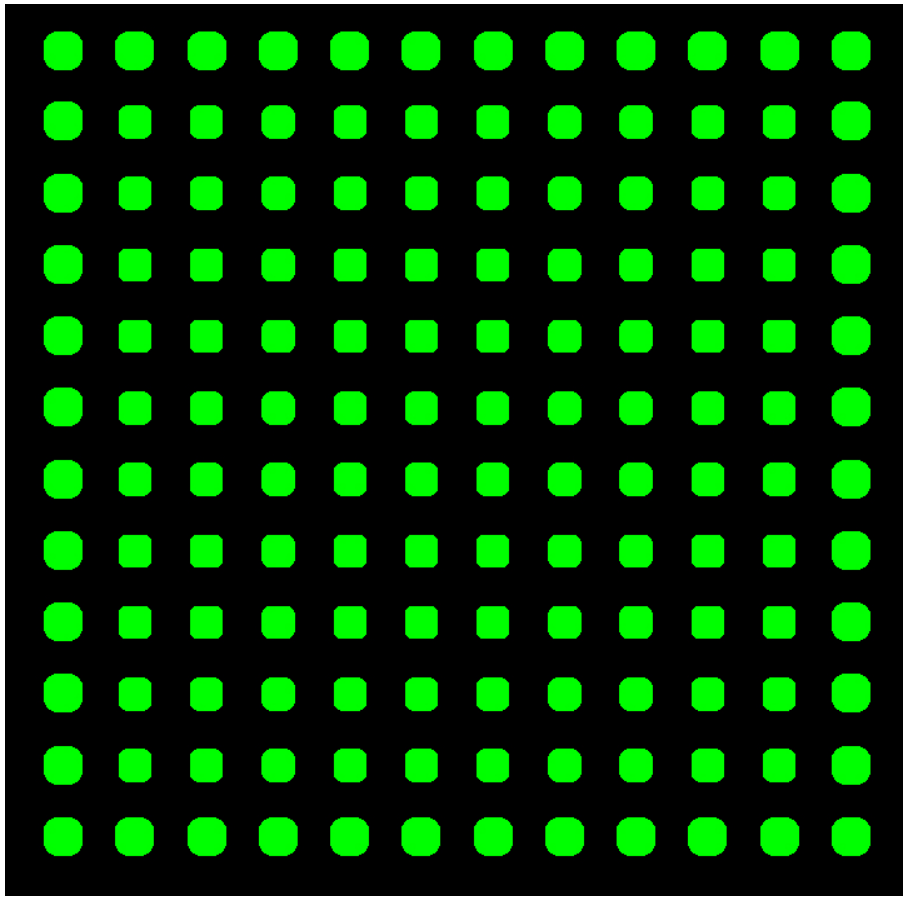
High number of HIP defects

A few HIP defects

Zero HIP defects

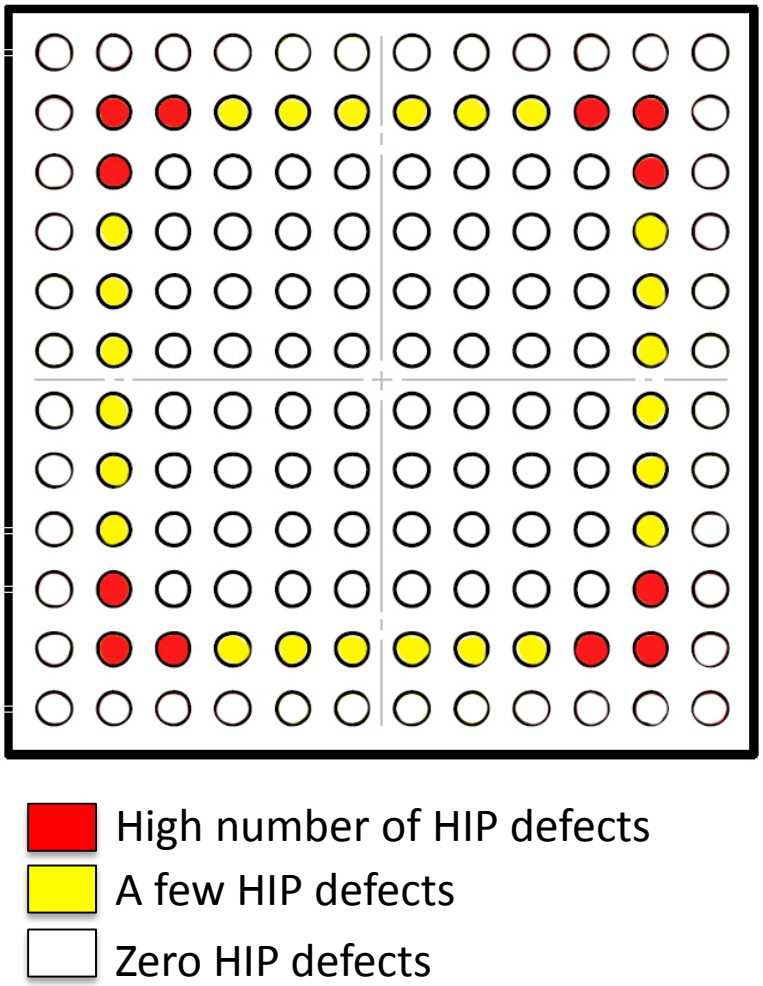
Attempt #1for Stencil Fix

- To add more paste and focused only on perimeter pads, where most HIP occurred.
- Outer pads were increased from 14 to 16 mils.
- This increased the volume of paste by about 1/3 on perimeter pads.



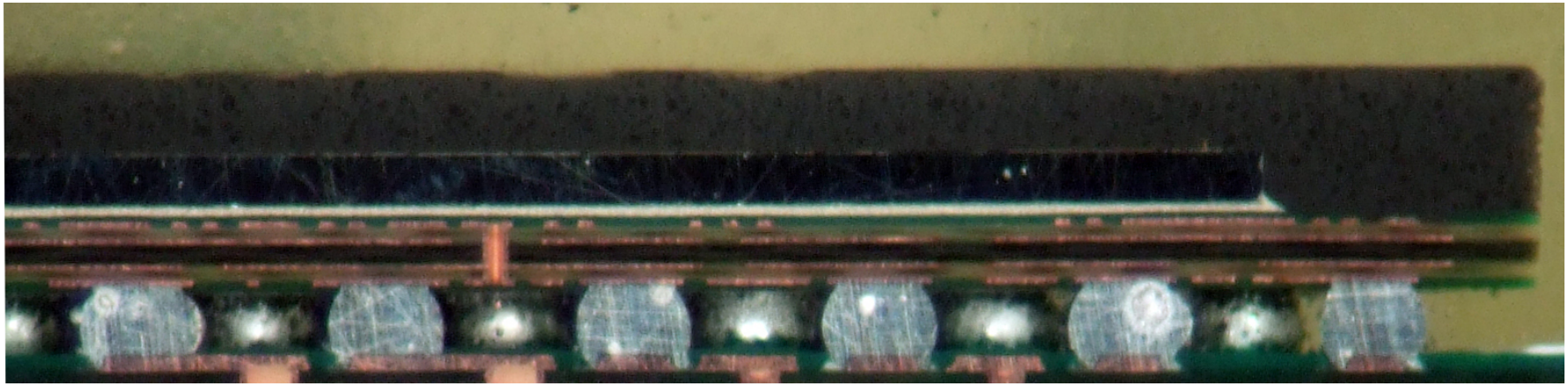
Results

- The overall number of defects did drop.
- However, some HIP defects still found.
- Defects moves to second row in.



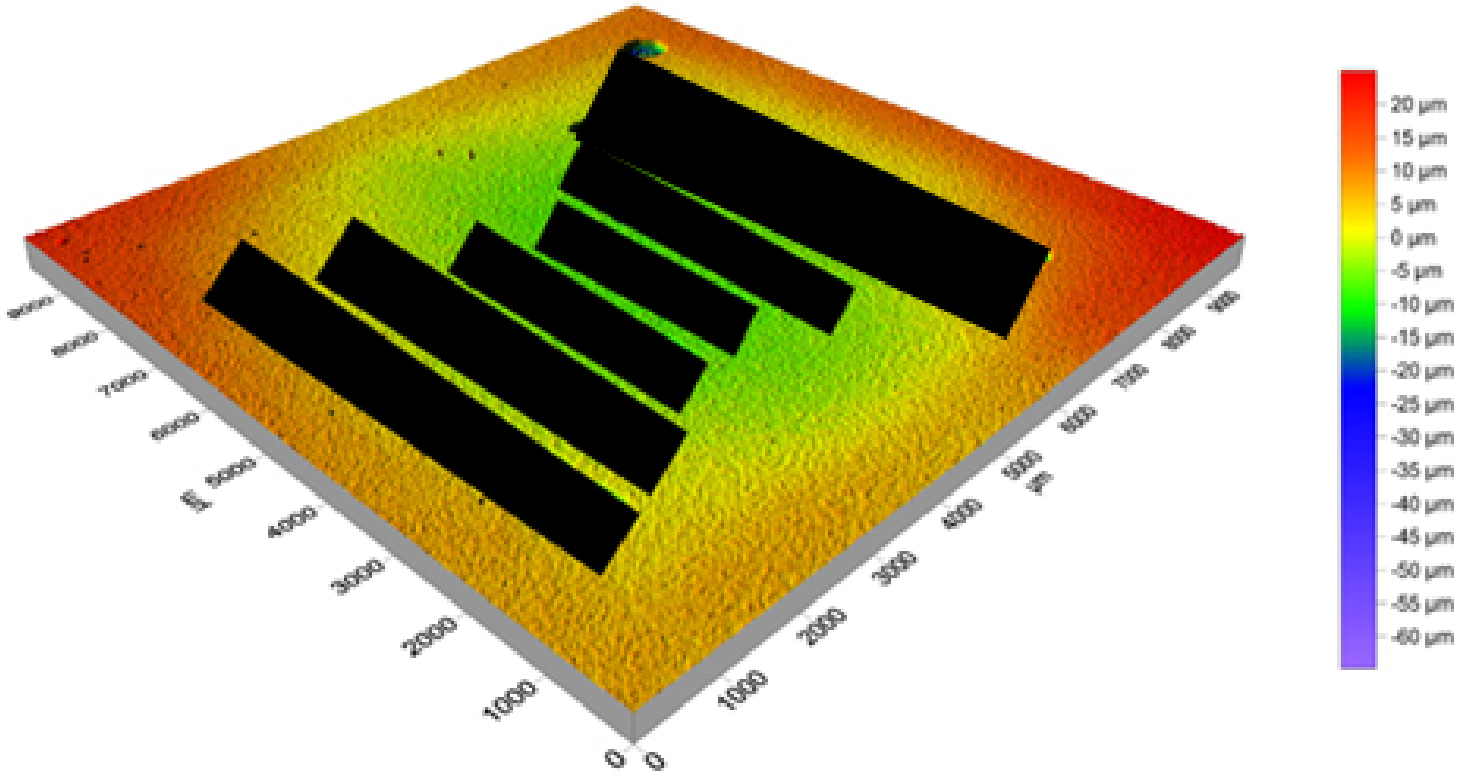
Second Design

- We determined that a more precise method of stencil design was needed.
- Our approach was match the warp contour of the bottom of the part with variable paste volume.

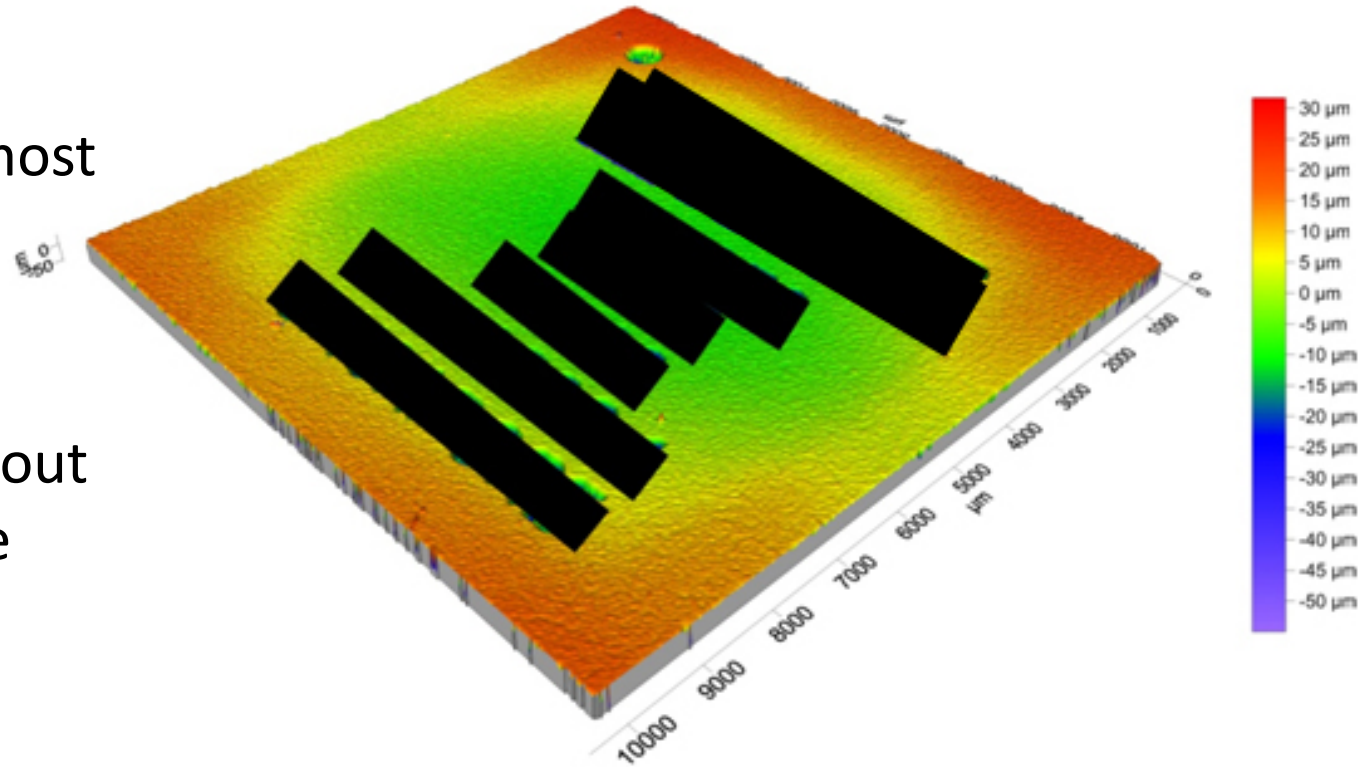


Diagonal cross section of soldered part. Note outer balls are taller than center balls.

- Flatness of unsoldered BGA measured with non-contact profilometer.
- Parts were found to have a warp of about 30 microns.



- A scan of a part soldered to the board shows almost the same warp.
- From this we concluded the flatness throughout reflow should be relatively stable.



Once we knew the part warp, the next step was to understand how this might impact HIP, and then how to counter it.

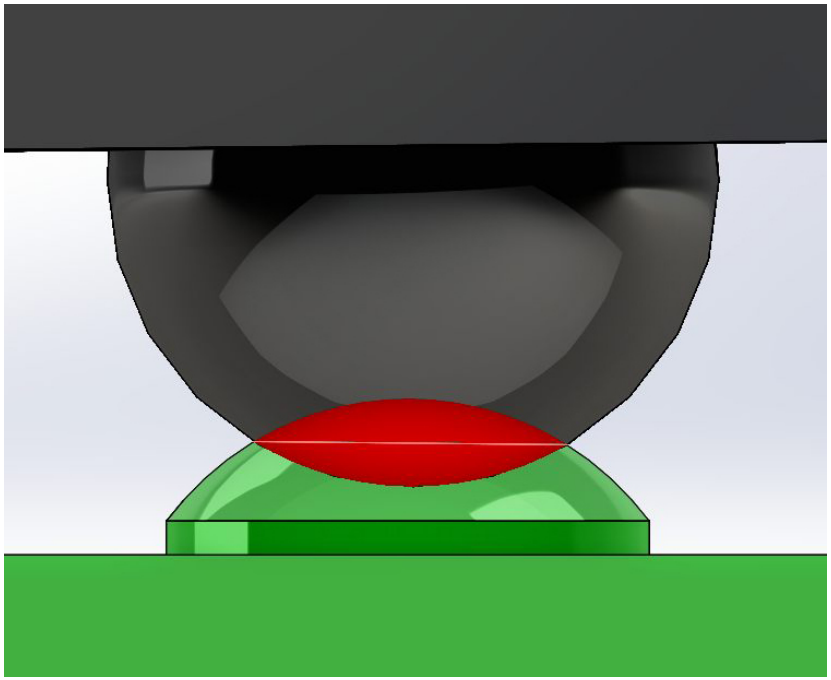
Production management encouraging the engineering problem solving process.

3D Model

- We created a 3D CAD model of the BGA and molten paste deposits.

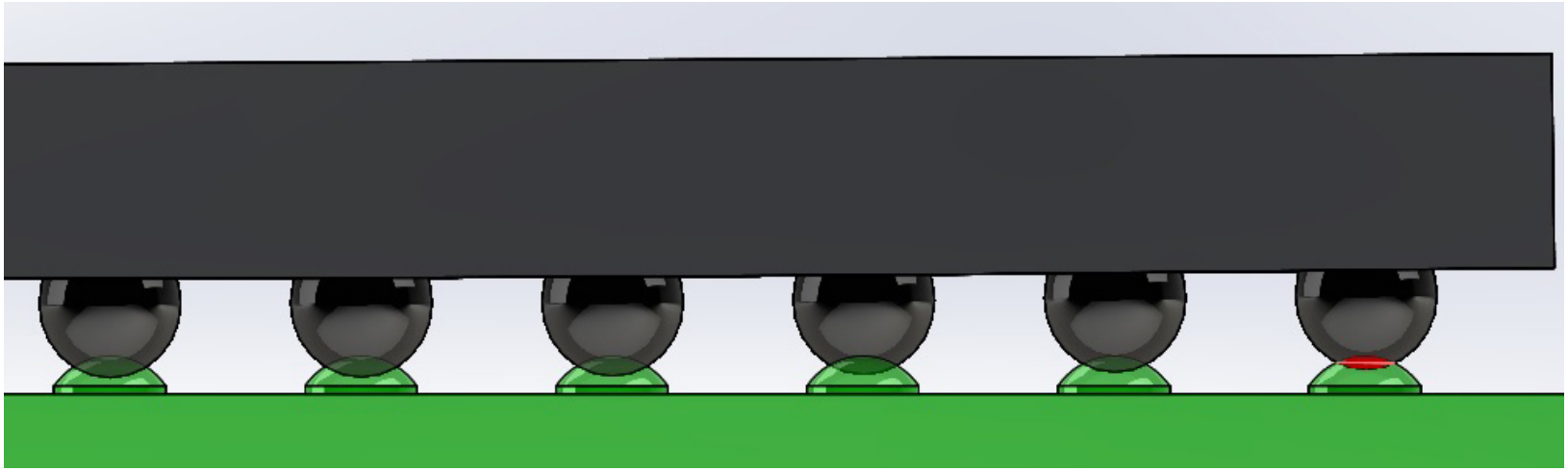
- The CAD model allows one to calculated interference volume between two overlapping objects.

- Interference volume should be proportional to wetting force.



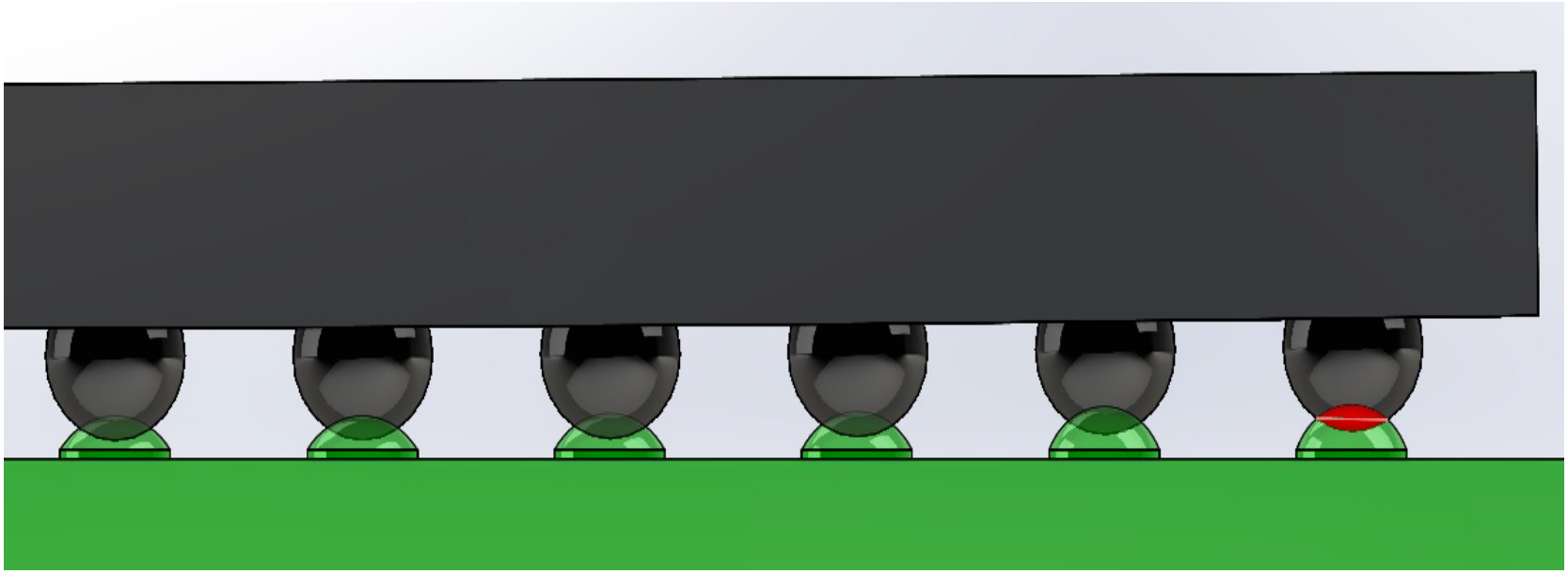
Model of solder ball in contact with molten bump. Interference area in red

As a result of the 30 micron warp, the contact area between the ball and solder bump is less on the outer rows.



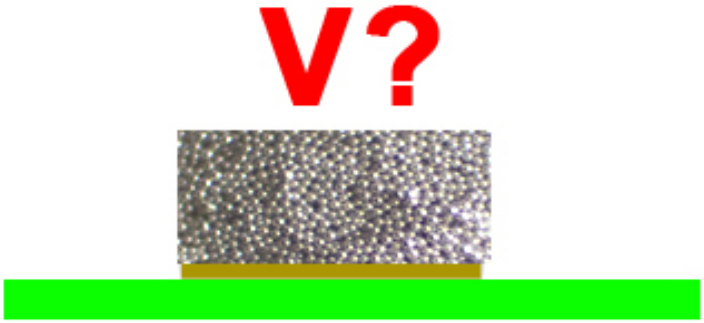
Ball Distance From Center (mm)	Interference Volume (mm^3)
0.6	0.0014
1.7	0.0013
2.8	0.0012
4.0	0.0010
5.1	0.0008
6.2	0.0005

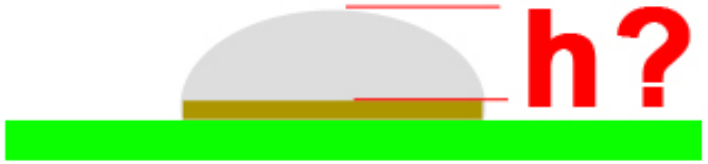
We believed that by matching the part warp with variable paste volume, we could achieve constant interferance volume and therefore contact wetting force between solder bump and ball.



Stencil Design Calculations

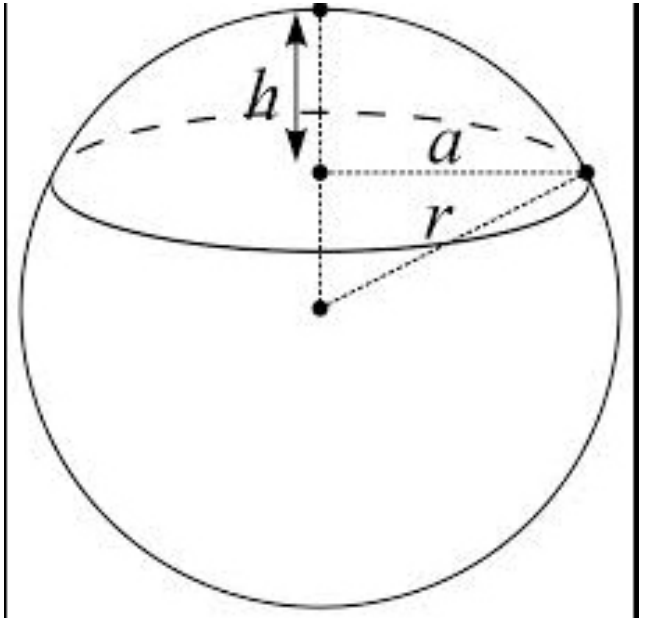
- We know how much the part is warp.
- Next we had to determine:
  1. Determine solder paste volume required to achieve bump height.
  2. How to calculate bump height required to match the warp.





Calculating bump height

- Assume solder bumps are shaped like spherical caps.
- V=volume of solder deposited
- a=pad radius
- h=height of bump after reflow



$$V = \frac{\pi h}{6}(3a^2 + h^2),$$

Solve for h

$$h = \frac{\sqrt[3]{\sqrt{\pi^2 a^6 + 9V^2} + 3V}}{\sqrt[3]{\pi}} - \frac{\sqrt[3]{\pi}\, a^2}{\sqrt[3]{\sqrt{\pi^2 a^6 + 9V^2} + 3V}}$$

Volume of solder printed

$$V = A_a \times t_s \times TE \times \rho_p$$

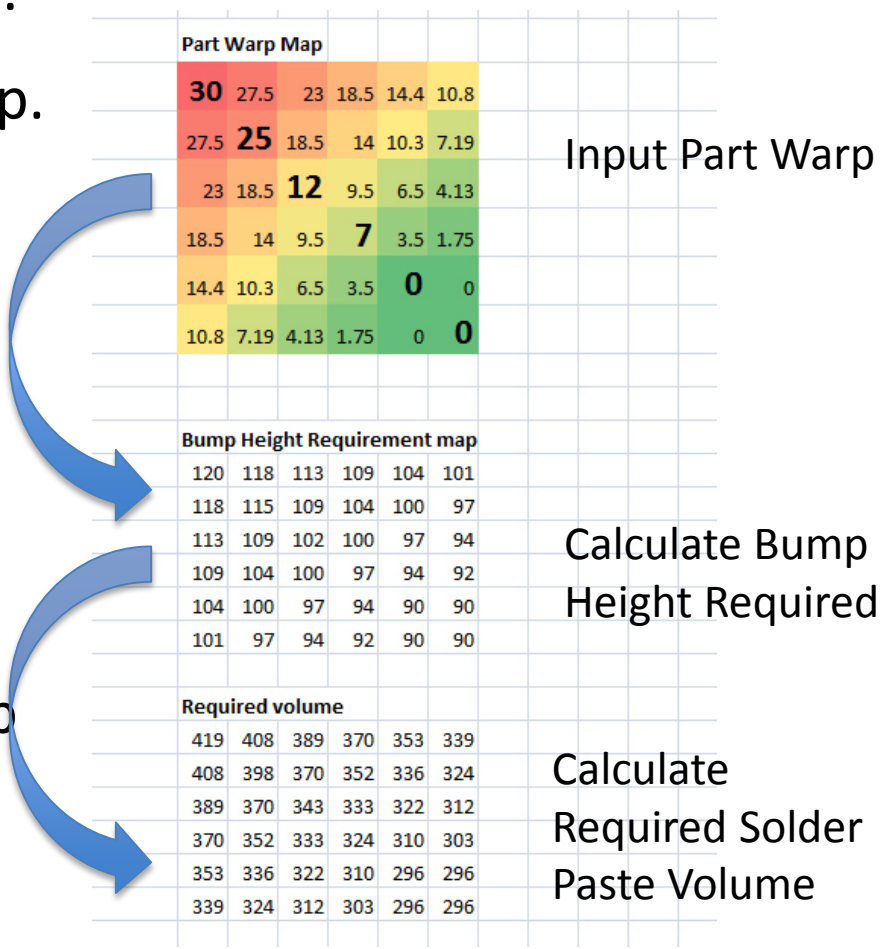
A_a=Aperture area
t_s=Stencil thickness
TE=Transfer efficiency
ρ_p=Paste Density

- Transfer efficiency assumed to be 75%.
- Paste density assumed to be 50%.

Putting this into a spreadsheet:

1. We first input the part warp.
2. Then calculated the bump height required to match that warp.
3. Then the volume of paste required to achieve that bump height.

- Only ¼ of the part is modeled assuming the warp is symmetrical.

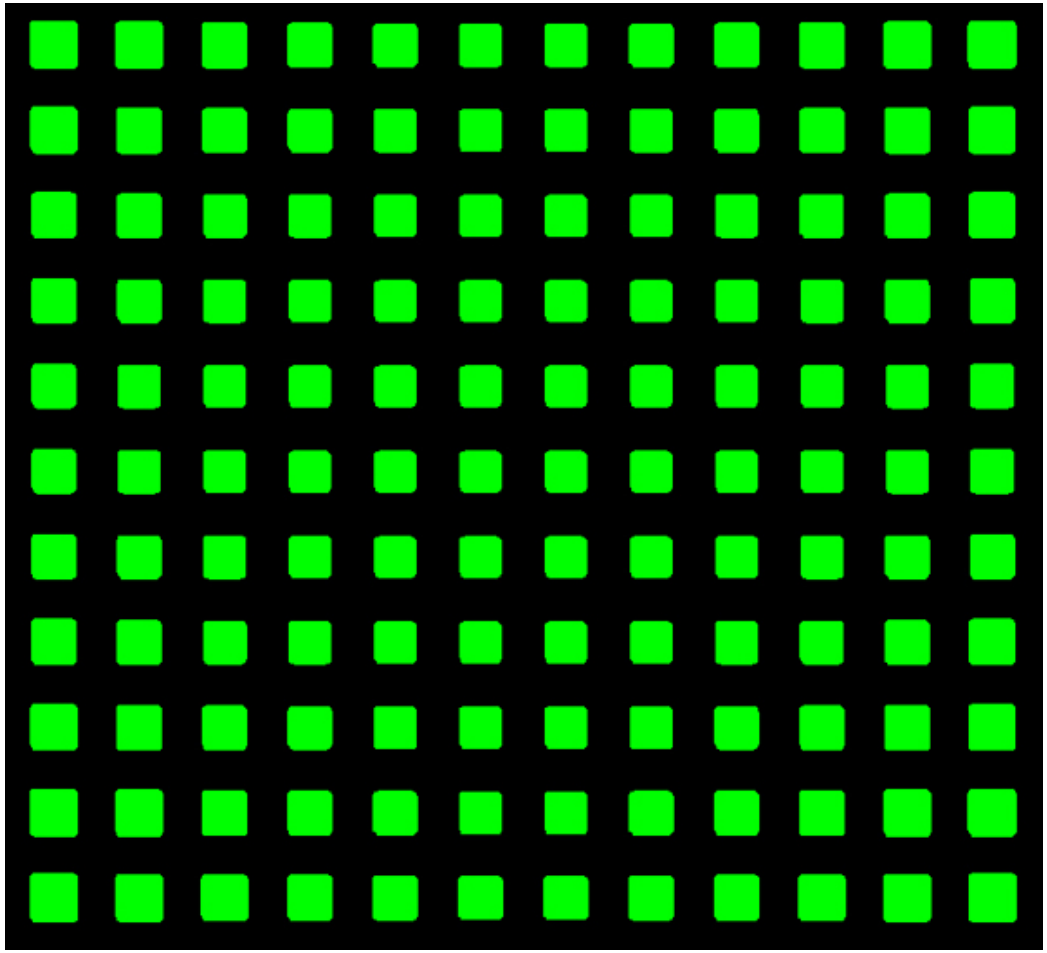


Finally: Spreadsheet outputs required pad dimensions to create a stencil which will match the part warp.

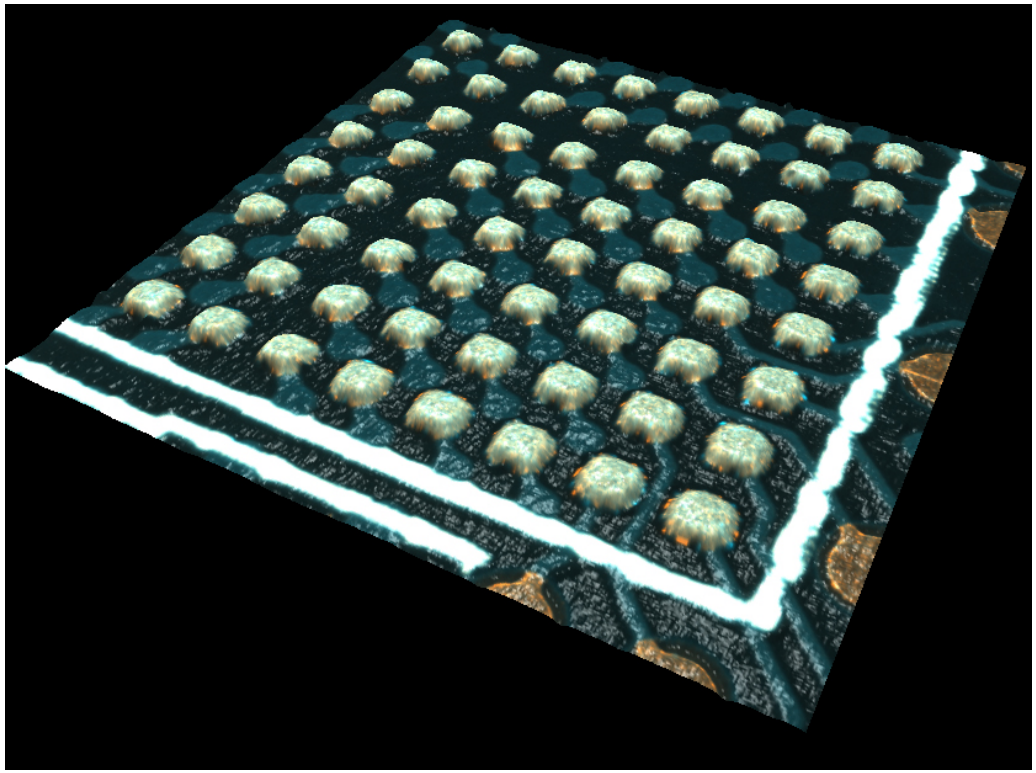
Square pad dims

17.7	17.4	17.0	16.6	16.3	16.0	16.0	16.3	16.6	17.0	17.4	17.7
17.4	17.2	16.6	16.2	15.9	15.6	15.6	15.9	16.2	16.6	17.2	17.4
17.0	16.6	16.1	15.8	15.6	15.4	15.4	15.6	15.8	16.1	16.6	17.0
16.6	16.2	15.8	15.6	15.3	15.1	15.1	15.3	15.6	15.8	16.2	16.6
16.3	15.9	15.6	15.3	15.0	15.0	15.0	15.0	15.3	15.6	15.9	16.3
16.0	15.6	15.4	15.1	15.0	15.0	15.0	15.0	15.1	15.4	15.6	16.0
16.0	15.6	15.4	15.1	15.0	15.0	15.0	15.0	15.1	15.4	15.6	16.0
16.3	15.9	15.6	15.3	15.0	15.0	15.0	15.0	15.3	15.6	15.9	16.3
16.6	16.2	15.8	15.6	15.3	15.1	15.1	15.3	15.6	15.8	16.2	16.6
17.0	16.6	16.1	15.8	15.6	15.4	15.4	15.6	15.8	16.1	16.6	17.0
17.4	17.2	16.6	16.2	15.9	15.6	15.6	15.9	16.2	16.6	17.2	17.4
17.7	17.4	17.0	16.6	16.3	16.0	16.0	16.3	16.6	17.0	17.4	17.7

The resulting stencil design shows a gradual change in aperture size across the BGA area.



Which correlates to a gradual change in paste volume across the BGA area.

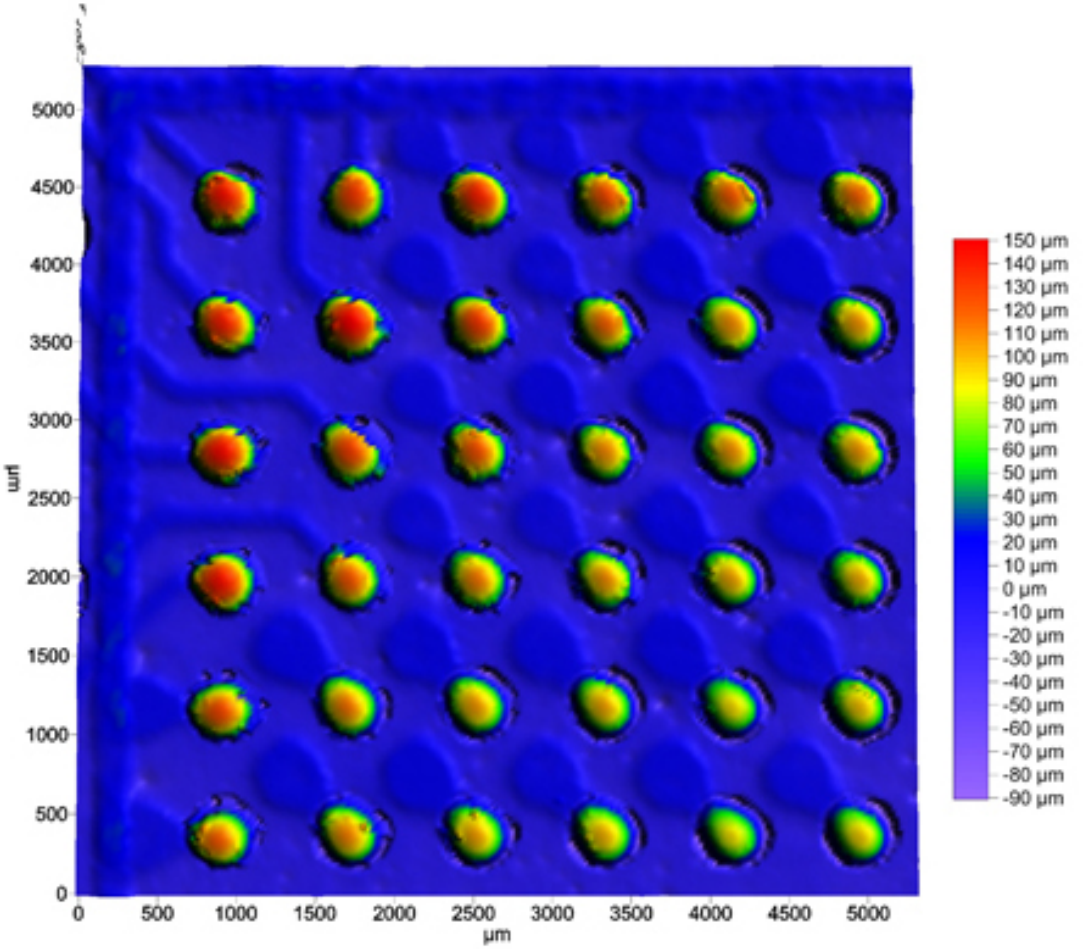


Comparison of calculated interference volumes with initial and variable aperture stencils.

Ball Distance From Center (mm)	Initial Stencil Interference Volume (mm^3)	Variable Aperture Stencil Interference Volume (mm^3)
0.6	0.0014	0.0014
1.7	0.0013	0.0013
2.8	0.0012	0.0014
4.0	0.0010	0.0014
5.1	0.0008	0.0016
6.2	0.0005	0.0015

Results

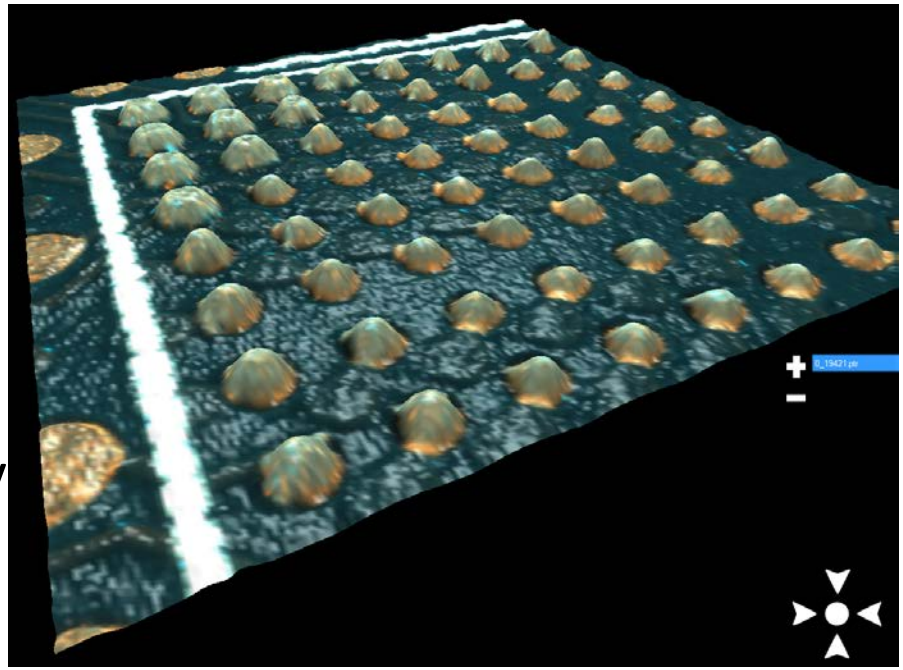
- Using the new stencil design, HIP defects were completely eliminated.
- The predicted difference in bump height from center to corners was 0.03 mm. Actual difference was found to be about 0.05 mm.



Scan of soldered bumps on bare board (center of part lower right).

- Paste release data, measured in SPI show that the difference in volume and bump height is greater than expected.

- We believe this was caused by differences in transfer efficiency between smaller and larger apertures.



SPI view of paste deposits, showing lower transfer efficiency in center (right side in picture)

Conclusions and Future Work

•We developed a method for designing BGA stencil apertures based on measured component warp.

•Further refinement is required. However, we believe it is still far superior to “shot in the dark” methods where stencil apertures are enlarged based on guesswork whenever HIP defects are found.

•Future work will focus on refining the paste volume requirements to factor in differences in transfer efficiencies based on area ratio.

- Tips for less well equipped facilities or if you are in a rush:
  - Use a straight edge and shim to determine approximated warp. Compared parts both un-mounted and soldered to PCB.
  - Keep steps between adjacent apertures to .02mm (1/2 mil) or less.