Overview Miniaturization on Large Form factor PCBA

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ABSTRACT
The world of electronics continues to increase functional densities on products. Many of the miniaturization technologies were developed for the consumer market with the smart phone specifically. Many designers in other areas such as infrastructure, medical, power, telecom, and other industries also desire to use similar components and are also looking at ways to miniaturize the product or increase the functional density.

This paper will explore some of the common miniaturization technologies and their application to larger form factor boards. Items such as 01005/0201 components, fine pitch CSP/QFN, component to component spacing, and package on package components will be explored through this paper.

Key items will be highlighted that will help designers and assemblers understand the advantages and disadvantages of using these various techniques on various board types. Items that are "easy" for a cell phone board may not be as easy on a network infrastructure board. There are many more components and items that need to be thought through and evaluated to determine if these miniaturization technologies are applicable.

Key words: Large Board, miniaturization, 0201, component spacing

INTRODUCTION
In today's fast moving world of consumer electronics, miniaturization has been a key element to enable smarter phones, wearable devices, and other technology advances. The miniaturization technologies used on the board assembly level include tighter component to component spacing (down to 0.100mm in some cases), use of package on package technology, finer pitches (direct flip chip down to 160um and CSP packages down to 0.3mm pitch). The use of these technologies has enabled greater functional density in the applications. When looking at the tear downs of many of the items, the PCBA is the smallest part of the overall system. Batteries and Displays in the smart phone take up most of the space within the mechanical assembly.

Advances in the assembly area have also enabled these capabilities and a trend of these miniaturization techniques are migrating to other products that typically have longer or harsher reliability requirements. Products such as server, storage and telecom would like to further increase functional density so would benefit from these technologies. However, there are some constraints to applying these technologies to these pcba types. Items like rework ability and the effects on the adjacent components need to be taken into account. This is a critical item as many of these products need to survive in the field upwards of 15-20 years. For the consumer level product 2-5 years is sufficient typically. For the various miniaturization technologies this paper will explore what is needed to use the technologies successfully and then explain some of the challenges that need to be addressed.

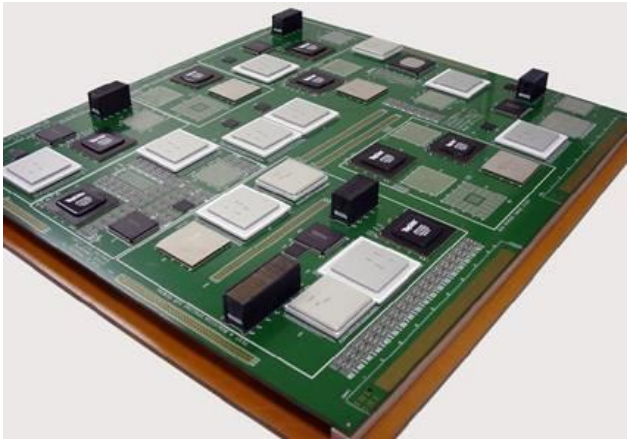


Figure 1

Miniaturization of Passive Components

As component packages continue to trend smaller, the office equipment boards, telecom, server, storage have usually not gone beyond the 0402 package size. In consumer electronics the trend is going beyond 01005 and down into m03015 or even m0201. A migration of traditional 0201 passive components is being seen, especially on rf types of boards.

The smaller components are desirable for the designers to help the signal integrity and also enable less amount of board real estate to be used.

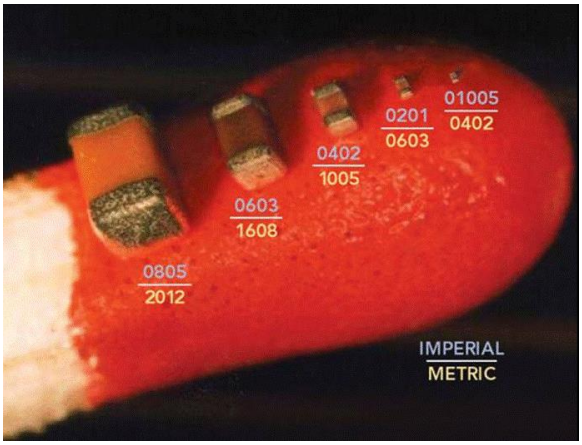


Figure 2

On these larger form factor boards overall real estate is not a main concern; however localized high density around critical circuits is required. In some cases, localized design rules are used for the high density areas. The processes for printing solder paste, placing the components, reflow and rework have all been developed many years ago, so now the challenges would be what are the effects of implementing the smaller packages onto these high value boards.

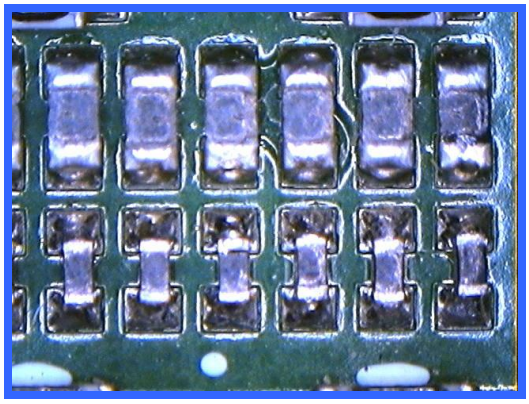


Figure 3: 0201 versus 0402 component on pcba

One of the key challenges in the process for 0201 on large form factor assemblies is the ability to print solder paste successfully. In many cases these boards were using 0.150mm to 0.125mm stencils while for the 0201 process it is ideal to use 0.100mm thick stencils. Solder paste particle size can help and the more common particle size being used today is type 4 especially for the high volume products. Also advances in stencil technologies with nano-coatings or fine grain stencils have helped create more consistent solder deposits and have helped reduce the area ratios that can be printed consistently.

A couple of solutions for applying 0201 onto the large form factor PCBA is to use a step stencil if 0.125/0.150mm is required for other components, the 0201 area can be stepped down to 0.100mm. However if the components are too close together then a step stencil may not be feasible. Then the solution can be to overprint the 0201s using the 0.125mm stencil and open the stencil aperture to allow for an area ratio around 0.6 to ensure good printability. In Figure 3 above a land pattern was designed to allow the use of a 0.150mm stencil to achieve a good print for the 0201 component. This pattern allowed high yields, however it did not take advantage of the actual 0201 space savings.

One other solution is to change the overall stencil to 0.100mm thick and only add more solder to the components that may need additional solder, such as connectors. A way to add more solder is to overprint the pad or pick and place a preform of solder onto the solder deposit. These techniques have been used for various solutions today.

Component to Component Spacing

Another area that the pcb designer would like to be able to do is to decrease the spacing between a BGA to the adjacent components. It is common to leave a spacing of up to 5mm between a BGA and the adjacent ICs. The main reason for this spacing is to allow for rework of the BGA without affecting the adjacent components which in turn could affect the overall reliability of the solder joints on the adjacent component. In the consumer products, this is not a concern as the long term reliability is shorter than the infrastructure or industrial type of products. The BGA rework process typically uses hot air through a nozzle that directs the heat to the targeted component however the heat spillover will affect the IC components next to it potentially causing partial reflow of the solder joint. (See Figure 4) The ideal condition is to prevent the adjacent component from reaching the reflow temperatures or ensuring that the full component solder joints see complete reflow temperatures.

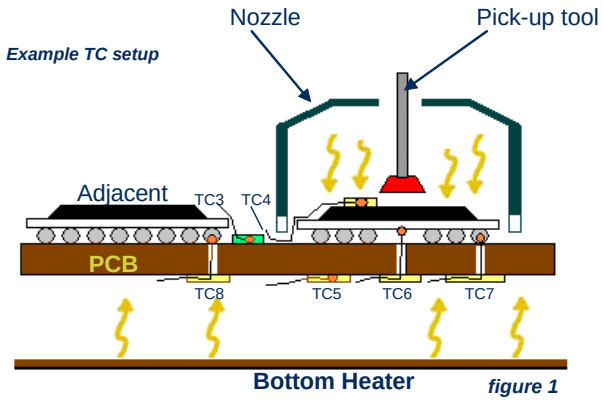


Figure 4: Conventional Setup for BGA rework

In order to allow closer component spacing between a BGA to another IC heat management needs to be resolved. Initial assembly of BGA to adjacent components is capable in the current manufacturing process. Spacing down to 0.250mm spacing can be achieved. This is commonly used for consumer level product where impact on rework ability is less of a concern.

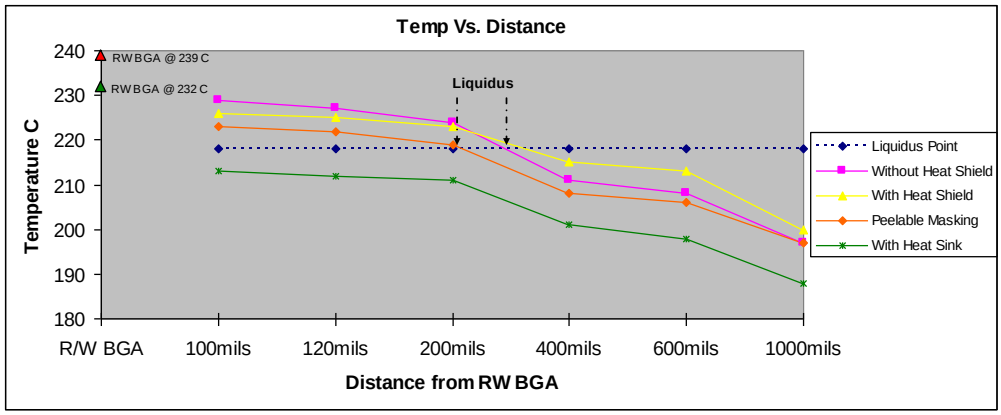
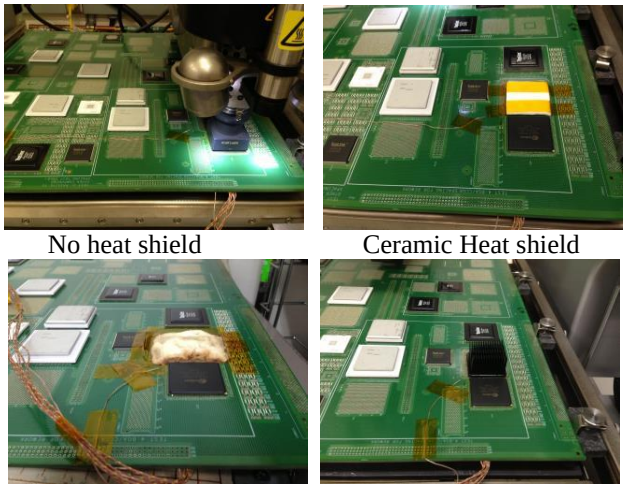


Figure 5: Peak Temperature versus Distance with various shielding.

Many techniques have been trialed to see which could be the best way to protect the adjacent components during the rework process. Figure 5 shows some results of a study performed to evaluate different shielding techniques. In this study no shielding, a heat shield made of ceramic filled material, a peelable solder mask over the adjacent components and a temporary heatsink were evaluated to see which would give the best results. Based on the data the temporary heatsink allowed the adjacent component down to 1.27mm (0.050") while allowing the solder joints of the target rework component to reach reflow temperatures.



No heat shield Ceramic Heat shield

Peelable Solder Mask Heatsink

Figure 6: Various Configurations

This ability to maintain the adjacent component temperatures below the reflow temperature can allow the BGA to IC components to be placed closer together in the designs. Further advances in rework technology will need to be pursued in order to help drive the component spacing down further. Most techniques today require some sort of fixturing in order to protect or have nozzles surround the device being reworked. Laser, Vapor Phase and other techniques are being explored to help move this technology even further.

For the passive components a lot of research has been done to place these components very close together. In consumer/miniaturized products the component to component spacing is down to 0.150mm and in some cases down to 0.100mm in limited areas. Figure 7 shows a spacing matrix of 0.125mm between 01005 and 0201 style capacitors.

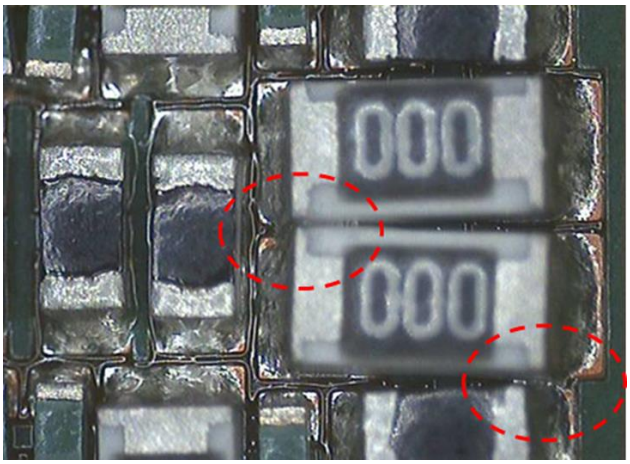


Figure 7: Component Spacing between 01005 and 0201 and 0402 components (100um)

In these cases printing is a key item to achieve good yields. In Figure 8 below it shows the yield of the various spacing versus the stencil thickness being used. A thinner stencil helps create a higher yield however at 0.250mm spacing good yields can be seen for the stencil thicknesses in the study.

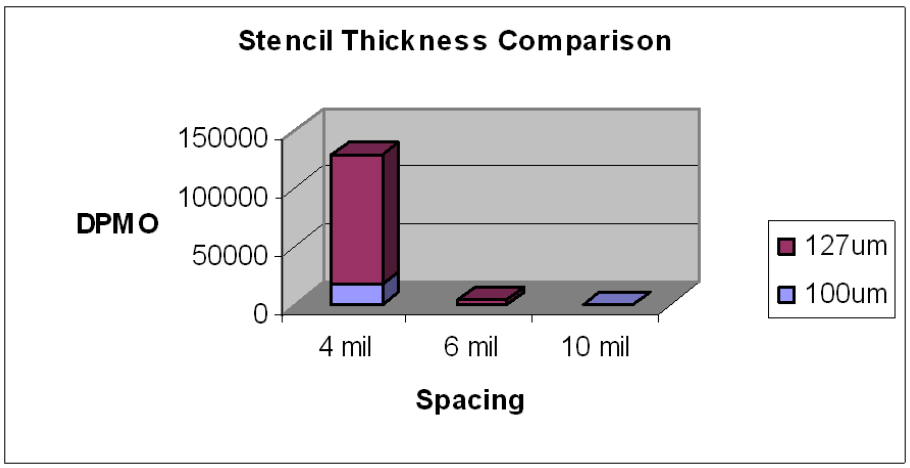


Figure 8: DPMO versus component Spacing versus Stencil thickness.

For larger form factor boards, components down to 0402 can still utilize a 125um thick stencil and still achieve component to component spacing down to 0.250um in localized areas.

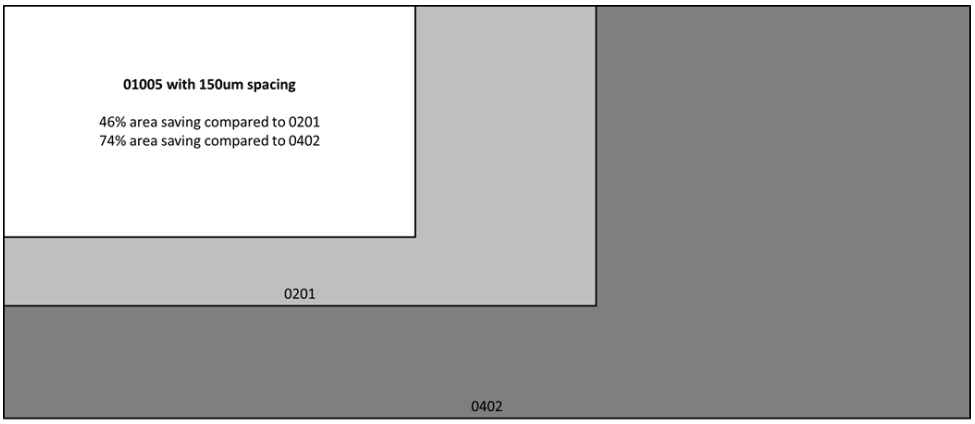


Figure 9: 0402 versus 0201 versus 01005 space taken

Some of the other key issues to be aware of is the placement sequences. In order to place the parts close together, the placement sequence needs to be able to place the shortest components first followed by the next shortest working the way up to the tallest components. This will help prevent the placement nozzle from disturbing the placement of the component already placed on the pcba.

FINER PITCH COMPONENTS

One last way higher density on a pcb can be obtained is through the use of components with finer pitch. Today the use of 0.4mm pitch bottom terminated components and chip scale packages are being used on the larger format boards. One reason they are being used has to do with the availability of these types of components. The consumer (smart phones and others) are using a large volume of the components such as memory which are also desirable to be used in server, storage and other infrastructure types of products. The same concerns exist on the finer pitches that currently have been discussed and that is the ability to print these fine pitches consistently. Moving to the thinner stencil help alleviate this concern and allows good consistent printing of solder paste to be able to be done.

Along with finer pitch components some designs want to use the package on package (PoP, Figure 10) technology where the packages are stacked during the SMT process. This process has been around for 10 years and is well understood.

Figure 10: Package on Package (PoP)

The key factors are the component warpage and the use of nitrogen in reflow to minimize the potential for open solder joints. One of the limiting factors is the lack of inspection techniques for these stacked solder joints. Current automated x-ray inspection systems are limited in the capability to inspect solder joints on a separate z plane. However, work is being done to address these issues. Inspection is a key element in the process to help ensure that the solder joints are robust for the long term reliability that the larger form factor products usually will have.

Another concern for the fine pitch process is the printed circuit board itself. With the unpredictable shrinkage of the pcbs, this can cause issues with the printing due to alignment of the stencil to the pcb. The stencil is typically made to the gerber and not adjusted for any shrinkage of the pcb after baking or reflow. The amount of shrinkage can cause the board pads to no longer align to the stencil apertures. One way this is overcome is by creating a stencil based on the batch of pcb received and adjusting the fabrication of the stencil to match those pcbs. The pick and place can make adjustments to the x,y position based on the fiducials and apply a scaling. The stencils do not have this ability as they are fixed and the only alignment that can be done is to create a best fit location based on fiducials. In some cases the outer components can be misaligned in the stencil print process.

SUMMARY

There are many techniques that have been used in consumer type of products for miniaturization. These are now migrating into infrastructure and industrial products as increasing functional density is still a driving factor in the design of products. Miniaturization in component size, finer pitches, stacked packages, and closer component spacing is capable of being used as long as the challenges are understood and can be addressed for a particular project. The trend will continue to create more density on the PCBA and with further desire to utilize miniaturization technologies. Another key not covered in this paper would be test and inspection technologies.

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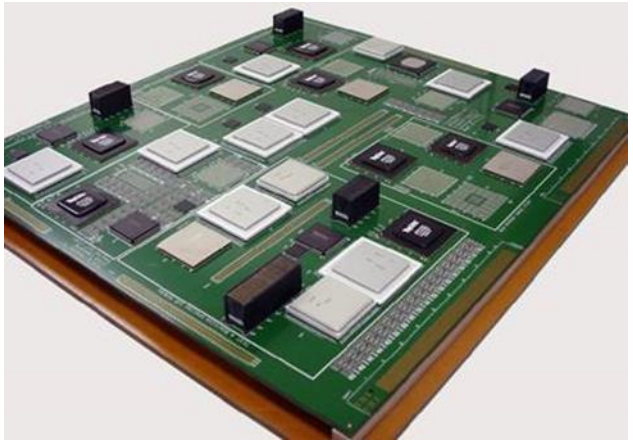
Outline/Agenda

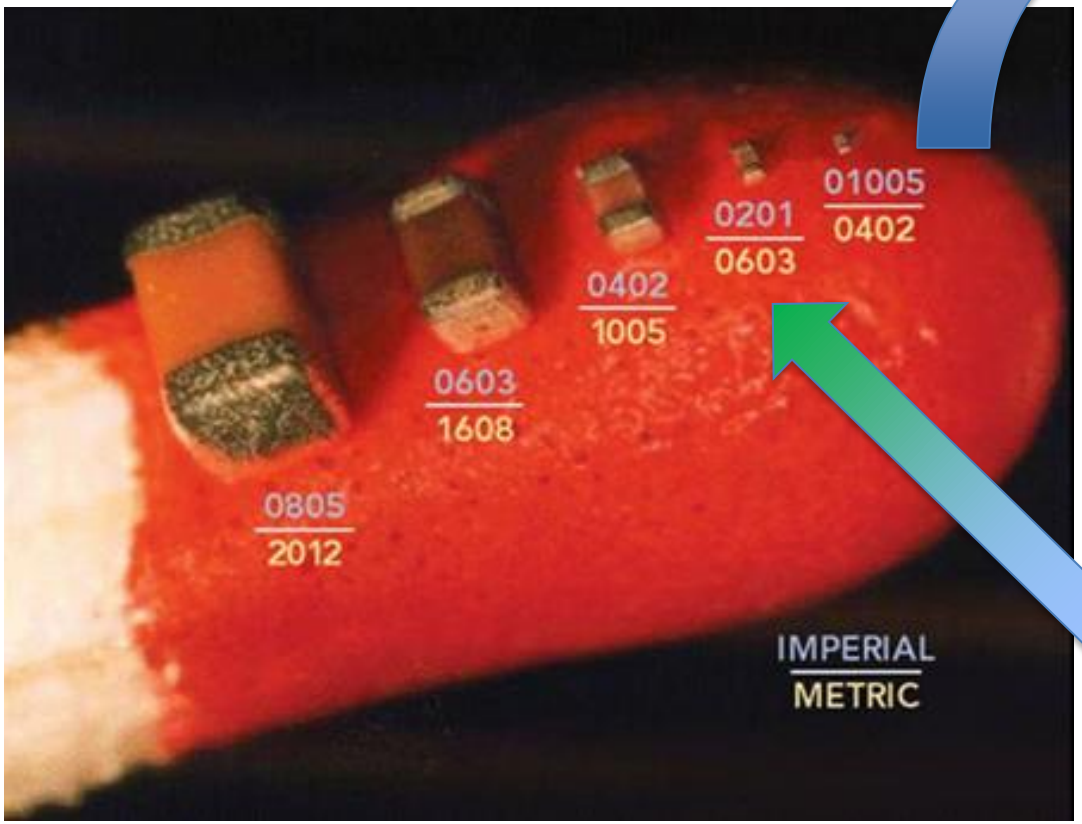
- Introduction
- Miniaturization of Passive Components
- Component to Component Spacing
- Finer Pitch Components
- Summary

Introduction

- Miniaturization continues to be a main driver for PCBA
  - Smart devices lead the way in miniature technologies
- Increasing functional density
  - x, y, & z
- Technologies migrating to larger form factor pcba
  - High volume components are used in the smart device
  - Same components are wanting to be used by designers in the larger form factor assemblies



Miniaturization of Passive Components

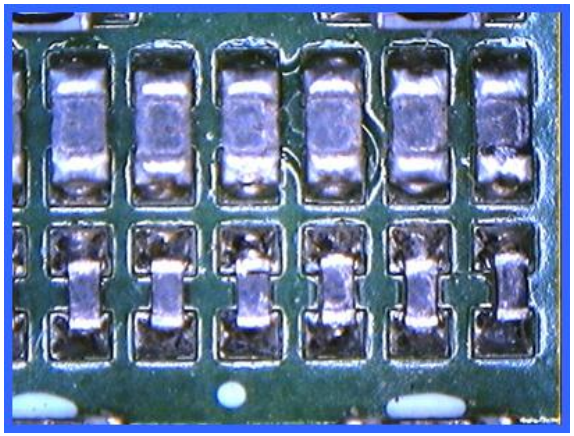


Smart Devices
- M03015
- M0201
- ??

Large Form factor designs

Miniaturization of Passive Components

- Smaller is better
  - Better electrical, less space, less mass
- Challenges on larger form factor pcba
  - Board shrink during reflow moves the actual position of the component pads. This leads to alignment issues of the stencil for paste printing.
  - Smaller aperture can lead to printability issues. Requires solder paste that prints well and stencils that release the solder paste well.
  - Various combinations of solder volumes may need to be managed



0402 versus 0201 on a large form factor PCB

Component to Component Spacing

- BGA to other component spacing
  - On large form factor, not uncommon to see 5mm spacing to allow for tooling clearances
  - Concern about adjacent components going through partial reflow
    - Either completely reflow or do not reflow the solder joints

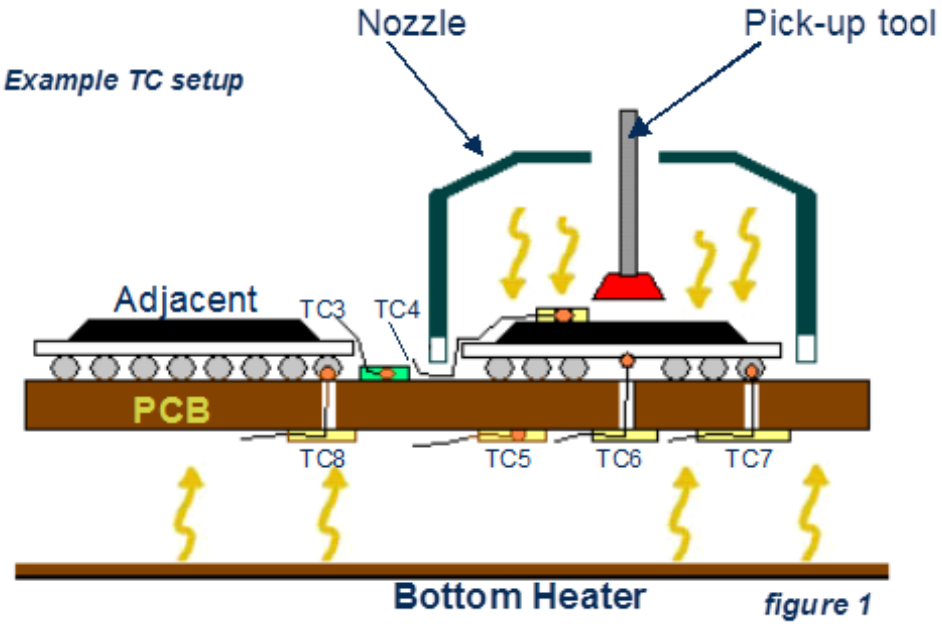
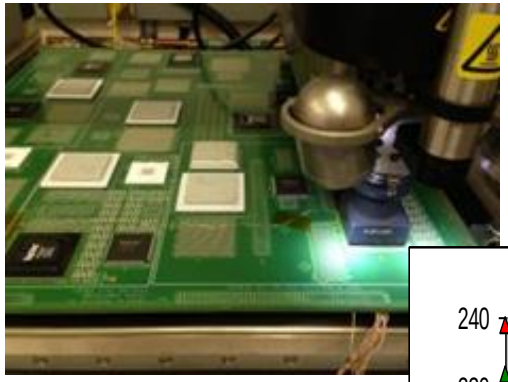
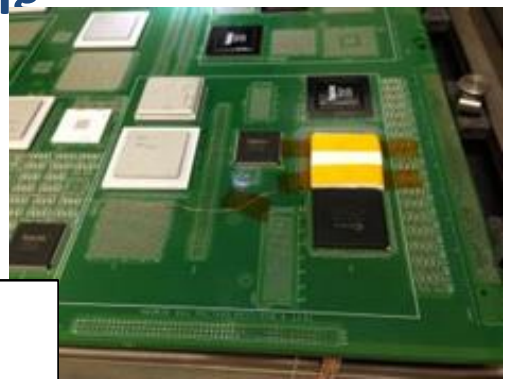


figure 1

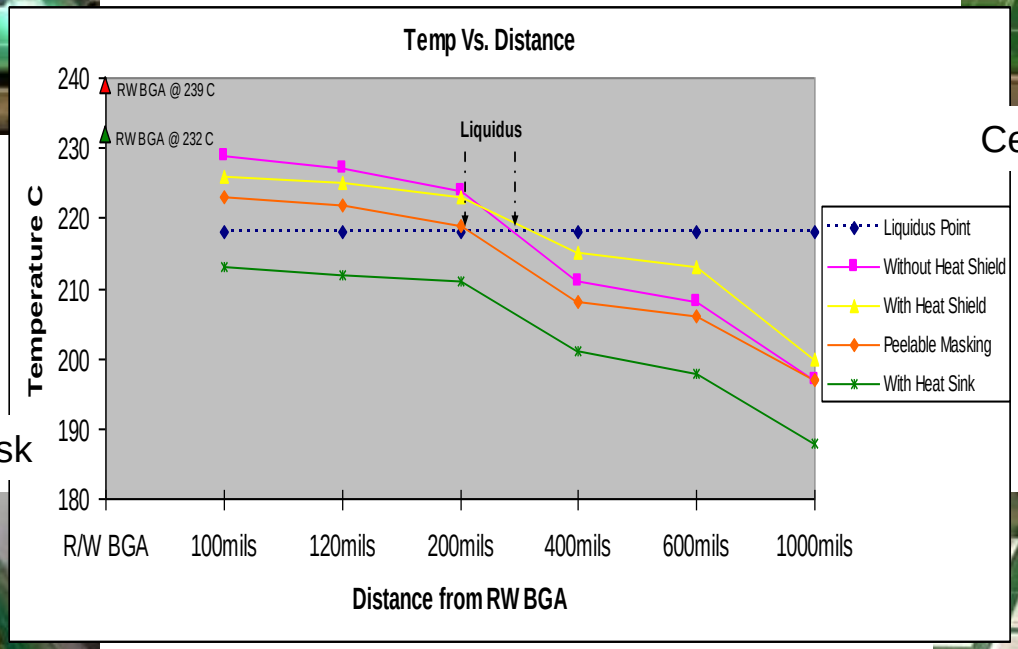
Component to Component Spacing



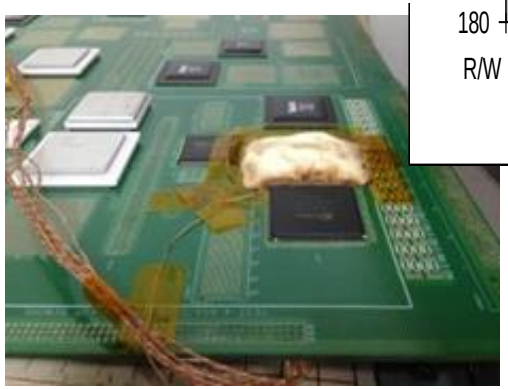
No Shielding



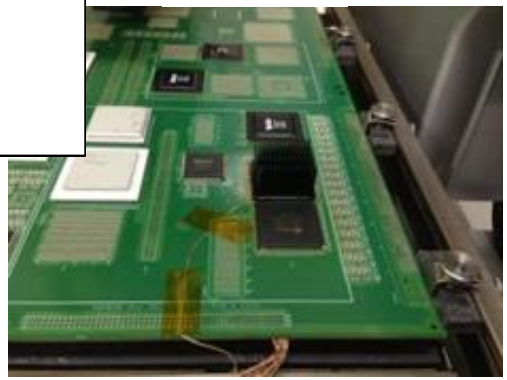
Ceramic Based Heat Shield



Peelable Solder Mask

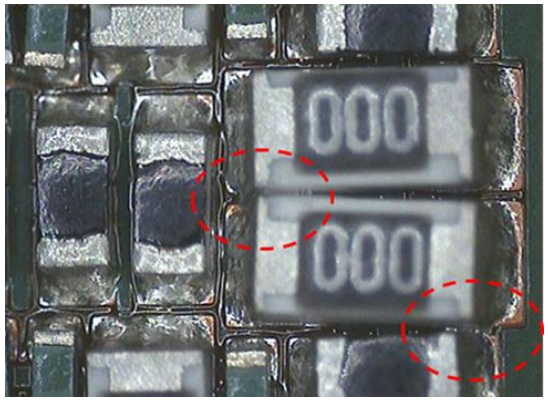


Heatsink



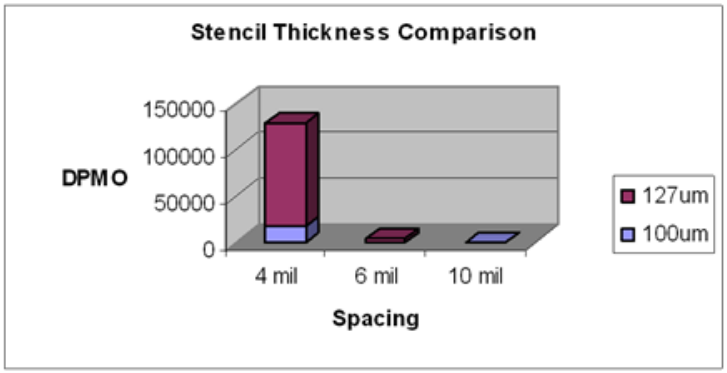
Component to Component Spacing - Passives

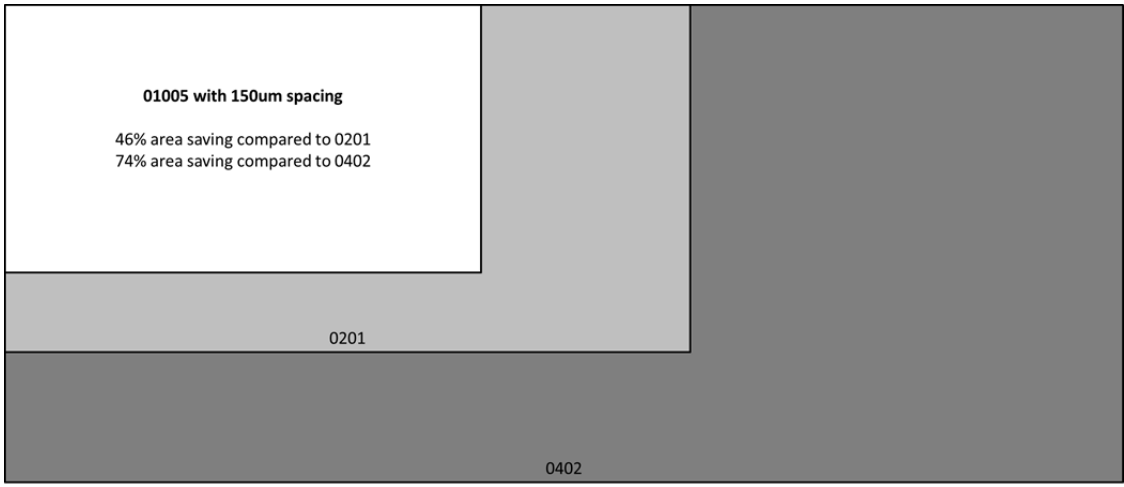
- Closer is better
  - Better electrical, less space
  - Component to component spacing is down to 0.150mm and in some cases down to 0.100mm in limited areas on Smart Devices
- Challenges on larger form factor pcba
  - Board shrink during reflow moves the actual position of the component pads. This leads to alignment issues of the stencil for paste printing.
  - Smaller aperture can lead to printability issues. Requires solder paste that prints well and stencils that release the solder paste well.
  - Printing is a key item to achieve good yields



Component to Component Spacing - Passives

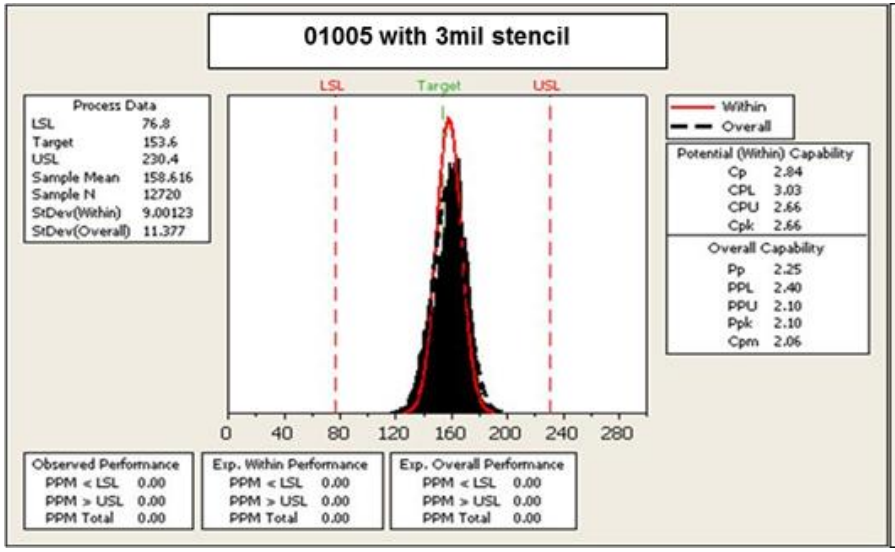
- A thinner stencil helps create a higher yields
- Components down to 0402 can still utilize a 125um thick stencil and still achieve component to component spacing down to 0.250um in localized areas
- The placement sequence needs to be able to place the shortest components first followed by the next shortest working the way up to the tallest components

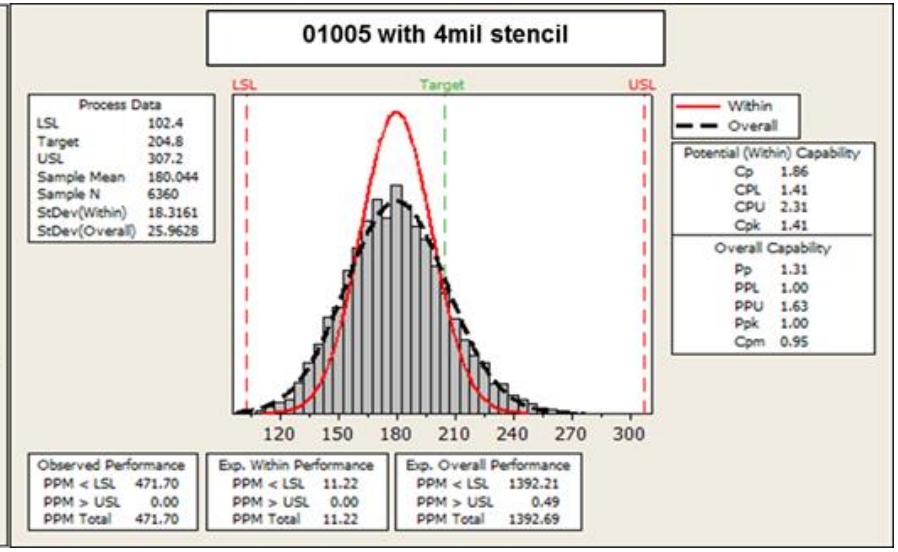




Paste Volume and Variations

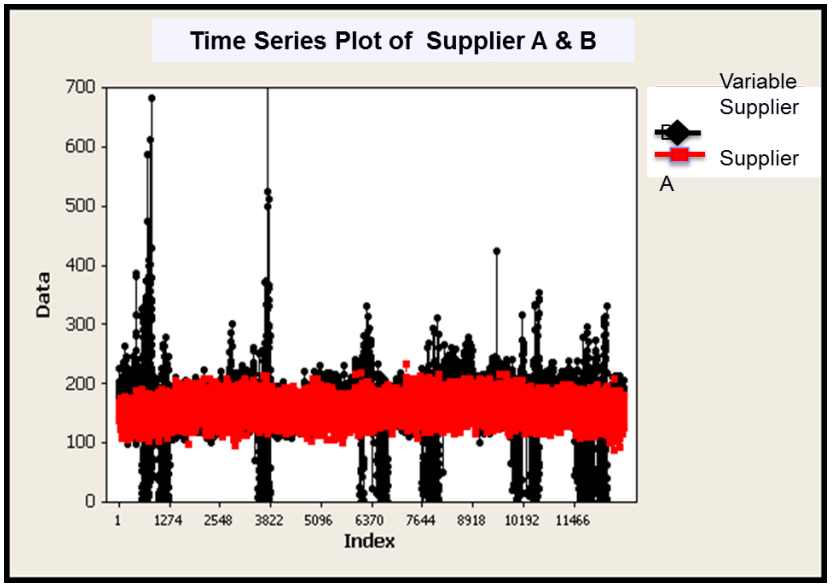
- Area Ratio for 75um stencil = 0.66
- Area Ratio for 0.100mm stencil = 0.5
- Wider variation with the lower area ratio
- For the 75um stencil 0 defects were seen in the printing
- For the 100um stencil a print DPMO of 1382 on the 01005s, these were sent through the rest of the process

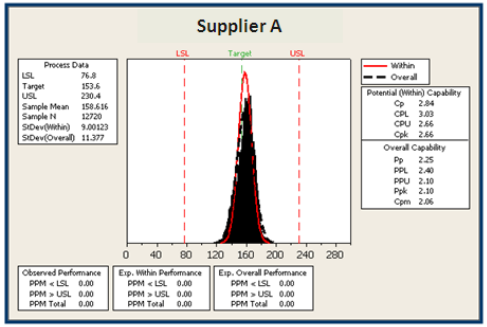
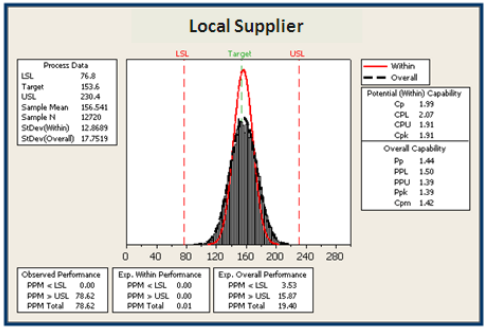




Component to Component Spacing - Passives

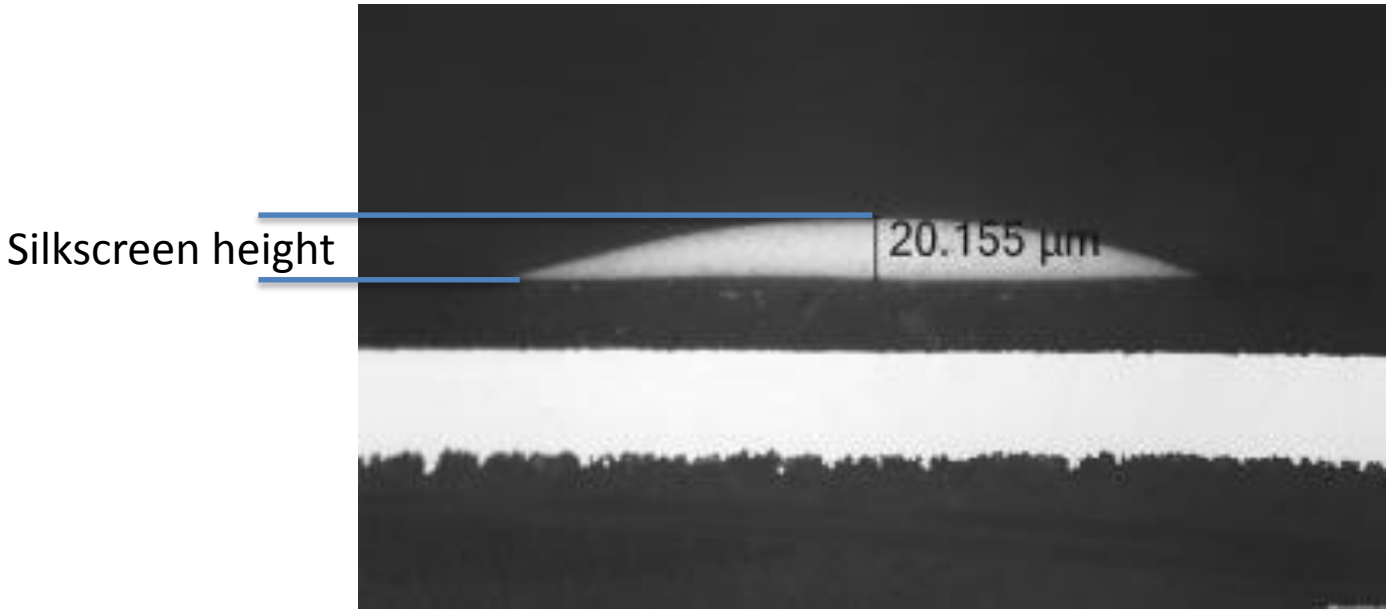
- Stencil technology will effect printability
- Solder paste selection can also effect printability



Screen Printing	
Supplier A (high end laser cut and coated)	Laser cut local supplier (Doumen)
	
Pp=2.25, PpK=2.06	Pp=1.44, PpK=1.42

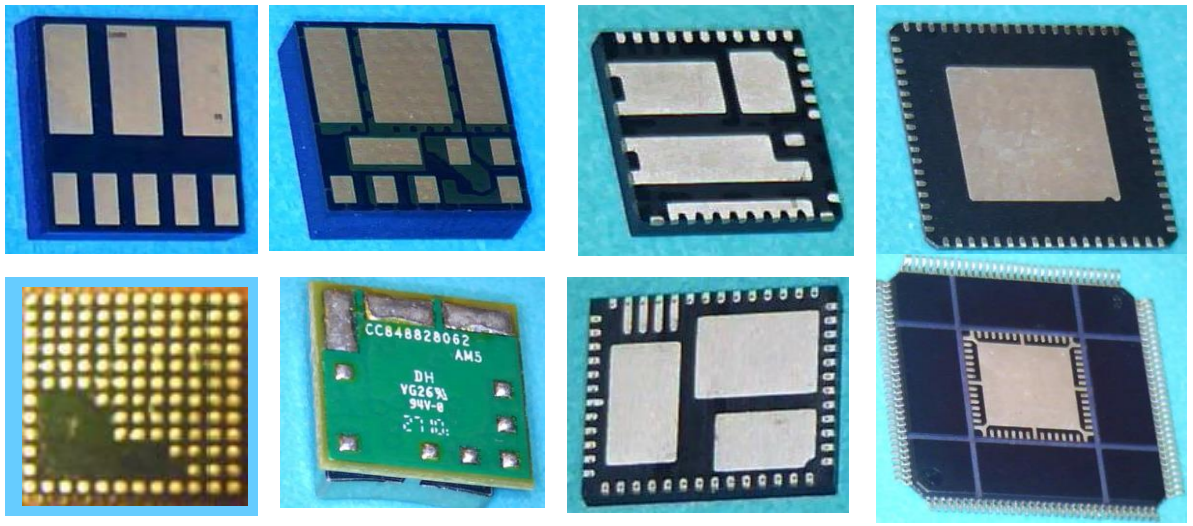
Component to Component Spacing - Passives

- Silkcreen will effect the printability of fine spacing, fine pitch components
- On miniaturized product, silkscreen is almost always not applied



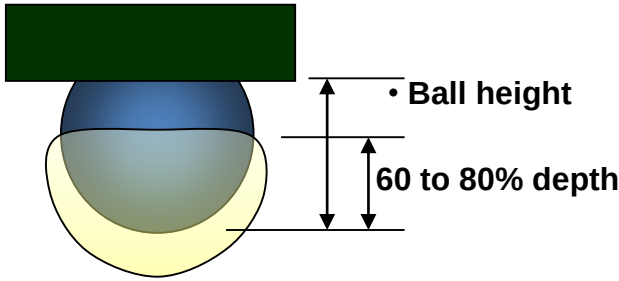
FINER PITCH COMPONENTS

- Use of 0.4mm pitch bottom terminated components
- 0.8mm chip scale packages are being used on the larger format boards
- 0.5mm pitch CSP are starting to see increase in usage
- Moving to the thinner stencil help alleviate this concern and allows good consistent printing of solder paste to be able to be done

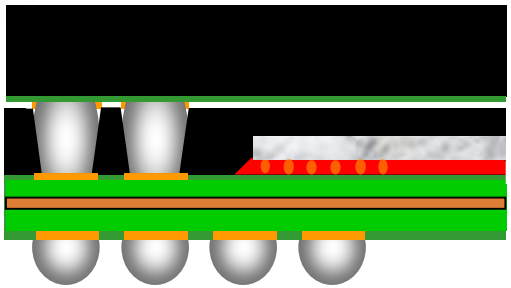


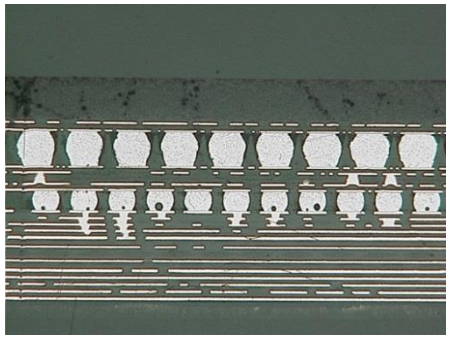
FINER PITCH COMPONENTS

- Use of PoP (package on package) components
- Adds flux dipping process to an SMT Line
- Well understood
- >10 years in industry
- Requires nitrogen reflow for highest yields



Dipped in Paste





Summary

- Various methods available for miniaturization
  - Miniaturization of passives
  - Component Spacing
  - Fine pitch components
- Most share the same issues in printing solder paste to ensure good yields
  - Stencil and paste technology will help enable these
- Other technologies not mentioned
  - Embedded components

Thank you for your attention!