Effect of Permittivity and Dissipation Factor of Solder Mask upon Measured Loss

Hao He
Senior Engineer, Non-aviation Industry Development Department
Aviation Industry Co.
Beijing, China
Rongyao Tang
Signal Integrity Engineer, R&D Department
Shennan Circuits Co., Ltd.
Shenzhen, China
Email: rytang@fiberhome.com

Abstract
Existing coated microstrip trace impedance estimation usually uses the dielectric constant (Dk) of solder mask ink measured at 1 MHz from its datasheet. Or, some printed circuit board (PCB) manufacturers tend to first calculate the impedance of surface microstrip line and multiply this value by an empirical coefficient such as 0.94 or 0.96 to get the impedance of coated microstrip line. In addition, PCB engineers always underestimate the loss caused by solder mask upon microstrip line (conductor-backed coplanar waveguide in this paper) of flexible printed circuit (FPC) or server PCB. However, as signal speeds move into the 10 Gbps range, standard FR-4 is gradually being replaced by low dissipation factor (Df) material like modified FR4 or PPO and the Df gap between laminate and solder mask is huge. Thus, it is significant to evaluate the effects of solder mask in 3D modeling and EM simulation. This paper describes a set of methods to extract the permittivity and dissipation factor of a standard and a low- loss solder mask ink. The measured S parameters have been de-embedded by AFR (Automotive Fixture Removed) calibration method. When modeling, copper surface roughness has been considered.

Introduction
When a SI engineer is working on EM simulation, an accurate model of a long transmission line carrying 1Gbps or above high-speed signal is essential. Except for the correct geometrical parameters, the dielectric properties of laminate materials and copper roughness which directly affect impedance and insertion loss are rapidly becoming crucial to maintain modeling accuracy. There have been many papers discussing influence mechanisms and modeling methods for laminate materials and copper foil roughness [1][2][3]. However, few researches [4] are focused on dielectric properties of solder mask and its effects on attenuation. As a necessary parameter in impedance calculation and loss prediction, the existing industry-standard Dk and Df of solder mask from vendor's datasheet is measured at 1MHz [5] and inadequate to maintain required levels of signal integrity on FPC and server PCB. This paper describes a method to extract the permittivity and dissipation factor of an ordinary and a low-loss solder mask ink.

Description of Used Solder Mask
The term solder mask, as used in this paper, is the same as the terms solder resist or soldermask, which are frequently used interchangeably in the PCB fabrication industry. It is a heat-resistant coating material applied to selected areas to prevent the deposition of solder upon those areas during subsequent soldering [6]. Although solder mask comes in different media depending upon the demands of the application, it is usually a mixture of solvents and polymers. Thus, there are many inclusions (filled with Si, Br, Cl, Mg, Ca, and O) in the solder mask to scatter and absorb electromagnetic power [3].

As a kind of dielectrics, polymer in solder mask has two important dielectric properties, the relative dielectric constant (Dk) and the dissipation factor (Df). The former describes how dipoles re-align in an electric field to increase capacitance and how much the material will increase the capacitance between two electrodes and the speed of light in the material while the latter describe how the dipoles slosh back and forth and contribute to a resistance with current that is in phase with the applied-voltage sine wave [7]. Therefore, we chose a conventional solder mask with Dk 4.5 @1MHz and Df 0.025 @1MHz and a new low loss solder mask with Dk 3.6 - 3.9 @1GHz and Df 0.0069 - 0.0079 @1GHz.

Description of PCB Test Vehicle
A PCB test vehicle designed and fabricated by the company for conductor-backed coplanar waveguide electrical property investigation is shown in Figure 1.

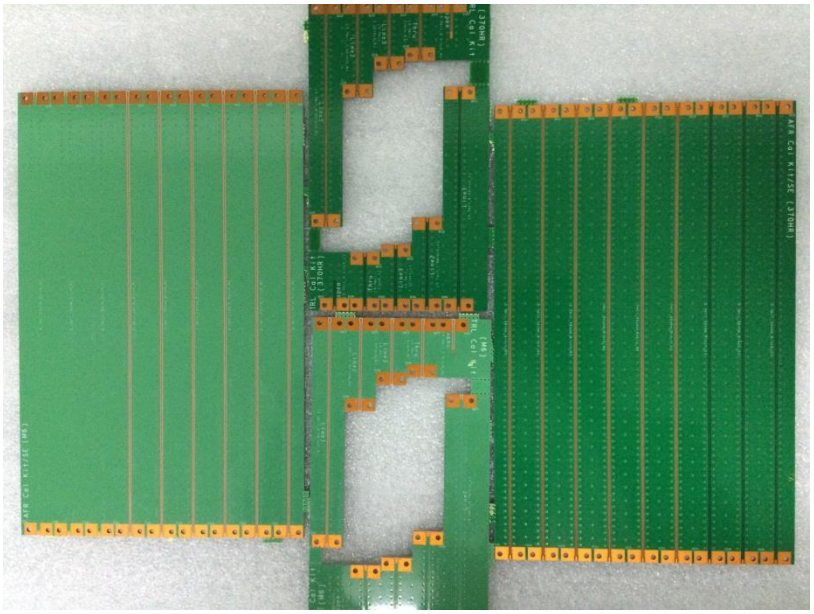


Figure 1 - Overview of the test vehicle

Two kinds of dielectric material, standard loss epoxy hi-temp FR-4 and very low loss PPO blend, are used in two 10-layer stack-ups respectively (shown in Figure 2). To minimize pressed dielectric thickness variation and extra losses introduced by copper roughness, we imposed a core rather than the prepreg with reverse-treated foil (RTF) as the structure of top and second layer.

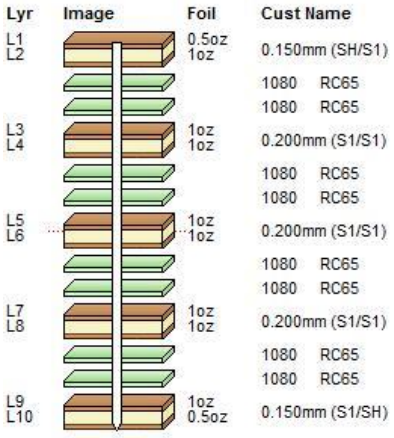


Figure 2 - Stack-up used for Epoxy FR-4 and PPO Blend Resin Systems

Except for top layer, the other 9 layers have no traces and add dummy pads instead. The test trace length is 210 mm while a trace of 25.4mm length is served as a through standard for AFR de-embedding. The test traces, designed as conductor-backed coplanar waveguide, are all tuned for target impedance of 50 ohms and divided into two parts: some are bare without any surface finish and the others are covered by solder mask. Due to solder mask, the bare copper traces are nearly 30 um wider than the coated ones.

To minimize copper thickness variation, a chemical metallization process named Electroless Copper, which was proved with +/- 5um variation at most over the whole panel, was utilized as compared to normal plating process. Before solder mask process, the semi-manufactured boards were separated to cover standard solder mask ink (labeled as SM-A) and low Dk and Df ink (labeled as SM-B). To compare with normal conductor surface finish, several test vehicles were further applied electroless nickel immersion gold (ENIG) and Immersion silver processing.

Description of Test Equipment and Technique

The instrument used for loss measurement is a four-port vector network analyzer, rated to 20 GHz, equipped with 2.92 mm

cables, 48” (1.22m) in length, rated to 40 GHz. To ensure excellent electrical connection, the production probe station is used together with two production microwave probes.

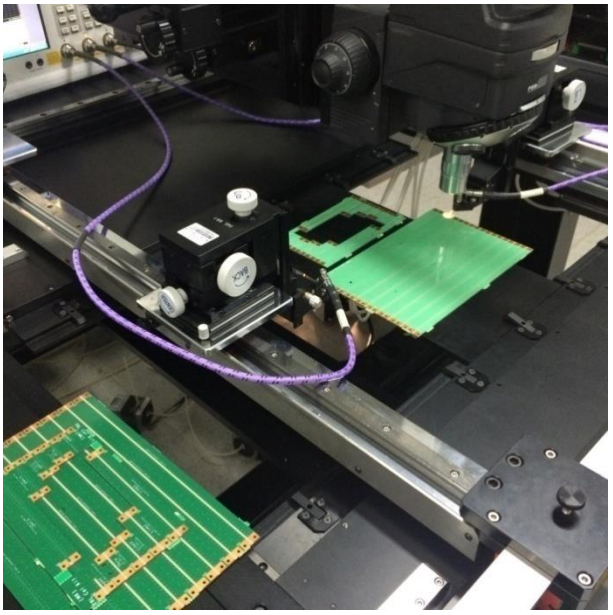


Figure 3 - Overview of VNA and Probe Station test platform

The Calibration of a VNA is required in order to de-embed the loss, phase lag and other effects induced by the cabling and connectors. Electronic Calibration (Ecal) technique is used for removing cable effects and AFR is used for removing probe effects [8].

Ecal modules can support many of the calibration acquisitions including the default type of unknown thru. A 12-term error correction could be acquired from the actual values of the reflection states as well as the S-parameters of the thru state in the Ecal module, which is very repeatable and stable because of the solid-state electronic switches inside. AFR makes use of time domain measurements on PCB fixtures to compensate for input and output mismatch, as well as loss, even if the input and output mismatch are not the same [9]. It has been proved as accurate as TRL calibration for the high-speed interconnect characterization up to 40 GHz [10].

Measurement Results

The loss measurements were done by sweeping frequency from 20 MHz to 18 GHz, capturing a total of 900 discrete measurement points over the frequency range. As another sanity check, the reflection loss was below -20 dB up to 18GHz. As FR4 material and solder mask are both sensitive to moisture, we heated the test vehicles in high temperature oven at 160℃for several hours. The S21 results comparison of standard loss epoxy hi-temp FR-4 test vehicles before and after heating are shown in Figure 4. Thus, the data discussed below are all measured on boards heating for at least four hours.

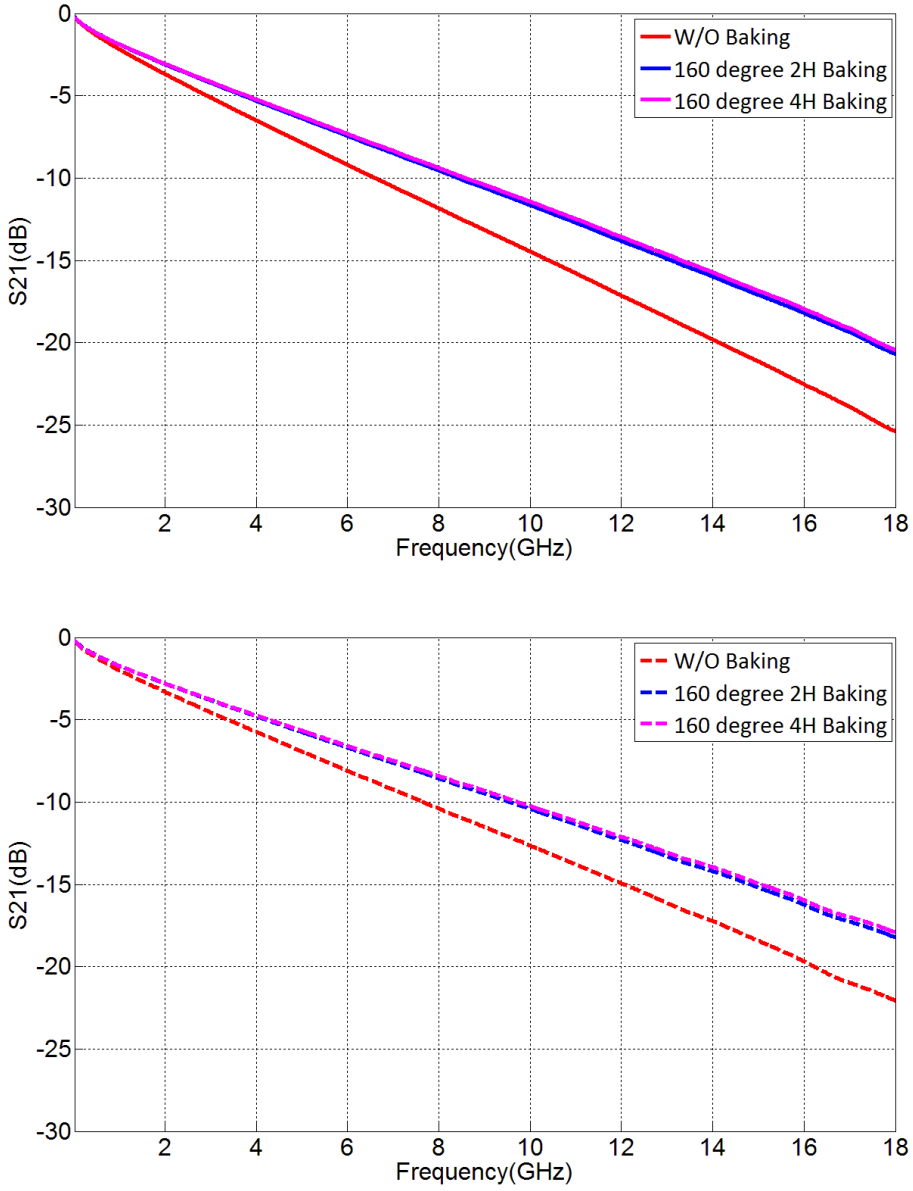


Figure 4 - S21 measurements for 8.265 inch long traces on epoxy FR-4 test vehicles (above: with solder mask SM-A; below: without solder mask)

The de-embedded S21 / loss measurements of all the traces are shown in Figure 5. As expected, there is a great discrepancy between bare and solder mask coated trace losses, since solder mask introduces more dielectric losses especially for ultra-low loss dielectric PPO blend material. For epoxy FR-4, there is no obvious advantage for low loss solder mask (less than 5% decrement in loss) when compared with standard formal solder mask. However, the difference becomes very considerable (up to 10% decrement in loss) when the loss comparison is established for PPO blend material, which features very low Df at a level approaching that of older systems based on PTFE or polybutadiene.

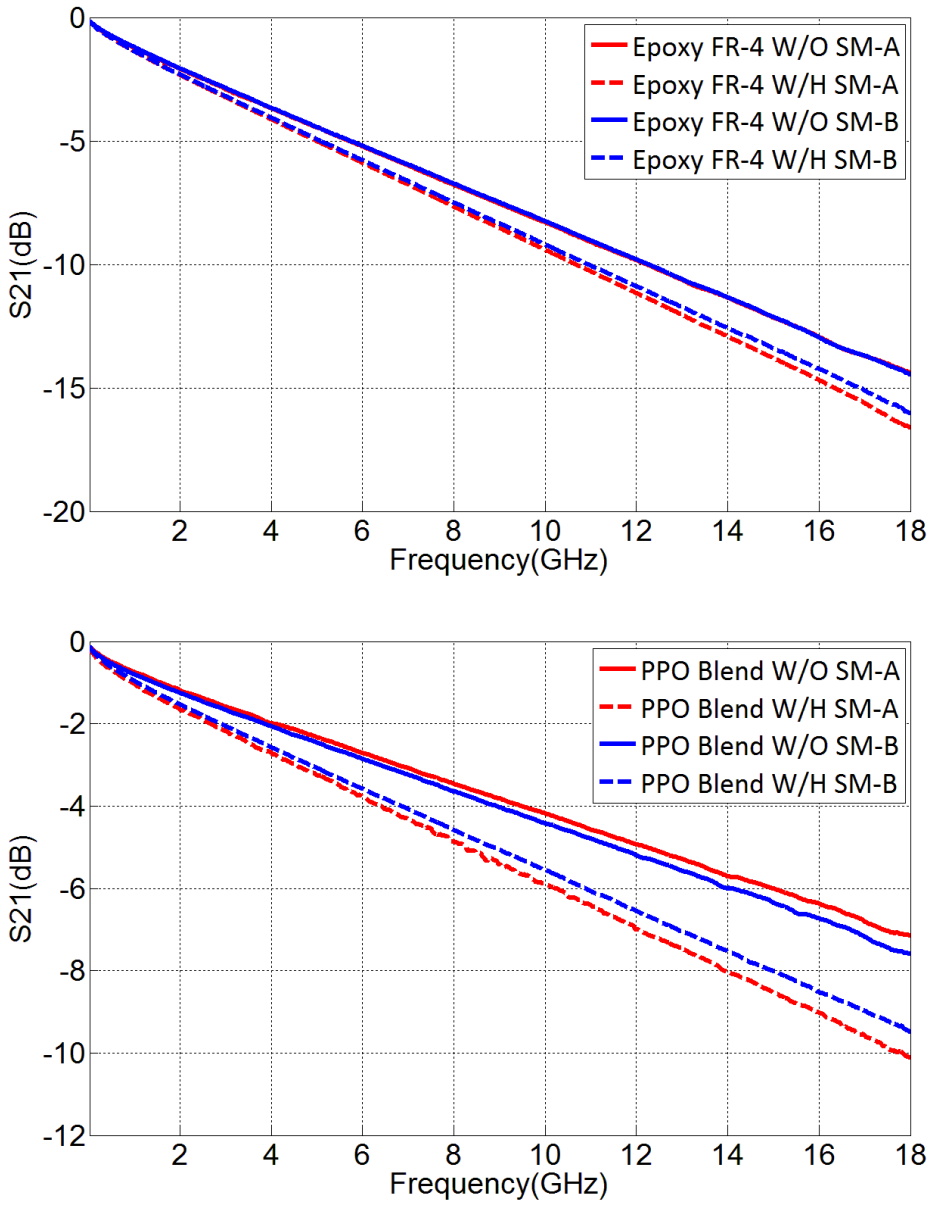


Figure 5 –De-embedded S21 measurements for7.265 inch long traces with and without solder mask (above: Epoxy FR-4; below: PPO Blend)

Figure 6 indicates the loss and group delay comparison between the bare copper line and line with surface finishes. With the increase of the frequency, the signal losses of the conductor-backed coplanar waveguide with surface finish increase. The maximum loss is the trace plated with ENIG while the trace with immersion silver has nearly the same loss as the bare trace. The resonance at 2GHz visible on measured ENIG insertion loss as well as on group delay graphs has been attributed to ferromagnetic properties of the nickel layer in [11].

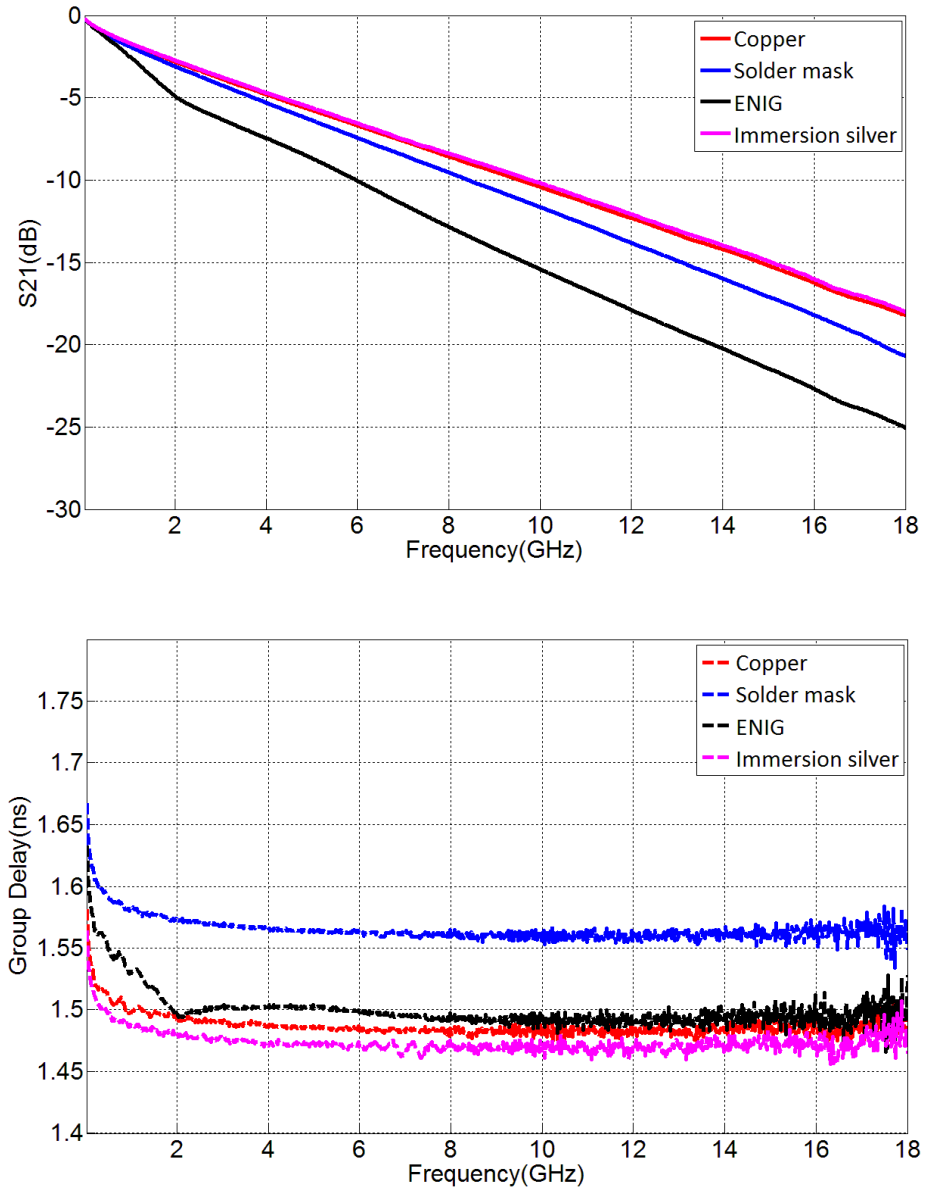


Figure 6 - S21 and delay measurements for 8.265 inch traces with different surface finishes (above: S21; below: group delay)

Extraction of Dk and Df for Solder Mask

We use the causal Djordjevic-Sarkar model [12] to characterize all dielectrics with parameters defined at 1 GHz in a 3-D field solver. Copper roughness effect was also considered as Huray model [3] on both sides of the outer layer trace. The cross-sectional geometrical-mean data of 5 cross-sections for each single trace are summarized in Table 1. An example of the micro-photograph, the basic dimensions of a test trace cross-section and 3-D field solver model with and without solder mask are shown in Figure 8. The conductivity of annealed copper was set to 5.8E7 S/m for both conductor and reference planes. The identified dielectric and roughness parameters used in the 3-D field solver model are summarized in Table 2.

Table 1 – Micro-section geometry of each measured trace

Test Vehicle	W1/um	W2/um	H1/um	T1/um	TSM1/um	TSM2/um
Epoxy FR-4-SM-A-NSM	192.9	161.8	99.5	51.5	-	-
Epoxy FR-4-SM-A-SM	158	124.6	99.4	50.5	20	42.89
Epoxy FR-4-SM-B-NSM	182	158	100.4	46.7	-	-

Epoxy FR-4-SM-B-SM	151.6	125.4	98	45.2	25	68.31
PPO Blend-SM-A-NSM	206.1	175	97.5	56.2	-	-
PPO Blend-SM-A-SM	172	135	96	53.3	34	63.13
PPO Blend-SM-B-NSM	195.2	170.4	97.8	55.3	-	-
PPO Blend-SM-B-SM	164.7	136.8	97	47.8	27	72.54

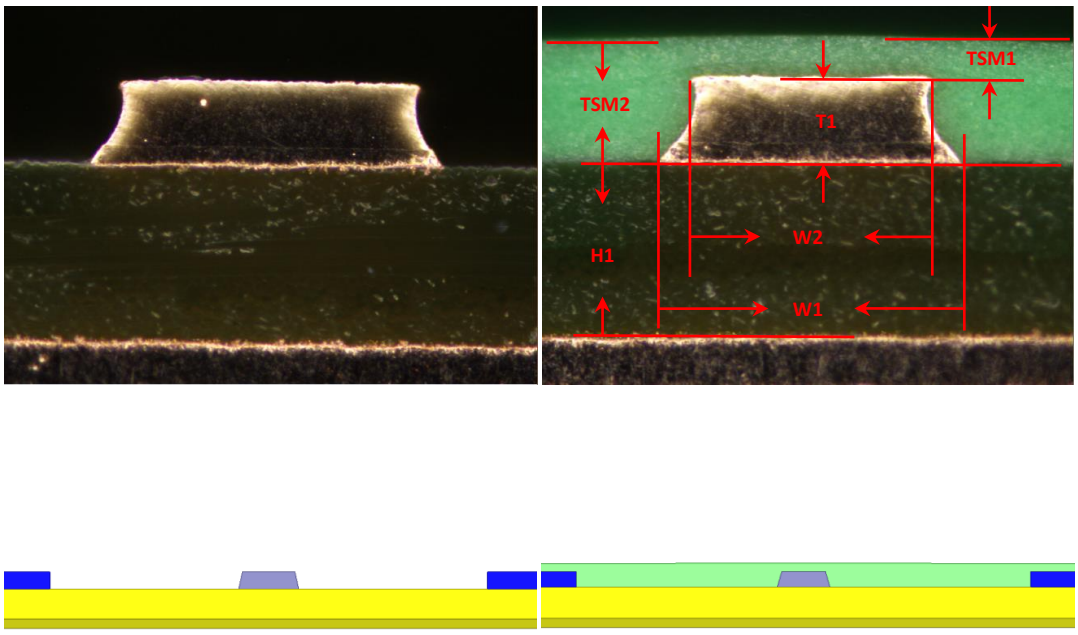


Figure 7 - Micro-photographs of cross-sections and 3-D Model views for measured traces (left: without solder mask; right: with solder mask)

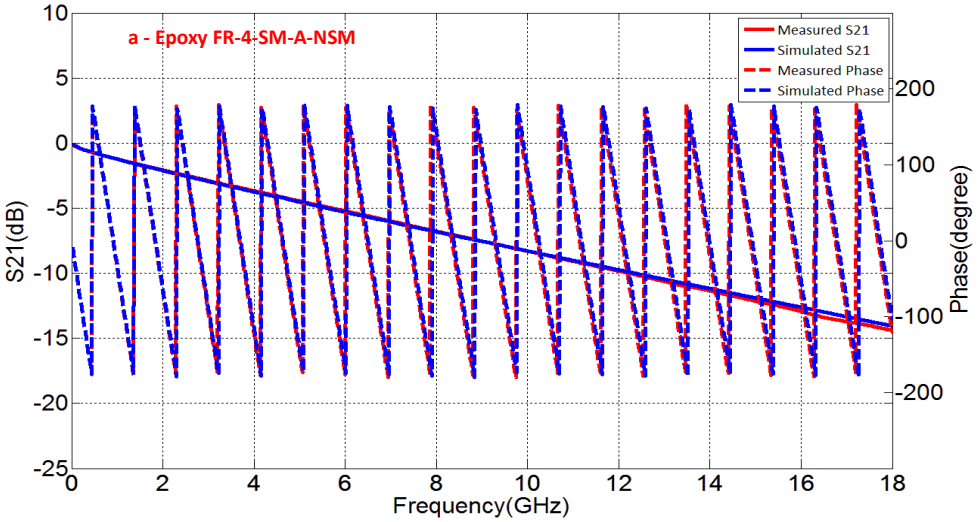
Table 2–Identified Djordjevic-Sarkar dielectric model and Huray conductor roughness model for each trace

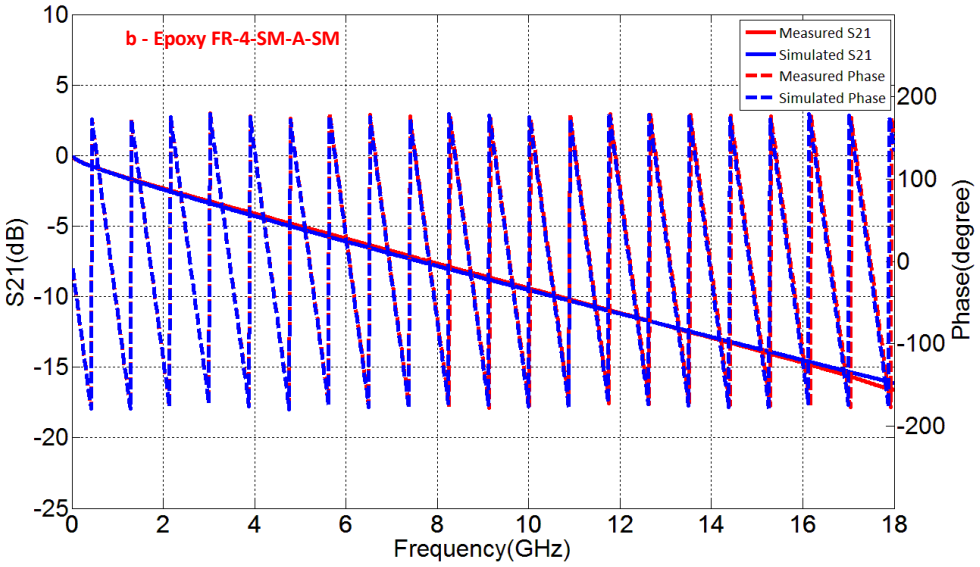
Test Vehicle	Dielectric Laminate		Solder Mask		Copper Roughness on both sides	
	Dk@1GHz	Df@1GHz	Dk@1GHz	Df@1GHz	Nodule Radius	Hall-Huray Surface Ratio
Epoxy FR-4-SM-A-NSM	4.3	0.02			0.15	8.8
Epoxy FR-4-SM-A-SM	4.3	0.02	4.3	0.025	0.15	8.8
Epoxy FR-4-SM-B-NSM	4.34	0.02			0.15	8.8
Epoxy FR-4-SM-B-SM	4.34	0.02	4.35	0.012	0.15	8.8
PPO Blend-SM-A-NSM	3.83	0.0045			0.15	8.8
PPO Blend-SM-A-SM	3.83	0.0045	4.3	0.025	0.15	8.8
PPO Blend-SM-B-NSM	3.92	0.0045			0.17	9
PPO Blend-SM-B-SM	3.92	0.0045	4.35	0.012	0.17	9

Since the minimum of three parameters required for the model can only be defined if detailed micro-photographs of the surface are available, Huray's snowball model parameters cannot be computed from the profilometer measurements mainly [13]. We didn't need accurate Huray's model defined from the physical structure of the surface since our main purpose for Dk and Df

extraction of solder mask. Thus, we chose to simply optimize the Huray roughness model parameters to achieve good correspondence with the original measured data (minimize the error between measured and simulated S-parameters).

Figures 8(a), (b), (c) and (d) show magnitude and phase of insertion loss for de-embedded 7.265 inch long traces with and without solder mask for the Epoxy FR-4 boards, respectively.





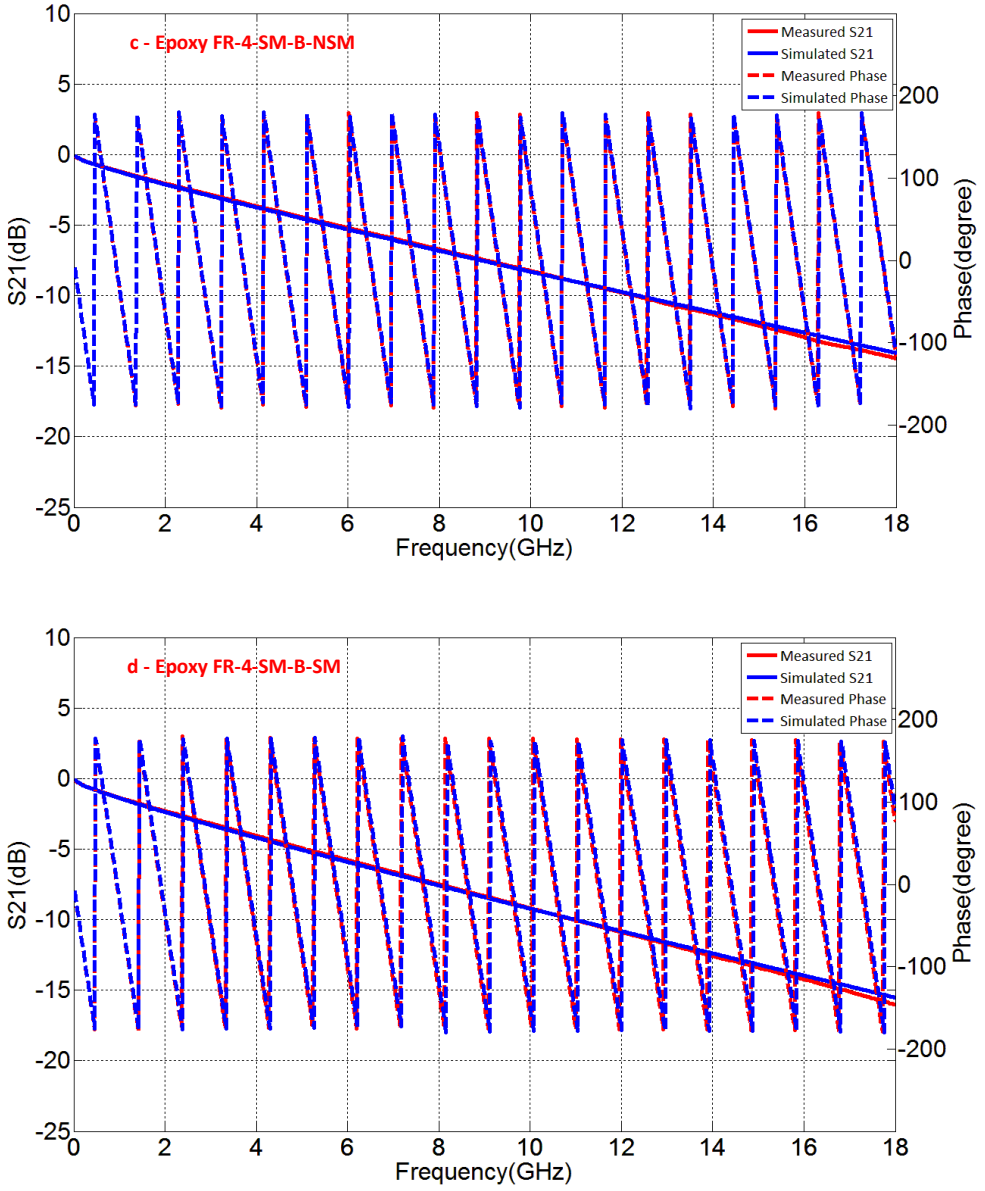
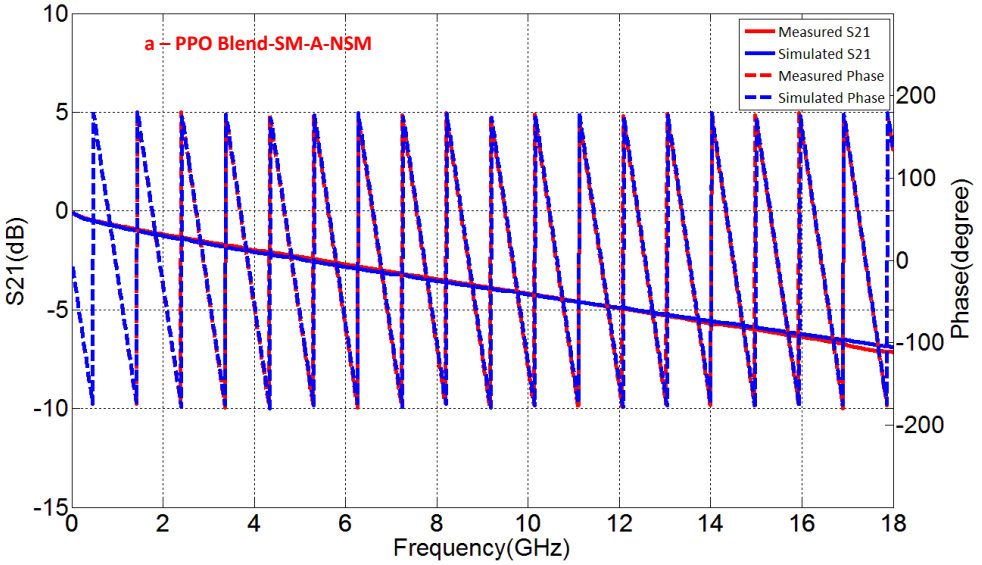
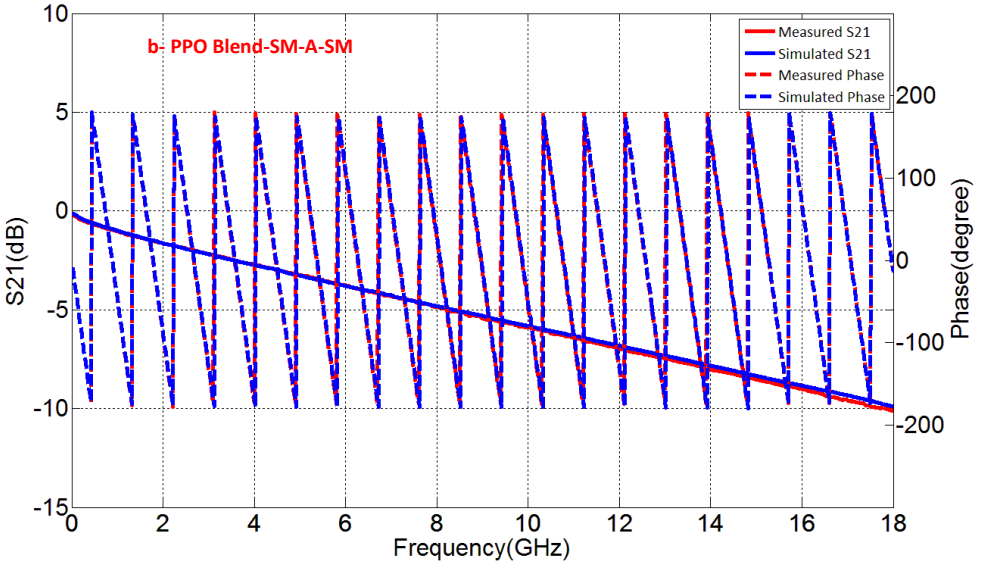


Figure 8– Measured and simulated S21 and phase data of the de-embedded traces on Epoxy FR-4 TVs (a: without SM-A; b: with SM-A; c: without SM-B; d: with SM-B)

Figures 9 (a), (b), (c) and (d) show magnitude and phase of insertion loss for de-embedded 7.265 inch long traces with and without solder mask for the PPO Blend boards, respectively.


a – PPO Blend-SM-A-NSM
Measured S21
Simulated S21
Measured Phase
Simulated Phase
S21(dB)
Phase(degree)
Frequency(GHz)
10
5
0
-5
-10
-15
200
100
0
-100
-200
0
2
4
6
8
10
12
14
16
18


b- PPO Blend-SM-A-SM
Measured S21
Simulated S21
Measured Phase
Simulated Phase
S21(dB)
Phase(degree)
Frequency(GHz)
10
5
0
-5
-10
-15
200
100
0
-100
-200
0
2
4
6
8
10
12
14
16
18

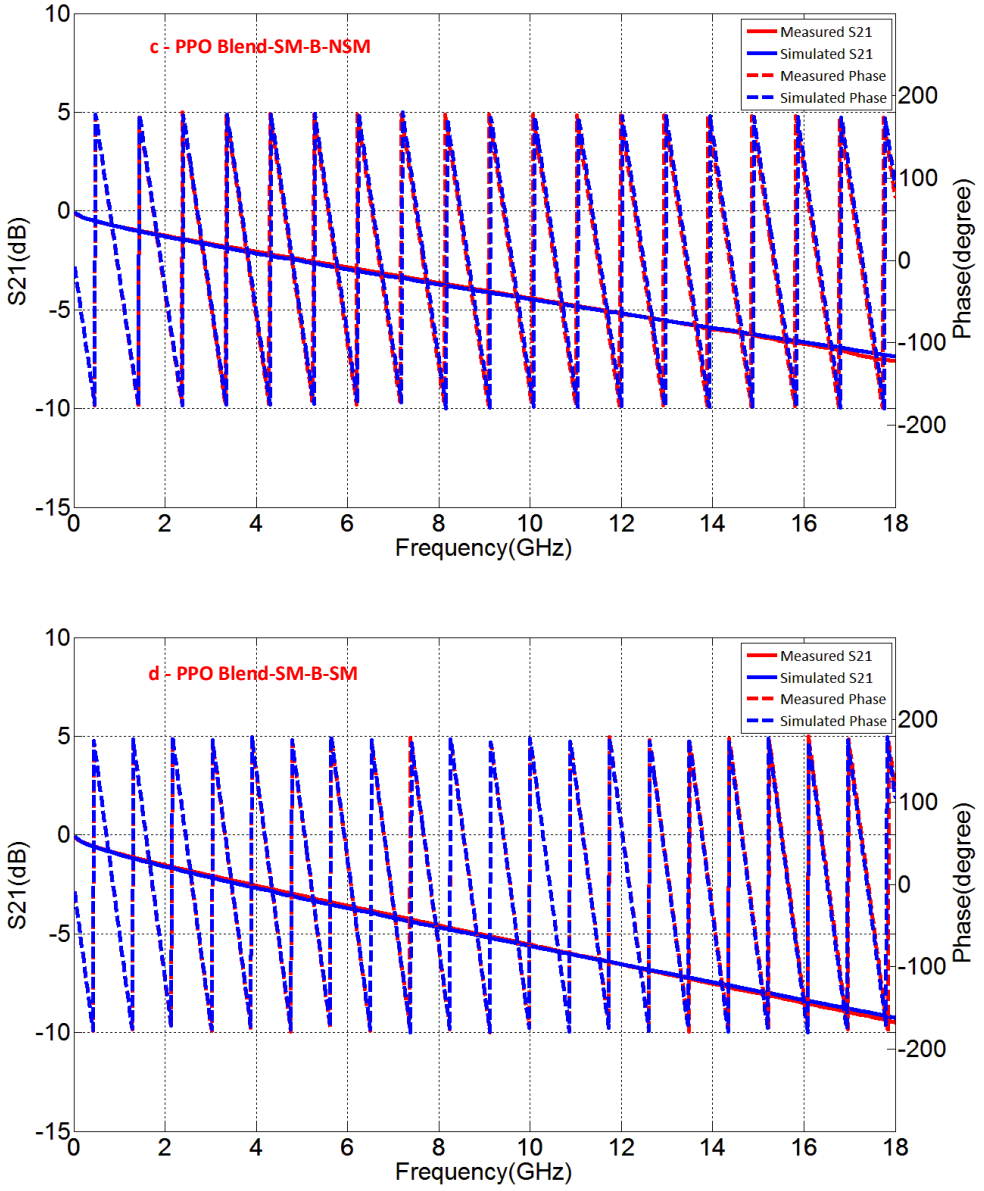


Figure 9–Measured and simulated S21 and phase data of the de-embedded traces on PPO Blend TVs (a: without SM-A; b: with SM-A; c: without SM-B; d: with SM-B)

The plots above indicate good agreements between the measurements and the extract model parameters for all four traces over a wide frequency range.

Conclusions

Development of new materials such as low loss solder mask applied to high-speed PCB products extends the need for practical wideband material characterization techniques. According to the paper, comparison of the material parameters for different implementations gives a quantitative idea about the influence of low loss solder mask and surface finishes on the high-frequency performance. When used on ultra-low loss material, the new low Df solder mask could reduce considerable 10% dielectric loss. Furthermore, a systematic and practical methodology for identifying the dielectric properties of solder mask ink is presented and proved to be effective.

References

1. Shlepnev, Yuriy, and Chudy Nwachukwu. “Practical methodology for analyzing the effect of conductor roughness on signal losses and dispersion in interconnects.” DesignCon2012, Feb. 1st (2012).
2. Hall, Stephen H., and Howard L. Heck. Advanced signal integrity for high-speed digital designs. John Wiley & Sons, 2011.

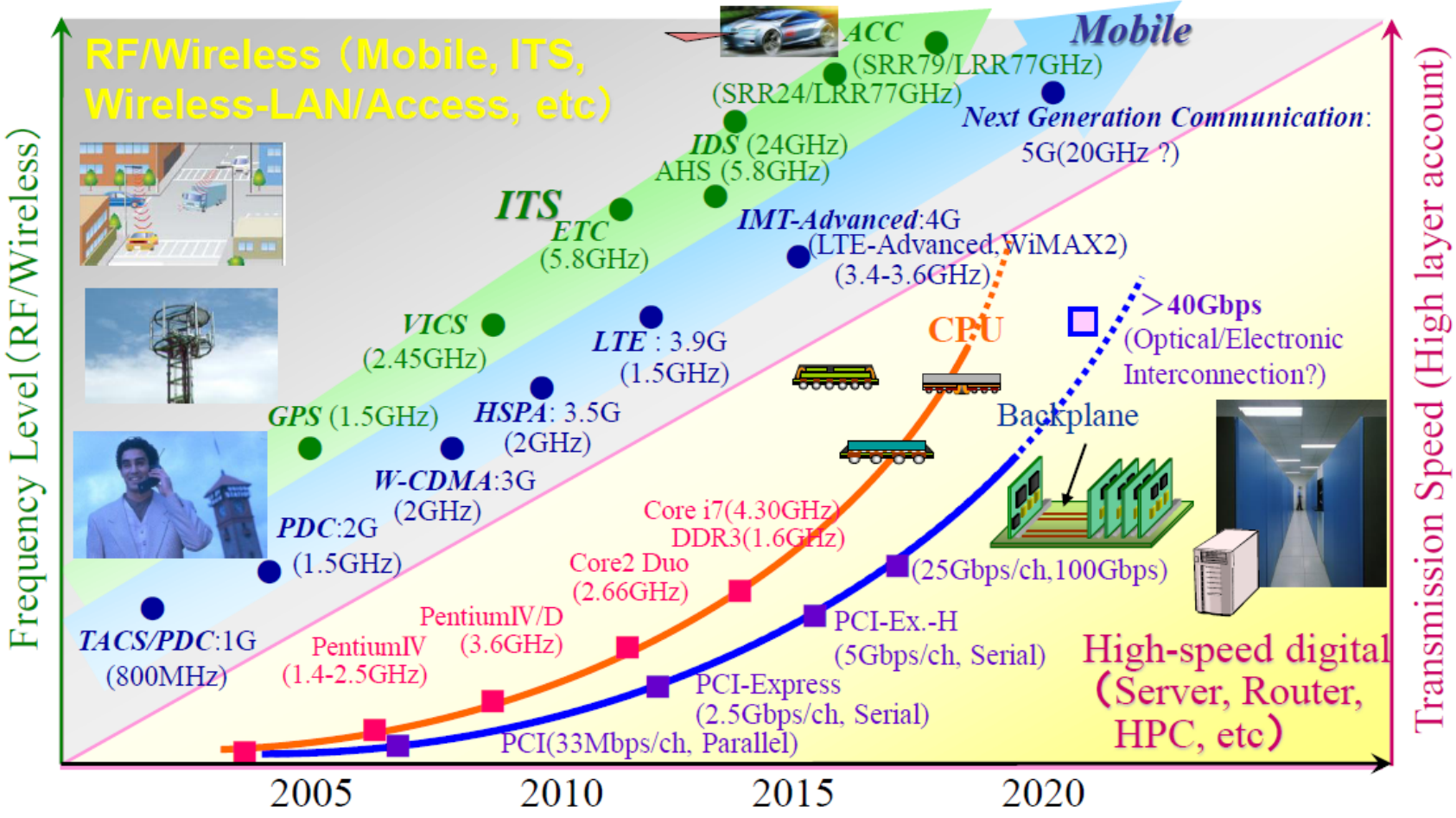
3. Huray, Paul G. The foundations of signal integrity. John Wiley & Sons, 2009.
4. Cauwe, Maarten, and Johan De Baets. “Broadband material parameter characterization for practical high-speed interconnects on printed circuit board.” Advanced Packaging, IEEE Transactions on 31.3 (2008): 649-656
5. JIS 6481 Test methods of copper-clad laminates for printed wiring boards, 1996
6. Bogatin, Eric. Signal and power integrity--simplified. Pearson Education, 2010.
7. Coombs, Printed circuits handbook. McGraw-Hill Professional Publishing, 2001.
8. Keysight Electronic Calibration Modules Reference Guide, viewable at:
http://literature.cdn.keysight.com/litweb/pdf/N4693-90001.pdf
9. Dunsmore, Joel P. Handbook of microwave component measurements: with advanced VNA techniques. John Wiley & Sons, 2012.
10. Moon, Se Jung, X. Ye, and R. Smith. “Comparison of TRL calibration versus 2x thru de-embedding methods.” Electromagnetic Compatibility and Signal Integrity, 2015 IEEE Symposium on IEEE, 2015:176-180.
11. Shlepnev, Yuriy, and Scott McMorrow. “Nickel characterization for interconnect analysis.” Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on. IEEE, 2011.
12. Djordjevic, Antonije R., et al. "Wideband frequency-domain characterization of FR-4 and time-domain causality." Electromagnetic Compatibility, IEEE Transactions on 43.4 (2001): 662-667.
13. Shlepnev, Yuriy, and Chudy Nwachukwu. “Practical methodology for analyzing the effect of conductor roughness on signal losses and dispersion in interconnects.” DesignCon2012, Feb. 1st (2012).

Effect of Permittivity and Dissipation Factor of Solder Mask upon Measured Loss

Hao He
Senior Engineer, Non-aviation Industry Development Department
Aviation Industry Co.

Rongyao Tang
Signal Integrity Engineer, R&D Department
Shennan Circuits Co., Ltd.

Trend of High-Frequency & High-Speed Applications



Insertion Loss Requirements on Server PCB

Segment	Platform	PCB Loss Requirements		
		Type	4GHz	8GHz
E3	Denlow	N/A		
	Greenlow			
E5	Romely	Stripline	-0.8dB/inch	-1.6dB/inch
		Microstrip	-0.84dB/inch	-1.68dB/inch
	Grantley	Stripline	-0.75dB/inch	-1.5dB/inch
		Microstrip	-0.79dB/inch	-1.58dB/inch
	Purley	Stripline	-0.65dB/inch	-1.25dB/inch
		Microstrip	-0.69dB/inch	-1.33dB/inch
E7	Brickland	Stripline	-0.48dB/inch	-0.96dB/inch
		Microstrip	-	-
	Purley-EX	Stripline	-0.48dB/inch	-0.9dB/inch
		Microstrip	-0.55dB/inch	-1.05dB/inch

Soldermask Dk & Df Test Methods from Vendors

類別	項目	測試方法	要求特性	結果
四、耐熱性	11.可焊性	IPC-SM-840C 3.7.1 塗上助焊劑後。室溫下放置5分鐘。 260±5℃預熱及浮焊方式10秒x3次	不應降低基板的可焊性	無異常
	12.防焊性	IPC-SM-840C 3.7.2 塗上助焊劑後。室溫下放置5分鐘。 260±5℃預熱及浮焊方式10秒x3次	油墨塗膜上不應附著焊錫	無異常
五、電氣特性	13.介質強度	IPC-SM-840C 3.8.1 依IPC-TM-650中TM2.5.6.1的規定	每0.025mm(0.001inch)厚度 最少加上500DV電壓	≧900 VDC/mil
	14.體積抵抗率	ASTM D-257		$>10^{12}\Omega$
	15.表面抵抗	ASTM D-257		$>10^{12}\Omega$
	16絕緣電阻	IPC-SM-840C 3.8.2 依IPC-TM-650中TM2.6.3.1的規定。需測量焊錫前、後之最小電阻值	IPC-B-25B A試驗基板最小值 $5\times10^{8}\Omega$ at500VDC	$2\times10^{13}\Omega$
	17. 介質損耗(tan δ)	JIS 6481	阻抗解析儀4192ALF(橫河Hulet Packard製) 1MHZ	0.029~0.038
	18. 介電常數(ε)	JIS 6481	1MHZ	4.2~4.4

- Bridge method & Q-meter method & Automatic balance bridge method
- Frequency 1 MHz

Source: ONSTATIC

Soldermask Dk & Df Test Methods from Vendors

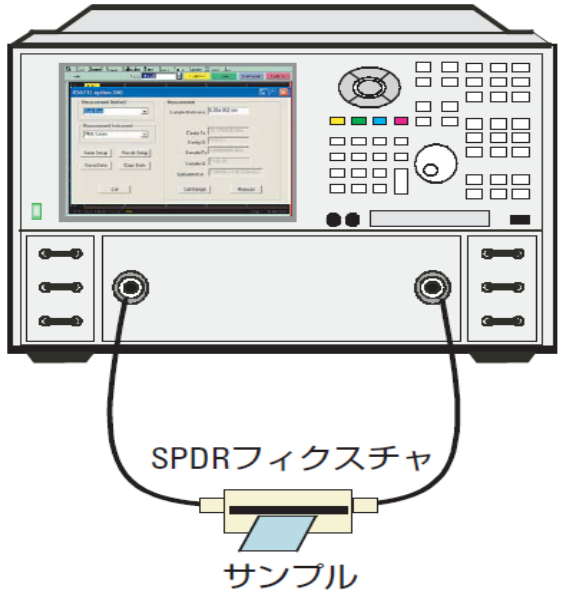
Test Item	Test Condition	Results
Adhesion	TAIYO Internal Test Method Crosscut tape peel test	100 / 100
Pencil hardness	TAIYO Internal Test Method No scratch on copper foil surface	9H
Solder heat resistance	Solder float test : Rosin flux, 260deg.C / 30 sec (1 cycle)	Passed
Insulation resistance	IPC comb type B pattern Humidify: 25-65deg.C, 90% RH, DC100V for 7 days Measurement: DC500V / 1 min. value at room temperature	Initial: 9.5×10^{13}Ohms Conditioned: 1.6×10^{13}Ohms
Dielectric constant	Taiyo Internal Test Method; Values at 1GHz	3.6-3.9
Dissipation factor	Taiyo Internal Test Method; Values at 1GHz	0.0069-0.0089

Equipment : RF Impedance Material Analyzer

Source: Taiyo

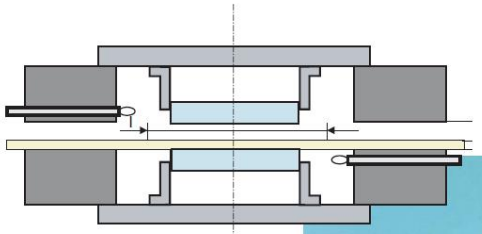
- Not enough details about the test method
- Frequency 1 GHz
- Sample is free film
- Sample thickness is 100 um at minimum
- Actual soldermask thickness above trace is around 10~30 um

Soldermask Dk & Df Test Methods from Vendors

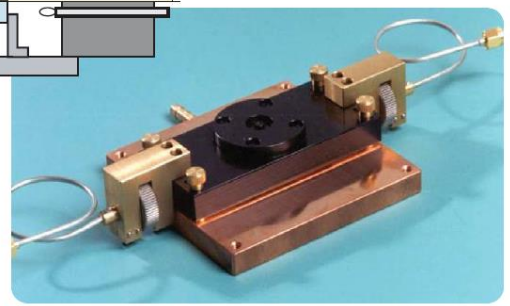


PNA

- SPDR method
- Frequency 5 GHz
- Sample is free film
- Sample thickness is 100 um at minimum



Split Post Dielectric Resonator



Source: Taiyo & Keysight

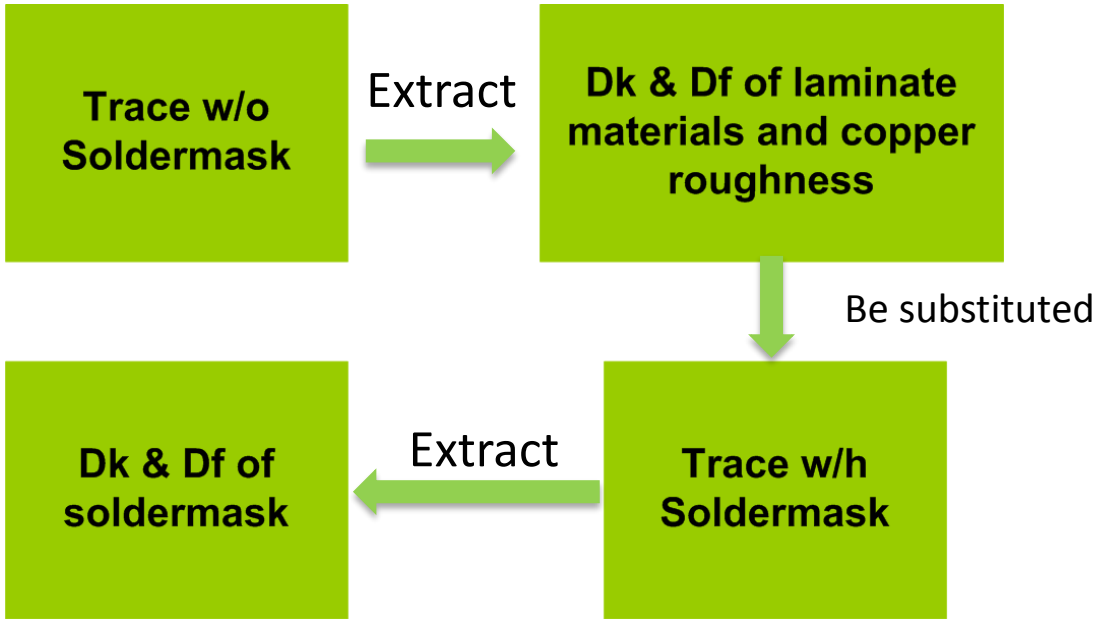
Total Signal Loss

Conductor Loss due to skin effect & copper roughness

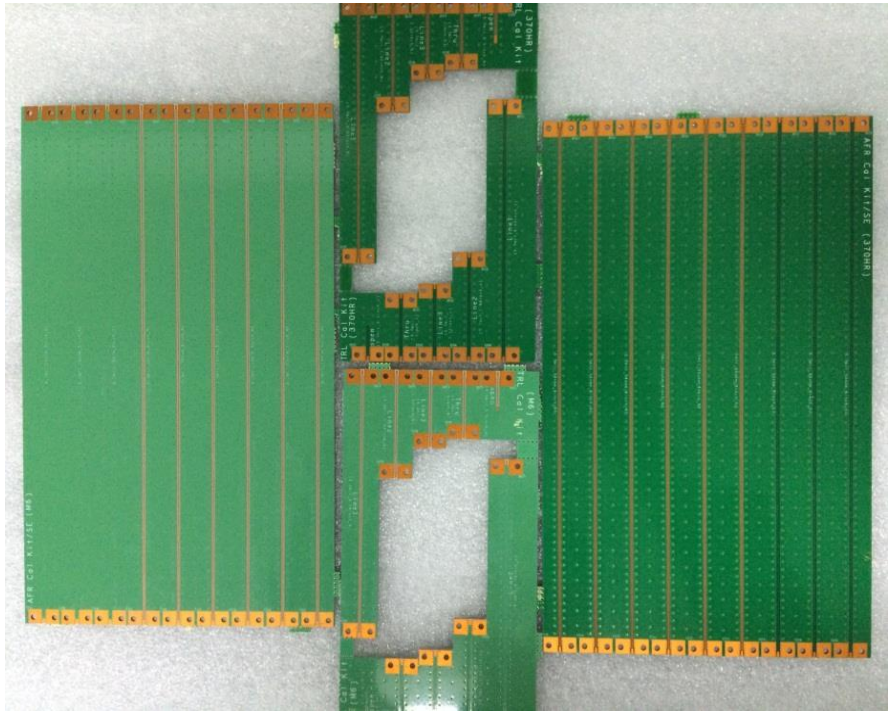
Dielectric Loss due to Dk & Df of dielectric material, including Soldermask

Purpose

- Could we find a way to extract the soldermask Dk & Df in real situation?
- How much loss is introduced by soldermask?
- Could we reduce the signal loss by using low-Df soldermask?

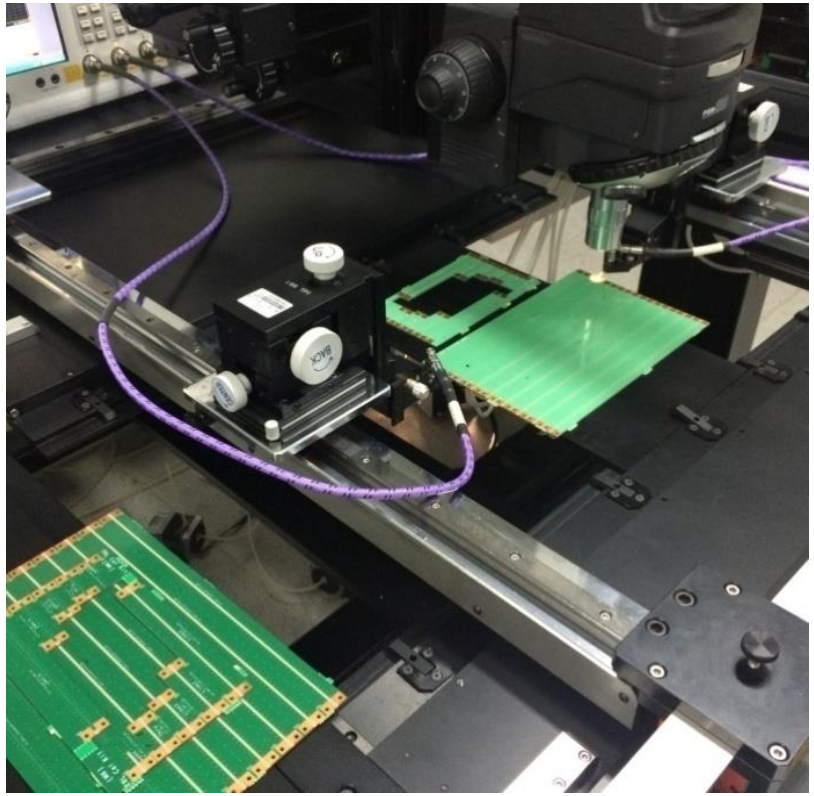


Test Vehicles



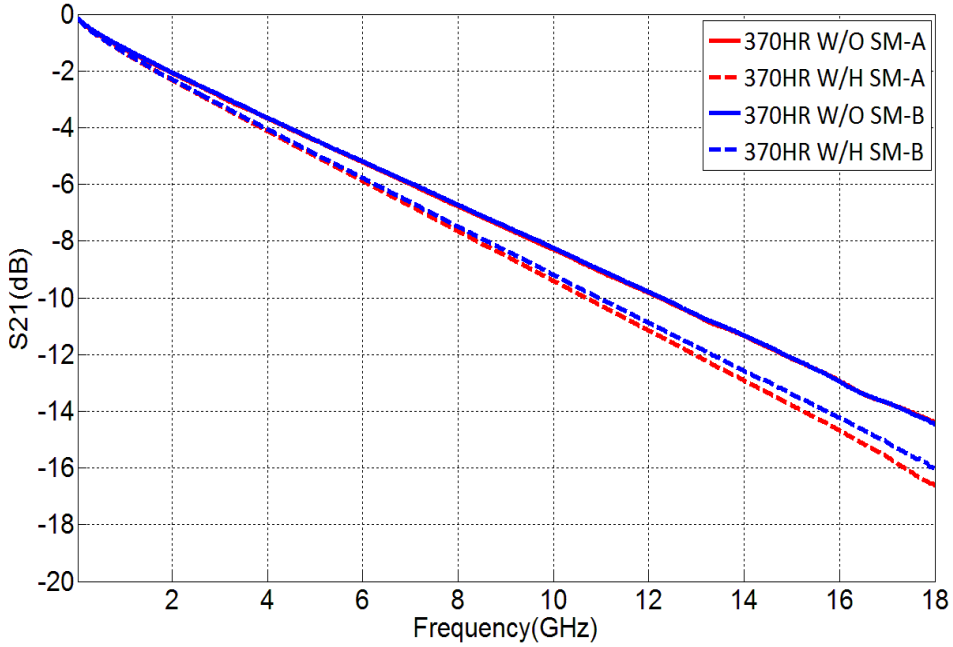
- 2 laminate materials: 370HR(std FR4) Megtron 6(very low loss)
- 2 soldermask: SM-A(std) SM-B(low loss)
- 10 layers with DUTs only on top layer
- 5~6 mil width 50ohms conductor-backed coplanar waveguide
- RTF copper to ensure low roughness
- Electroless Copper process to minimize copper thickness variation

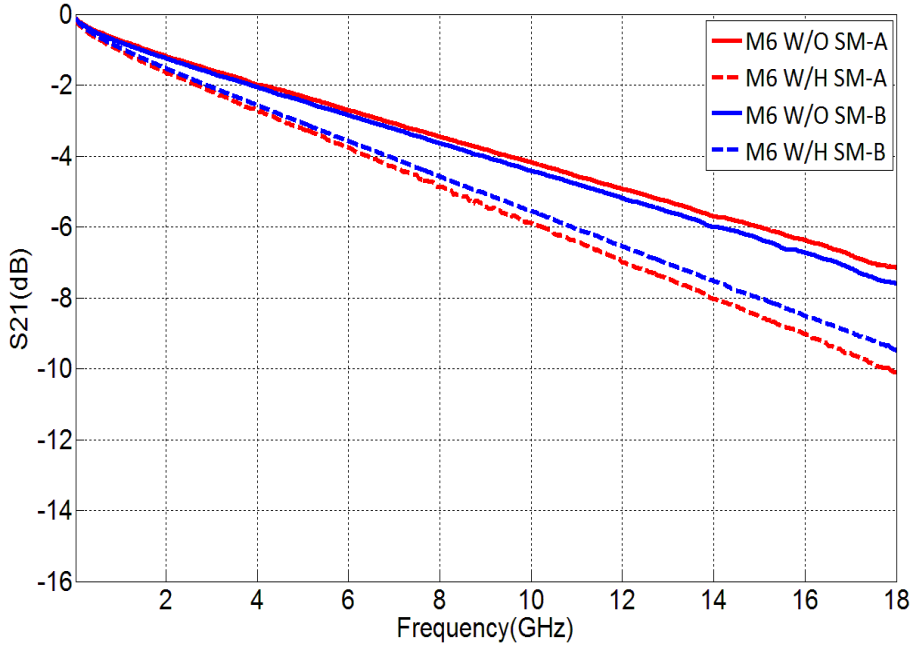
Test Setup



- E5071C VNA with ECal Module, 20 GHz BW
- Gore 2.92mm cable, 40 GHz BW
- GGB Model 40A-GSG-1000-LP MW Probe
- 1 inch trace used for AFR de-embedding
- 8.265 inch trace for test and simulation
- 10 MHz-18 GHz, 900 points
- Calibration method: Ecal and AFR from Keysight

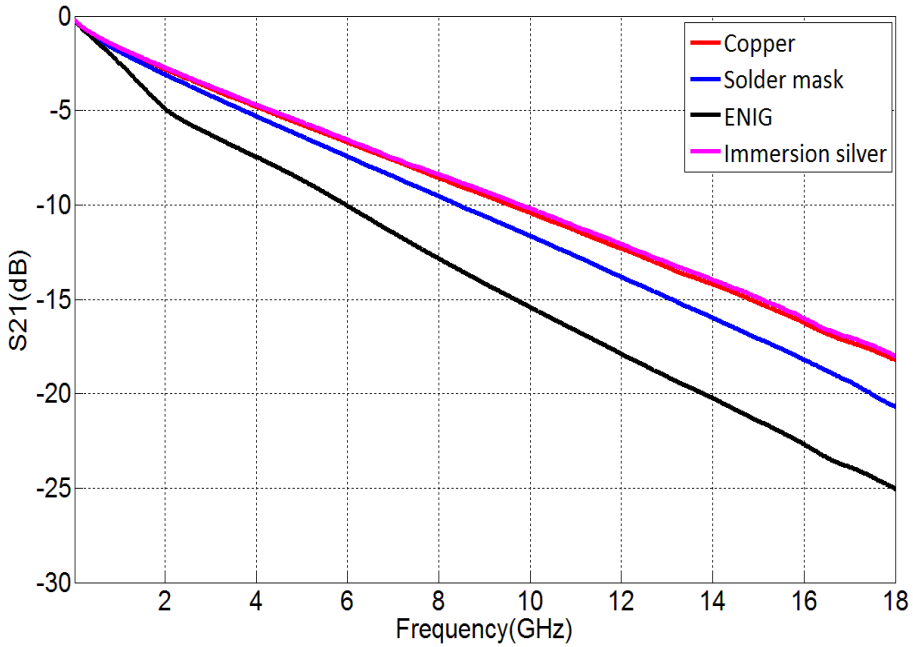
Test Results

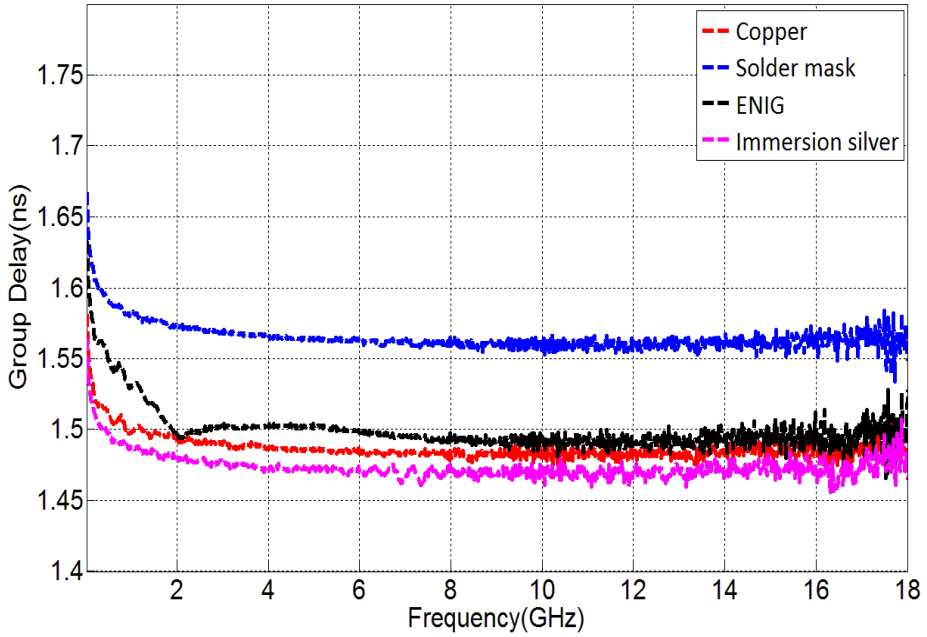




- Baking the boards for 4 hours at 160 degrees
- A great discrepancy between bare and solder mask coated trace losses (10 -12 % @ 8 GHz for 370HR; 20% -30 %@ 8 GHz for M6)
- For std and low DkDf soldermask : 10% decrement in loss @ 8 GHz for M6 with low DkDf sodermask

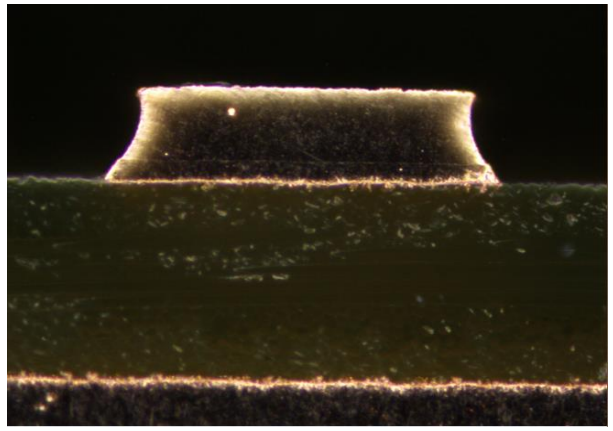
Test Results

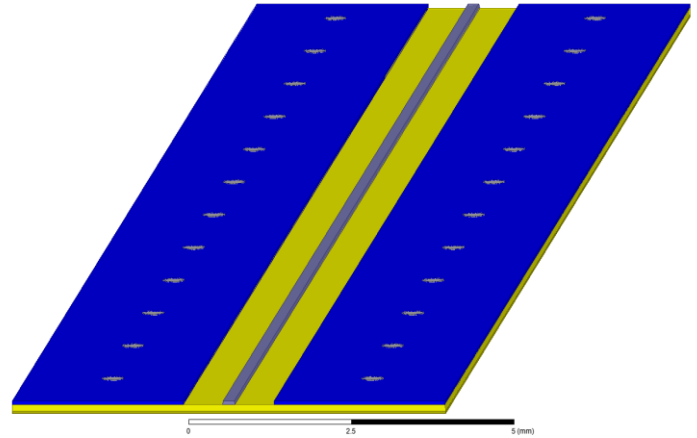


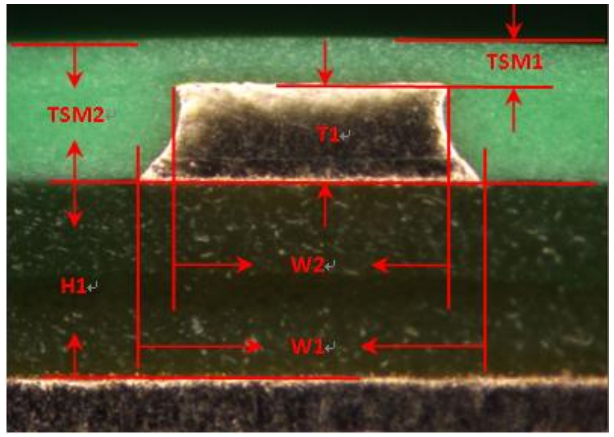


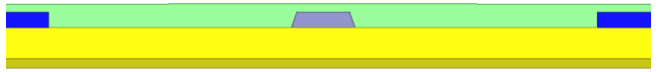
- For 370HR, ENIG nearly doubles the loss (to bare trace)
- For 370HR, Immersion silver doesn't introduce any extra loss

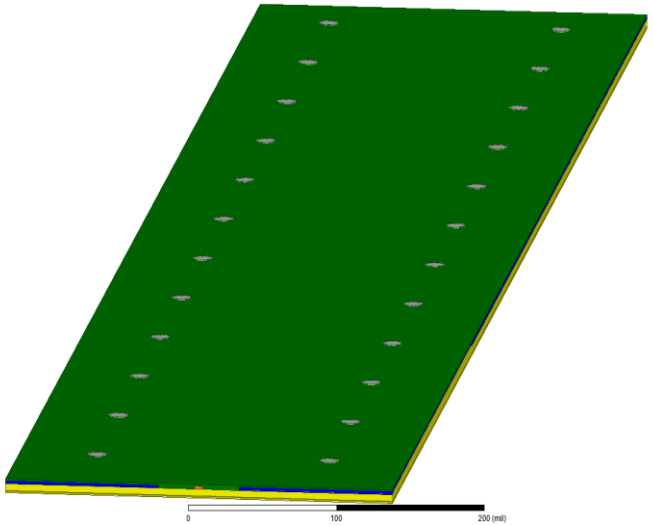
Cross sections for HFSS 3D Model







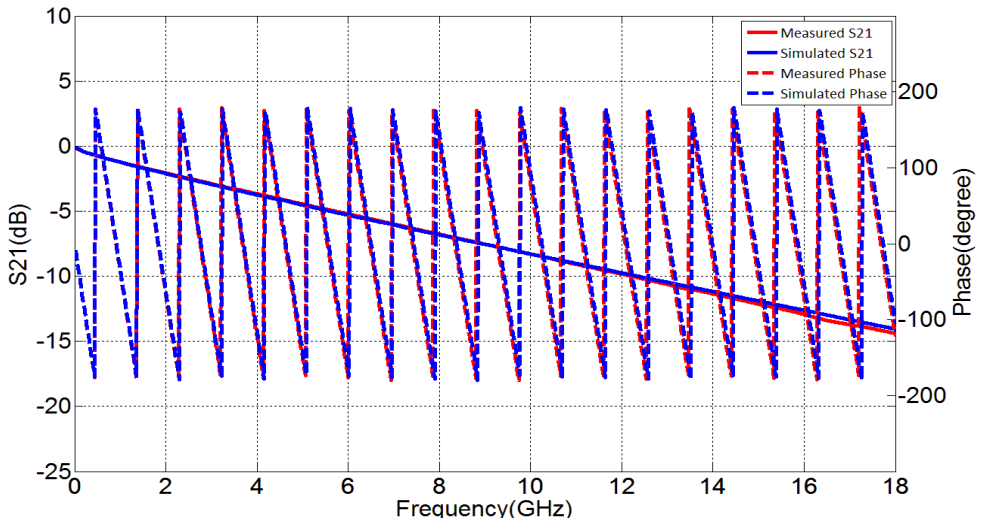




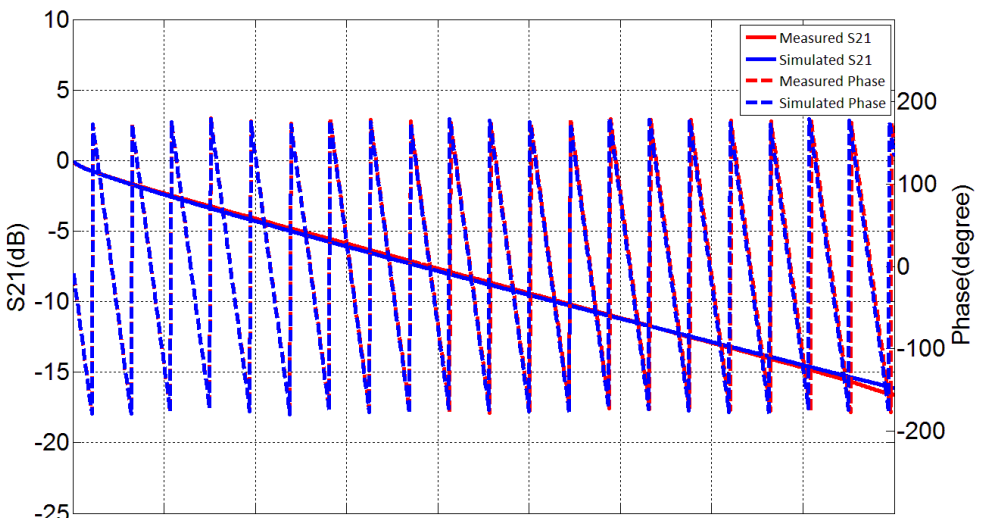
- Djordjevic-Sarkar dielectric model and Huray conductor roughness model

Simulations vs Measurements for 370HR

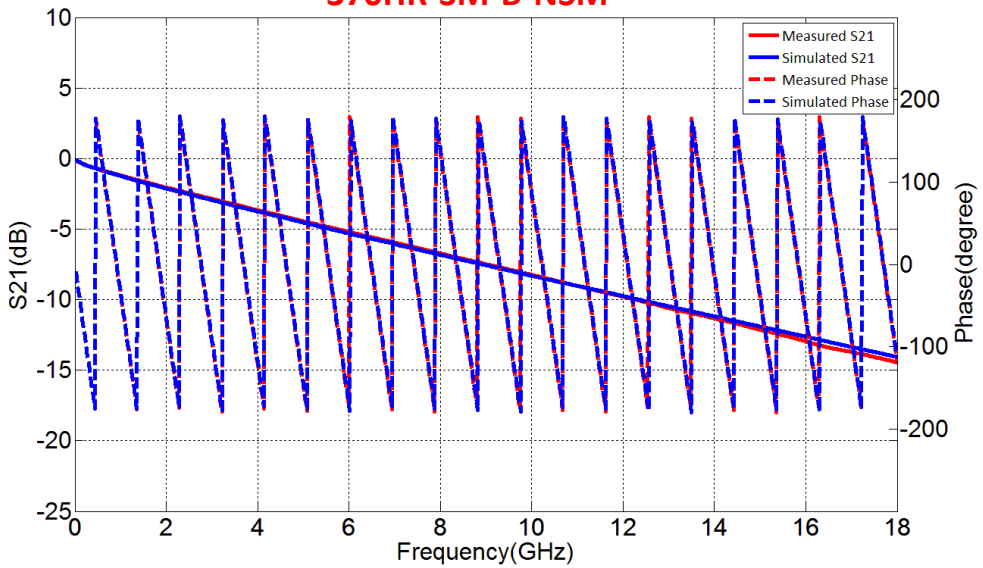
370HR-SM-A-NSM



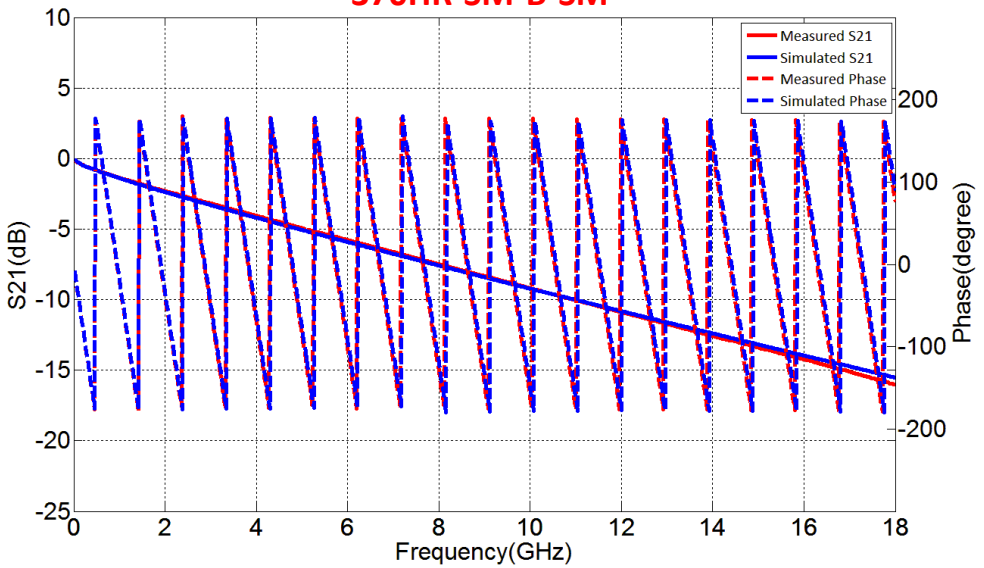
370HR-SM-A-SM



370HR-SM-B-NSM

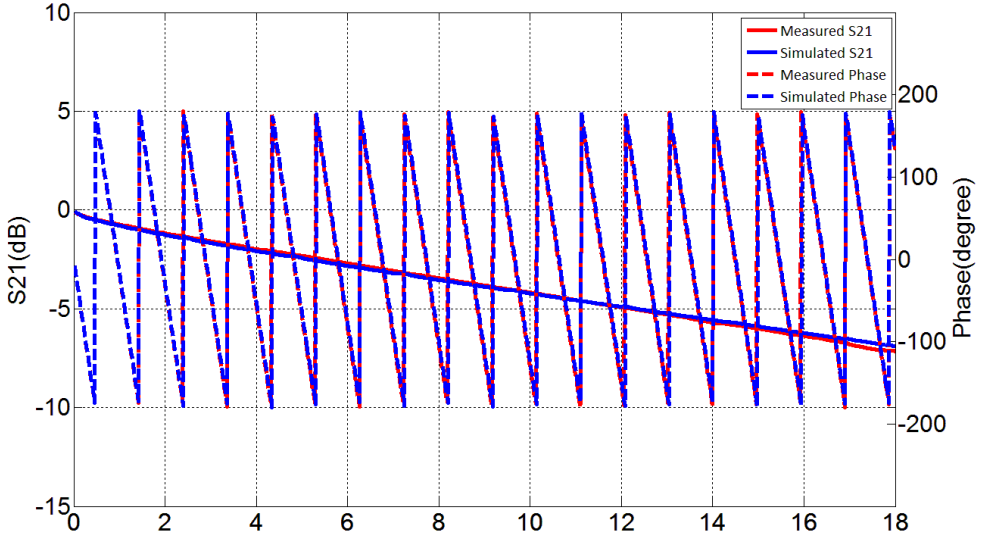


370HR-SM-B-SM

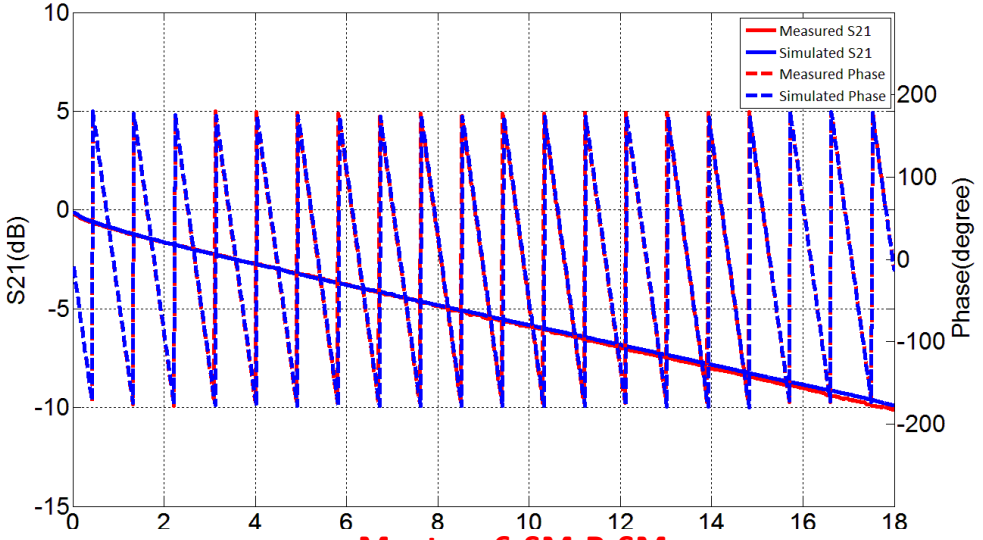


Simulations vs Measurements for Megtron6

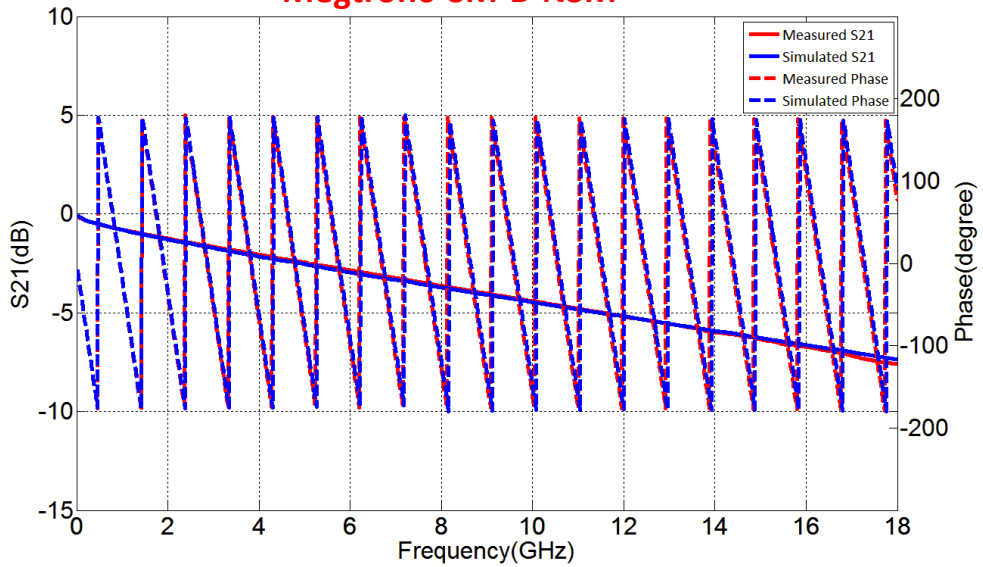
Megtron6-SM-A-NSM



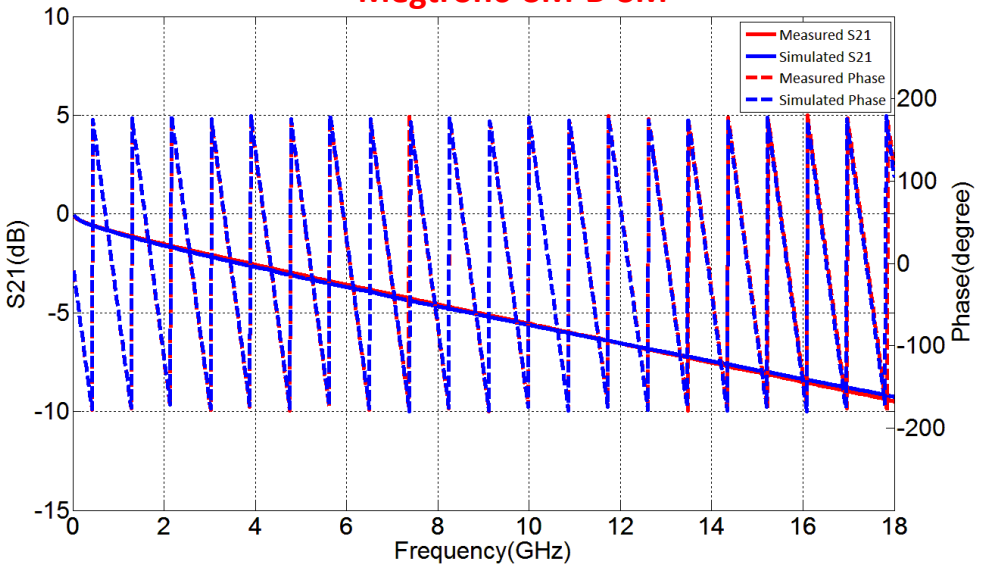
Megtron6-SM-A-SM



Megtron6-SM-B-NSM



Megtron6-SM-B-SM



Identified Parameters

Test Vehicle	Dielectric Laminate		Solder Mask		Copper Roughness on both sides	
	Dk@1GHz	Df@1GHz	Dk@1GHz	Df@1GHz	Nodule Radius	Hall-Huray Surface Ratio
370HR-SM-A-NSM	4.3	0.02			0.15	8.8
370HR-SM-A-SM	4.3	0.02	4.3	0.025	0.15	8.8
370HR-SM-B-NSM	4.34	0.02			0.15	8.8
370HR-SM-B-SM	4.34	0.02	4.35	0.012	0.15	8.8
M6-SM-A-NSM	3.83	0.0045			0.15	8.8
M6-SM-A-SM	3.83	0.0045	4.3	0.025	0.15	8.8
M6-SM-B-NSM	3.92	0.0045			0.17	9
M6-SM-B-SM	3.92	0.0045	4.35	0.012	0.17	9

Summary

- Standard soldermask with Dk 4.3-4.4 & Df 0.02 @ 1 GHz
- Low loss soldermask with Dk 4.3-4.4 & Df 0.012 @ 1 GHz
- ENIG introduces quite a lot losses
- A great discrepancy between bare and solder mask coated trace losses (10 -12 % @ 8 GHz for 370HR; 20% -30 %@ 8 GHz for M6)
- Large Df gap between laminate materiel and soldermask highlights the importance of low loss soldermask for high-speed applications