

# Thermo-Electric Cooler Module Reliability improvement for CT Detector Subsystem

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## Abstract

Thermo-electric coolers (TEC's) are becoming increasingly popular in the medical device industry, where design space is limited and high heat transfer capacity is needed. For a Computed Tomography (CT) reference module application, an integrated TEC + copper heat pipe assembly was used to regulate temperature of a precision photodiode sensor array. Due to the extended service life of a CT scanner, 10 year reliability of all components is required. Through accelerated testing of the TEC assembly using rapid switching of the TEC in both heating and cooling modes, it was determined that the existing design only met one year of life.

Failure analysis was performed on the TEC units and dice cracking as well as burned dice due to thermal hotspots were observed. Through discussions with the TEC vendor, a higher temperature TEC solder material was evaluated on future assemblies, allowing for higher thermal excursions and also better CTE matching to the TEC ceramic. Subsequent reliability testing on the higher temperature solder assemblies showed more than 3x performance improvement, thereby exceeding the 10 year life requirement. In addition high temperature/humidity/biased (85C/85%RH) was tested for 500hr. At the end of the test a small drift in performance was observed, failure analysis will be presented.

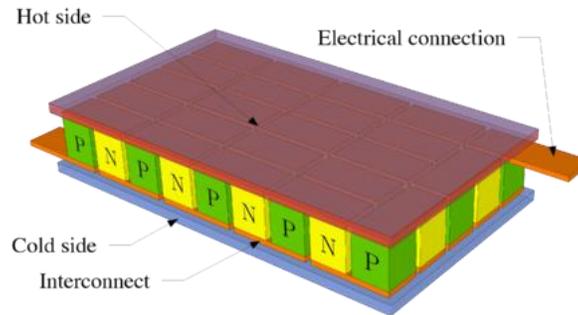
In addition to the design improvement and learnings, the reliability experimental setup showcased an effective method for acquiring quick cycling data on TEC while evaluating the assemblies over a wide thermal range. This setup utilized the self-heating/cooling of the TEC and mounted the assembly on a fixed temperature plate.

Finally, specifics as to boundary condition testing of a TEC assembly and also the PID control implementation of the TEC via an FPGA based design will be discussed.

## Overview of TEC Assembly design and architecture

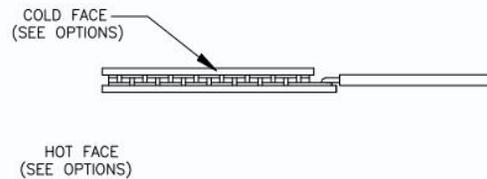
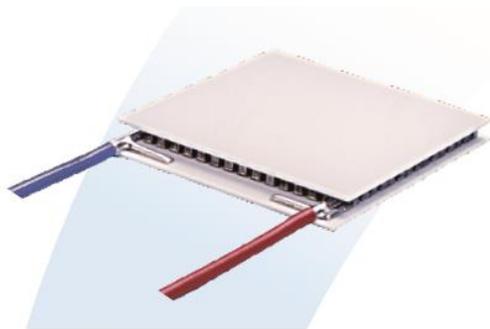
In a current Computed Aid Tomography (CT) Detector scanner, a reference detector located near the tube source is used for various purposes, including gain reference normalization, tracking of tube focal spot position, and independent kVp measurement. This reference detector will be referred to as the source side reference detector (SSRD) within this paper. Due to the sensitive detector electronics, a tightly controlled temperature of the detection element is essential to maintain an accurate reference signal throughout the patient scan. Through various design tradeoffs and considerations, including location, space and power constraints within the design, a Thermoelectric Cooler (TEC) was chosen as the heating/cooling element within the SSRD subassembly.

A thermoelectric cooler is a bi-directional device that utilizes the Peltier effect to create a heat flux between the junctions of two types of materials. The primary advantages include lack of moving parts, small size, long life, and a flexible shape. Disadvantages include relatively high cost and poor power efficiency. Due to the electric structure of the PN junction connection, both heating and cooling modes are available by simply changing the bias voltage across the electrode junctions. A schematic of the TEC is shown below:



**Figure1. Peltier TEC schematic, ref [1]**

In our application, a specific TEC was selected, primarily due to power and size constraints. A picture and appropriate specification of the TEC selected is shown in Figure 2 below.

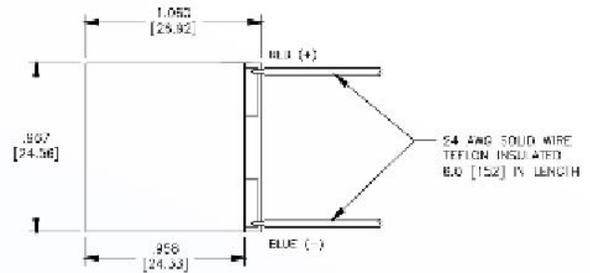


Ceramic Material 96% Alumina Ceramics  
Solder Construction: 138°C BiSn

**PERFORMANCE SPECIFICATIONS**

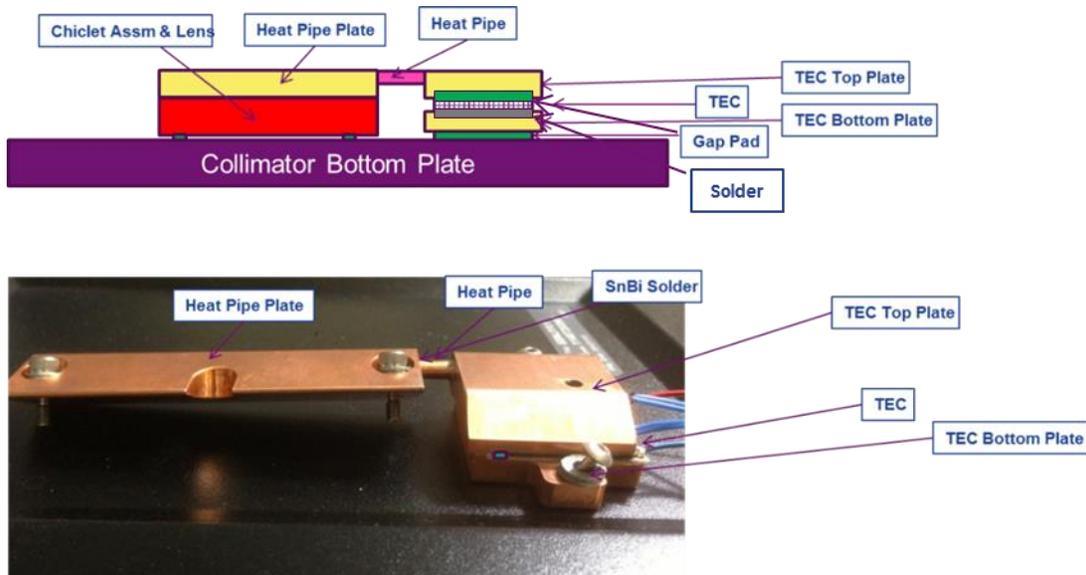
Hot side temperature (°C)	25	50
Qmax (watts)	69	75
Delta Tmax (°C)	69	79
I <sub>max</sub> (amps)	7.9	7.99
V <sub>max</sub> (volts)	14.4	16.2
Module resistance (ohms)	1.678	1.892

**MECHANICAL DRAWING**



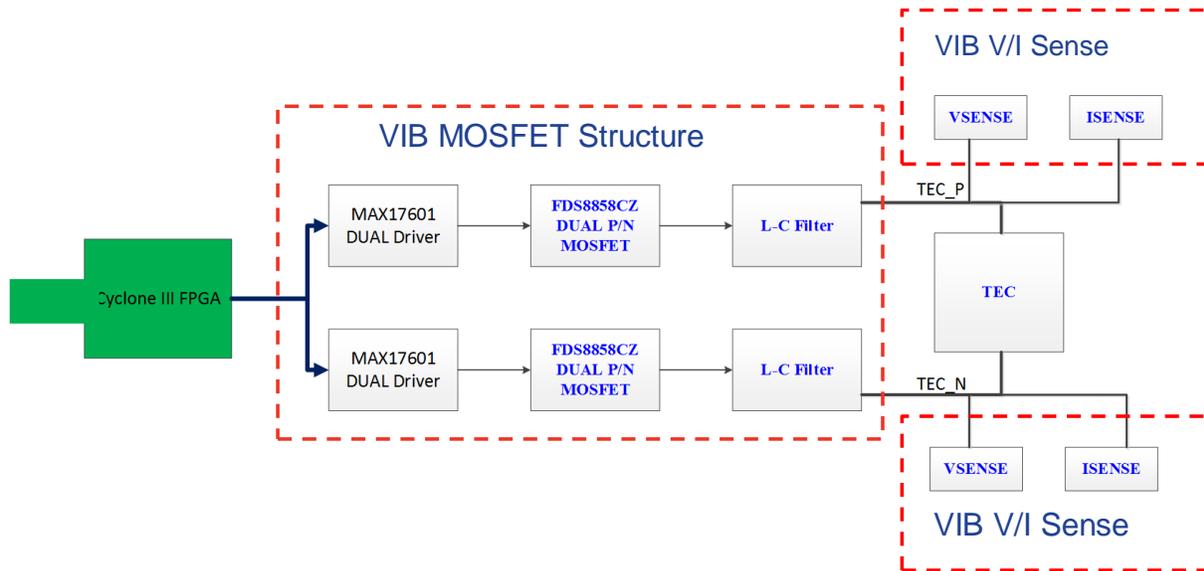
**Figure 2. Product TEC design**

In the SSRD design, an integrated TEC assembly is utilized to heat and cool the detector element, herewith referred to as the Chiclet. The TEC assembly includes the TEC element, top and bottom plates that attach to the cold and hot side respectively, a heat pipe and an angle plate that interfaces with the Chiclet. Between the TEC cold side and the TEC top plate (Cu), there is a thermal gap pad. Between the TEC hot side and the TEC bottom plate (Cu), a solder interface exists, that is, the TEC hot side is soldered directly to the TEC bottom plate. Between the TEC bottom plate and collimator (which acts as a heat sink), another thermal gap pad exists. The TEC top and bottom plate are screwed together. The heat pipe serves to transfer the heat effectively from the TEC to the Heat Pipe Plate, which is connected directly to the Chiclet subassembly. A detailed diagram of the SSRD TEC assembly is shown below:



**Figure 3. SSRD TEC Assembly design construction**

The TEC Assembly is controlled through a PID scheme from an FPGA. Essentially, the FPGA controls a gate driver/MOSFET hardware circuit, which delivers the appropriate voltage to the TEC electrodes, only variable DCV is applied to TEC. In addition, current and voltage sense circuitry can monitor the TEC parameters back to the FPGA. The board which contains this circuitry is known as the Vyper Interface Board, or VIB. The details of the control scheme are outside the scope of this paper, but for completeness, a high-level block diagram of the control hardware is shown.



**Figure 4. SSRD Hardware control block diagram of TEC Assembly**

Lastly, the detector Chiclet subassembly is shown below, assembled into a housing that is bolted onto the collimator bottom plate. This element is responsible for collecting the reference X-ray signal, digitizing the signal, and passing the digital signal to the VIB electronics via the flexible circuit shown.



**Figure 5. SSRD Chiclet subassembly**

Due to the rotational nature of the CT scanner, the TEC assembly goes through numerous G-load conditions under normal operation, as well as thermal cycles during startup and shutdown of the scanner. The estimated amount of thermal cycling that the TEC experiences is approximately 2 cycles/day – worst case condition. This paper focuses on quantifying the life of the TEC assembly given.

#### Reliability assessment and testing plan

Following the Design for Reliability (DFR) process within the company [2], to assess reliability risks one of tools available is the FMEAs (Failure Mode Effect Analysis). We use the FMEA to identify critical design/process failure modes/mechanisms and on the failure modes/mechanisms with reliability relevance, we identify what stresses can be used to precipitate those failure modes. Then empirical or physics of failure models are used to identify acceleration factors such that we can perform a robust reliability assessment during the development phase of new product introduction.

Based on this process the following reliability test plan was developed:

Test ID	Test conditions
PTC	Power cycling, 6 min/cycle (1680cy/week), 3min +5V, 3min -5V Load plate temperature -5 to 55C, heatsink plate set at 20C Reliability goal is 7k cycles, ten years equivalent, assuming two cycles a day
THB	85C/85%RH power cycle 30min ON, 30 min OFF Test for 500hr
Operating vibration	Demonstrate that the TEC can handle the shipping vibration stresses and the 10yr vibration usage in a CT mobile application
g-load vibration	Demonstrate that the TEC can handle the CT g-load stresses at the highest rotational speed for the number of exams expected in 10 yr usage

**Table 1.- TEC's Reliability Test Plan**

#### Power-Thermal Cycle (PTC) testing experimental setup

Temperature cycling is the ideal stressor for stack-up structures where materials have different CTE (coefficient of thermal expansion) values. This is the case of our TEC structure. To minimize shear stresses only one TEC plate is soldered, the other one has a gap pad as interface which diminishes shear loads. In this regards, within the company we developed a guidelines document to assess the reliability robustness of electronic assemblies, in particular of solder joints [3].

In this application, the temperature range is in our favor, once the CT scanner arrives to a hospital, it has survived the shipping/storage stresses (temperature wise – a couple of cycles -40 to 70 degrees Celsius). At the hospital, the TEC will experience temperature cycles from 15-26C to 40-50C, a couple of cycles per day. In our test set up we are stressing over a wider temperature range -5C to 55C, almost twice the range. If we were to use the solder joints empirical model, Coffin-Manson [4] provides a 3x acceleration factor. In our number of cycle testing goal calculation we did not assume an acceleration factor, so if we pass, we would have a 3x margin.

Four devices were available for PTC testing. Parts were attached to a large cold plate set at 20C with water circulating to maintain the temperature. The two TEC plates temperatures were monitored as well as the current drawn by means of R-

shunt circuits. A production data logger was used to collect data. Two 5VDC power supplies, two SSRs (Solid State Relays) and a production controller [5] were used to power up the TECs and to change voltage polarity every 3 minutes. A picture of the test set up can be seen in Figure 6. Power supplies were connected in reverse polarity and the production controller timed the corresponding SSRs such that, at all times, only one power supply was connected to TECs. Full current was applied to TECs (~2Amps).

The temperatures seen by the load (upper) plate fluctuates from -5C to 55C (Figure 7), this plate will experience the largest thermos-mechanical stress, having the gap pad as interface mitigates the shear stresses expected. The heat sink is a cold plate connected to a reservoir (heat exchanger) set at 20C. Since we apply full load, the heatsink TEC plate can not follow the cold plate set point, there are transients of ~2 mins, where the temperature drifts by 5 to 10C above/below the set point. After this transient the plate reaches a stable 22C (Figure 8).

During this test the current drawn is monitored, Figure 9 is an example. The current profile also has a small transient at the beginning of power cycle transitions, the transient is ~30 sec. During cooling the current draw is 1.8Amps and during heating it is -1.3Amps.

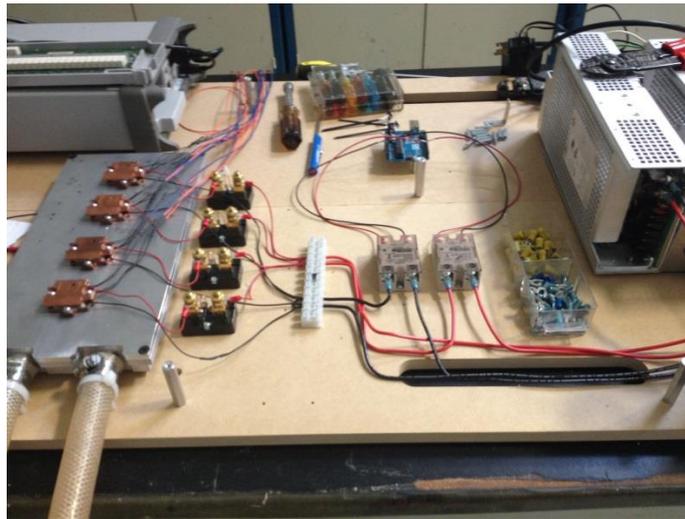


Figure 6.- PTC test set up

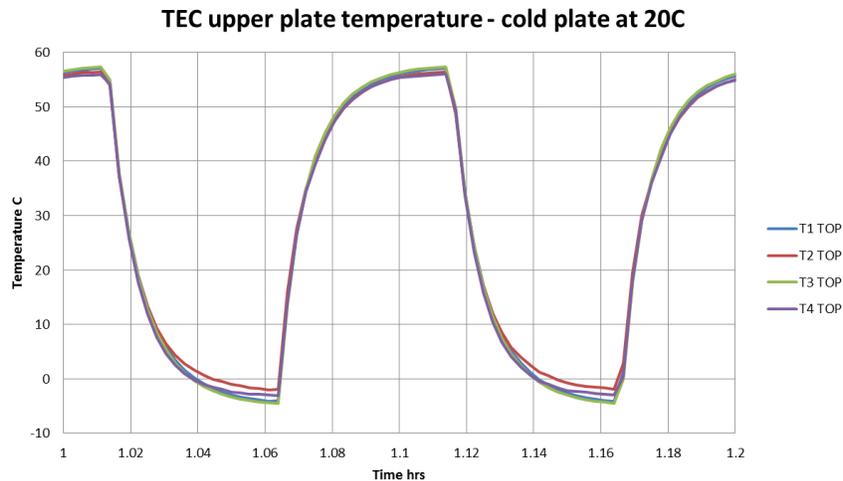
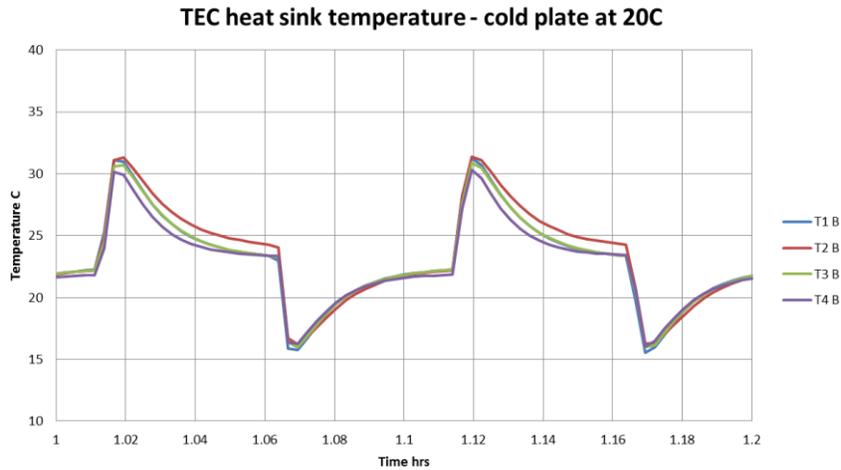
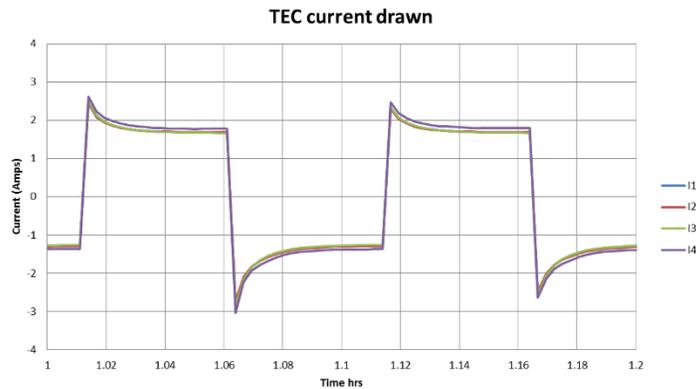


Figure 7.- Load plate temperature



**Figure 8.- Heat sink plate temperature**



**Figure 9 - Current drawn by TEC**

### Temperature-Humidity Bias (THB) testing

Temperature/humidity/bias testing was performed with similar set up as PTC testing, one module was attached to a large aluminum plate (heatsink) and power was cycled every 30 min from zero to full current. This set up was placed inside a production environmental chamber and kept at 85°C and 85%RH. Plate temperatures and current drawn were monitored.

The 85/85 testing is a standard electronic industry test, heavily used in telecom industry [6]. It is an accelerated test aim to accelerate degradations caused by process/assembly defects due to cleaning/contamination, environmental pollutants, flux residue, moisture sealant quality. Passing this test for 1000 hrs demonstrate 20 years in a telecom office environment.

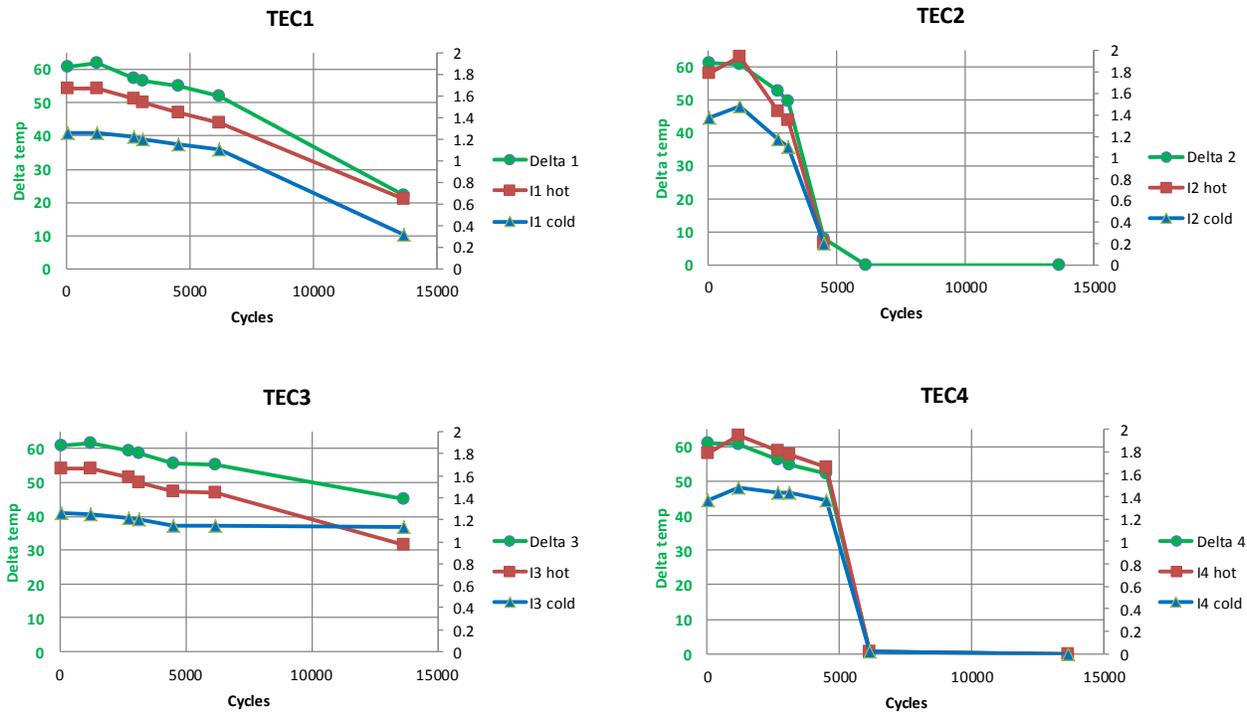
### Vibration testing

The company has developed internal standards [7] to qualify CT scanners and subassemblies for shipping vibration/shock stresses and usage vibration in particular for mobile applications. Any new subassembly need to pass these tests to be used in any scanner. For CT applications and for subassemblies without moving parts the company developed an internal standard vibration based that simulates the g-load expected at the highest rotational speed patient exams.

Vibration testing was performed at collimator level, the whole structure (detector/heatpipe/TEC) was attached to collimator (which acts as heatsink). Performance data was collected before/after vibration stresses. First we performed the shipping/use vibration stresses and then the g-load vibration.

Experimental Testing data – Baseline

The most stressful condition is power thermal cycle. It was performed on 4 units, with results shown below:



**Figure 10.- Power thermal cycle results on baseline parts**

This data shows that parts cannot survive 5000 cycles. Current draw and delta temperature start to decrease after 2000 cycles for the weakest part. The best part shows decent stability up to 5000 cycles. TEC2 and TEC4 are worst compared to TEC1 and TEC3. TEC1 and TEC3 were covered with thermal insulation during testing. This insulation likely diminished the delta temperature between hot plate and environment, making these TEC's last longer.

The requirement is to pass 7000 cycles. Using binomial distribution, to demonstrate this goal with 90% confidence level, with four parts, we need to run for 38k cycles without failures. The assumption is that life means a B10 of 10yrs (B10 means 90% of parts surviving), so current design is not meeting reliability goal.  
 TEC Failure Root Cause Investigation and Design Change

To investigate the root cause of the failing thermal cycling TEC assemblies, the assemblies were sent to the TEC product company for autopsy/ failure analysis. The failure symptom was a high resistance connection (> 200 ohms) between the TEC terminals. A normal connection is less than 5 ohms AC resistance. A picture of the exposed TEC assembly is shown in Figure 11 below:



The AC resistance is about 219ohm, but when pressing the TEC, the resistance would fluctuate hugely.

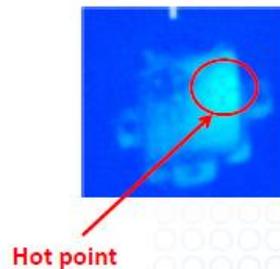


**Figure 11.- Exposed TEC assembly (>200 ohms AC resistance between terminals)**

No cracks were found in the external ceramic upon investigation, during IR imaging, a localized hot spot was observed within the TEC. This is shown in the Figure 12 below:

## 2.2 Checked the IR image by IR image instrument

The TEC have a serious hot point, see right picture.



**Figure 12. Exposed Hot spot on IR camera**

The following standard dye-pry procedure was followed to inspect the TEC in a non-invasive manner:

Place the sample in a beaker, then immerse sample in the dye.

Place the beaker and sample into a vacuum chamber. Draw a vacuum for 3 minutes. Partially vent and reapply vacuum to the chamber three times to aid in dye penetration.

Turn off vacuum pump and leave the sample in the dye for 5 minutes under vacuum.

Vent any remaining vacuum and remove sample.

Dry the sample in an oven by baking at 100°C for up to 50 minutes.

Remove sample from oven, and cool down.

Pry sample by mechanical force.

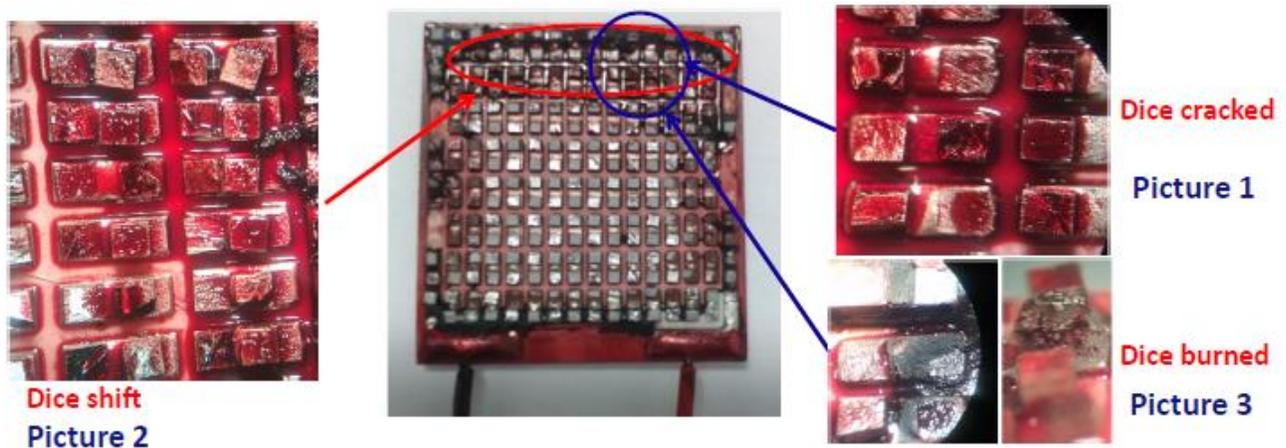
Inspect sample using microscope to check internal condition of sample.

Upon inspection of the internal dice, the following observations were noted:

Some cracked dices surface were pressed red dye as Picture 1 in Figure 13, so these dices have been damaged before prying TEC. These cracked dice will cause high resistance, high current and high temperature. The high temperature will cause solder reflow, dice shifted and dice burned.

Some dices were obvious shifted as Picture 2 in Figure 13.

One dice were serious burned as Picture 3 in Figure 13.



**Figure 13. Internal die inspection**

Through these observations, more likely the TEC got damaged by an uneven external force during assembly process. The thermal excursions likely propagated the dice microcracks and eventually caused the resistance increase.

Based on this autopsy/ failure analysis investigation, a design change to the TEC dice solder material was proposed. The new solder is a high temperature solder material that would withstand the high thermal excursions. Samples with the new solder material were created by the vendor and given to the company for further cycling.

Below in Table 2 is a comparison of the material properties of the two solders used.

Table 2

	Temperature liquidus ( C)	Elastic Modulus (GPa)	Tensile strength (Mpa)	CTE (um/mC)
<b>Sn 58%Bi</b>	138	11.9	60.4	15
<b>Sn 5%Sb</b>	232	44.5	35.2	20

The higher temperature solder seems not to be the ideal candidate as it is a bit stiffer and has lower strength, with CTE wise comparable. Likely process parameters were as important or more so such as load-plate screws torque control, solder height, and flatness.

Reliability testing on higher temperature solder TEC's

Power-Thermal Cycle (PTC) results

The PTC data on high temperature solder TEC's shows great improvement. No current degradation up to 80 thousand cycles, with parts still under test beyond this cycle count. Only two degrees Celsius degradation on delta temperature, with TEC3 and TEC4 showing higher degradation since these modules are not thermally insulated.

The reliability goal is to demonstrate a B10 of 10yrs with 90% confidence level. As indicated before to achieve this goal, we need to pass ~40k cycles. B10 means that 10% of parts can fail in 10 years, 10 years means 7k cycles. With this high temperature solder, we met and exceeded this goal.

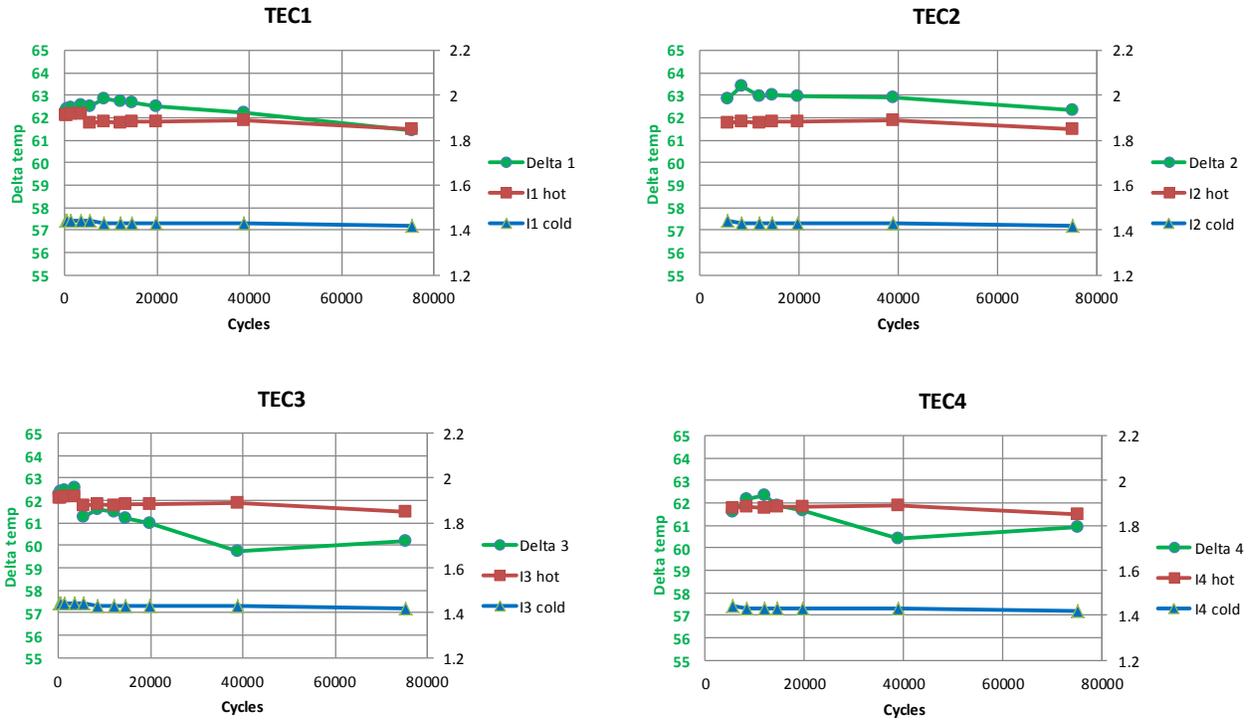


Figure 14.- PTC results with high temperature solder

**Temperature/Humidity/Bias Results**

One TEC was subjected to temperature/humidity/ power bias testing. Below are the results:

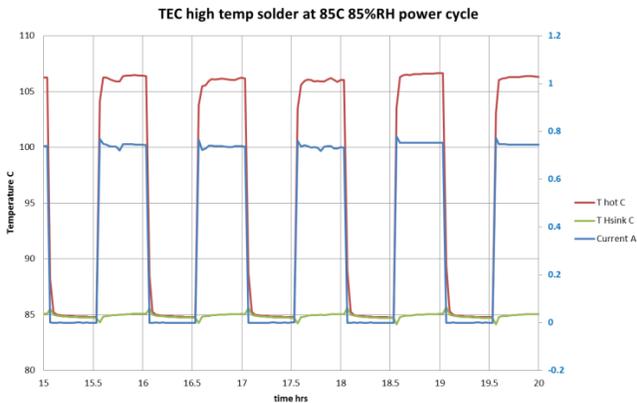


Figure 15.- Initial data (time ~0hrs)



Figure 16.- Final data (time ~1000hrs)

Practically no change in current drawn was observed up to 970 hours. The only difference observed at the end of the test is that a current spike transient was now present.

The delta temperature of the hot plate decreased a little, initially the delta temperature was 22C, at 970hr the delta was 21C, so some small degradation was observed.

We observed a temperature drift on the heatsink thermistor. At end of test the temperature sensor was reading 3C lower than the chamber temperature. This may be due to the temperature difference being driven by a cracked thermistor.

**Vibration Results**

Vibration testing was performed at the collimator level (the collimator acts as the heatsink). The operating vibration is applied on all three axis directions – with no failures observed. Sequentially the g-load vibs were applied only perpendicular to the radial direction, which for TEC translates to mostly compression load (by design) – with no failures observed.

Conclusions

The TEC assembly in the SSRD detector subsystem is a critical component to regulate the key detector element temperature. Through power-thermal cycling (PTC) of the current TEC assembly design, a weakness in the material stackup of the TEC was discovered. The baseline data only validated an assembly life of 1 year versus the goal of 10 years.

Through detailed autopsy/failure analysis of the failing units, the investigation pointed to a failure within the dice/solder interface. A higher temperature solder material was selected for the internal dice connection, and after PTC, THB, and vibration testing, no failures were identified, except for the potential cracked thermistor. The new assemblies can be confirmed suitable for 10 years life usage on CT scanners.

## 7. References

- [1] TEC fundamentals, [https://en.wikipedia.org/wiki/Thermoelectric\\_cooling](https://en.wikipedia.org/wiki/Thermoelectric_cooling)
- [2] Company internal document, "5250084GSP, Design For Reliability Process"
- [3] Company internal document, "DOC1455616, Electronic Assembly Reliability Qualification Guidance"
- [4] S. S. Manson, "Thermal Stress and Low-cycle Fatigue", McGraw-Hill Book Company, New York 1966
- [5] Arduino Uno controller, <https://www.arduino.cc/en/Main/ArduinoBoardUno>
- [6] Telcordia, "GR1312 Generic Requirements for Optical Fiber Amplifiers and Proprietary Dense WDM Systems"
- [7] Company internal document, "DOC 46-316745, Mechanical Environment Test Guideline"
- [8] T. Siewert, S. Liu, D. Smith, J C Madeni, "Database for solder properties with emphasis on new lead-free solders", NIST, 2002

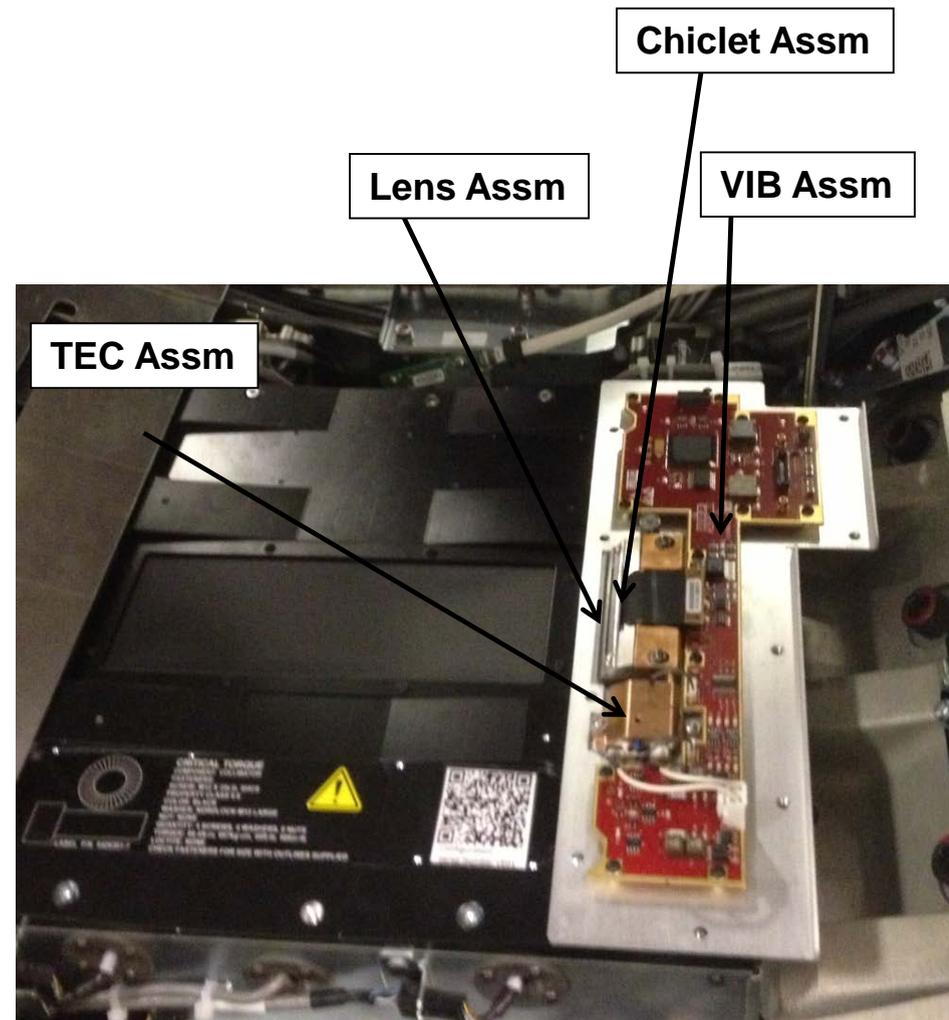
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**March 2016**

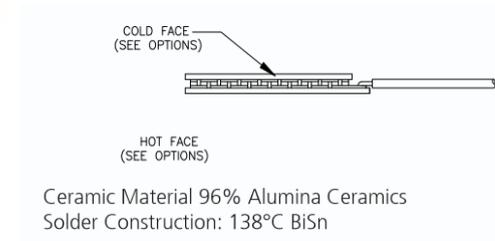
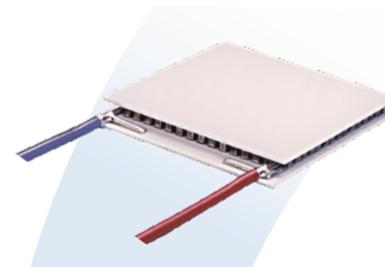
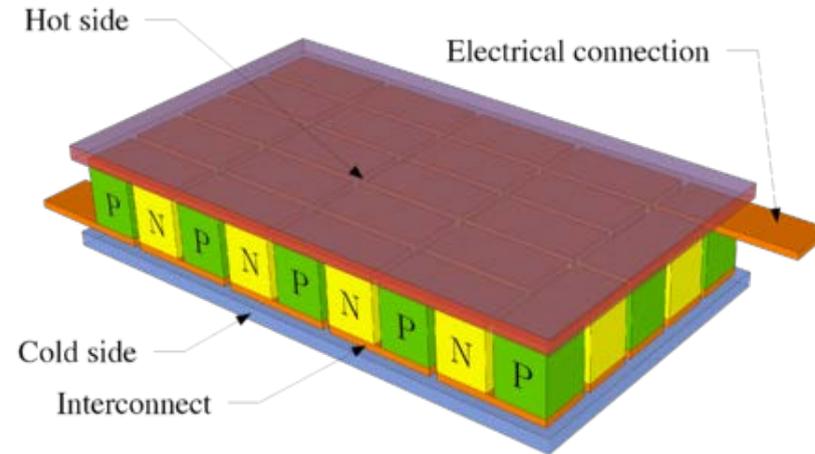
# Overview – Source Side Reference Detector (SSRD)

- SSRD – external detector close to X-ray source that measures key X-ray tube parameters and is also the main reference normalization signal for the imaging detector
- TEC Assembly – Responsible for active heating cooling of the SSRD detector element.



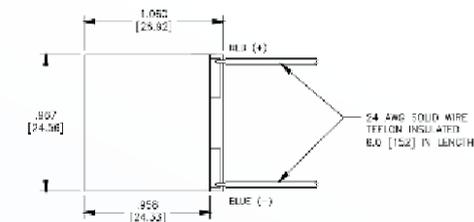
# Overview – TEC Basics

- Thermo-Electric Cooler
  - Bi-directional device that utilizes the Peltier effect to create a heat flux between the junctions of two types of materials.
  - The primary advantages include lack of moving parts, small size, long life, and a flexible shape.
  - Disadvantages include relatively high cost and poor power efficiency. Due to the electric structure of the PN junction connection
  - Both heating and cooling modes are available by simply changing the bias voltage across the electrode junctions
  - Key parameters include Qmax, Delta Tmax, and Module resistance.
- TEC selected for SSRD application was optimized for Qmax, voltage operating range and physical size.



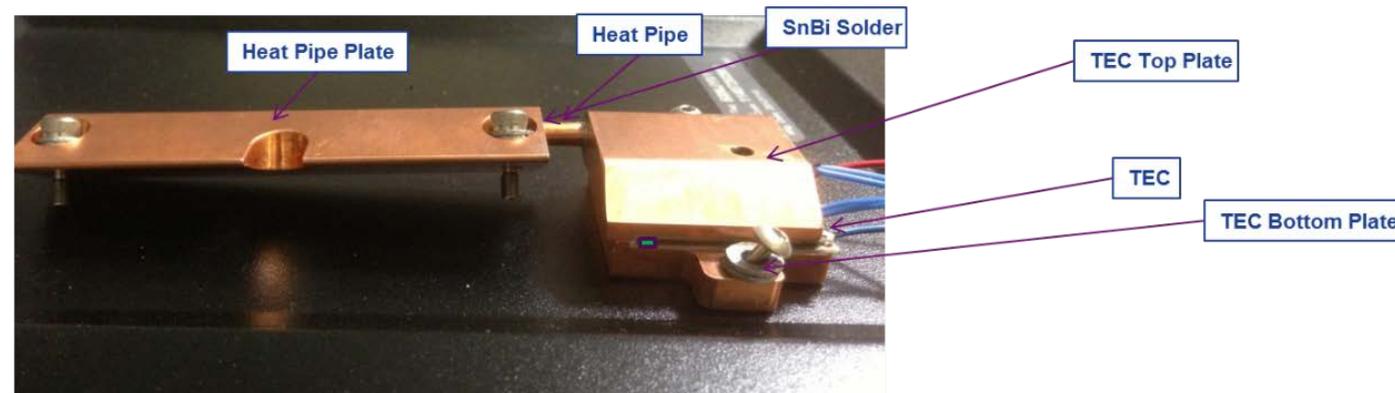
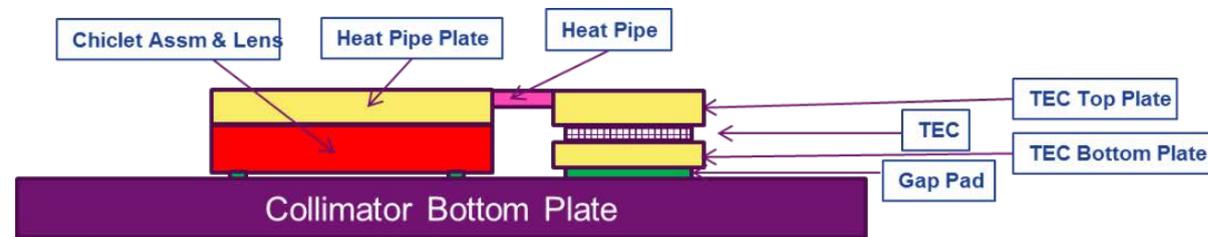
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Module resistance (ohms)	1.678	1.892

## MECHANICAL DRAWING

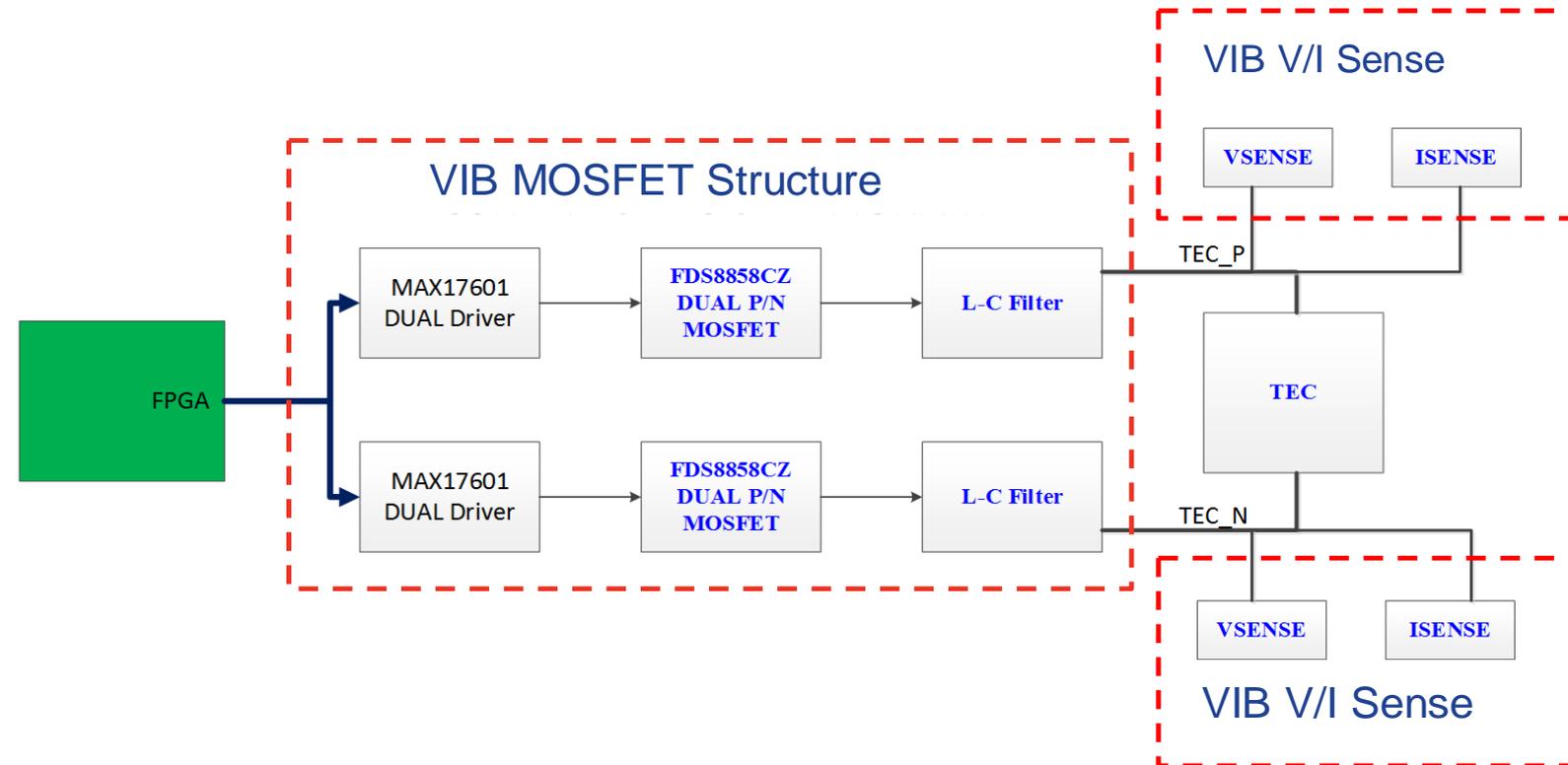


# Overview – TEC Assembly

- TEC Assembly for SSRD subsystem: Key Components
  - TEC
  - TEC Top/Bottom Plate – allows conduction from TEC to Collimator plate (sink) and to Detector element
  - Heat Pipe – heat transfer between TEC top plate and Heat Pipe plate
  - Heat Pipe plate – main interface to Detector element
  - Other consummables (gap pads and solder) are used between various TEC interfaces.
  - Key components (Top/Bottom Plate, Heat Pipe, Heat Pipe plate) made out of copper for optimal conduction



# Overview – TEC Hardware Control



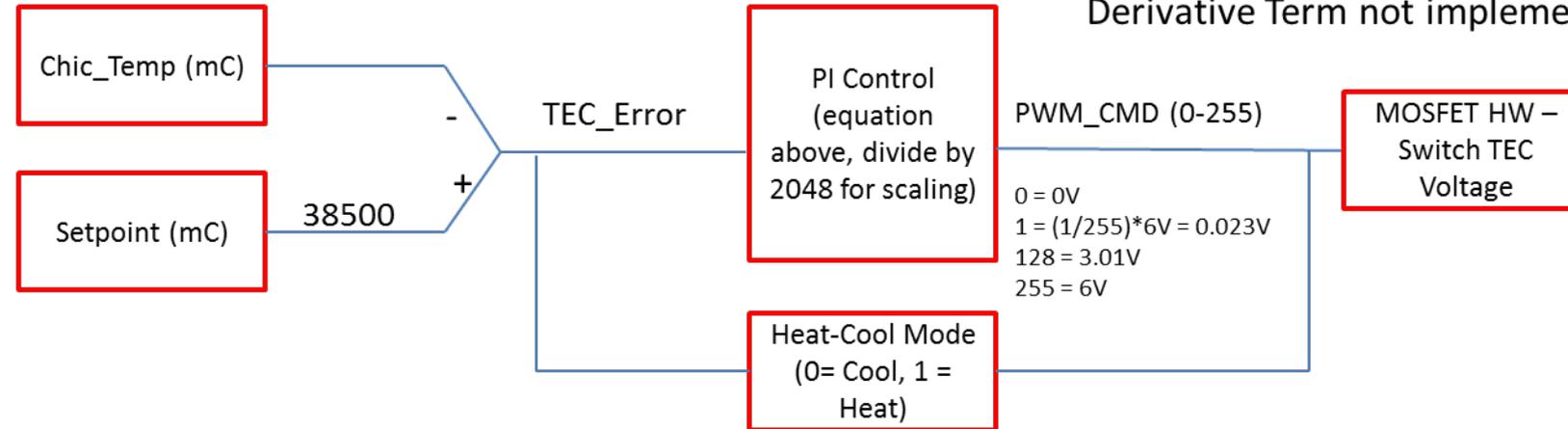
- Hardware Control Overview
  - FPGA control based (PI scheme)
  - FPGA PWM output signals feed into driver circuit – supplies current for MOSFETs
  - 2 Dual P/N MOSFETs used to create H-Bridge topology to TEC
  - L-C Filter at output of MOSFETs used to filter PWM signal to DC level
  - TEC accepts DC voltage between 0V and 6V, TEC current varies from 0A to 3A max
  - Voltage and Current sense circuitry used to monitor TEC parameters

# Overview – TEC Software Control

PI Control  
Implementation

$$PWM\_CMD(n) = Kp * e(n) + Ki * \sum e(n) + \boxed{Kd * (e(n) - e(n - 1))}$$

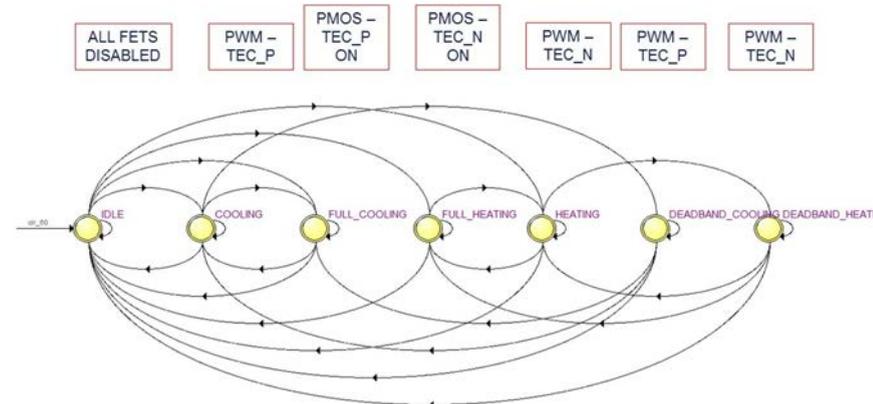
Derivative Term not implemented



- Software Control Overview

- PI equation used to generate PWM Command signal
- State machine with PWM Command signal as input to determine PWM output signals
- Deadband region implemented to avoid fast cycling on TEC
- Anti-windup feature implemented to avoid integral term saturation

PWM State Machine  
Implementation



# Overview – Detector Element



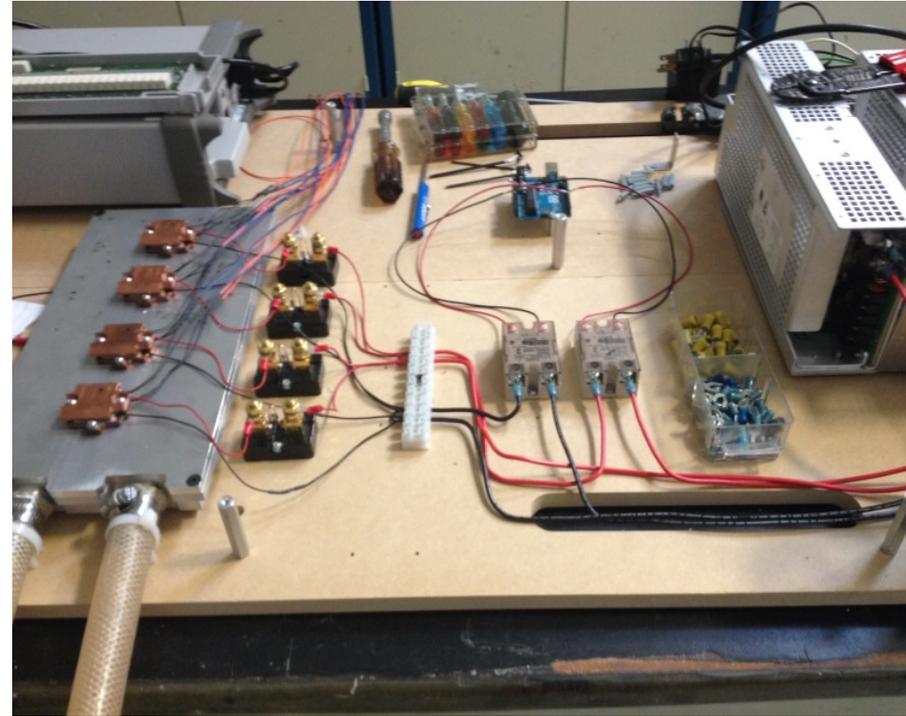
- Detector Element
  - Proprietary technology for the x-ray sensor element
  - Detector element housed in a stainless steel housing for dimensional stability
  - TEC assembly bolts on directly to stainless steel housing
  - Based on gantry environmental conditions, appropriate accelerated cycling conditions were setup for the TEC assembly.

# Reliability Assessment and Testing Plan

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Following the design for reliability process within the company, the FMEAs are used to define the reliability test plan based on failure modes/mechanisms with reliability risk.

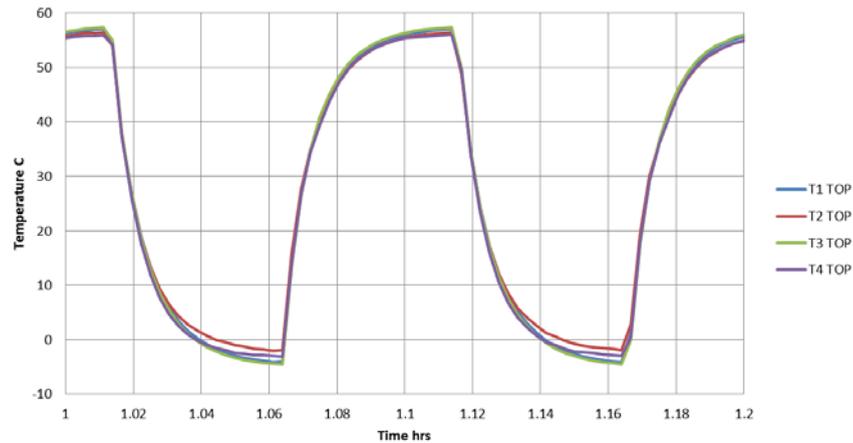
# Power-Thermal Cycle Test Setup



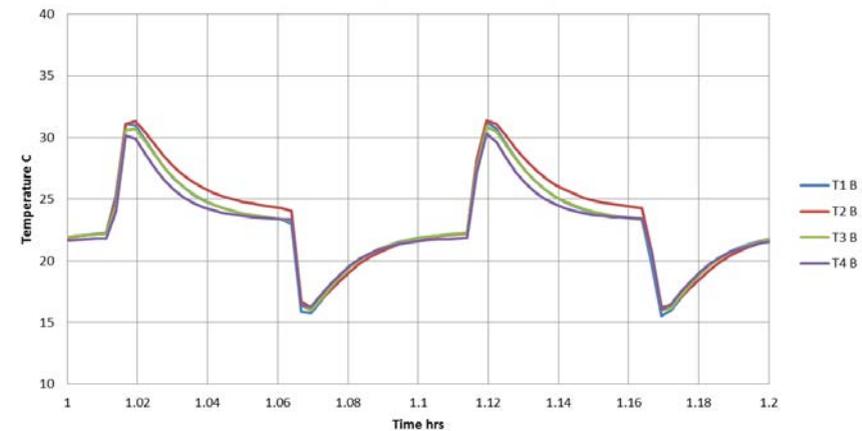
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- Two 5VDC power supplies, two SSRs (Solid State Relays) and
- A production controller [5] was used to power up the TECs and to change voltage polarity every 3 minutes
- Power supplies were connected in reverse polarity and the production controller timed the corresponding SSRs such that, at all times, only one power supply was connected to TECs

# Temperature Cycle Data

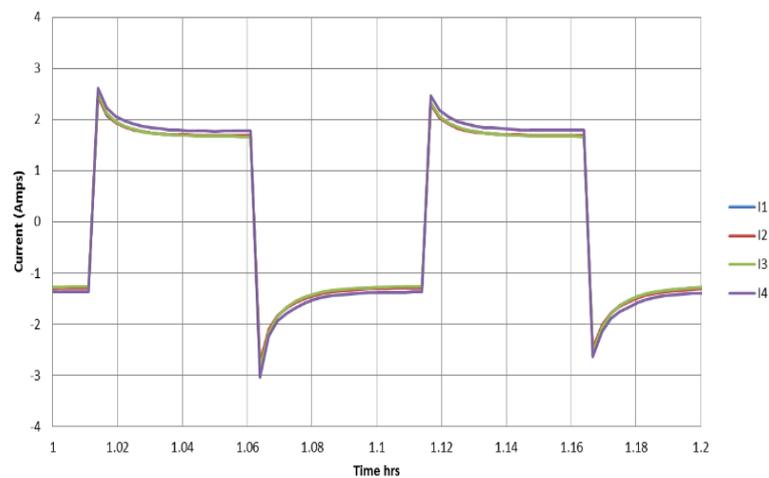
TEC upper plate temperature - cold plate at 20C



TEC heat sink temperature - cold plate at 20C



TEC current drawn



- Load plate temperature cycles from -5C to 55C
- Heat sink plate at 22C with relatively large transients at beginning of power transition
- During heating current draw is -1.3Amps and during cooling, the current draw is 1.8Amps
- Small spikes seen when voltage reverses polarity

# Temperature Humidity Bias Testing

- Temperature/humidity/bias testing was performed with similar set up as PTC testing, one module was attached to a large aluminum plate (heatsink) and power was cycled every 30 min from zero to full current. This set up was placed inside a production environmental chamber and kept at 85C and 85%RH. Plate temperatures and current drawn were monitored.
- The 85/85 testing is a standard electronic industry test, heavily used in telecom industry [6]. It is an accelerated test aim to accelerate degradations caused by process/assembly defects due to cleaning/contamination, environmental pollutants, flux residue, moisture sealant quality. Passing this test for 1000 hrs demonstrate 20 yrs in a telecom office environment

# Vibration Testing

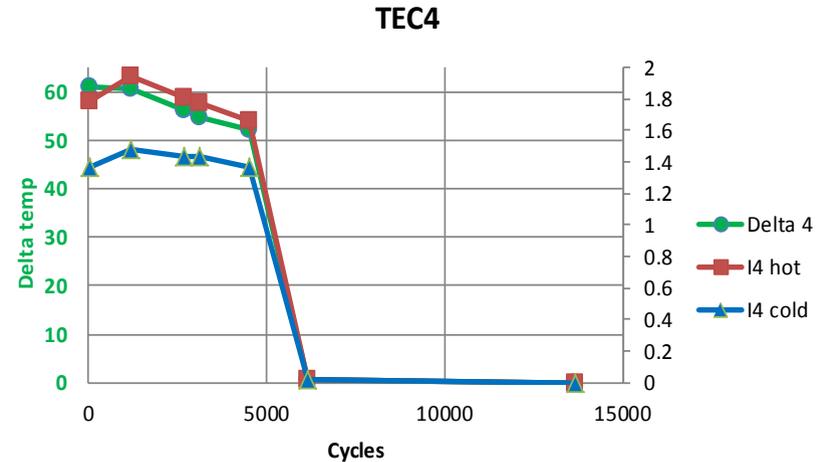
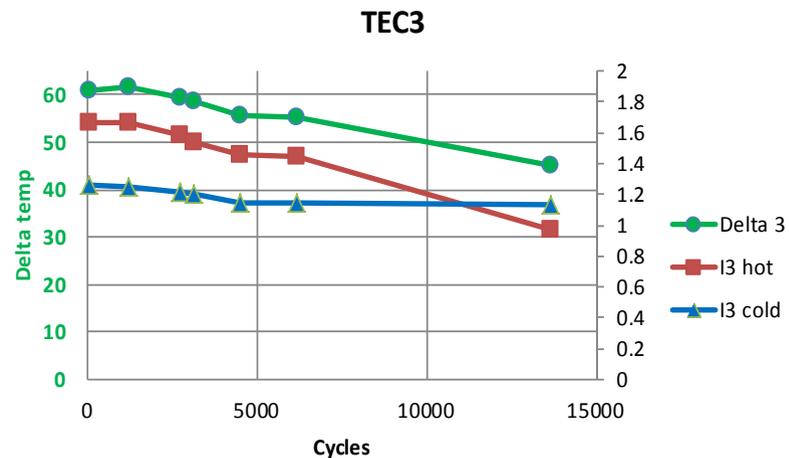
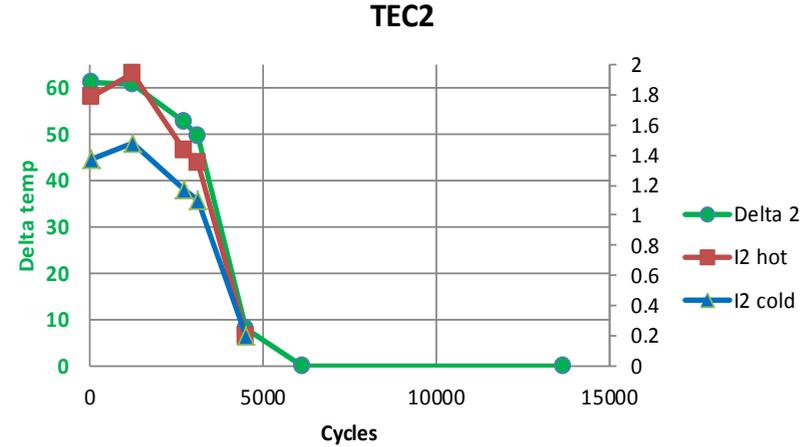
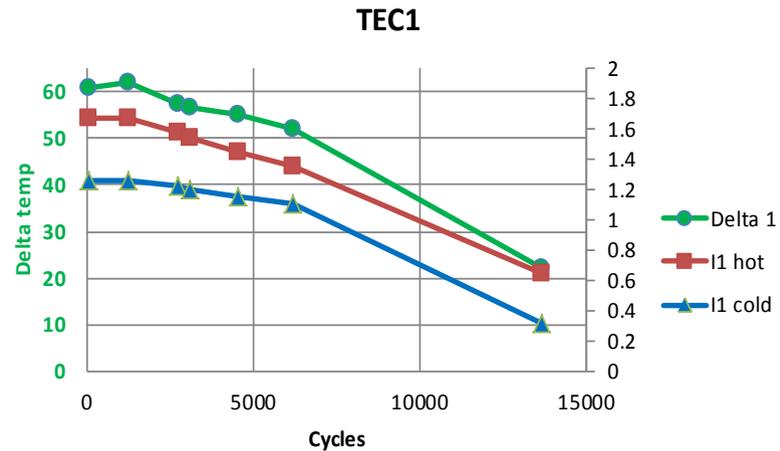
The company has developed internal standards to qualify CT scanners and subassemblies for shipping vibration/shock stresses and usage vibration in particular for mobile applications.

Any new subassembly need to pass these tests to be used in any scanner.

For CT applications and for subassemblies without moving parts the company developed an internal standard vibration based that simulates the g-load expected at the highest rotational speed patient exams.

Vibration testing was performed at collimator level, the whole structure (detector/heatpipe/TEC) was attached to collimator (which acts as heatsink).

# Initial Thermal Cycle Results



This data shows that parts cannot survive 5000 cycles. Current draw and delta temperature start to decrease after 2000 cycles for the weakest part. The best part shows decent stability up to 5000 cycles.

# Reliability Goal

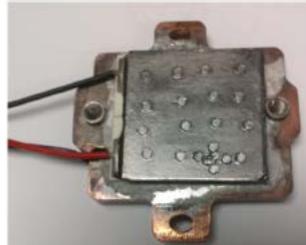
The reliability goal is to pass 7000 cycles.

Using binomial distribution, to demonstrate this goal with 90% confidence level, with four parts, we need to run for 38k cycles without failures.

The assumption is that life means a B10 of 10yrs (B10 means 90% of parts surviving)

So current design is not meeting reliability goal.

# TEC Failure Overview and Root Cause



## • Failure Overview

- The failure symptom was a high resistance connection ( $> 200$  ohms) between the TEC terminals.
- A normal connection is less than 5 ohms AC resistance.

The AC resistance is about 219ohm, but when pressing the TEC, the resistance would fluctuate hugely.



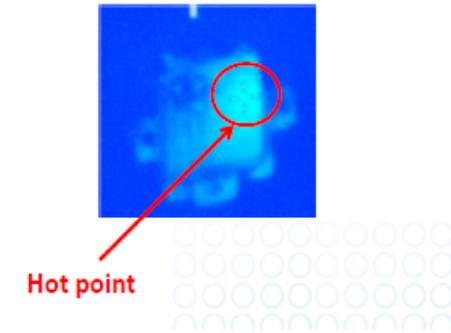
# TEC Failure Overview and Root Cause

The following standard dye-pry procedure was followed to inspect the TEC in a non-invasive manner:

- Place the sample in a beaker, then immerse sample in the dye.
- Place the beaker and sample into a vacuum chamber. Draw a vacuum for 3 minutes. Partially vent and reapply vacuum to the chamber three times to aid in dye penetration.
- Turn off vacuum pump and leave the sample in the dye for 5 minutes under vacuum.
- Vent any remaining vacuum and remove sample.
- Dry the sample in an oven by baking at 100C for up to 50 minutes.
- Remove sample from oven, and cool down.
- Pry sample by mechanical force.
- Inspect sample using microscope to check internal condition of sample.

2.2 Checked the IR image by IR image instrument

The TEC have a serious hot point, see right picture.

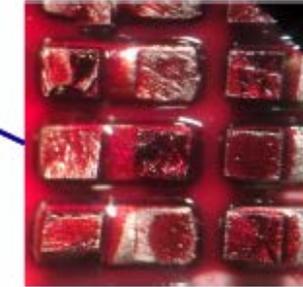


Hot spot determined using IR Imaging, standard destructive autopsy performed on TEC.

# TEC Failure Overview and Root Cause

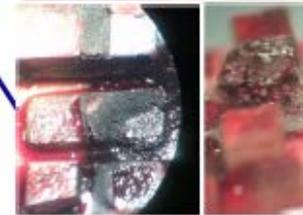


Dice shift  
Picture 2



Dice cracked

Picture 1



Dice burned

Picture 3

Evidence of dice cracking, shifting and burning observed within TEC

Through these observations, more likely the TEC got damaged by an uneven external force during assembly process. The thermal excursions likely propagated the die microcracks and eventually caused the resistance increase.

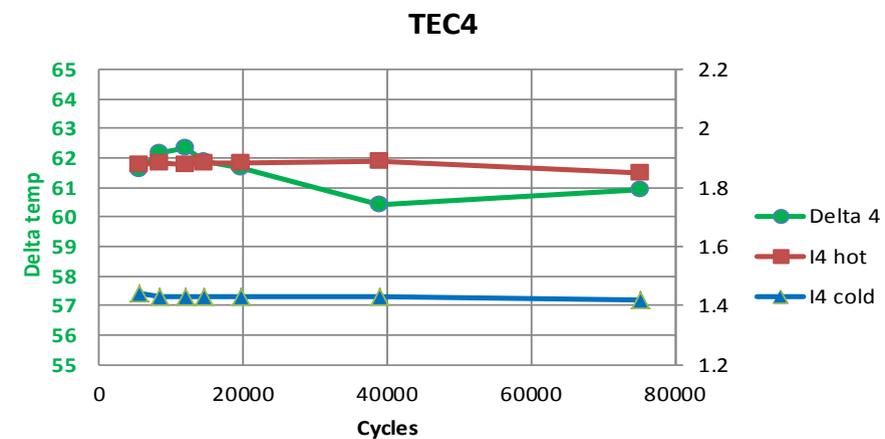
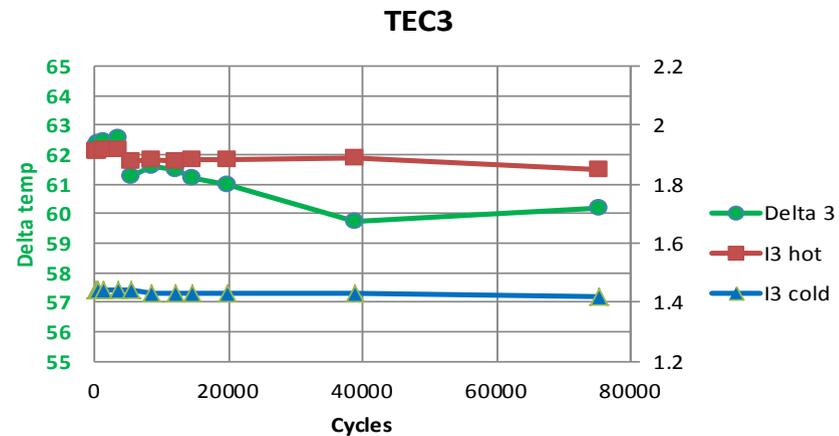
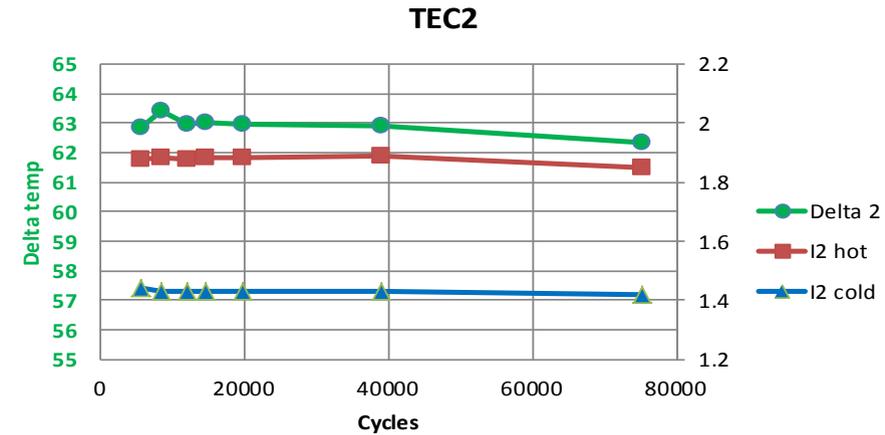
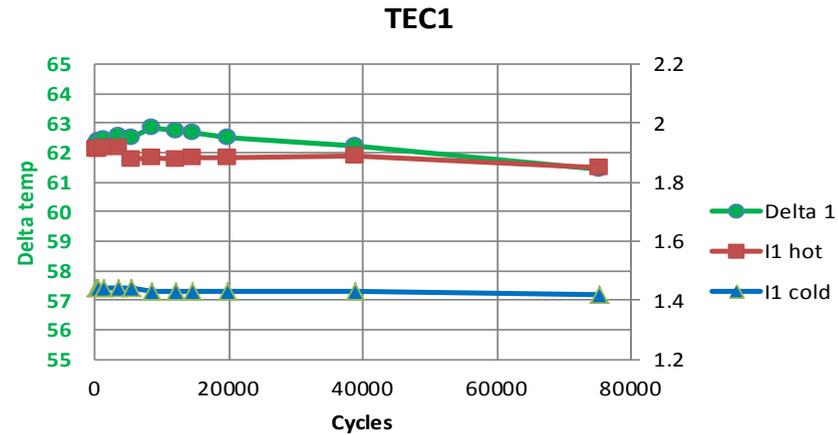
# TEC Design Change – High Temp Solder

- Based on this autopsy/ failure analysis investigation, a design change to the TEC dice solder material was proposed.
- The new solder is a high temperature solder material that would withstand the high thermal excursions.
- Samples with the new solder material were created by the vendor and given to the company for further cycling.

	Temperature liquidus ( C)	Elastic Modulus (GPa)	Tensile strength (Mpa)	CTE (um/mC)
Sn 58%Bi	138	11.9	60.4	15
Sn 5%Sb	232	44.5	35.2	20

The higher temperature solder seems not to be the ideal candidate, it is a bit stiffer and has lower strength, CTE wise comparable. Likely process parameters were as important or more so such as load-plate screws torque control, solder height, and flatness

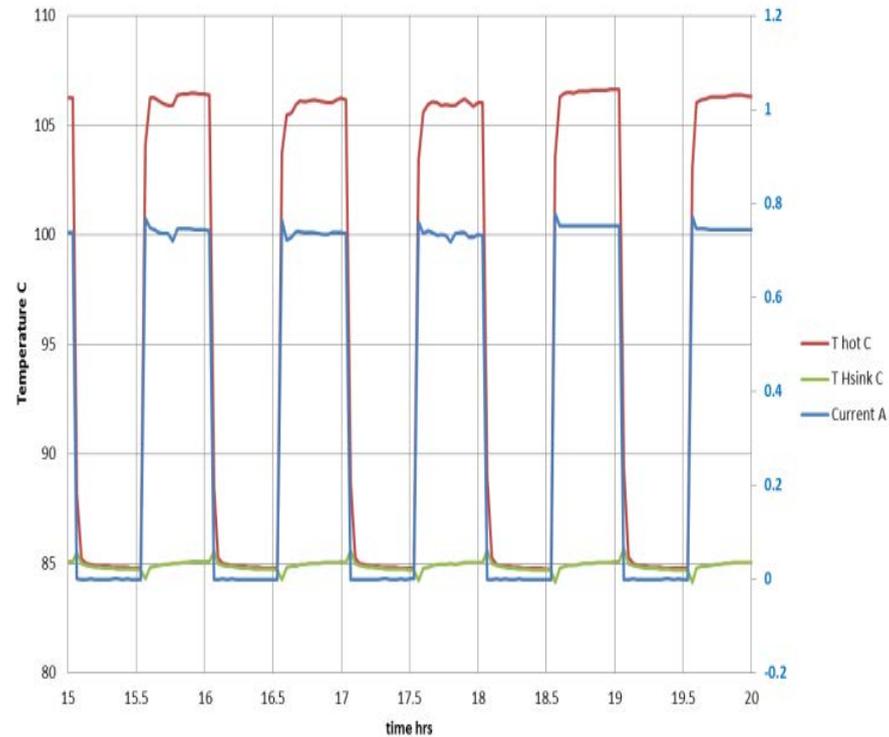
# High Temperature Solder PTC Results



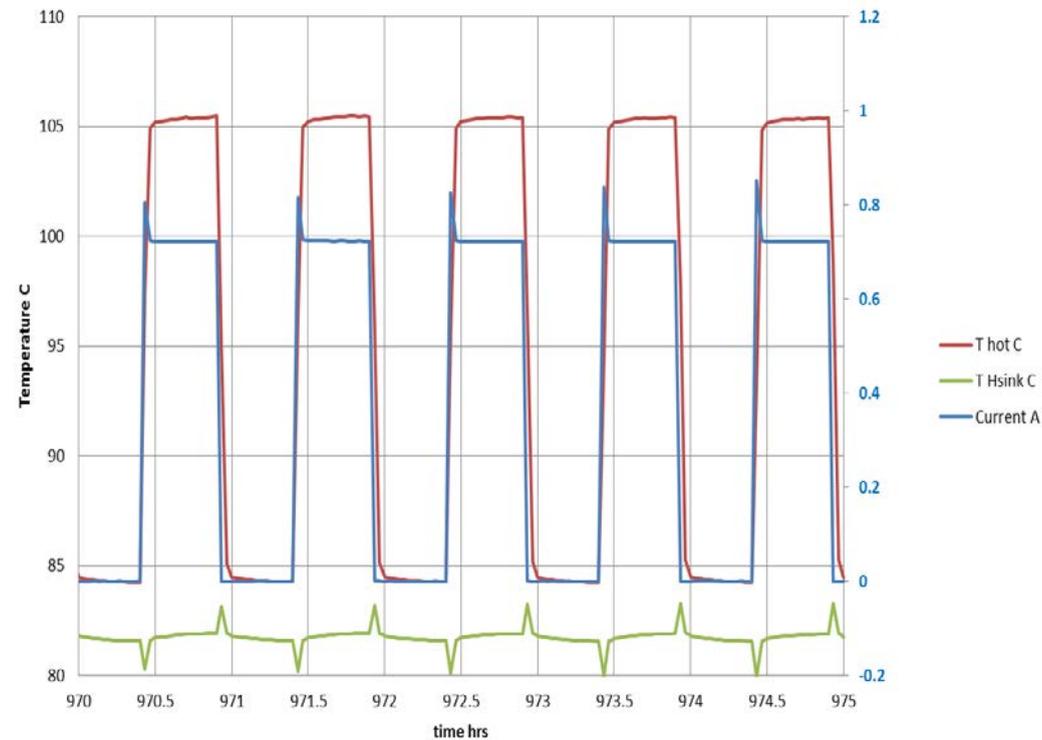
The PTC data on high temperature solder TEC's shows great improvement. No current degradation up to 80 thousand cycles, parts still under test beyond this cycle count. Only two degree Celsius degradation on delta temperature, TEC3 and TEC4 show higher degradation since these modules are not thermally isolated

# High Temperature Solder THB

TEC high temp solder at 85C 85%RH power cycle



TEC high temp solder at 85C 85%RH power cycle



Practically no change in current drawn observed up to 970hrs. The only difference observed at end of test is that a current spike transient is now present

The delta temperature of hot plate decreased a bit, initially the delta temperature was 22C, at 970hr the delta was 21C, so some small degradation observed.

We observed a temperature drift on the heatsink thermistor. At end of test the temperature sensor is reading 3C lower than the chamber temperature. We think this temperature difference is driven by a cracked thermistor.

# High Temperature Solder Vibration

Vibration testing was performed at collimator level (the collimator acts as heatsink).

The operating vibration is applied on all three axis directions – no failure observed.

Sequentially the g-load vibrate was applied only perpendicular to radial direction, which for TEC translates to mostly compression load (by design) – no failures observed

# Conclusions

The TEC assembly in the SSRD detector subsystem is a critical component to regulate the key detector element temperature. Through power-thermal cycling (PTC) of the current TEC assembly design, a weakness in the material stackup of the TEC was discovered.

The baseline data only validated an assembly life of 1 year versus the goal of 10 year. Through detailed autopsy of the failing units, the investigation pointed to a failure within the dice/solder interface.

A higher temperature solder material was selected for the internal dice connection, and after PTC, THB, and vibration testing, no failures were identified, except for the potential cracked thermistor.

The new assemblies can be confirmed suitable for 10 years life usage on CT scanners.

# References

- [1] TEC fundamentals, [https://en.wikipedia.org/wiki/Thermoelectric\\_cooling](https://en.wikipedia.org/wiki/Thermoelectric_cooling)
- [2] Company internal document, *"5250084GSP, Design For Reliability Process"*
- [3] Company internal document, *"DOC1455616, Electronic Assembly Reliability Qualification Guidance"*
- [4] S. S. Manson, *"Thermal Stress and Low-cycle Fatigue"*, McGraw-Hill Book Company, New York 1966
- [5] Arduino Uno controller, <https://www.arduino.cc/en/Main/ArduinoBoardUno>
- [6] Telcordia, *"GR1312 Generic Requirements for Optical Fiber Amplifiers and Proprietary Dense WDM Systems"*
- [7] Company internal document, *"DOC 46-316745, Mechanical Environment Test Guideline"*
- [8] T. Siewert, S. Liu, D. Smith, J C Madeni, *"Database for solder properties with emphasis on new lead-free solders"*, NIST, 2002