High Frequency RF Electrical Performance Effects of Plated through Hole Vias

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Abstract

Plated Though Hole (PTH) vias are common in the PCB industry, however their impact on electrical performance can sometimes be unclear. The confusion can be due to several different issues. Some PTH related circuit affects are due to frequency dependency, circuit thickness, circuit construction, PTH structure and PTH function. This paper will give summaries of several different studies regarding PTH via influence regarding high frequency RF performance. The typical PTH via functions are signal transition, grounding vias and power transitions. For this work the signal transition and grounding vias will be evaluated. There are several PTH structures and some are through-circuit-via, buried-via, micro-via, etc. Evaluations were done considering through-circuit-vias and buried-vias. The varieties of circuit thickness and construction can be nearly endless, however studies will be done using 2 copper layer circuits (Grounded Coplanar Waveguide) of different thickness using different repetitive grounding via pitch which will show the effectiveness of propagation mode suppression as it relates to different frequencies. Another circuit construction will be considered for evaluating signal vias by using buried vias and through-circuit-vias in a 4 copper layer circuit design. This multilayer construction will evaluate the different PTH vias in regards to frequency dependencies. Additionally, the impact of back-drilling through-circuit-via signal vias will be considered as well.

Introduction

Multilayer circuits are common in today's high frequency or high speed digital PCB applications. There can be very large differences in these two different PCB design concepts, where the design emphasis for high frequency RF circuits may be very different than the concerns for high speed digital circuits. In some cases the design will have the signal trace transiting from one copper plane to another through plated through hole (PTH) vias. As a general statement PTH vias are used in three manners:

1. they are used to transition the signal trace (or data traces) to other copper planes,
2. they are used for grounding and
3. they are sometimes used to transition high current / power traces to other conductive planes.

In this study, most of the attention will be related to the transitioning of a signal trace from plane-to-plane. This type of transition is typically avoided at all costs for the high frequency RF applications however due to the nature of some new technologies, these transitions are becoming more desired. There are some applications where high speed digital signals are transitioned through different conductive layers, again this is not desired, but many times necessary. The electrical concerns for both of these applications have some concerns in common, like impedance anomalies due to the via. These two types of applications have some differences of concern where the high frequency RF is more concerned with return loss, insertion loss and clean wave propagation and the high speed digital designs have similar concerns with the added caveat of signal integrity of the digital pulse and eye diagrams.

A quick description of the different via constructions used in this paper follow. There are PTH vias that go through the entire thickness of the circuit (thru-circuit via) and there are buried vias which are connecting only a few inner layers together and do not go through the whole thickness of the circuit. There are also micro-vias which are similar to the buried vias where they do not go through the entire board and are isolated to connecting just a few conductive layers, but these vias are typically at the surface of the multilayer and then via down to other layers which are not too distant. The micro-vias are as the name implies and are capable of very small vias.

Back drilling is often done to minimize the PTH stub length of a thru-circuit via. This is often done to minimize several issues such as radiating energy in the via area, smooth impedance reflections, improve return loss, improve signal integrity and eye diagram performance. The desired length of the PTH to be removed is related to wavelength and / or pulse rise time.

The test vehicle which was used for this study is defined as a 4 conductive layer PCB, using common high frequency laminate and prepreg. The circuit construction and different via structures that will be considered in this study are shown in Figure 1.

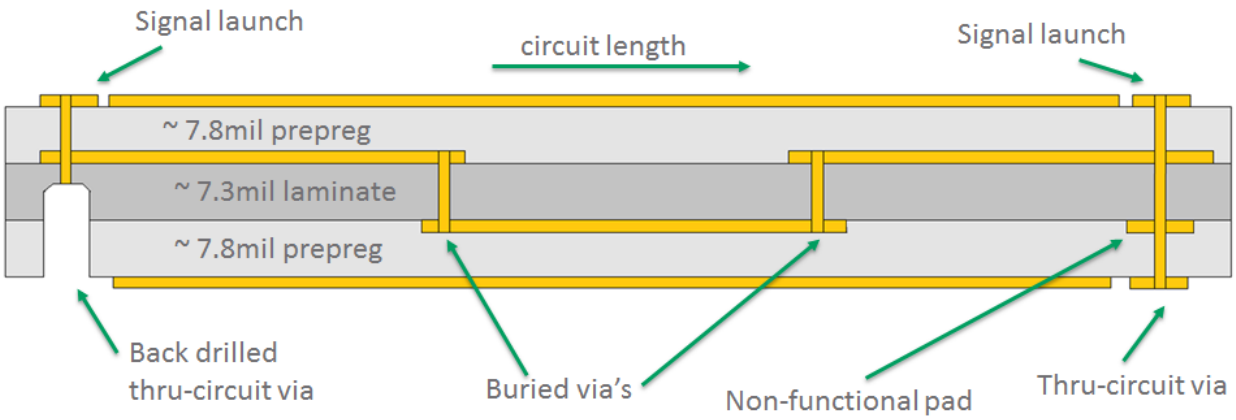

Figure 1. Cross-sectional view of the test vehicle for this study with via definitions.

The high frequency circuit materials used to construct the test vehicle were two plies of 4mil ceramic-filled, glass reinforced hydrocarbon prepreg (A) between copper layers 1 (top) and 2 and copper layers 3 and 4 (bottom). The laminate used for this test vehicle was 7.3mil ceramic-filled, glass reinforced hydrocarbon laminate (B) and the different via structures which are considered in this study are shown in Figure 1.

In some cases the signal via transitions shown in Figure 1 as buried vias, were also considered with thru-circuit vias. In this study there were also comparisons between the signal launch via being a thru-circuit via as compared to a back-drilled via. The signal launch via is where the connector from the outside world, transfers energy into the multilayer stripline structure. As a specific example and to ensure clarity of the test vehicle, in Figure 1 this is a stripline transmission line, using two buried vias which gives two layer-to-layer transitions between the input and output, which are the signal launch vias on the left and right sides of the picture, respectively. For this study, the signal launch vias for a particular circuit under evaluation will always have the same via construction on both ends of the circuit, even though Figure 1 shows them different.

Simple Overview of transmission lines, via electrical definitions and impedance

The transmission line circuit can be defined in schematic form as a simple circuit using a resistor, inductor, capacitor and inverse-resistor. The property of the inverse-resistor is given in terms of conductance, which is the inverse of resistance. For a simple example, Figure 2 shows the lumped element version of a microstrip transmission line circuit.

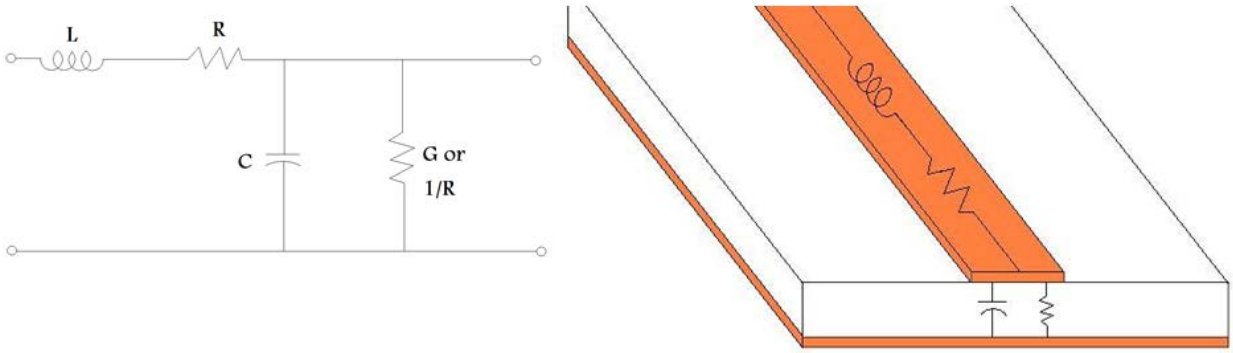

Figure 2. Lumped element representation of a microstrip transmission line circuit.

The lumped element illustration for the transmission line circuit is typically valid for very low frequencies where the voltage amplitude and phase do not have a significant change from one point to another along the transmission line. It can be seen that the signal conductor is associated with a series resistor and inductor and the dielectric is associated with a shunt capacitor in parallel with the inverse-resistor. An important point to make here is the capacitance is the parallel plate capacitance between the signal conductor and the ground plane. As an example, when the signal conductor is widened there will be an increased capacitance due to more area between the parallel plates of the signal conductor and ground plane.

Additionally if the signal conductor remains the same width, but the copper is made thicker, then the impedance decreases which is associated with either a decrease in inductance or an increase of capacitance. The lumped element representation is good to understand the basics of the transmission line structure, however for high frequency and high speed digital applications the appropriate illustration of the transmission line is a distributed representation. Lumped element assumes there is no significant difference of voltage amplitude and phase along the transmission line, but distributed representation does assume these differences to be significant. Figure 3 illustrates the distributed representation of the microstrip transmission line circuit.

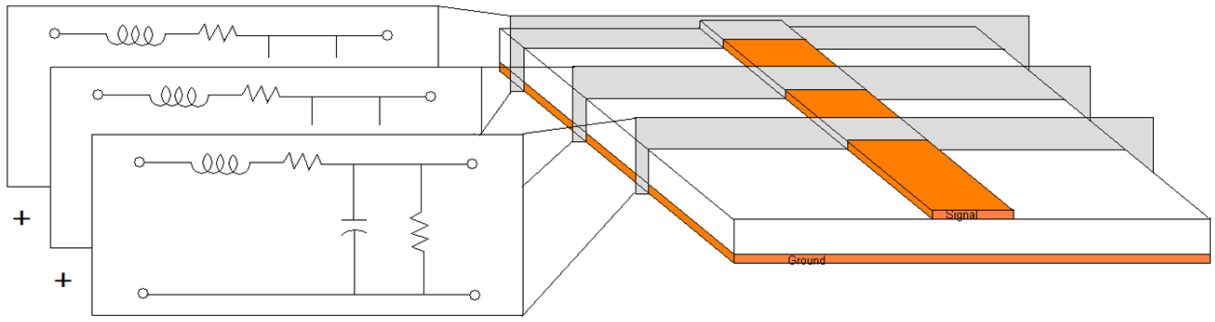

Figure 3. Distributed representation of a microstrip transmission line circuit, as should be used for high frequency RF and high speed digital applications.

The distributed representation makes use of the same lumped element schematic however it is applied to discrete thin slices of the circuit, where each slice will have a slightly different voltage amplitude and phase depending on the frequency dependent wavelength of the applied signal.

There are many different models for the PTH via and the model which is shown in Figure 4 is from a study by Wang, et al. [1], which describes the procedure to predict the impedance of the via with closed form equations.

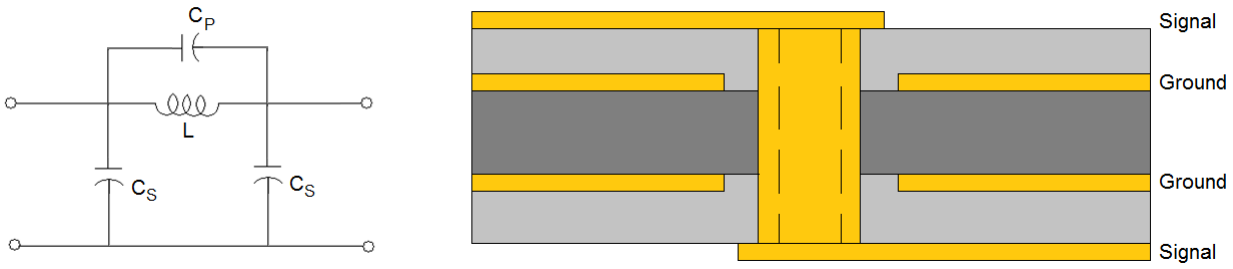

Figure 4. An illustration of a PTH via per Wang, et al. [1]

The representation of the via shown in Figure 4 which is used to transition the signal conductor from the top to the bottom of this double microstrip circuit, has several capacitance properties to consider. The variable C_S is a little more complicated than first glance. This variable is partially due to the normal microstrip shunt capacitance when applied to the microstrip transmission line segments which are on top and bottom of the multilayer circuit. Additionally the C_S variable has the capacitance due to the inner layer ground planes and the gap between these

ground planes and the PTH via sidewalls. The variable C_P is the parallel capacitance in regards to the series inductance due to the PTH via itself. This capacitance is due to open ended fringing of the signal conductor at the via transition on the signal layer, which is on top and bottom of the multilayer.

The transmission line and PTH via models shown here are simpler compared to the stripline test vehicle that will be used in this study. The representations shown here are for instruction only, however the basic and important capacitance-inductance relationships discussed do apply to the stripline structure.

Now we will put together some of these concepts which will be evaluated in this study, as it relates to capacitance. If the inner layer ground plane gaps next to the PTH via are varied that will cause a difference in capacitance. A smaller gap will increase capacitance. Additionally a PTH via with more metal, such as larger via hole diameter, will increase capacitance. Also a short PTH via (back drilled) will decrease capacitance. The circuit pad size and the anti-pad size can also influence capacitance, where an increase in the circuit pad size will cause an increase in capacitance and an increase in the anti-pad diameter will cause a decrease in capacitance.

The emphasis on capacitance or inductance is a practical matter for a designer wanting to fine tune a design, where the PTH via has minimal impact on the high frequency performance. Ideally this is done by the via having the same characteristics as the signal conductor which it transitions. More specifically, when viewing the entire circuit by an impedance curve, the via transition should be the same impedance as the transmission lines, or in other words there would be no impedance anomaly where the signal transition vias occur along the entire length of the circuit.

Modeling impedance for a transmission line is relatively simple by using closed form equations, software or field solving software. However modeling impedance of vias can be more difficult. The best way to perform a via model is with the use field solving software. These softwares are typically expensive and can be very time consuming to achieve an accurate model. The use of closed form equations is typically easier and much faster, however the accuracy is not as good as the field solvers. Additionally there can be empirical data collected, which is time consuming and easy, but at some cost. Once the circuit construction is fixed, a simplified version of the design can be fabricated to have circuits which can be evaluated to understand the impact of different PTH via designs on the transmission line. This study used empirical data collection from many circuits made with different via designs.

Signal launch via experiments

The experiments for signal launch are simply the comparison between the signal launch vias with thru-circuit vias and back-drilled vias. Keeping the via structure comparison simple is advantageous because with less variables it is easier to understand what via design change will cause a via performance change. Signal launch is critical for any high frequency design, because it is signal launch that can make or break a design. If the energy is not transferred efficiently into the stripline due to poor signal launch, then the circuit performance is limited mostly by the quality of the signal which is incident on the stripline signal conductor.

In an effort to compare signal launch via constructions, initially the impedance curves will be evaluated and then other circuit attributes. The test vehicle is as shown in Figure 1, but the signal launch vias are the same on both ends of the circuit; one circuit has thru-circuit signal launch vias for both connectors and the other circuit will have back-drilled signal launch vias. The circuit is a 2 inch long stripline circuit with no transition vias in the body of the circuit. The test vehicle is strictly a standard stripline transmission line circuit and comparing the signal launch attributes of the different via structures, in regards to impedance is shown in Figure 5.

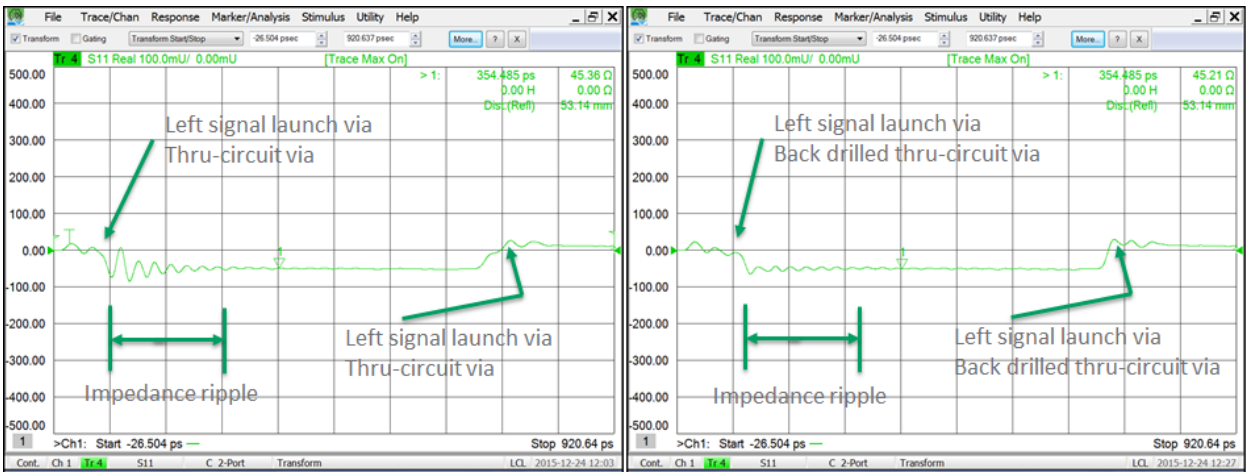

Figure 5. Impedance curves (green curves) for a 2 inch stripline transmission line circuits with two different signal launch via constructions.

The impedance curves are generated from using a PNA (Performance Network Analyzer) capable from 10 MHz to 67 GHz and placed in time domain mode. The time domain mode uses the basic frequency domain measurements of the PNA, performs an inverse Fourier transform on the frequency dependent reflection coefficient and generates an impedance curve as shown in Figure 5. Considering the very wide frequency bandwidth, the transform will yield a pulse rise time of 5.3 ps, which gives very accurate impedance results. The connectors used in this study were 2.4mm compression contact connectors. With these connectors there is no soldering and the connection is made by pressure contact. This is very good for a study such as this, giving more consistency to the signal launch comparison since the same connectors can be used on the different circuits. Additionally since the connectors are not matched, it was necessary to ensure the orientation for each connector is kept consistent in regards to which port the connectors were used.

The impedance curve (green curve) shown in Figure 5 is for the S11 curve of the network and that basically means the impedance is a reflection measurement in regards to port 1 of the PNA, which relates to the connector on the left side of the circuit. There is also a reference marker placed in the body of the circuit at about 354 ps from the reference plane of the S11 curve (port 1 reference plane). The reference plane was established by an SOLT calibration (Short, Open, Load, Thru) and that plane is the contact interface between the connector on the circuit and the connector for the PNA cable.

In Figure 5 it can be seen that the impedance ripple is minimized for the circuit using back-drilled signal launch vias. Having less impedance ripple, means the impedance transition in the signal launch area is more efficient and the circuit performance will have less issues with return loss, radiation and overall signal integrity.

Additionally another comparison of the thru-circuit signal launch via and the back-drilled signal launch via is shown in Figure 6, which is in regards to insertion loss and return loss.

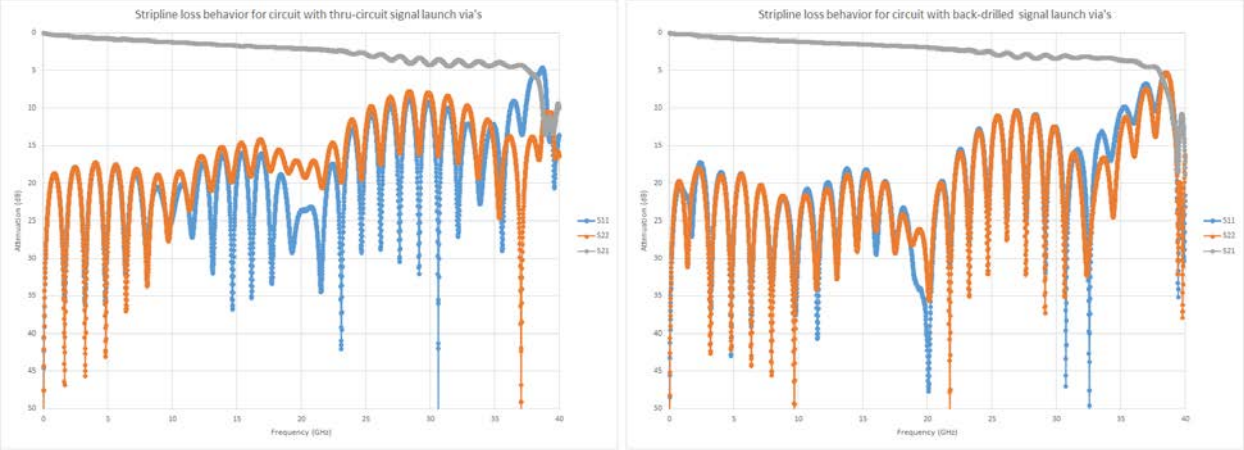

Figure 6. Loss behavior for stripline transmission line circuits with different signal launch via configurations.

The loss characteristics shown in Figure 6 are for a 2 inch long stripline transmission line circuits. The blue curve (S11) and the orange curve (S22) are the return loss curves and the grey curve (S21) is the insertion loss curve. As a rule of thumb for judging the quality of S parameter measurements for a transmission line circuit, the return loss curves should be 15 dB or greater and the insertion loss curve should be relatively smooth with a slight negative slope.

The return loss curve for the circuit with the thru-circuit signal launch vias (left chart of figure 6), violates the 15 dB return loss criteria at about 15 GHz and the circuit with the back-drilled signal launch vias violates the 15 dB return loss criteria at approximately 23 GHz. Additionally the circuits with the back-drilled signal launch vias has a smoother insertion loss curve than the circuit with the thru-circuit signal launch vias. Figures 5 and 6 demonstrate that back-drilling the signal launch vias can improve the impedance behavior as well as the loss behavior for stripline transmission line circuits. The back-drilled circuits had smoother impedance curves in the area of the signal launch and they had a wider useable band of frequencies considering the 15 dB rule for return loss; the back-drilled signal launch via option had a wider useable band by about 8 GHz when compared to the thru-circuit signal launch via circuit.

The following are the details for via design in the signal launch area: drilled via was 0.008” (0.203mm) diameter, with approximately 0.001” (0.025mm) copper plating thickness, circuit pad on all layers was 0.017” (0.432mm) diameter, the anti-pad on all layers was 0.053” (1.346mm) diameter and the back-drilling was done to remove the via up to within 2mils of the signal plane.

Layer-to-layer signal transitions with PTH vias

The next portion of this study is evaluating the signal trace transition from one inner layer to another for the stripline transmission line circuits. Ideally the transition via for the signal trace should have the same impedance as the signal trace. If there are impedance differences between the via and the signal trace, there will be more reflections, noisier impedance curve, poorer return loss, more noise in the insertion loss curve and a potential to have more radiated energy which can be detrimental to EMI (Electro-Magnetic Interference) concerns.

These studies done on signal-via-transitions from layer-to-layer all used the same signal launch construction which was the thru-circuit back-drilled signal launch via and they were all 8” (230.2mm) long stripline transmission line circuits.

The first signal transition study evaluated stripline transmission line circuits with 3 signal transitions in the body of the circuit and each of these transitions used thru-circuit vias. The impedance curves had gating applied to minimize the influence of the signal launch impedance anomalies. An impedance curve is subject to “masking”, which basically means that each impedance anomaly which varies from the calibration impedance (50 ohms in this case) will decrease the amplitude of a following impedance anomaly. As a practical example, given a 50 ohm

transmission line with two areas of impedance spikes, one spike is 55 ohms and another spike further down the transmission line is 60 ohms. The 55 ohm spike will indicate its impedance value correctly, however the 60 ohm spike will have a lower value than 60 ohms. This is what is meant by masking for impedance curves and this will be compounded with multiple impedance spikes (or dips). Additionally the spike in the impedance curve is reference to an increase in inductance and a dip in the impedance curve is reference to an increase in capacitance. To illustrate the masking, impedance issues along with the concept of the stripline transmission line circuit with three signal-via-transitions, Figure 7 shows the comparison with gating on and off.

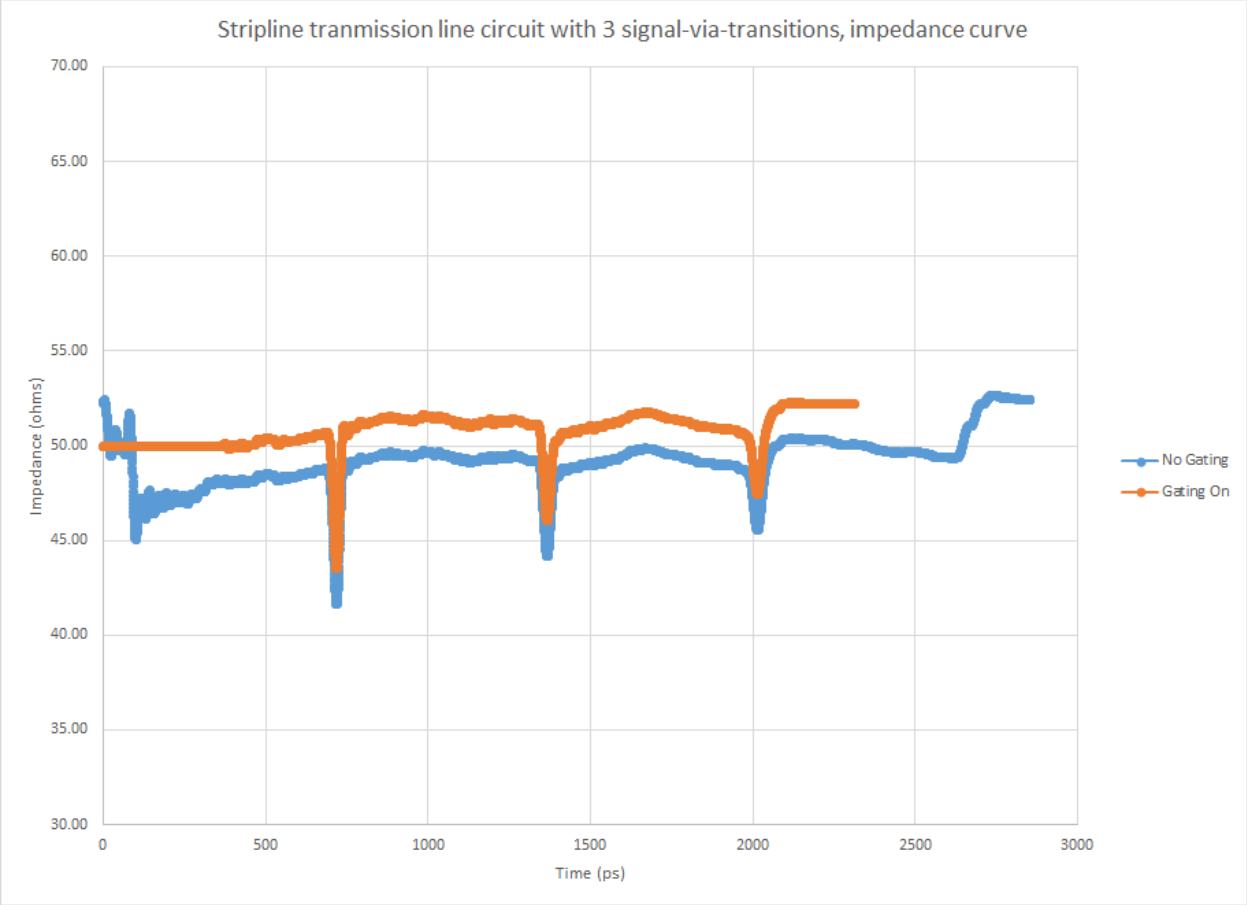

Figure 7. Impedance curves for a stripline transmission line circuit with 3 signal-via-transitions and comparing the results with gating turn on and off.

It can be seen in Figure 7 that the impedance trends are about the same for the gating being on or off, however a more accurate impedance value will result with gating on and specifically for the first impedance anomaly after the gating and in this case that occurs at about 700 ps. The gating being applied in Figure 7 is in regards to minimize the impedance anomaly with the signal launch via. With this in mind the following comparisons will be evaluating the first signal-via-transition only, with gating on and at higher resolution.

The impedance curves and the loss curves are shown in Figure 8 for the first signal-via-transition evaluation with three via transitions in the body of the 8” long stripline transmission line circuit.

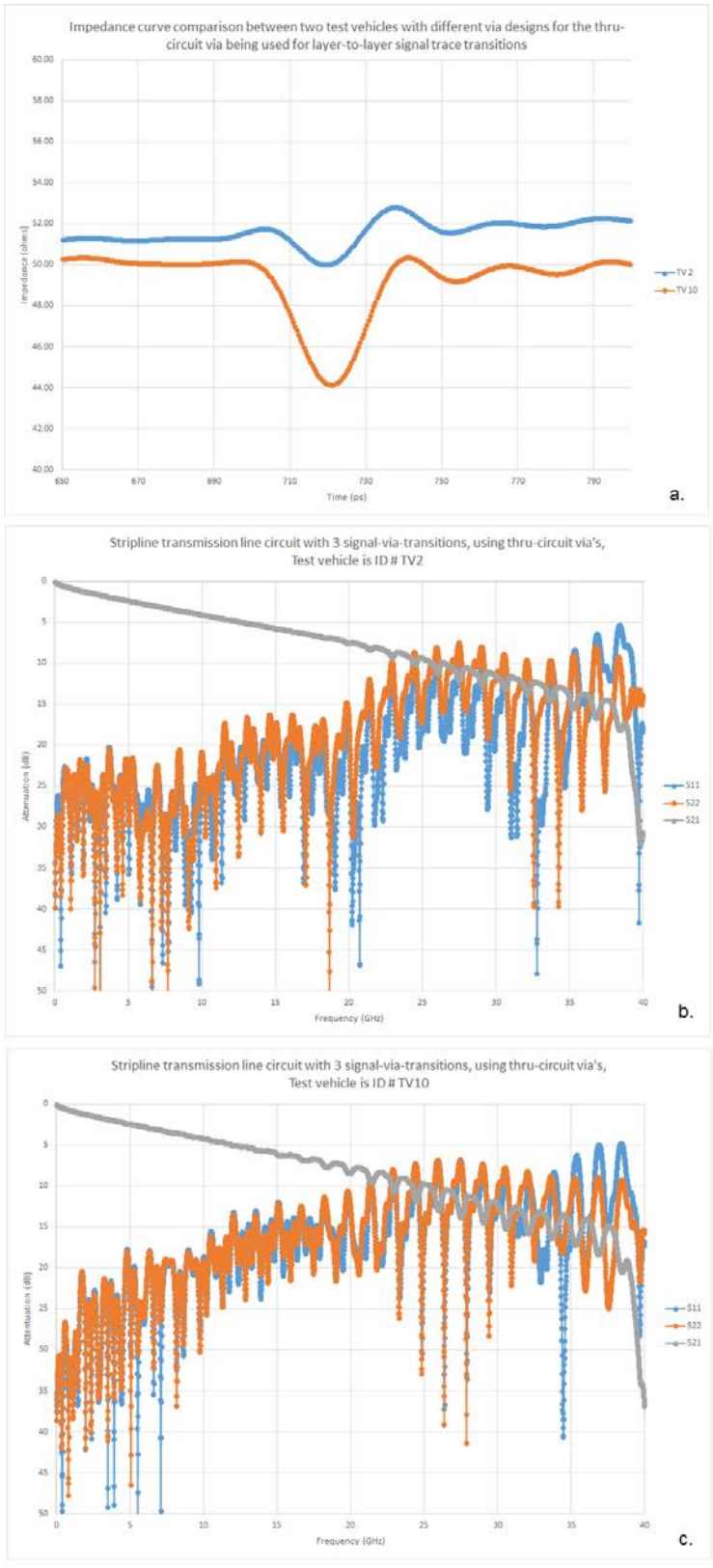

Figure 8. Electrical performance comparisons between test vehicle TV 2 and TV 10 for a.) impedance. The loss curves for TV 2 is shown in illustration b. and the loss curves for TV 10 is shown in c.

Looking at the impedance curves in Figure 8a it can be seen that test vehicle TV 2 has a smoother impedance transition as compared to TV 10. The dip in the impedance curve (lower impedance) for TV 10 suggests an increase capacitance for TV 10 as compared to TV 2. Smoother impedance transitions impacts the loss curves in a very beneficial manner. It can be seen when comparing Figure 8b to Figure 8c that the return loss allows for a much wider band of operating frequencies for the TV 2 circuit. The TV 2 circuit has good return loss up to about 19 GHz and the TV 10 circuit has good return loss to only about 11 GHz.

The next portion of this study was to make the same comparison except with buried vias being used for the signal-via-transitions and summary charts are shown in Figure 9.

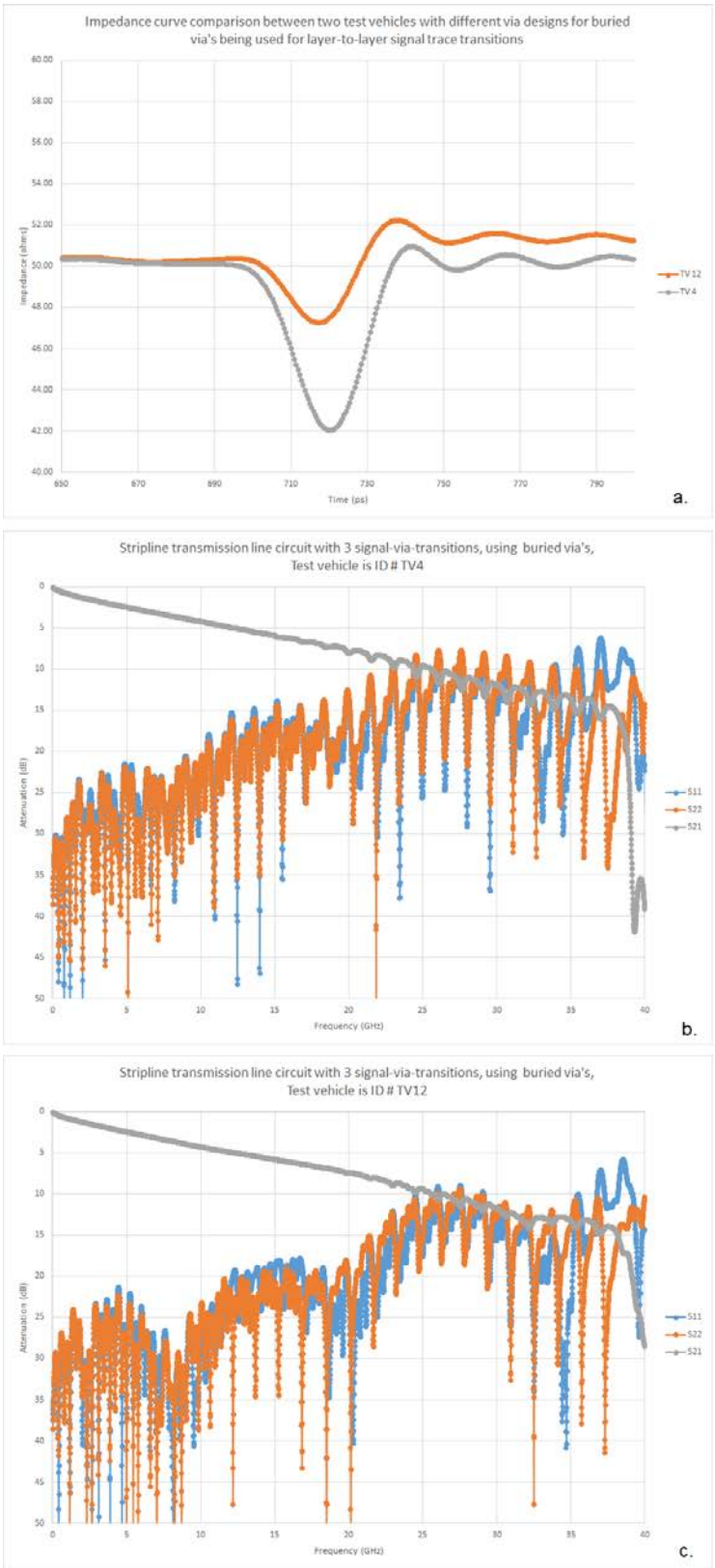

Figure 9. Electrical performance comparisons between test vehicle TV 4 and TV 12 for a.) impedance. The loss curve for TV 4 is shown in illustration b. and the loss curve for TV 12 is shown in c.

The impedance for TV 12 is much smoother than TV 4 and more importantly the impedance transition for TV 12 is centered around 50 ohms. The loss characteristics show a dramatic difference, where TV 4 has good return loss characteristics up to about 12 GHz and the TV 12 circuit had good return loss up to approximately 22 GHz. Most RF engineers would find it remarkable to have a circuit with 3 signal-via transitions which is well behaved up to 22 GHz, but it obviously can be achieved.

The information summarized in Table 1 gives design details for the different via configurations used in this study.

Test Vehicle	Type of via	Via hole diameter	Copper plating thickness (mils)	Via length (mils)	outer layer via pads		inner layer via pads		Good return loss, Freq (GHz)
					circuit pad	anti-pad	circuit pad	anti-pad	
TV 2	thru-circuit	8	1	28	20	34	20	53	19
TV 10	thru-circuit	12	1	28	24	36	24	53	11
TV 4	buried	8	1	9.5	20	34	20	53	12
TV 12	buried	12	1	9.5	24	36	24	53	22

Table 1. Summarized information regarding the stripline transmission line circuits with three signal-via-transitions.

Conclusions

In summary it can be seen that simple prototype circuits with different via designs can be used to fine-tune the via transitions for both the signal launch and the layer-to-layer signal transition. The main concern is minimizing the impedance transitions due to the vias.

As an example if a via transition has too much inductance (impedance spike up) then capacitance needs to be added to offset the inductance. The added capacitance can be done by having smaller diameter anti-pads or larger circuit pads which will increase the capacitance. If the opposite case is true and there is too much capacitance (impedance dip), then enlarging the anti-pads or making the circuit pads smaller will decrease capacitance and increase inductance.

Additionally there are several PTH via considerations. The PTH via size can be altered to adjust the capacitance and inductance, where a larger drilled via diameter will yield an increase in capacitance. A shorter via length, such as the case for the buried vias or the back-drilled vias will decrease the capacitance of the via. Lastly the copper plating thickness will impact the via impedance somewhat, where thicker copper plating will increase capacitance and thinner will decrease capacitance.

References

[1] Wang, Taoyun, et al., "Quasi-static Analysis of a Microstrip Via Through a Hole in a Ground Plane," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-36, No. 6, June 1988, pp. 1007-1013.

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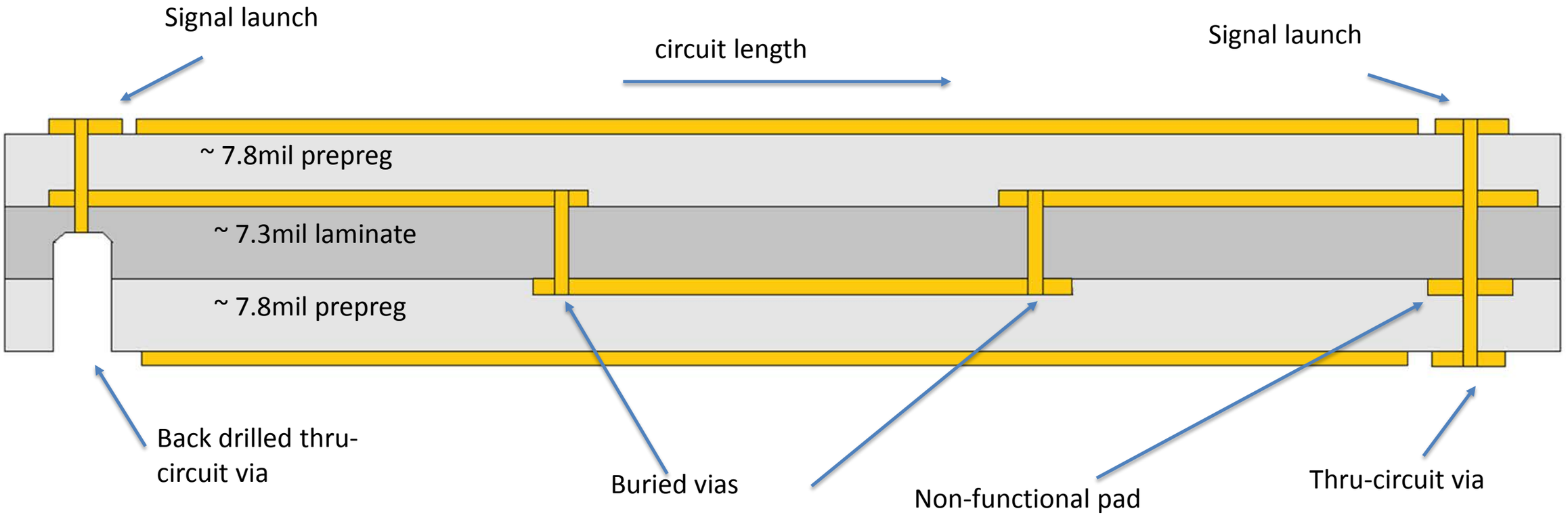
Agenda

- Test vehicle for this evaluation
- Basic overview of transmission line circuits and plated through hole vias
- Simple overview of impedance
- Signal launch via experiments
- Layer-to-layer signal via transition experiments

High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Test vehicle for this evaluation



Circuit materials used in this study:

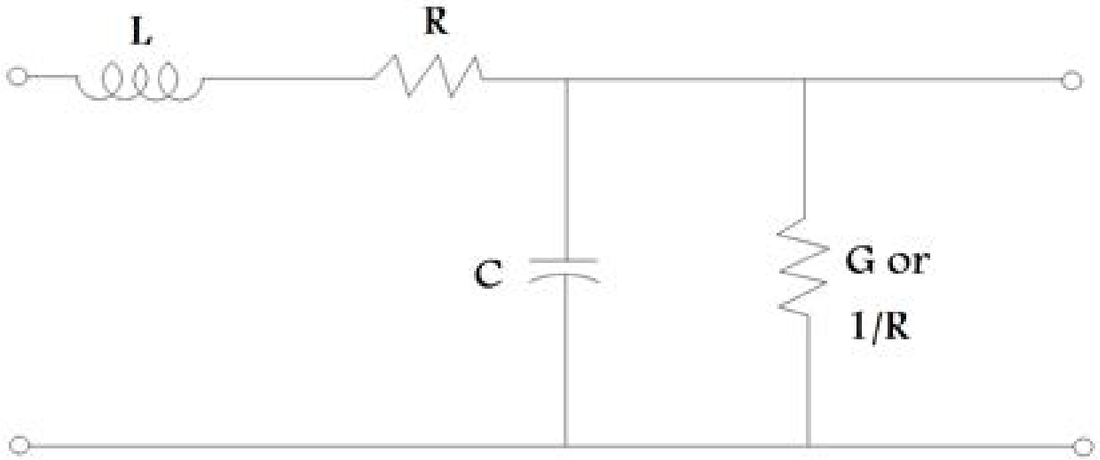
- 2 plys of 4mil *ceramic-filled*, glass-reinforced *hydrocarbon* prepreg (A) between layers 1 (top) and 2
- 7.3mil thick *ceramic-filled*, glass-reinforced *hydrocarbon* laminate (B)
- 2 plys of 4mil *ceramic-filled*, glass-reinforced *hydrocarbon* prepreg (A) between layers 3 and 4 (bottom)

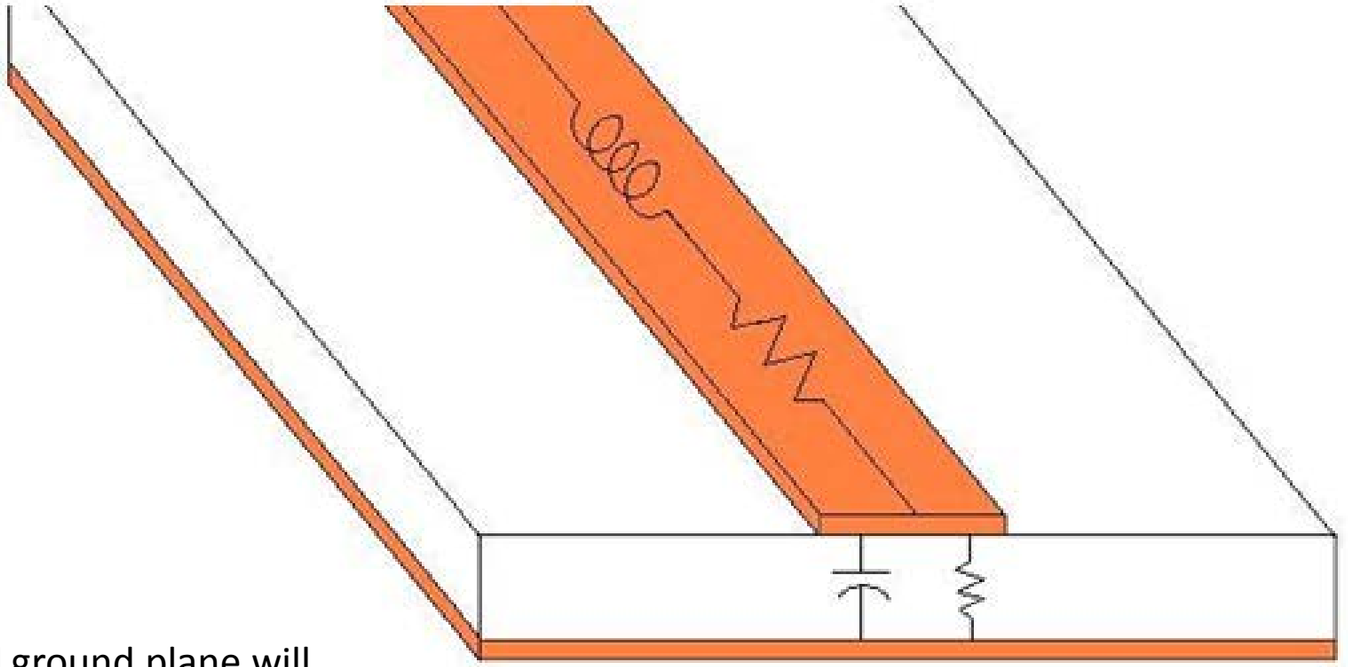
High Frequency RF Electrical Performance Effects of Plated Through Hole Vias

Basic overview of transmission line circuits and plated through hole vias

- A simple microstrip transmission line circuit can be represented by a RLGC schematic
  - R-Resistor, L-Inductor, G-Inverse Resistor (conductance), C-Capacitor

- In a practical sense, it is good to realize what PCB feature relates to inductance and capacitance



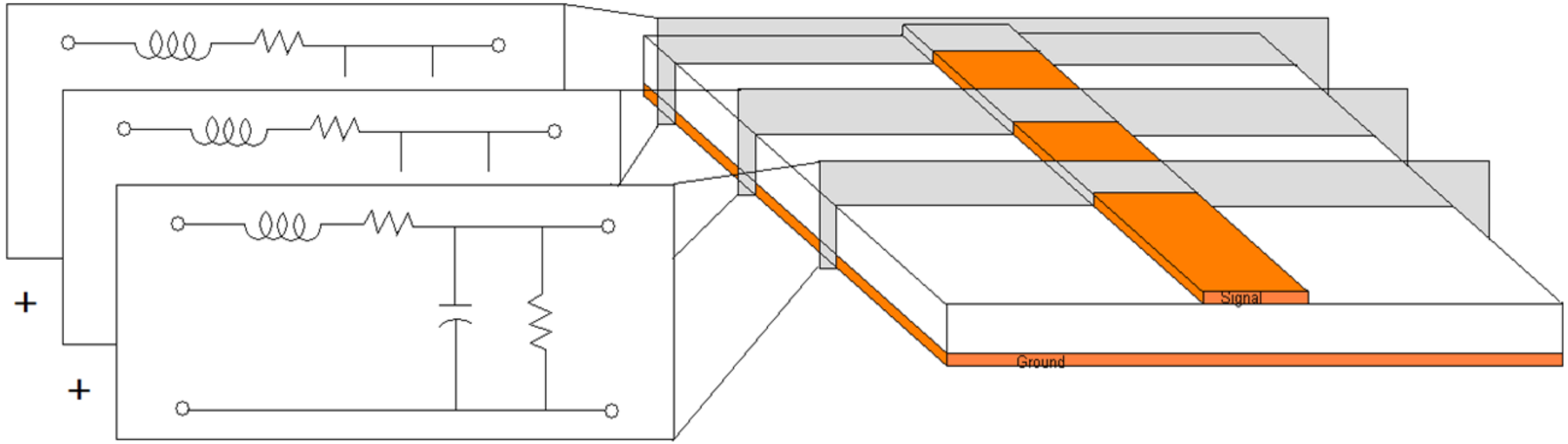


- In general
  - A more narrow signal trace will increase inductance
  - An increased area between the signal conductor and ground plane will increase capacitance; this means a wider conductor will have increased capacitance or in other words it will decrease inductance

High Frequency RF Electrical Performance Effects of Plated Through Hole Vias

Basic overview of transmission line circuits and plated through hole vias

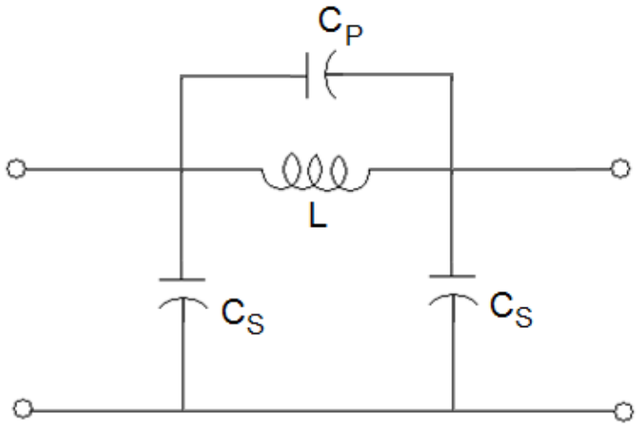
- The previous representation for a microstrip transmission line circuit was a “lumped element” model
- For high frequency or high speed digital (HSD), the correct model for this circuit is using “distributed elements”
- Distributed elements uses very small slices of the lumped element model and cascade them together



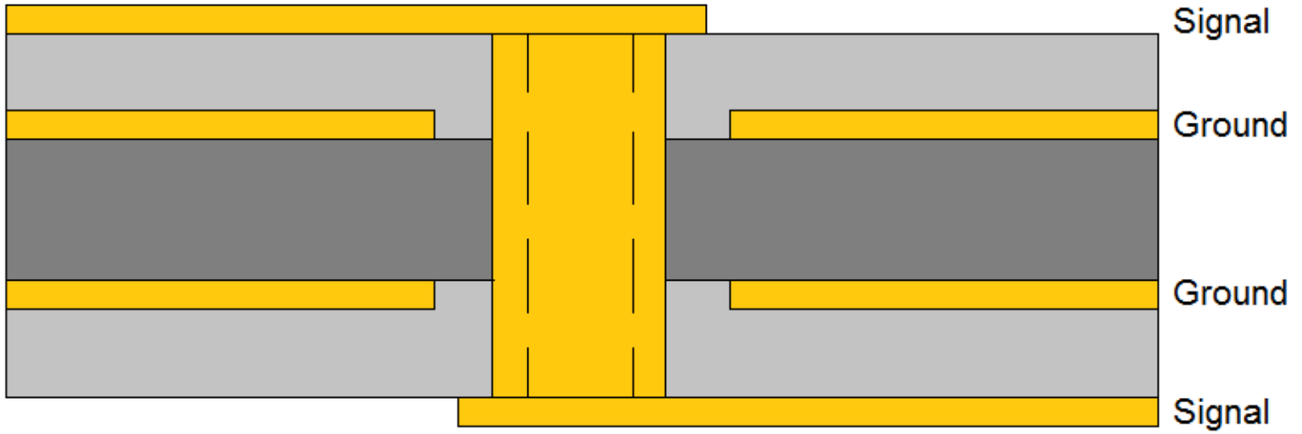
High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Basic overview of transmission line circuits and plated through hole vias

- Some electromagnetic modeling software has very good PTH via models
- It is difficult to find a good model for a PTH via, using closed form equations
- Sometimes a simple study, in an effort to collect empirical data, is done to evaluate the effects of the PTH via
- This study is a simple tutorial on how to collect empirical data and from the data, understand which design aspects of the PTH via need to change for optimum high frequency performance



Representation of a PTH via



High Frequency RF Electrical Performance
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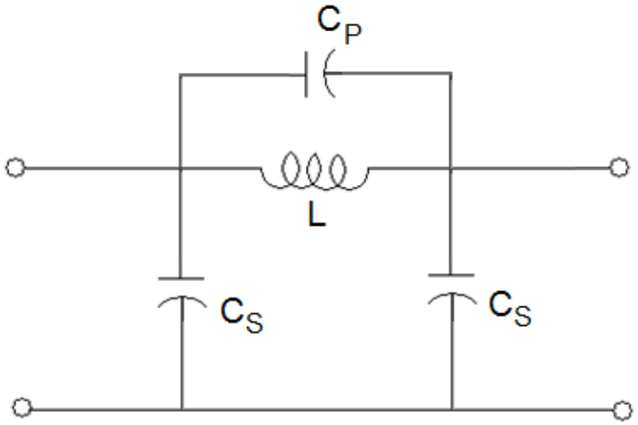
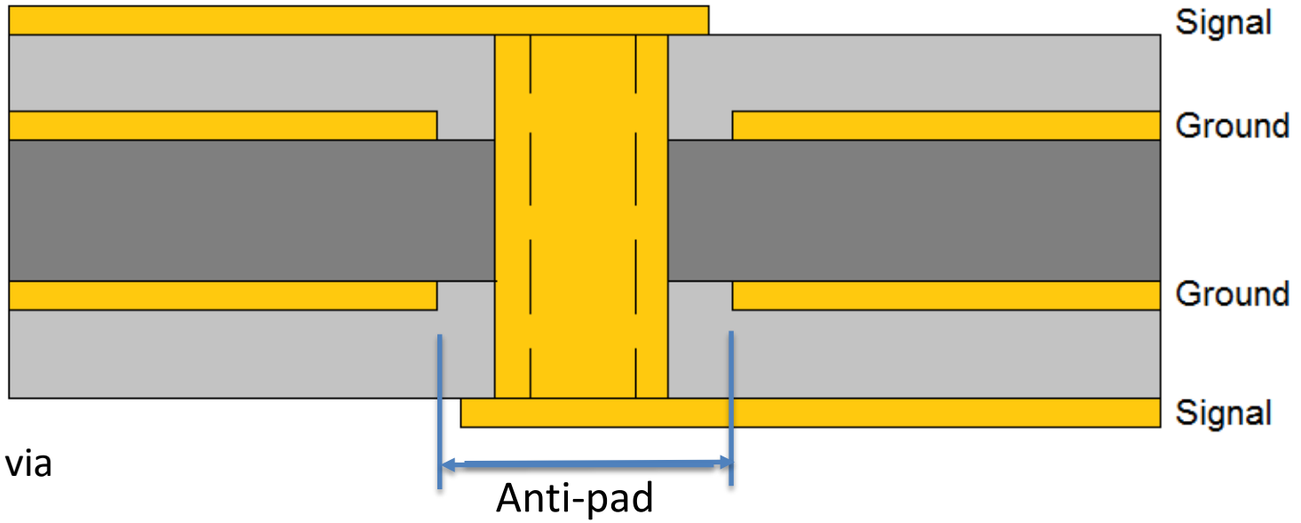
Basic overview of transmission line circuits and plated through hole vias

- Understanding the attributes of the via regarding inductance and capacitance can help the designer fine tune the design based on empirical data

  - PTH via design aspects related to inductance and capacitance:
    - An increased via diameter will increase capacitance (or decrease inductance)
    - An increased copper plating thickness will increase capacitance
    - A decreased circuit pad diameter will decrease capacitance (or increase inductance)
    - A decreased anti-pad diameter (grounded) will increase capacitance



Representation of a PTH via



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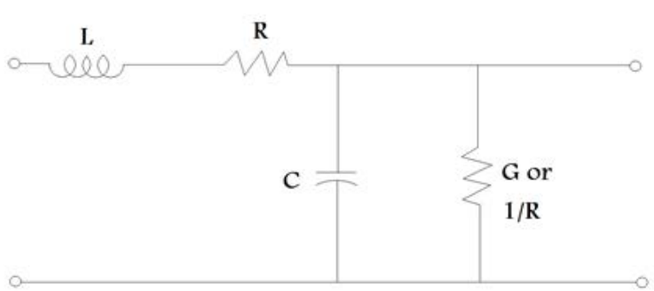
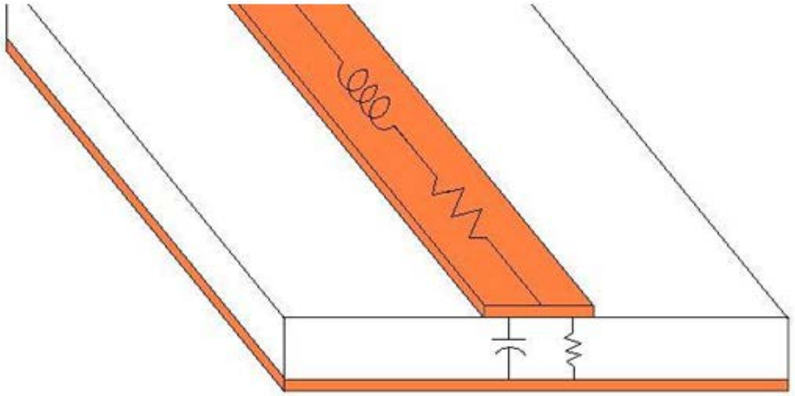
Simple overview of impedance

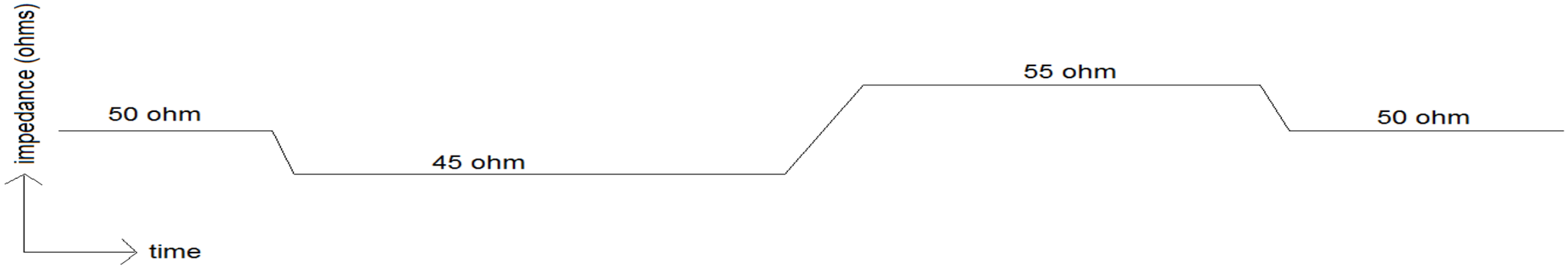
- A simplified view on impedance for a microstrip circuit is:





$$Z_0 = \sqrt{\frac{L}{C}}$$

- With an increased inductance, the impedance will increase
- With an increased capacitance, the impedance will decrease
- Impedance curve example below, assuming a 50 ohm system, the 45 ohm portion could be due to an increase in capacitance and the 55 ohm portion could be due to an increase in inductance



High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

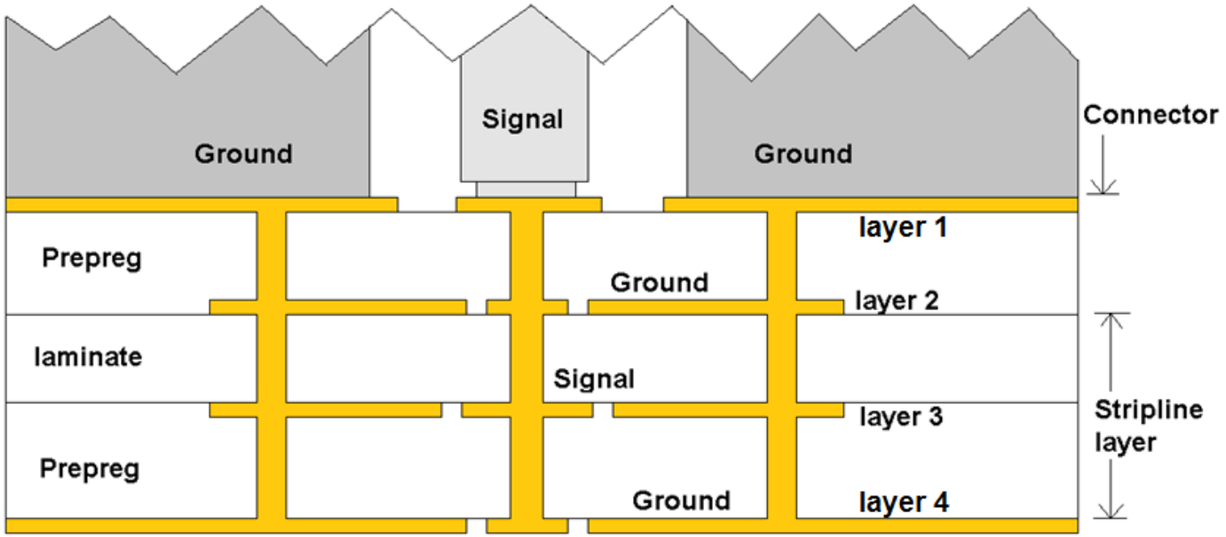
Simple overview of impedance

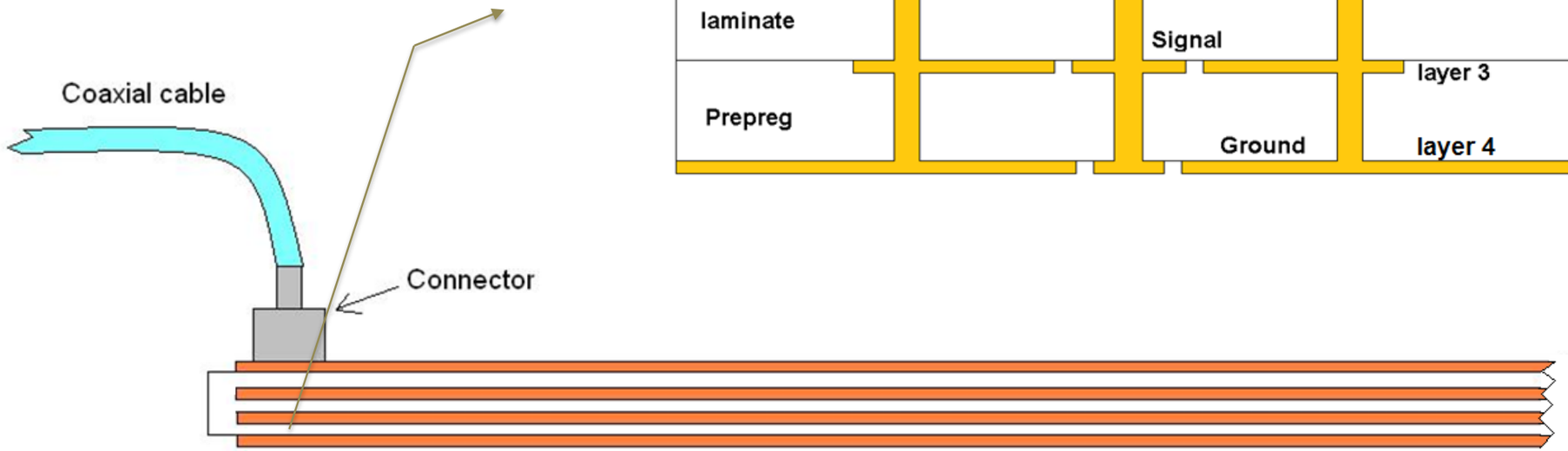
- Connectors cause impedance differences
- PTH vias cause impedance differences
- Impedance anomalies can cause many problems for high frequency or high speed digital applications
- With significant impedance anomalies, the circuit issues can be:
    - More reflections
    - Worse return loss
    - More noisy insertion loss
    - Increased radiated energy, which can cause more EMI (Electro-Magnetic Interference)
    - More noisy eye-diagrams and signal integrity issues
- If the design can minimize impedance differences between the circuit and the connectors or vias, then there will be a much smoother impedance curve and overall better circuit performance

High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Signal launch experiments

- Previous capacitance, inductance and impedance concepts referenced microstrip structures
- Stripline will have some differences, but the same basic relationships and thought process will apply
- Signal launch is a term that describes the signal energy transition from the connector to the PCB and for stripline, inside the PCB to the signal conductor
- At low RF frequencies or slower digital rates, signal launch is not an issue

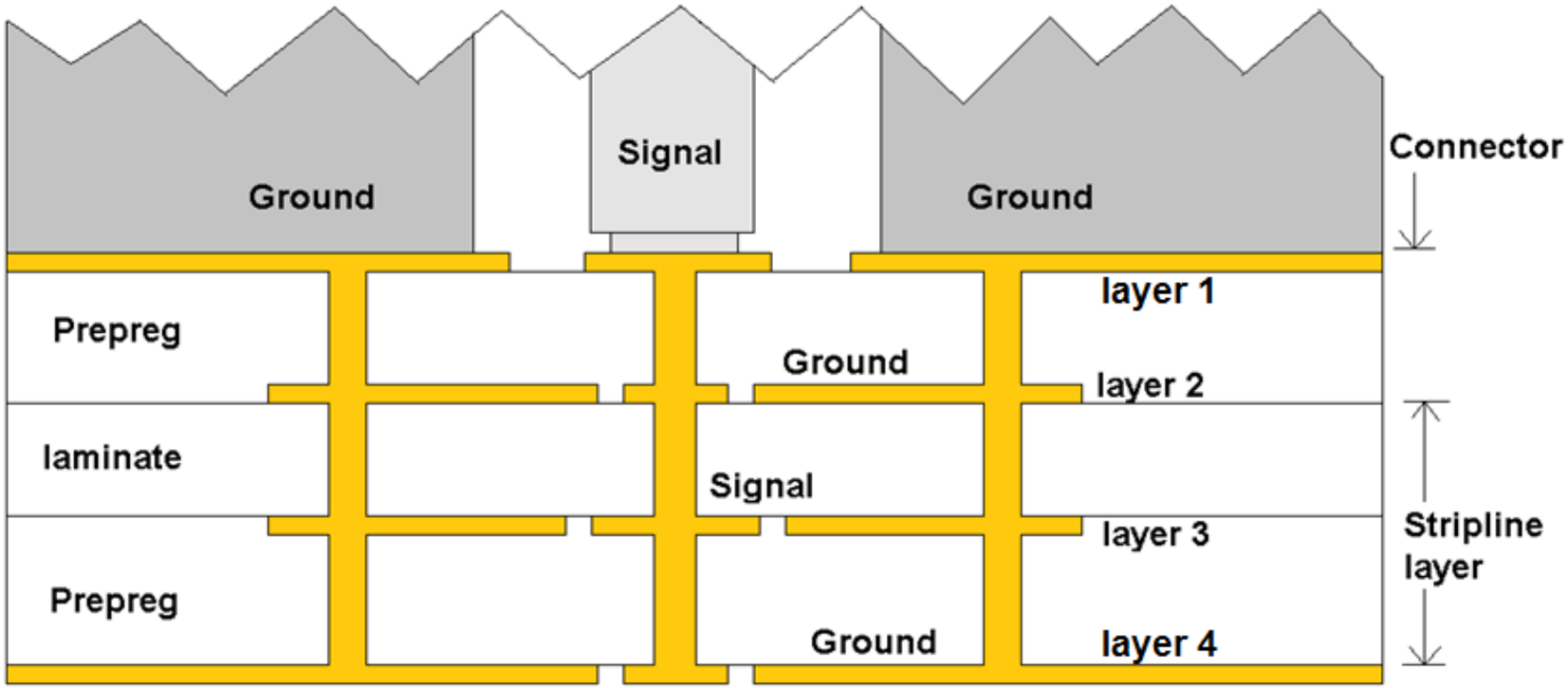




High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Signal launch experiments

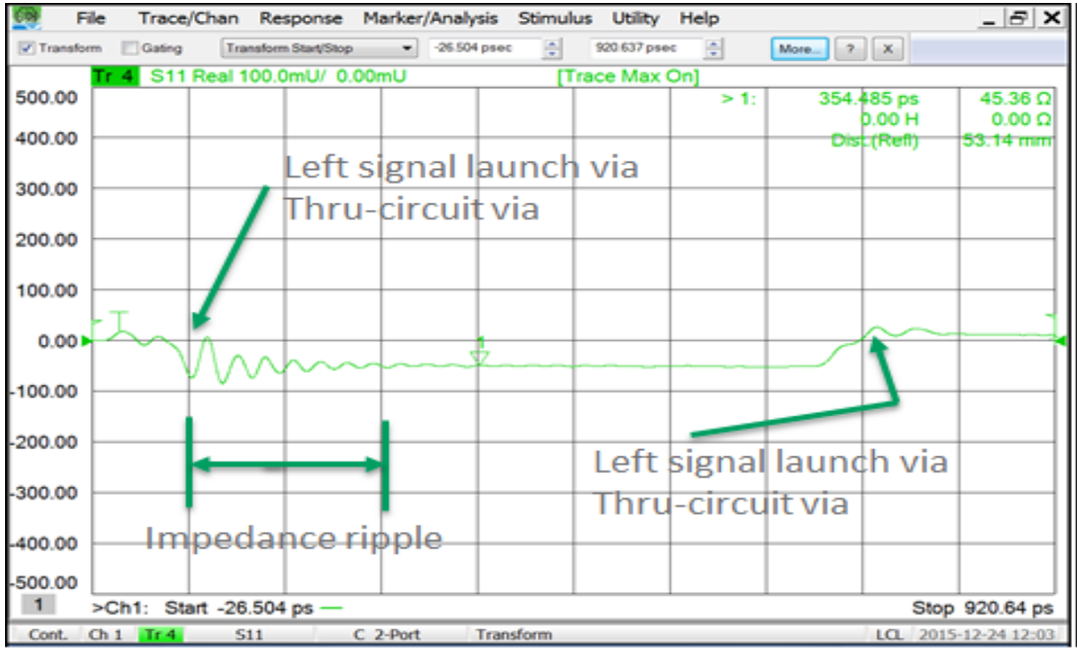
- Good signal launch is critical to get the energy efficiently into the circuit, for high frequency or HSD
- There are multiple impedance transitions for a stripline signal launch:
- Connector has its own impedance
- Impedance at layer 1 surface (low Z_0)
- Impedance of PTH via between layer 1 and layer 2 (high Z_0)
- Impedance at the layer 2 plane (low Z_0)
- Impedance of PTH via between layer 2 and layer 3 (high Z_0)
- Impedance at the layer 3 plane (low Z_0)
- The stub of the PTH via between layer 3 and layer 4 (high Z_0) can radiate energy



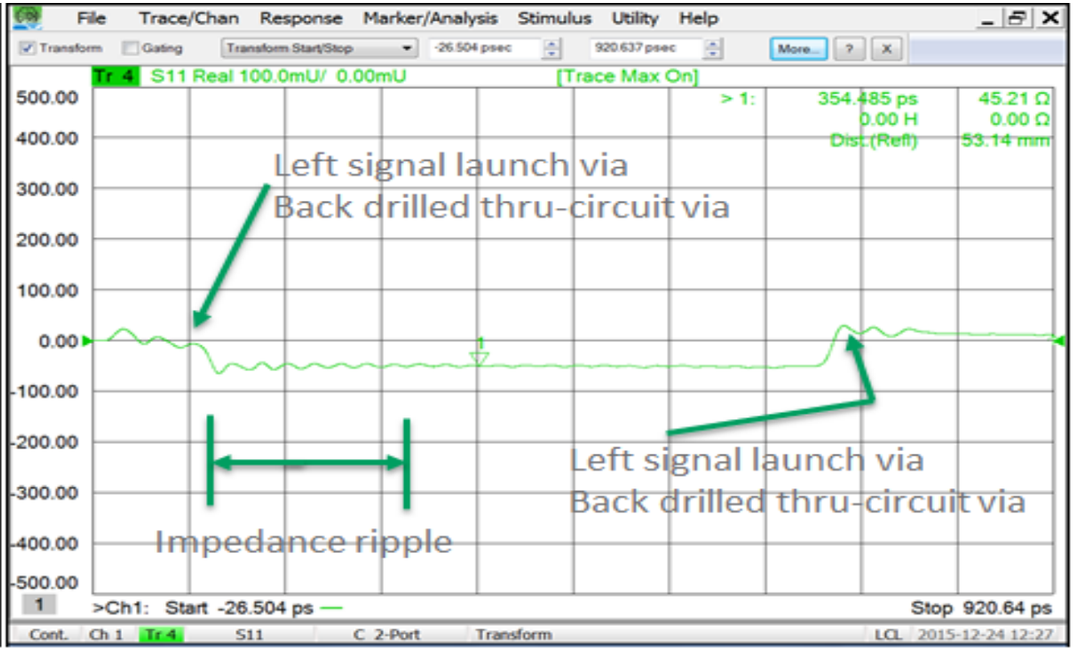
High Frequency RF Electrical Performance Effects of Plated Through Hole Vias

Signal launch experiments

- Experiments were done with back-drilling, removing the portion of the via between layers 3 and 4
- Using a 2 inch (50.8mm) long stripline transmission line circuit, comparisons were done with back-drilled signal launch vias and not back-drilled signal launch vias



Circuit with thru-circuit via for signal launch



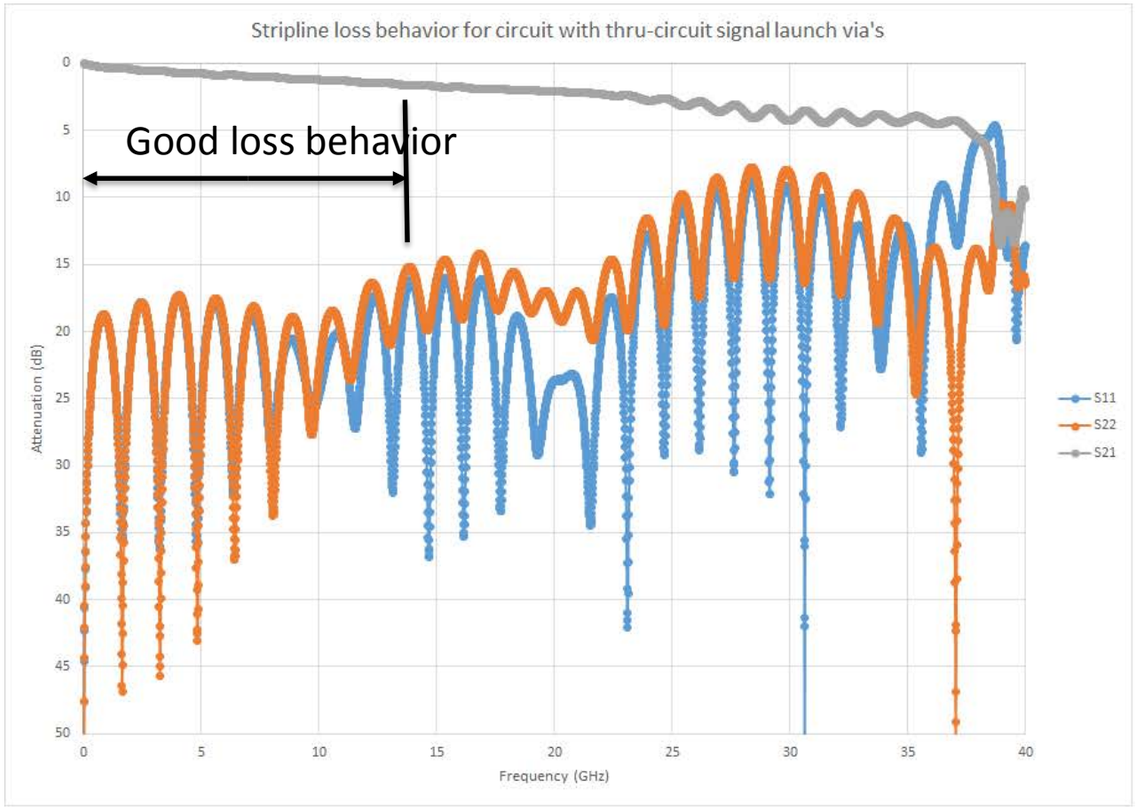
Circuit with back-drilled via for signal launch

- Note the removal of capacitive dip for left signal launch via with back-drilling
- Less impedance ripple with back-drilled via due to smoother impedance curve

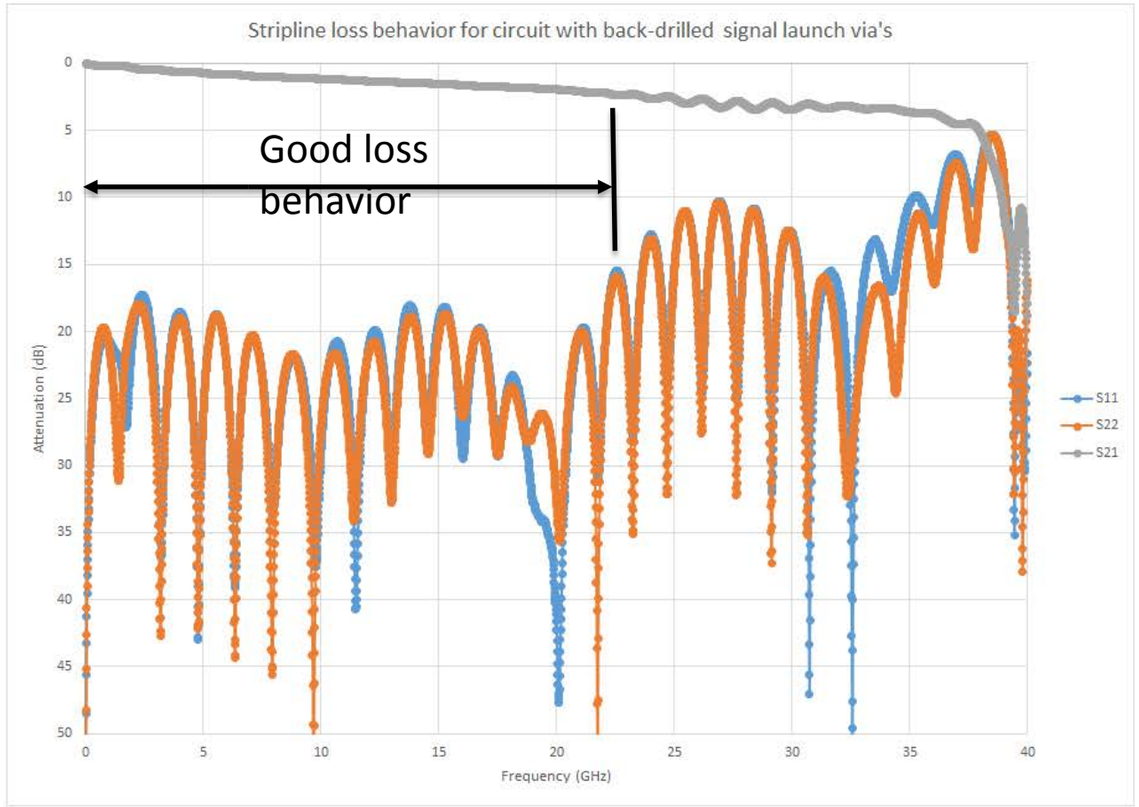
High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Signal launch experiments

- Back-drilling experiment results, continued: Loss impact
  - Return loss is S11 (blue curve) and S22 (orange curve)
  - Insertion loss is S21 (grey curve)



Circuit with thru-circuit via for signal launch



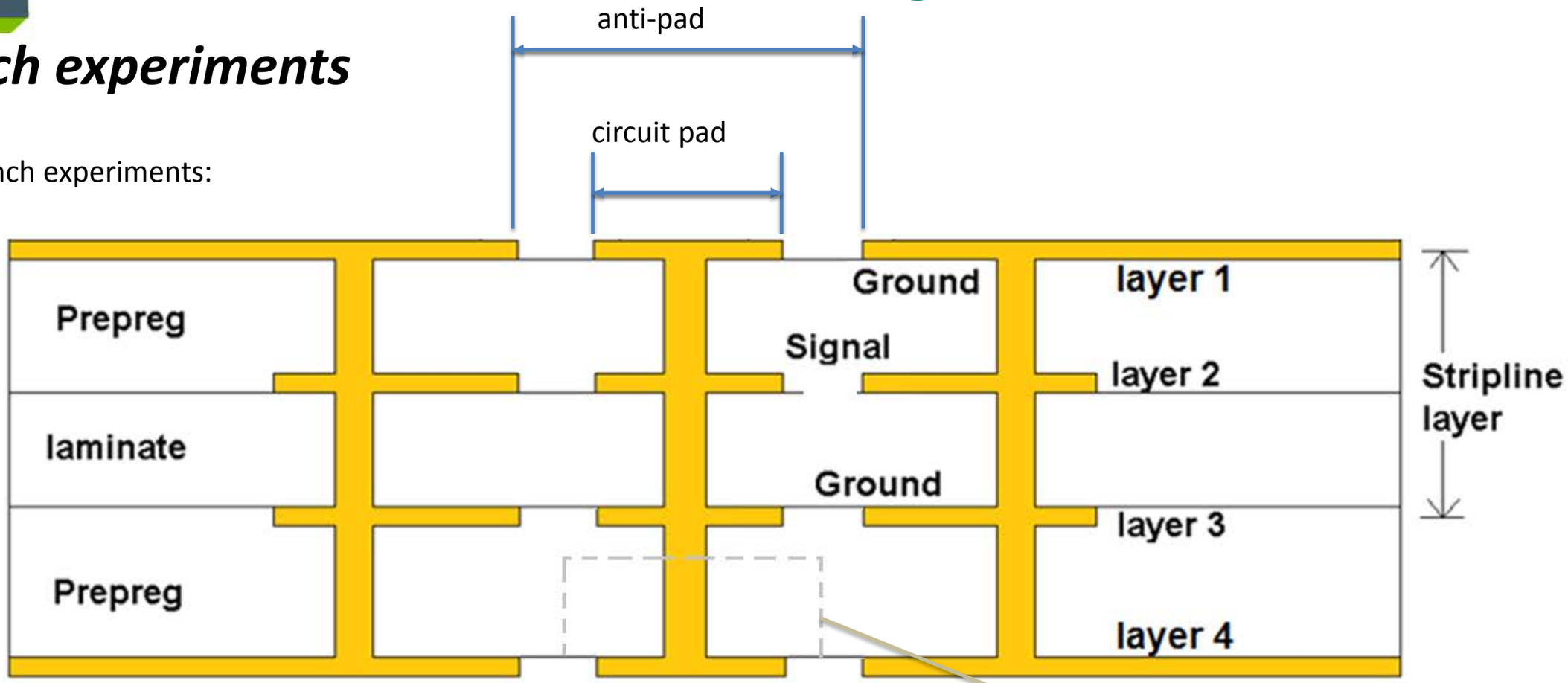
Circuit with back-drilled via for signal launch

- Rule of thumb: good loss behavior is with return loss greater than 15 dB and insertion loss with smooth, slight negative slope
- Using 15 dB rule, the back-drilled via has a much wider band of useable frequencies

High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Signal launch experiments

- Details of signal launch experiments:



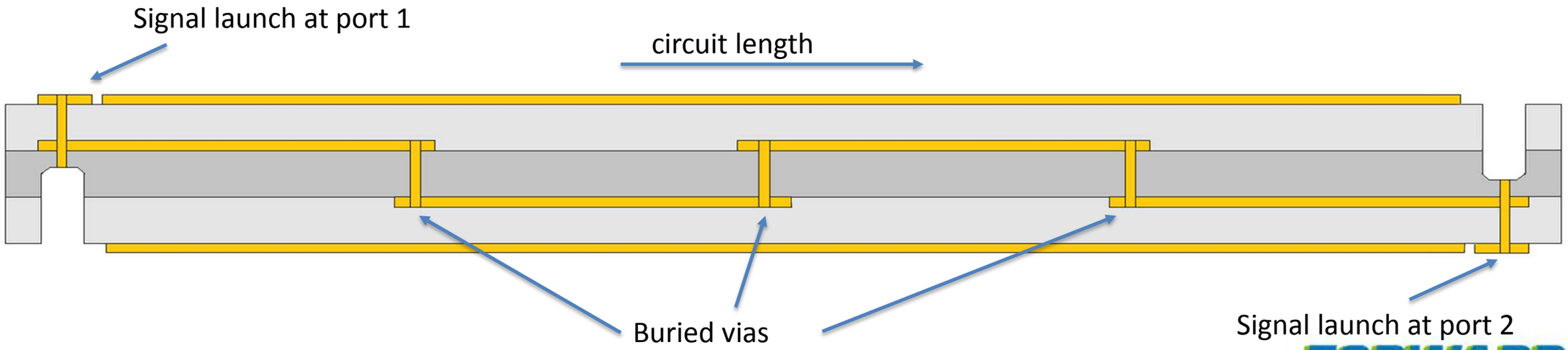
Connector: 2.4mm compression contact

Circuit pad diameter: 0.017” (0.432mm)
Anti-pad diameter: 0.053” (1.346mm)
Drilled via hole size: 0.008” (0.203mm)
Copper plating thickness: 0.001” (0.025mm)
Back-drill depth: 0.005” (0.127mm)

High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Layer-to-layer signal via transition experiments

- For high frequency RF, it is typically avoided to transition a signal trace, through vias to another copper layer, but sometimes it must be done
- These signal transitions can be very difficult to achieve without compromising the overall signal integrity
- Experiments were done using 3 signal-via transitions within the body of the stripline circuit

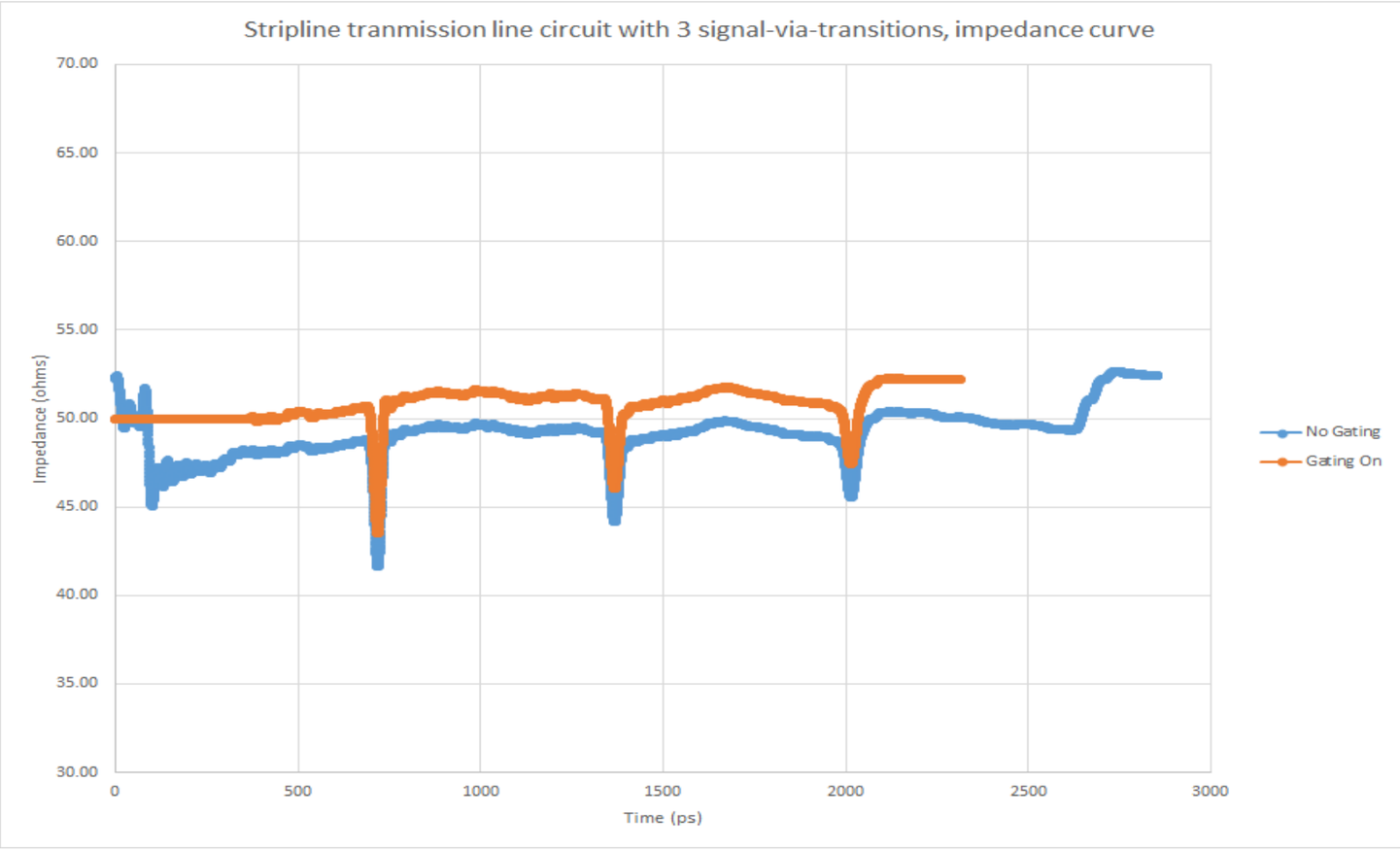


- The buried via option is shown, but also thru-circuit vias were evaluated
- Not shown is the alternating ground planes on layer 2 and 3 to maintain the balanced stripline structure

High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Layer-to-layer signal via transition experiments

- Gating was used to minimize the impedance masking effect on the signal-transition-vias
- The impedance of the first signal-transition-via was evaluated on several test vehicles

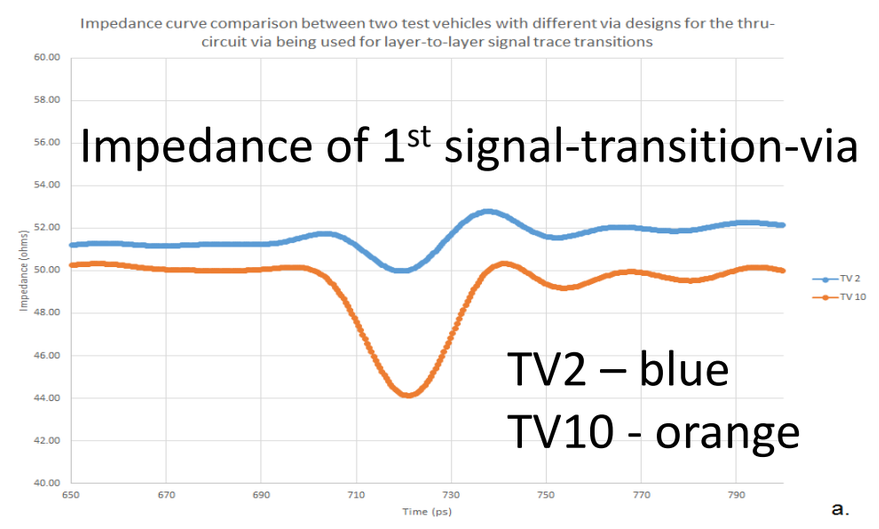


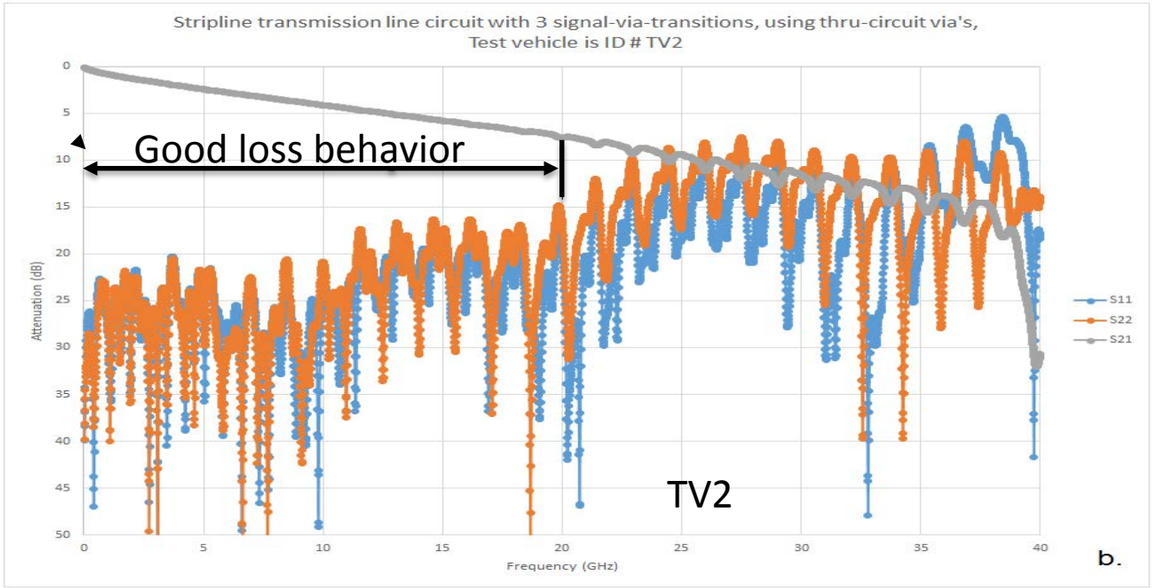
8” long stripline transmission line circuits with 3 signal-via-transitions

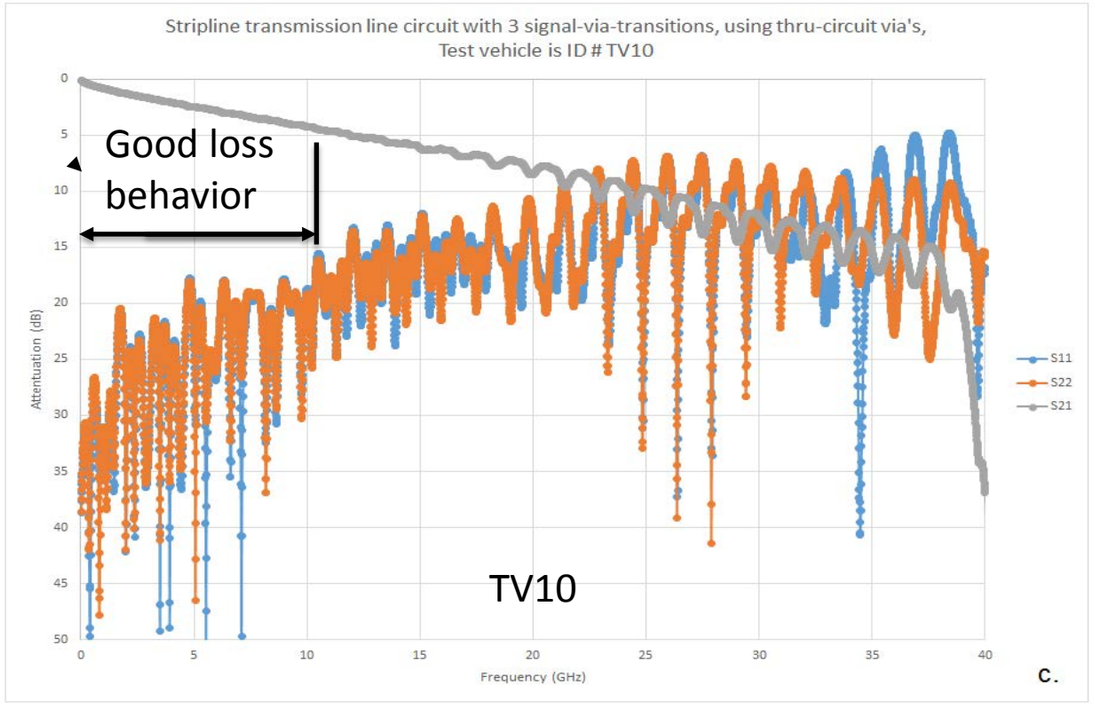
- **Chart shown to the left, shows the difference with Gating on-off**
- **The signal-transition-vias in the body of the circuit are too capacitive (low impedance dips)**
- **To correct the excessive capacitance, reducing the circuit pad diameter and / or increasing the anti-pad diameter will decrease the capacitance**
- **Additionally, a PTH via that is smaller diameter or shorter will also reduce the capacitance**

High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Layer-to-layer signal via transition experiments





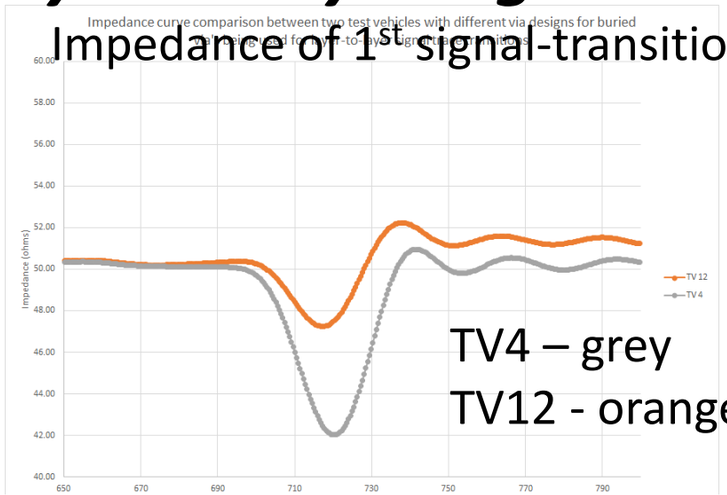


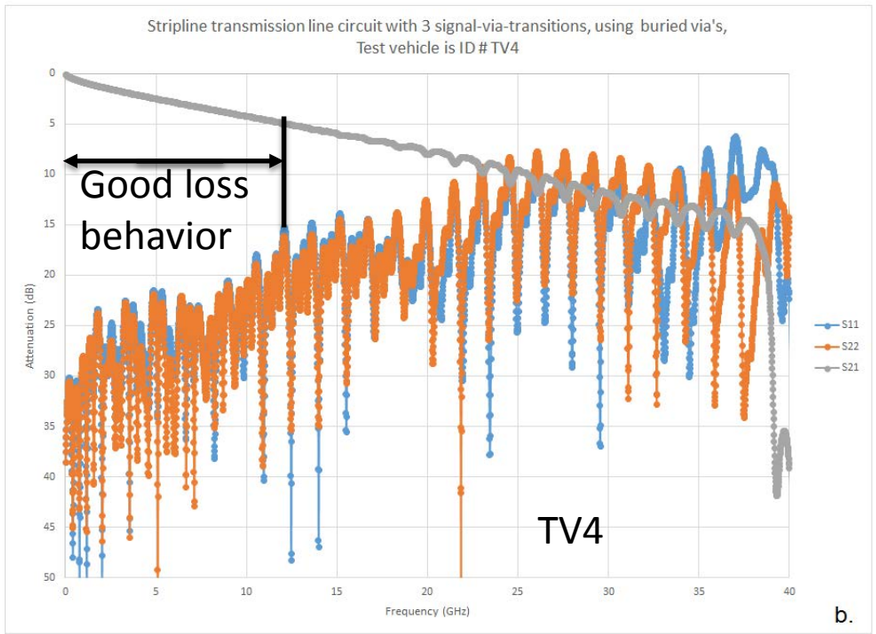
- Thru-circuit vias used for the signal-transition-vias
- TV2 had much better overall performance
- The differences in TV2 versus TV10 are PTH via diameter, signal circuit pad diameter and anti-pad diameter

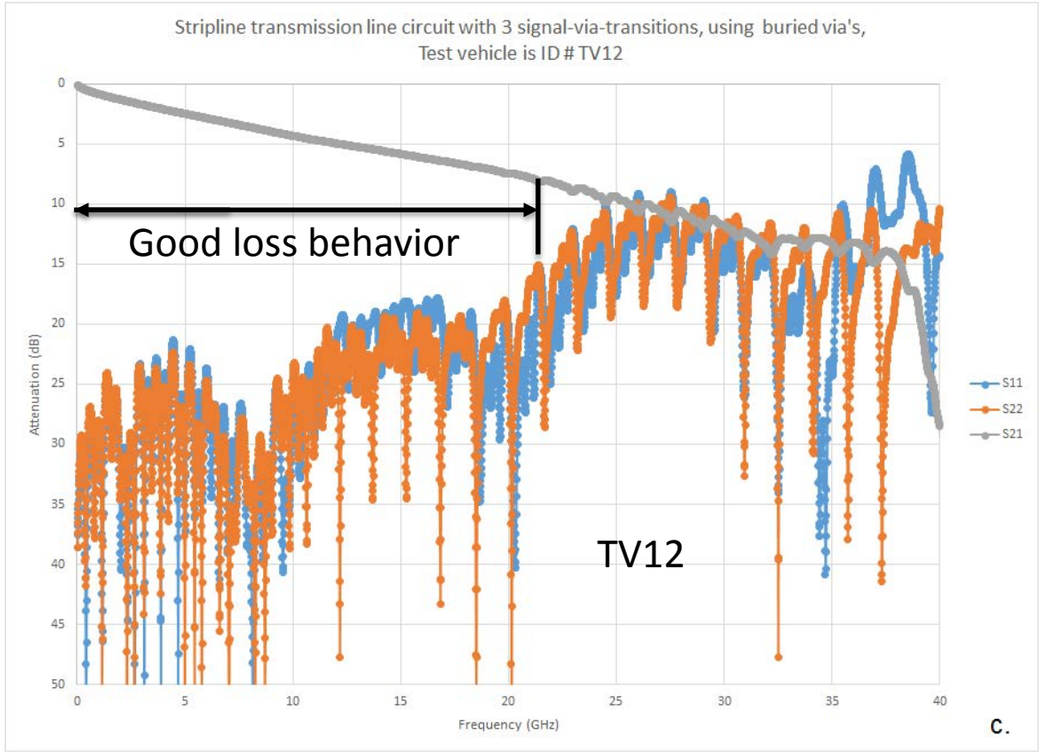
High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Layer-to-layer signal via transition experiments

Impedance of 1st signal-transition-via







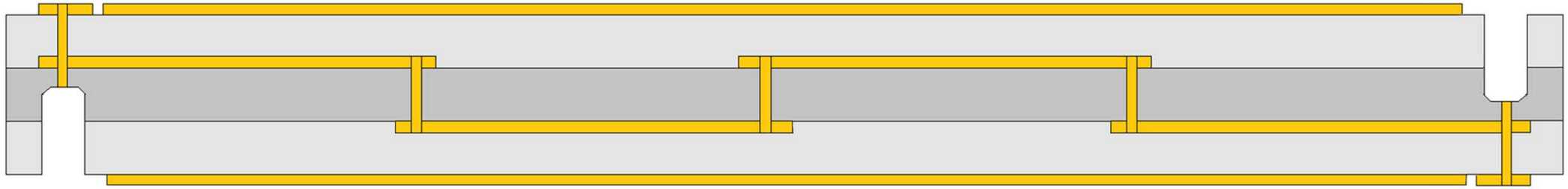
- Buried vias used for the signal-transition-vias
- TV12 had much better overall performance
- The differences in TV12 versus TV4 are PTH via diameter, signal circuit pad diameter and anti-pad diameter

High Frequency RF Electrical Performance
Effects of Plated Through Hole Vias

Layer-to-layer signal via transition experiments

Test Vehicle	Type of via	Via hole diameter	Copper plating thickness (mils)	Via length (mils)	outer layer via pads		inner layer via pads		Good return loss, Freq (GHz)
					circuit pad	anti-pad	circuit pad	anti-pad	
TV 2	thru-circuit	8	1	28	20	34	20	53	19
TV 10	thru-circuit	12	1	28	24	36	24	53	11
TV 4	buried	8	1	9.5	none	none	20	53	12
TV 12	buried	12	1	9.5	none	none	24	53	22

- For the thru-circuit transition vias, TV2 was better and had a smaller PTH via diameter and circuit pads were smaller; all of which reduces capacitance
- For the buried-via transition vias, TV12 was better and had a larger PTH via diameter and larger circuit pad; both of which increase capacitance
- When comparing the thru-circuit transition vias to the buried-via transition vias, the buried vias have a shorter length, which will decrease capacitance as compared to the longer thru-circuit vias



Thank You