IPC Midwest 2011

Common Mistakes in Electronic Design

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DfR Solutions

Executive Summary:

Board-level designers are constantly expected to cram more computational power, into a smaller space, at lower cost, and accomplish this task in less time and with fewer resources. In this rush to meet customer requirements, common and costly hardware design mistakes are often made. Examples include part selection, component placement, board layout and specifications, and understanding the role design plays in ensuring long-term reliability. This presentation provides hardware designers with case studies of some common mistakes and the process by which these mistakes were inserted or overlooked during the design process. The presentation will also provide a checklist to avoid these mistakes, why these mistakes caused failures, and optimized corrective actions necessary to avoid these problems, but still ensure a successful product launch.

Common Mistakes in Electronic Design

Dr. Craig Hillman, CEO, DfR Solutions
Dr. Nathan Blattau, VP, DfR Solutions

Who Controls Electronic Design?

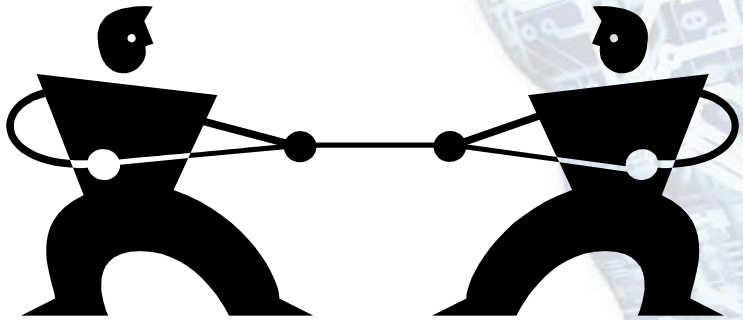
Electrical Designer

- Component selection
  - Bill of materials (BOM)
  - Approved vendor list (AVL)

Mechanical Designer

- PCB Layout
- Other aspects of electronic packaging

Both parties play a critical role in minimizing hardware mistakes during new product development

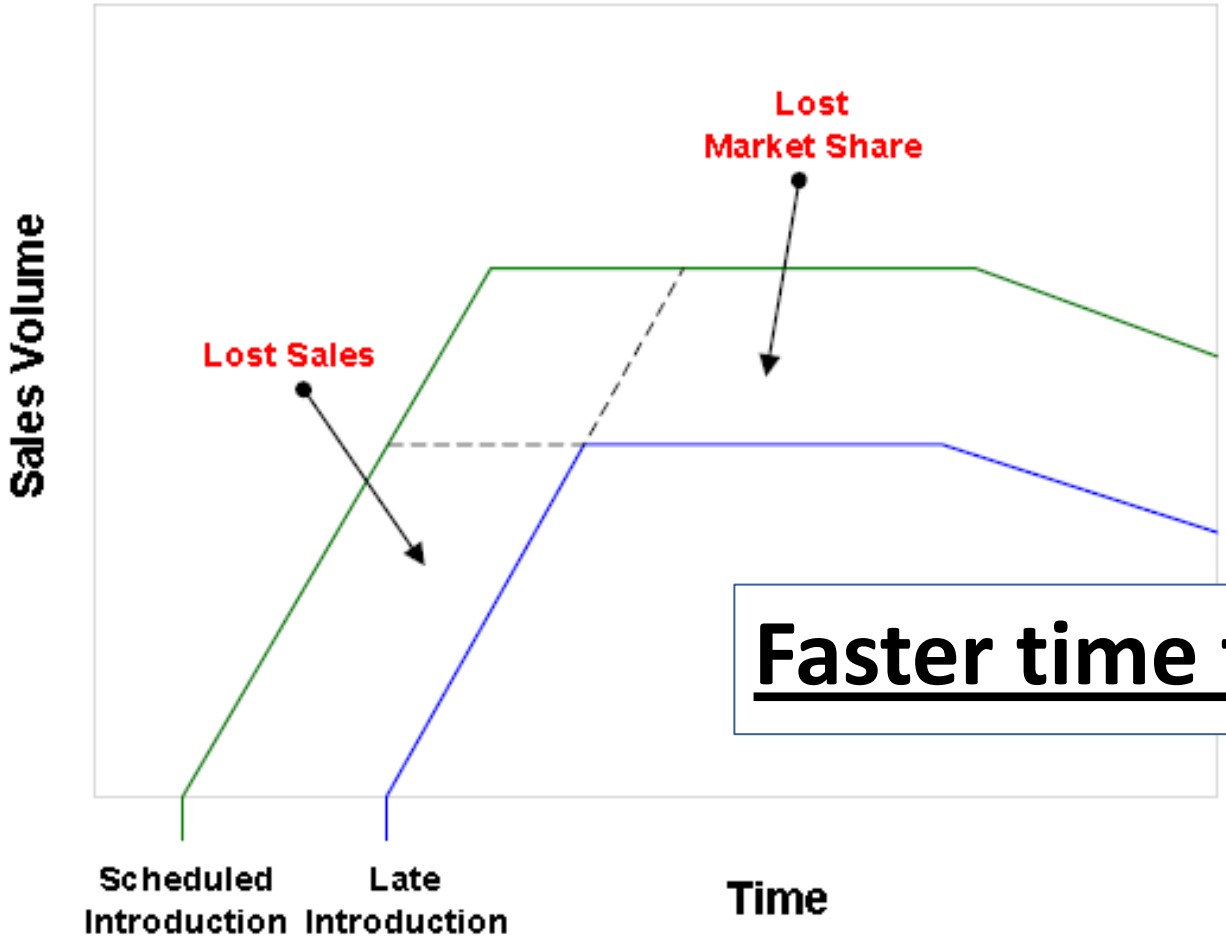


Why Do Design Mistakes Occur?

- Insufficient exchange of information between electrical design and mechanical design
- Poor understanding of supplier limitations
- Customer expectations (reliability, lifetime, use environment) are not incorporated into the new product development (NPD) process

There can be many things that "you don't know you don't know"

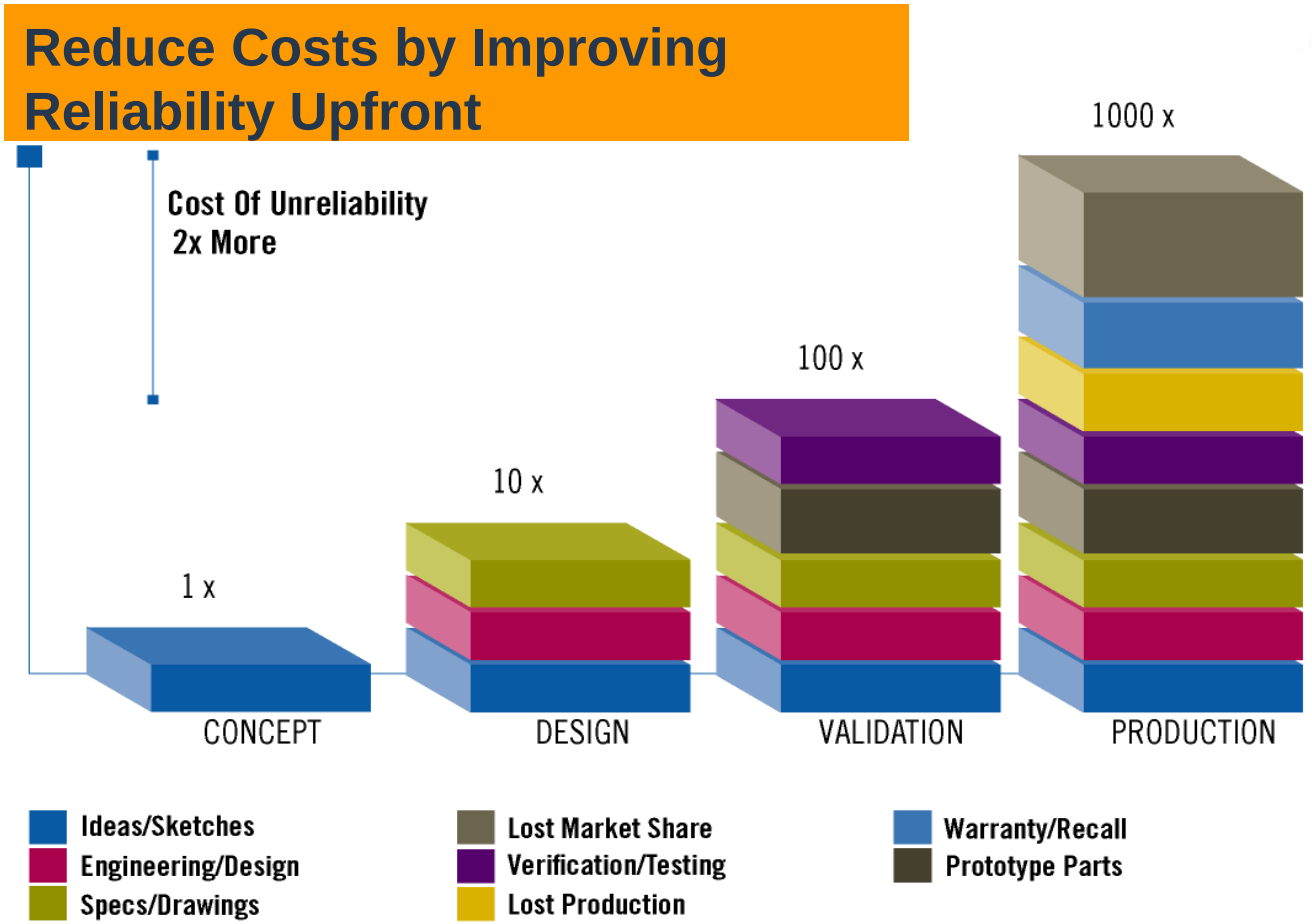
Why Fix Design Mistakes?



Faster time to market

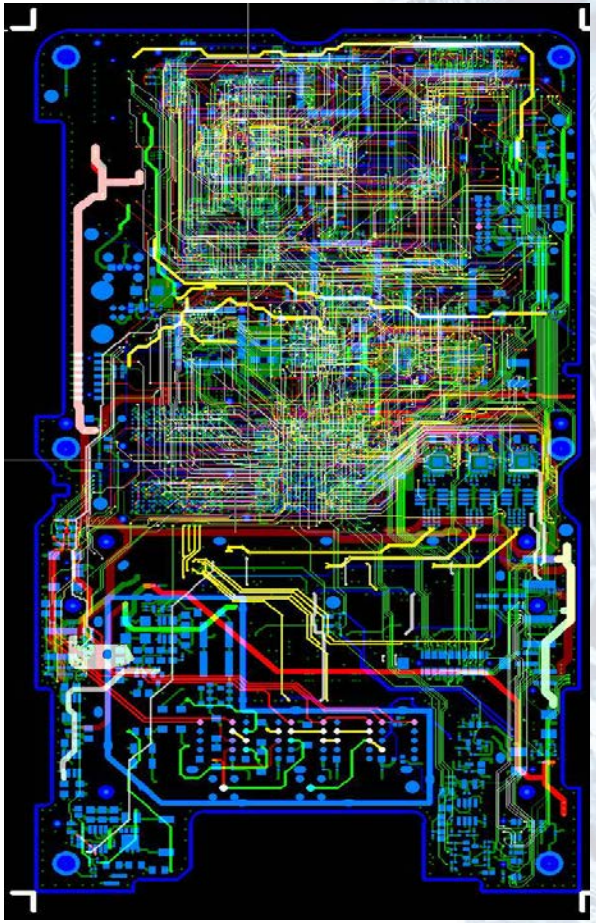
P. Smith and D. Reinertsen. Developing Products In Half The Time (New York Van Nostrand Reinhold. 1991). 4.

Why Fix Mistakes: Save Money



Increase in Hardware ‘Mistakes’

- Avoiding hardware mistakes is becoming increasingly difficult
  - Increasing complexity of electronic circuits
  - Increasing power requirements
  - Introduction of new component and material technologies
  - Introduction of less robust components
- Results in multiple potential drivers for failure



When do Design Mistakes Occur?

- Concept / Block Diagram
- Schematic / Bill of Materials (BOM)
- Layout / Mechanicals

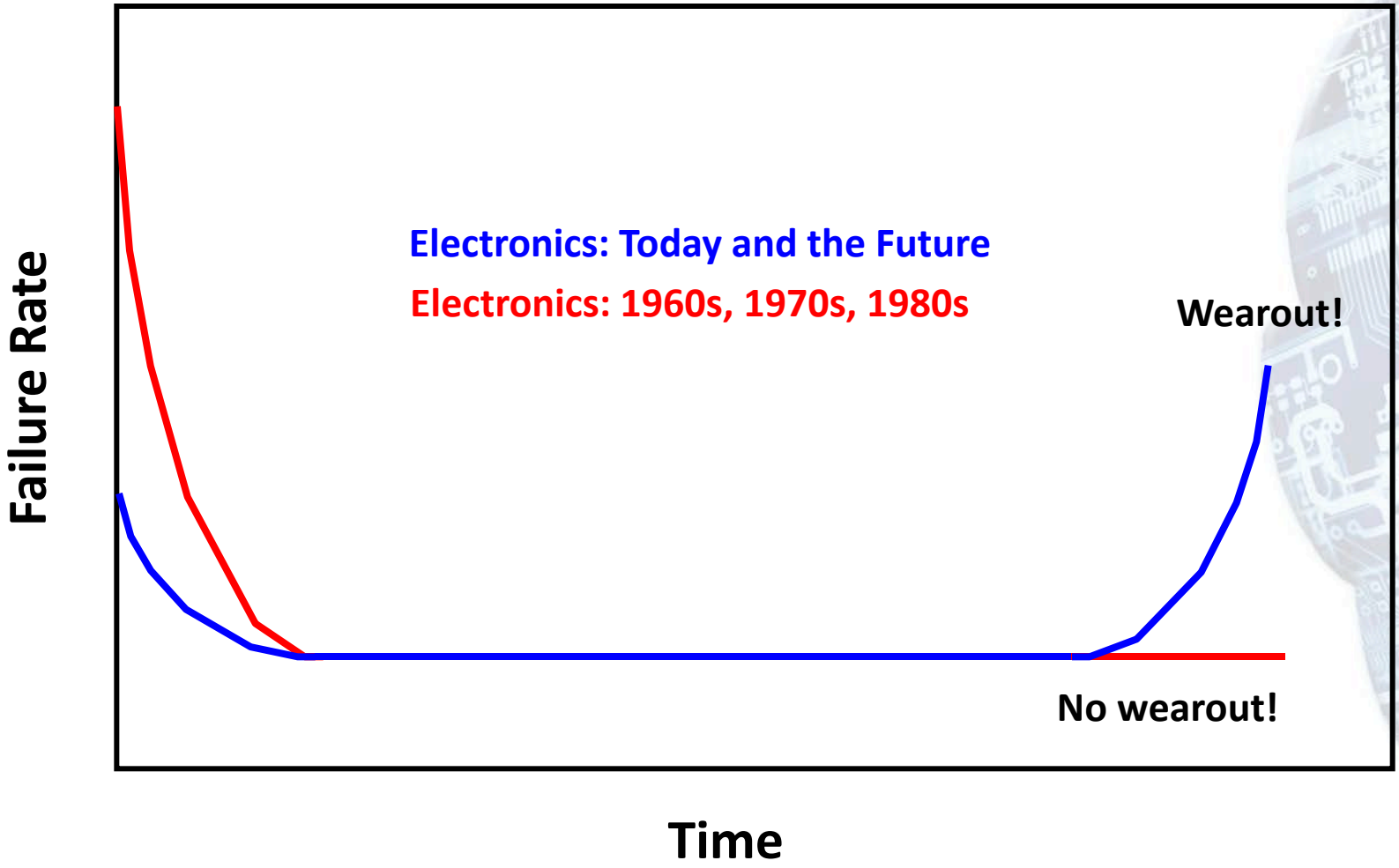
Concept / Block Diagram

- Can hardware mistakes occur at this stage?
  - No…….and Yes
- Failure to capture and understand product specifications at this stage lays the groundwork for mistakes at schematic and layout
  - Reliability expectations, Use environment, Dimensional constraints

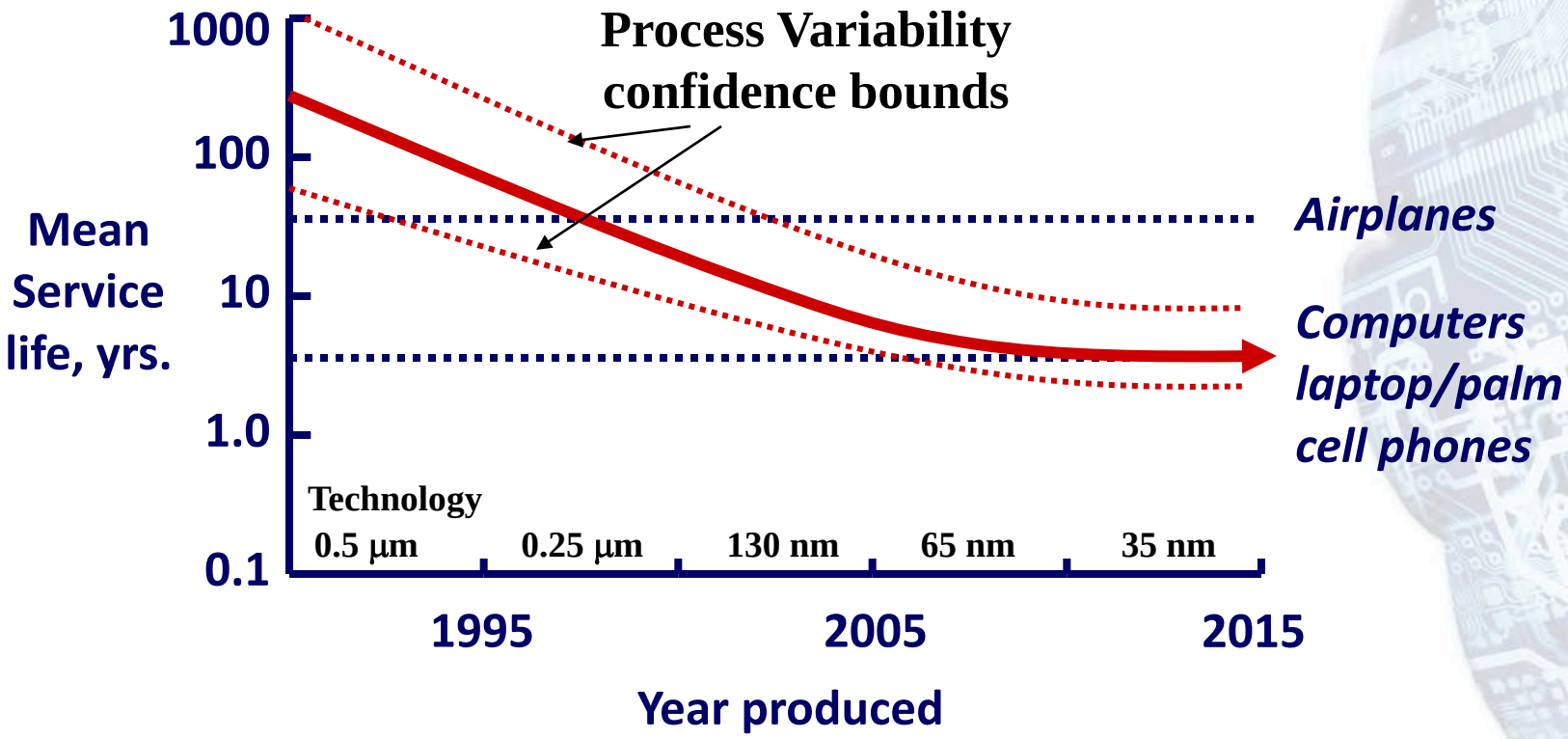
Reliability Goals

- Reliability is the measure of a product's ability to
  - …perform the specified function
  - …at the customer (with their use environment)
  - …over the desired lifetime
- Typical reliability metrics: Desired Lifetime / Product Performance
- Desired lifetime
  - Defined as when the customer will be satisfied
  - Should be actively used in development of part and product qualification
- Product performance
  - Returns during the warranty period
  - Survivability over lifetime at a set confidence level
  - Try to avoid MTBF or MTTF

Why is Desired Lifetime Important?

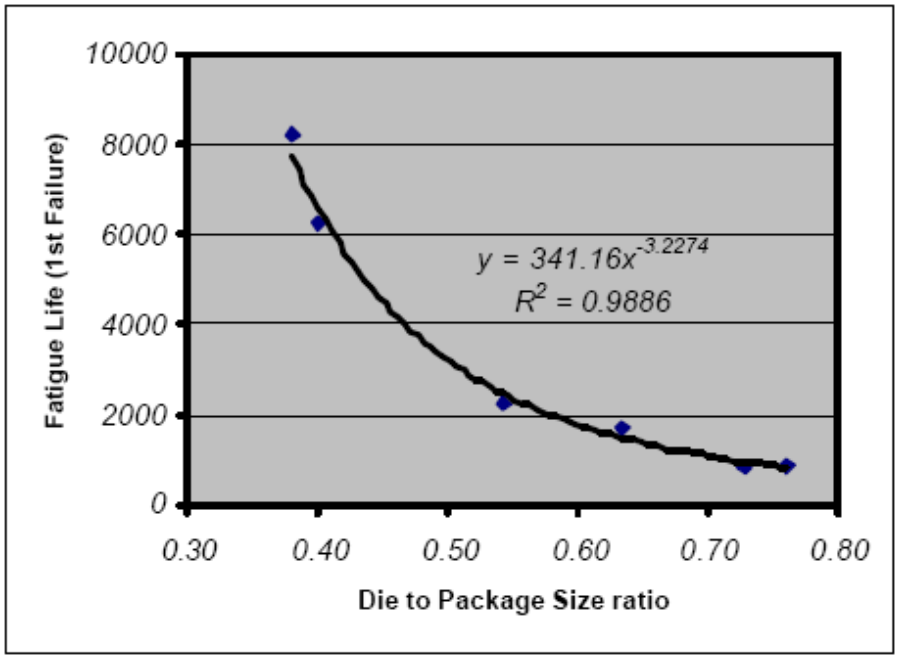


Desired Lifetime (IC Wearout)



Desired Lifetime (Solder Wearout)

- More silicon, less plastic (CSP, Stacked Die, etc.)
- Elimination of leads (DFN, QFN, BTC, etc.)

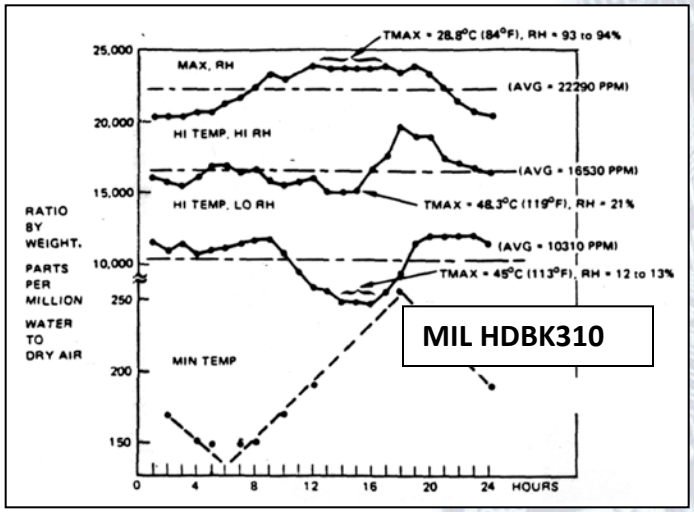


BOARD LEVEL ASSEMBLY AND RELIABILITY CONSIDERATIONS FOR QFN TYPE PACKAGES, Ahmer Syed and WonJoon Kang, Amkor Technology.

Identify Field Environment

- Approach 1: Use of specifications
  - MIL-STD-810, MIL-HDBK-310, IPC-SM-785, Telcordia GR3108, IEC 60721-3, etc.
  - Low cost and can be very comprehensive
  - Agreement throughout the industry
  - Major disadvantage is always less or greater than actual (by how much, unknown)

- Approach 2: Based on actual measurements
  - Determine average and realistic worst-case
  - Identify all failure-inducing loads
  - Include all environments

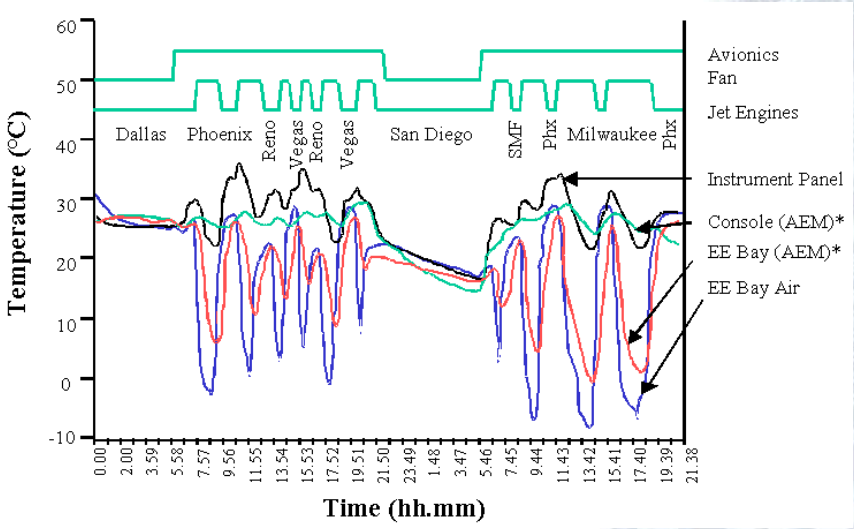


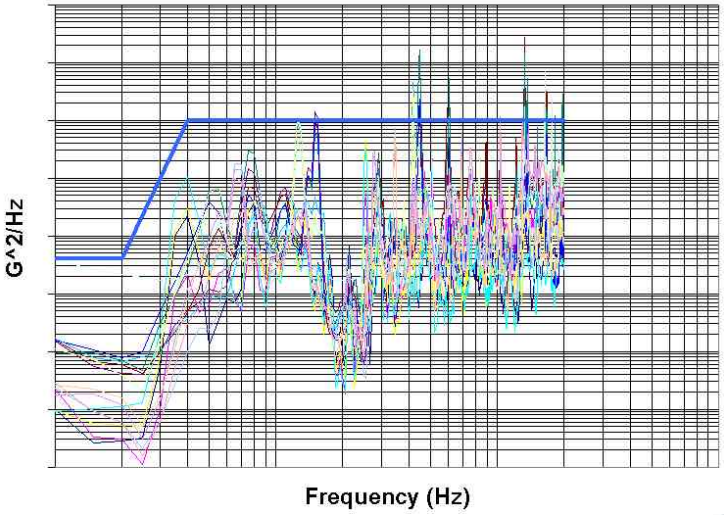
USE CATEGORY	WORST-CASE USE ENVIRONMENT Tmin °C	Tmax °C	ΔT(1) °C	t_D hrs	Cycles/ year	Typical Years of Service	Approx. Accept. Failure Risk, %	ACCELERATED TESTING Tmin °C	Tmax °C	ΔT(2) °C	t_D min
1) CONSUMER	0	+60	35	12	365	1-3	1	+25	+100	75	15
2) COMPUTERS	+15	+60	20	2	1460	5	0.1	+25	+100	75	15
3) TELECOM	- 40	+85	35	12	365	7-20	0.01	0	+100	100	15
4) COMMERCIAL AIRCRAFT	-55	+95	20	12	365	20	0.001	0	+100	100	15
5) INDUSTRIAL & AUTOMOTIVE PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1	0	+100	100 & COLD(3)	15
6) MILITARY GROUND & SHIP	-55	+95	40 &60	12 12	100 265	10	0.1	0	+100	100 & COLD(3)	15
7) SPACE leo geo	-55	+95	3 to 100	1 12	8760 365	5-30	0.001	0	+100	100 & COLD(3)	15
8) MILITARY AVIONICS a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0.01	0	+100	100	15
9) AUTOMOTIVE UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	5	0.1	0		& COLD(3) & LARGE ΔT(4)	

IPC SM785

Failure Inducing Loads

- Temperature Cycling
  - Tmax, Tmin, dwell, ramp times
- Sustained Temperature
  - T and exposure time
- Humidity
  - Controlled, condensation
- Corrosion
  - Salt, corrosive gases (Cl_2, etc.)
- Power cycling
  - Duty cycles, power dissipation
- Electrical Loads
  - Voltage, current, current density
  - Static and transient
- Electrical Noise
- Mechanical Bending (Static and Cyclic)
  - Board-level strain
- Random Vibration
  - PSD, exposure time, kurtosis
- Harmonic Vibration
  - G and frequency
- Mechanical shock
  - G, wave form, # of events





Field Environment: Worst-Case Temp

Temperature	Avg. U.S. CLIM Data	Avg. U.S. Weighted by Registration (Source: Confidential)	Phoenix (hrs/yr)	U.S. Worst Case (hrs/yr)
95F (35C)	0.375%	0.650%	11% (948)	13% (1,140)
105F (40.46C)	0.087%	0.050%	2.3% (198)	3.8% (331)
115F (46.11C)	0.008%	0.001%	0.02% (1.4)	0.1% (9)

Field Environment: Long-Term Temp

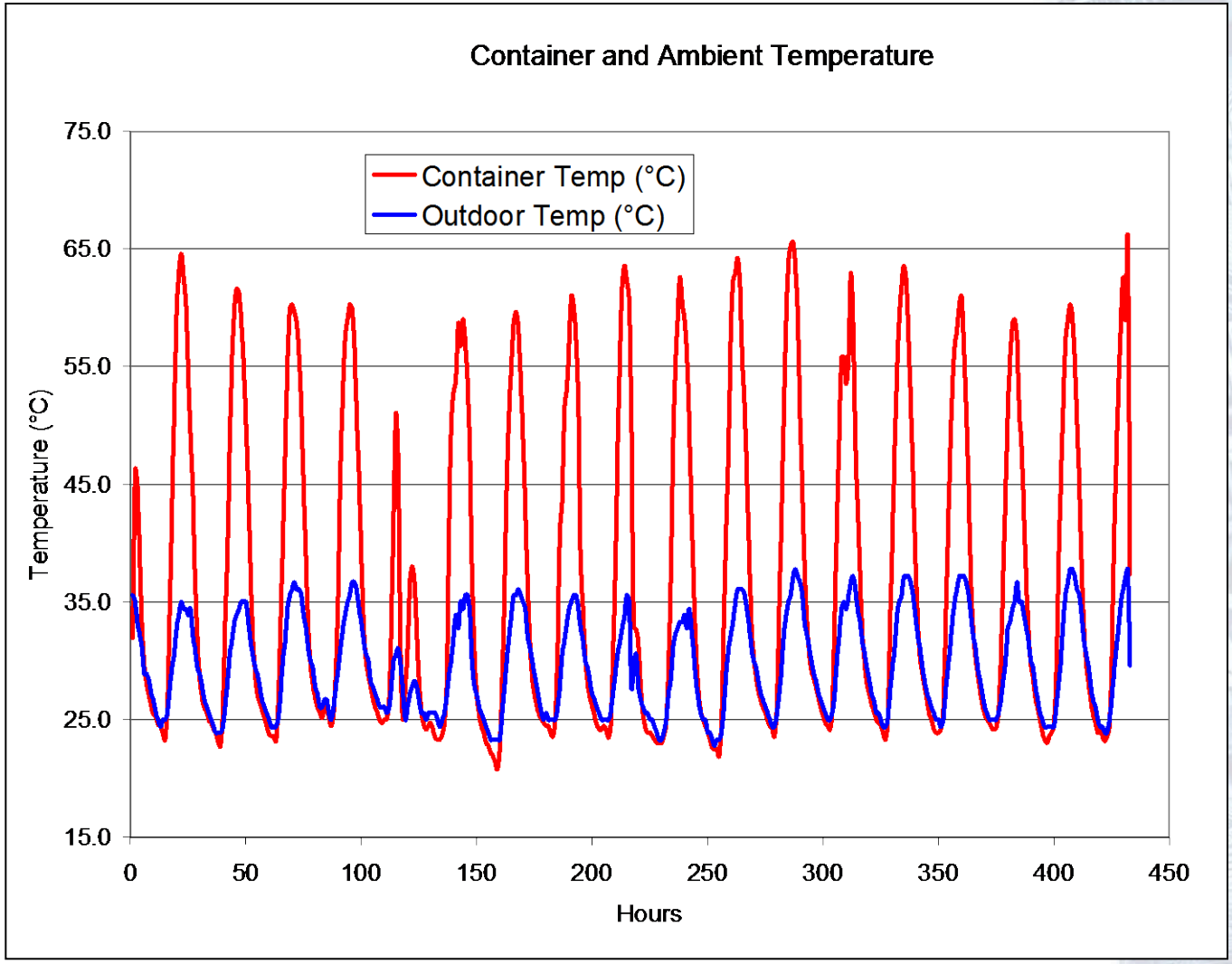
Phoenix, AZ

Month	Cycles/Year	Ramp	Dwell	Max. Temp (^{o}C)	Min. Temp. (^{o}C)
Jan.+Feb.+Dec.	90	6 hrs	6 hrs	20	5
March+November	60	6 hrs	6 hrs	25	10
April+October	60	6 hrs	6 hrs	30	15
May+September	60	6 hrs	6 hrs	35	20
June+July+August	90	6 hrs	6 hrs	40	25

Field Environment: Closed Container Temp

Temp. Variation

Trucking Container



Field Environment: Electrical

- Often very well defined in developed countries, but new markets can introduce surprises
  - China: Can have issues with grounding (connected to rebar?)
  - India: Numerous brownouts (several a day)
  - Mexico: Voltage surges

Dimensions

- Keep dimensions loose at this stage
  - Large number of hardware mistakes driven by arbitrary size constraints
  - Examples include poor interconnect strategies and poor choices in component selection
- Case study: Use of 0201 chip components
  - Tight dimensional requirements push designer towards wholesale placement of 0201 components
  - 0201 is not yet an appropriate technology for systems requiring reliability
  - Result: Major issues at customers
- Use the Toyota approach

Toyota Approach

- Toyota's development engineers are 4X as productive as U.S. counterparts.
- Why?
  - Focus on learning as much as possible
  - Use of that knowledge to develop a stream of excellent products

- **Western engineers**
  - Define several product concepts
  - Select the one that has the most promise
  - Draw up specifications and divide them into subsystems;
  - Subsystems are designed, built and rolled up for system testing.
  - Failures? Rework the specs and the designs accordingly (non-optimized and confusing endeavor)

- **Toyota engineers**
  - Efforts concentrated at lowest possible design level
  - Thorough understanding of the technology of a subsystem so it can be used appropriately in future designs

Toyota Example: Radiators

- Traditional approach: Design radiator for a specific vehicle based on mechanical specifications written for that vehicle

- Toyota considers a range of radiator solutions based on cooling capacities and the cooling demands of various engines that might be used.
  - How the radiator actually fits into a vehicle would be kept loose so that Toyota's knowledge of radiator technology could be used to create the optimum design

- Toyota's system is "test & design" rather than the traditional "design & test."
  - Toyota engineers test at the fundamental knowledge level so they don't have to test at the later, more expensive stages of design and prototyping

Schematic / Bill of Materials

- What are the most common mistakes at this stage?
  - Poor component selection
  - Failure to properly derate

Component Selection

- KIS: Keep it Simple
  - New component technology can be very attractive
  - Not always appropriate for high reliability embedded systems
  - Be conservative
- Reality: Marketing hype FAR exceeds actual implementation
  - Component manufacturers typically use portable sales to boost numbers
  - Claim: We have built 100's of millions of these components without a single return!
  - Actuality: All sales were to two cell phone customers with lifetimes of 18 months

Component Selection (cont.)

- Even when used by hi-rel companies, some modifications may have been made
  - Example: State-of-the-art crystal oscillator required specialized assembly to avoid failures one to three years later in the field
- Prior examples of where care should have been taken
  - New technologies: X5R dielectric, SiC diodes, etc.
  - New packaging: Quad flat pack no lead (QFN), 0201, etc.

Derating: Component Ratings

- Definition
  - A specification provided by component manufacturers that guides the user as to the appropriate range of stresses over which the component is guaranteed to function
- Typical parameters
  - Voltage
  - Current
  - Power
  - Temperature

MSP430FG43x
MIXED SIGNAL MICROCONTROLLER

SLAS380B – APRIL 2004 – REVISED JUNE 2007

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} ..... –0.3 V to 4.1 V
Voltage applied to any pin (see Note) ..... –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal ..... ±2 mA
Storage temperature, T_{stg}: (unprogrammed device) ..... –55°C to 150°C
(programmed device) ..... –40°C to 85°C

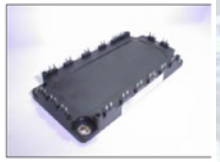
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

	MIN	NOM	MAX	UNITS
Supply voltage during program execution (see Note 1), V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})	1.8		3.6	V
Supply voltage during program execution, SVS enabled, PORON=1 (see Note 1 and Note 2), V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})	2		3.6	V
Supply voltage during flash memory programming (see Note 1), V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})	2.7		3.6	V
Supply voltage, V_{SS} (AV_{SS} = $DV_{SS1/2}$ = V_{SS})	0		0	V
Operating free-air temperature range, T_A	–40		85	°C

IGBT MODULE (U series)
600V / 100A / PIM



■ **Features**
- Low Vce(sat)
- Compact Package
- P.C. Board Mount Module
- Converter Diode Bridge Dynamic Brake Circuit

■ **Maximum ratings and characteristics**

● **Absolute maximum ratings (Tc=25°C unless otherwise specified)**

Item		Symbol	Condition	Rating	Unit
Inverter	Collector-Emitter voltage	V_{CES}		600	V
	Gate-Emitter voltage	V_{GES}		±20	V
	Collector current	I_C	Continuous	100	A
		I_{CP}	1ms	200	A
		$-I_C$		100	A
		$-I_{CP}$ pulse	1ms	200	
	Collector power dissipation	P_C	1 device	378	W
Brake	Collector-Emitter voltage	V_{CES}		600	V
	Gate-Emitter voltage	V_{GES}		±20	V
	Collector current	I_C	Continuous	50	A
		I_{CP}	1ms	100	A
	Collector power dissipation	P_C	1 device	187	W
Converter	Repetitive peak reverse voltage	V_{RRM}		600	V
	Repetitive peak reverse voltage	V_{RRM}		800	V
	Average output current	I_O	50Hz/60Hz sine wave	100	A
	Surge current (Non-Repetitive)	I_{FSM}	T_j=150°C, 10ms half sine wave	700	A
	I²t (Non-Repetitive)	I^2t		2450	A²s
Operating junction temperature		T_j		+150	°C
Storage temperature		T_{stg}		-40 to +125	°C
Isolation voltage	between terminal and copper base *2	V_{iso}	AC : 1 minute	AC 2500	V
	between thermistor and others *3			AC 2500	V
Mounting screw torque				3.5 *4	N·m

Derating

- Derating is the practice of limiting stress on electronic parts to levels below the manufacturer's specified ratings
  - Guidelines can vary based upon environment ("severe, protected, normal" or "space, aircraft, ground")
  - One of the most common design for reliability (DfR) methods
- Goals of derating
  - Maintain critical parameters during operation (i.e., functionality)
  - Provide a margin of safety from deviant lots
  - Achieve desired operating life (i.e., reliability)
- Sources of derating guidelines
  - Governmental organizations and 3rd parties
  - OEM's
  - Component manufacturers
- Derating is assessed through component stress analysis

Part Type	Derating parameters	Severe	Benign
Aluminium electrolytic caps	Voltage (% max rated)	70%	80%
	Temperature (°C)	T_{max} – 20°C	T_{max}– 20°C
Ceramic capacitors	Voltage (% max rated)	60%	70%
	Temperature (°C)	T_{max}– 10°C	T_{max}– 10°C
Solid tantalum capacitors	Voltage (% max rated)	70%	80%
	Temperature (°C)	T_{max}– 20°C	T_{max}– 20°C
	Reverse voltage (% max fwd)	2%	2%
Signal diodes	Forward current (% max rated)	90%	<100%
	Reverse voltage (% max rated)	70%	80%
	Max. junction temperature	95°C	115°C
Chip resistors	Power dissipation(% max rated)	50%	70%
Digital MOS and bipolar ICs	Fanout (% max rated)	90%	<100%
	Frequency (% max rated)	90%	<100%
	Output current (% max rated)	90%	<100%
	Max. junction temperature	95°C	115°C
Linear MOS and bipolar ICs	Frequency (% max rated)	90%	<100%
	Output current (% max rated)	90%	<100%
	Max. junction temperature	95°C	115°C

Criticality of Component Stress Analysis

- Failure to perform component stress analysis can result in higher warranty costs, potential recalls
  - Eventual costs can be in the millions of dollars
- Perspective from Chief Technologist at major Original Design Manufacturer (ODM)

  "…based on our experience, we believe a significant number of field returns, and the majority of no-trouble-founds (NTFs), are related to overstressed components."

Derating Failures

- Where are the derating mistakes?
- Problem #1: Designers do not derate
  - Failure to perform component stress analysis
- Problem #2: Derating does not have a practical or scientific foundation
  - Extraordinary measures are taken when inappropriate
  - Derating is excessive: ‘The more, the better’ rule

Failure to Derate: Common Examples

- Analog / Power Designs
  - Derating is typically overlooked during transient events
  - Especially turn-on, turn-off
- Digital
  - Excessive number of components and connections tends to limit attempts to perform component stress analysis

The Foundation of Derating

- To be effective, derating must have a practical and scientific foundation
  - Problem: Manufacturer's ratings are not always based on a practical and scientific foundation
- Manufacturers' viewpoint
  - Ratings are based on specific design rules based on materials, process, and reliability testing
- The reality
  - Ratings can be driven by tradition and market forces as much as science
- Best practice
  - Based on data from field returns
  - Based on test to failure qualification (especially for new suppliers)

Manufacturer's Derating (example)

- Tantalum capacitor
  - MnO_2 cathode
- Derating based on desired failure rate
  - 10 ppm at startup
- Why not 10 ppm failure rate at rated voltage?
- Was 0.3% failure rate acceptable?
  - 50% derating is a legacy

	MnO_2 (27Batches)
100 PPM FR % V_{Rated}	68%
@50% V_{Rated} FR(PPM)	9
@80% V_{Rated} FR(PPM)	458
@90% V_{Rated} FR(PPM)	1,700
@100% V_{Rated} FR(PPM)	2,943

Courtesy of Kemet

Derating Decision Tree

- Step 1: Derating guidelines should be based on component performance, not ratings
  - Test to failure approach (i.e., HALT of components)
  - Quantifies life cycle cost tradeoffs
  - For smaller OEMs, limit this practice to critical components

Derating Decision Tree (cont.)

- Step 2: Derating guidelines should be based on recommendations from the component manufacturer
  - They built it; they should know it
  - Don't trust the manufacturer? Use someone else
- Step 3: Derating guidelines should be based on customer requirements
- Step 4: Derating guidelines should be based industry-accepted specification/standard

Be flexible, not absolute

Layout / Mechanicals

- The biggest mistake at this stage of the design?
  - Manufacturability

- Problem is getting better, but suppliers will always try to build what you send them
  - If it doesn't work, rework!
  - Even some design for manufacturability (DfM) is limited; major problems are not always addressed

DfM

- Definition
  - The process of ensuring a design can be consistently manufactured by the designated supply chain with a minimum number of defects
- Requirements
  - An understanding of best practices (what fails during manufacturing?)
  - An understanding of the limitations of the supply chain (you can't make a silk purse out of a sow's ear)

DfM Failures

- DfM is often overlooked in the design process
- Reasons
  - Design team often has poor insight into supply chain (reverse auction, anyone?)
  - OEM requests no feedback on DfM from supply chain
  - DfM feedback consists of standard rule checks (no insight)
  - DfM activities at the OEM are not standardized or distributed

DfM Checklist

- Baseline
  - Your design matches their capabilities (75% ‘sweet spot’)
  - Design is transferable
- Bare Board
  - Trace width and spacings
  - Laminate material
  - Symmetry of stackup
  - Complexity of via connections
  - Incorporation of new materials (embedded passives)
  - Single-sided vs. double-sided
- System
  - Blind connections
  - Z dimension limitations
- Assembly
  - Elimination of hand soldering or wave soldering when possible
  - Proximity of components to flex points
  - Component spacing
  - Size of components and complexity of packaging
  - Orientation of components to wave solder
  - Shadowing during wave solder
  - Appropriate dimensions and spacings for PTHs and bond pads
  - Attachment methods
  - Moisture sensitivity level (MSL)

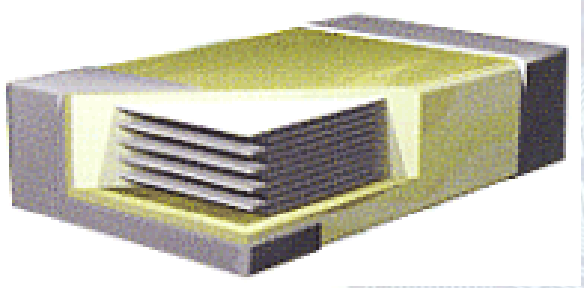
Designing for Defects

Solder Process	Defects per Million Opportunities	
	Standard	Best in Class
Hand	5000	N/A
Wave	500	20 - 100
Reflow	50	<10

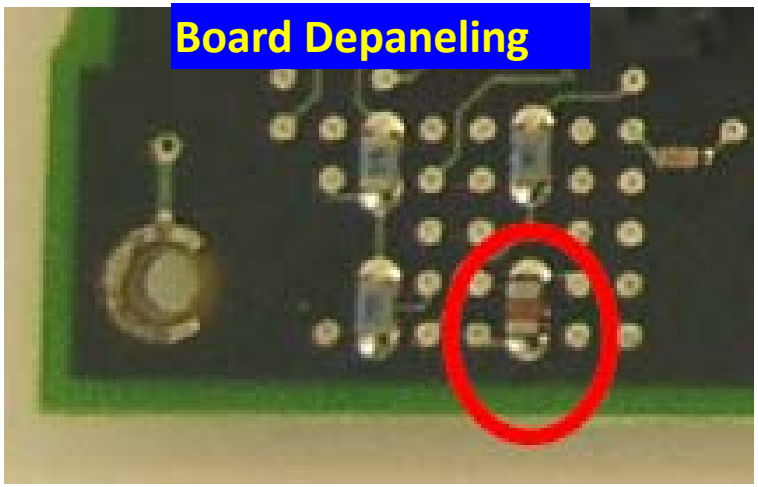
- Designs that avoid manual soldering operations reduce defects

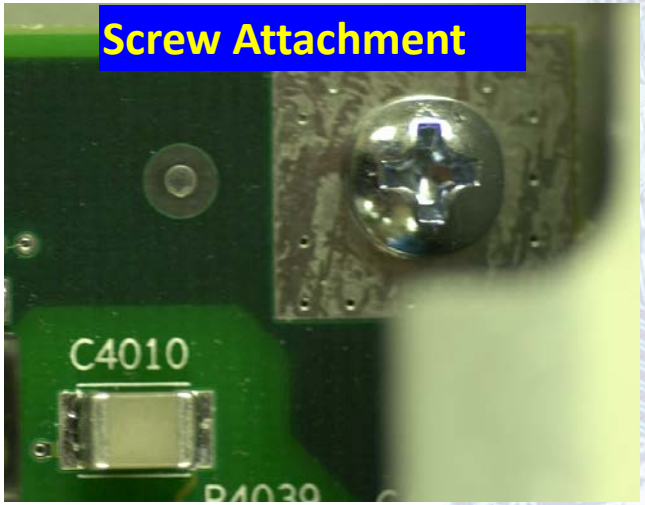
DfM Example: Flex Cracking of Ceramic Caps

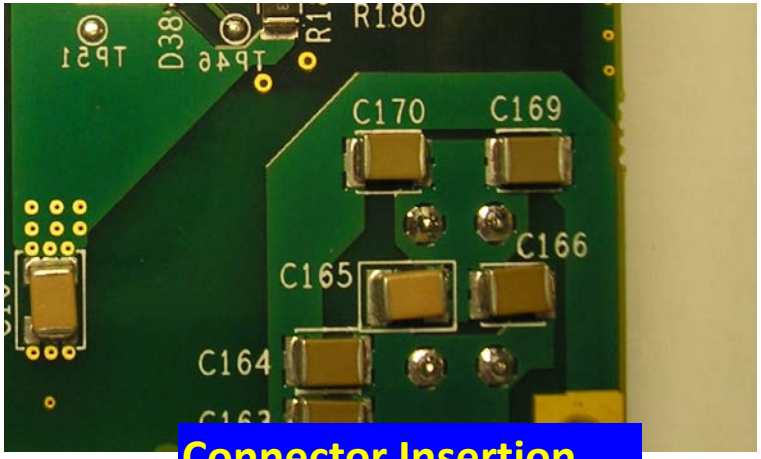
- Due to excessive flexure of the board
- Occurrence
  - Depaneling
  - Handling (i.e., placement into a test jig)
  - Insertion (i.e., mounting insertion-mount connectors or daughter cards)
  - Attachment of board to other structures (plates, covers, heatsinks, etc.)

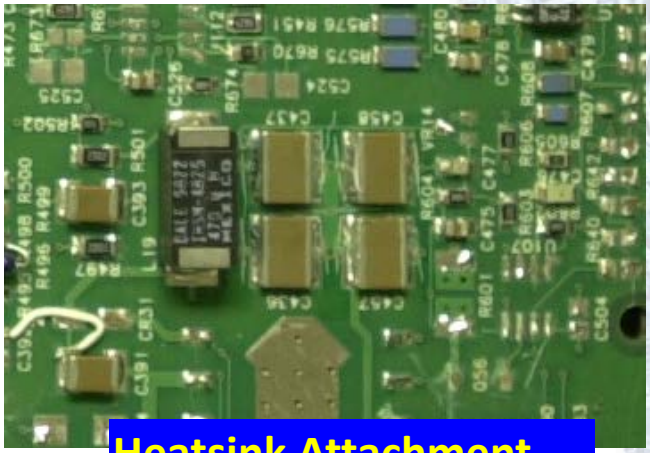


Flex Cracking (Case Studies)









Flex Cracking (cont.)

- Drivers
  - Distance from flex point
  - Orientation
  - Length (most common at 1206 and above; observed in 0603)
- Solutions
  - Avoid case sizes greater than 1206
  - Maintain 30-60 mil spacing from flex point
  - Reorient parallel to flex point
  - Replace with Flexicap (Syfer) or Soft Termination (AVX)
  - Reduce bond pad width to 80 to 100% of capacitor width
  - Transition to smaller case size
  - Measure board-level strain (maintain below 750 microstrain)

DfM Example (Plated Through Hole vs. Microvia)

- What should be the minimum diameter of a PTH in your design?
- What should be the maximum aspect ratio (PCB Thickness / PTH Diameter)?
- When should you switch to microvias?
- Answer: Depends!
  - Supplier
  - Reliability needs

Courtesy of CAT

PTH Diameter

- Data from 26 board shops
  - Medium to high complexity
  - 62 to 125 mil thick
  - 6 to 24 layer
- Results
  - Yield loss after worst-case assembly
  - Six simulated Pb-free reflows

Process Attribute	Hole/land (mils)	Count	Min	Q1	Median	Q3	Max
Yield Loss from Assembly Simulation (%) Threshold: Open	8 / 18	6	0.00	0.00	0.31	3.24	17.16
	10 / 20	15	0.00	0.00	0.00	1.13	4.60
	12 / 22	26	0.00	0.00	0.00	0.00	5.23
	13.5 / 23.5	26	0.00	0.00	0.00	0.00	4.09
	14.5 / 24.5	19	0.00	0.00	0.00	0.00	0.00
	16 / 26	11	0.00	0.00	0.00	0.00	0.00

Yield loss can results in escapes to the customer!

Are Microvias more reliable than PTHs?

- Depends!!
- Quality
  - Some fabricators have no problems
  - Some have more problems with microvias
  - Some have more problems with PTHs
  - Some have problems with both
- Reliability
  - A well-built microvia is more robust than a well-built PTH

Courtesy of CAT

PTH vs. Microvia

PTH Quality

Process Attribute	Hole/land (mils)	Count	Min	Q1	Median	Q3	Max
Defect Density (Defects per Million Vias)	8 / 18	6	25	60	177	380	737
	10 / 20	15	0	15	44	178	2947
	12 / 22	26	0	0	6	30	1013
	13.5 / 23.5	26	0	0	0	27	512
	14.5 / 24.5	19	0	0	0	17	173
	16 / 26	11	0	0	0	0	44

Microvia Quality

Process Attribute	Annular Ring (mils)	A	B	C	D	E	F	G
Defect Density (Defects per Million Vias)	2 / 8	7384	8007	26598	68	61	598	81
	3 / 9	5527	2558	1736	38	8	76	24
	4 / 10	2370	1187	17	23	0	53	0
	5 / 11	2092	372	0	15	0	91	32

Summary (PTH and Microvias)

- The capability of the PCB industry in regards to hole diameter tends to segment
  - Very high yield (>13.5 mil)
  - High yield (10 – 13.5 mil)
  - Lower yield (< 10 mil)

- If 8 mil drill diameter is required
  - Consider using PCQR^2 to identify a capable supplier
  - Consider using interconnect stress test (IST) coupons to ensure quality for each build
  - Consider transitioning to microvias (6 mil diameter)

Summary of Lessons Learned

- Step 1: Don’t paint yourself into corner too early in the design process
- Step 2: Be aware of ALL requirements
- Step 3: Try to perform concurrent engineering
- Step 4: Use a design check list (don’t rely on tests to develop a robust design)
  - Part selection
  - Derating
  - ESD
  - EMI / EMC
  - Design for Manufacturability / Testability / Environment
  - Components that wearout