IPC Midwest 2011

Evolution Toward a Workmanship Standard For Underfill

Bev Christian, Ph.D.

Research in Motion Limited

Executive Summary

There is no issued industry standard for the workmanship of underfills – either from the perspective of visual examination (a la A-610) or by more intrusive techniques like cross-sectioning. This presentation will highlight what has been put together and submitted to the appropriate IPC standards committee for consideration. Further some challenges faced by trying to meet this standard may be delineated as well.

Evolution towards a Workmanship Standard for Underfill

Bev Christian, PhD
Director, Materials Interconnect Research
Research In Motion

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Why are Underfills Used?

- Underfills are used in the handheld industry for three reasons:
- Security
- Reliability
  - Mismatch of thermal coefficients of expansion
  - Shock (being dropped)

History of Underfill

- Preceded by use of potting compounds, solder masks, temporary solder masks, conformal coatings, adhesives, paste fluxes, solder pastes
- First used when flip chips moved from ceramic substrates to FR4
- Now also used for BGAs and CSPs
- IPC Task group first starting working on a guide for their use in 1997
- Issued in September 2005

What has Transpired?

- The guidebook good, but not specific enough
- Wrote a strawman using:
  - the guide
  - material from a course written by Dr. Brian Toleno (Henkel)
  - experience using the materials
- Posted it on TechNet
- Debate followed
- Edited and morphed the document

What has Transpired? (cont'd)

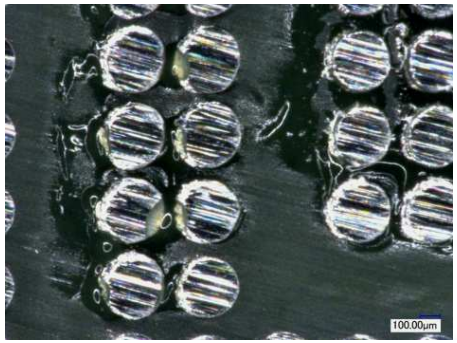
- Received additional information from Celestica
- Wrote two documents
  - One in IPC format with sections dealing with Class 1, 2 and 3 products
  - The other document is an internal RIM document for our Class 2 product

Current Situation

- Have handed the former document over to the underfill task group of the IPC
- Where would it go?
  - Stand alone?
  - In IPC-A-610?
  - In a new, separate document?
  - As an addition to the next edition of the guidebook?

Challenges Using Underfill

- Matching coefficient of thermal expansion and modulus of elasticity to product
- Finding an adequate, reliable source
- Transportation and storage (pot life)
- Making sure material does not cause corrosion
- Interaction between some underfills and solder paste residues



Challenges Using Underfill

- **Knowing if you applied it correctly**
  - Dealing with one piece RF cans
    - Cans with limited holes
  - Less than ideal spacing between components
  - Increasingly low standoff of components

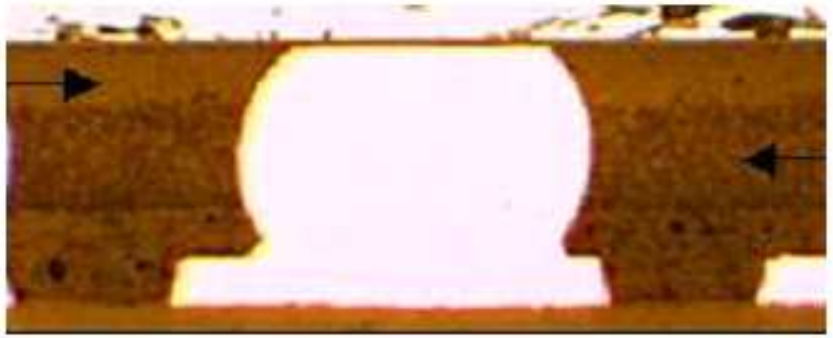
Examination of Applied Underfills

- Can't use X-ray inspection
- Can't use acoustic microscopy once you move from flip chips to CSPs and/or BGAs (too many layers)
- Visual inspection
  - Only good for detecting flow-out and fillet formation
  - Very difficult, if single piece RF cans are over components
- Nothing beats cross-sectioning

Cross-sectioning

- Traditional cross-sectioning (xz or yz planes)
  - Familiar
  - Shows if you have filler settling
  - Only shows you one plane of solder balls, unless you sequentially grind/polish through to additional planes

Low density of fillers



High density of fillers

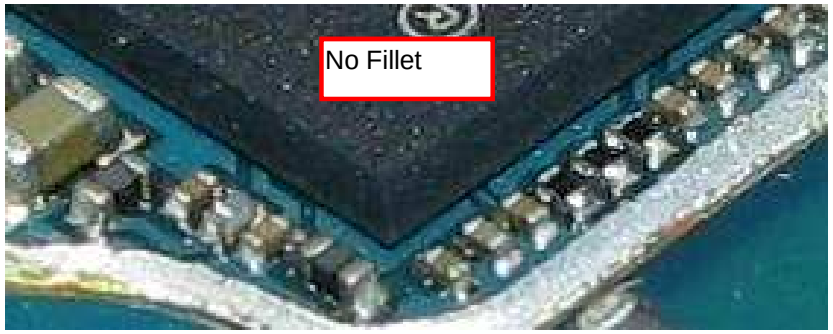
Cross-sectioning (cont'd)

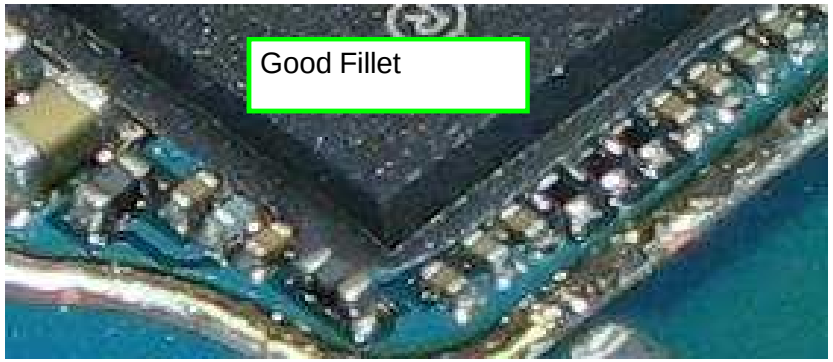
- Planar cross-sectioning (x-y plane)
  - Requires considerable skill
    - Where do you stop your grinding?
  - Really the only way to get more than a cursory inspection result for underfill application

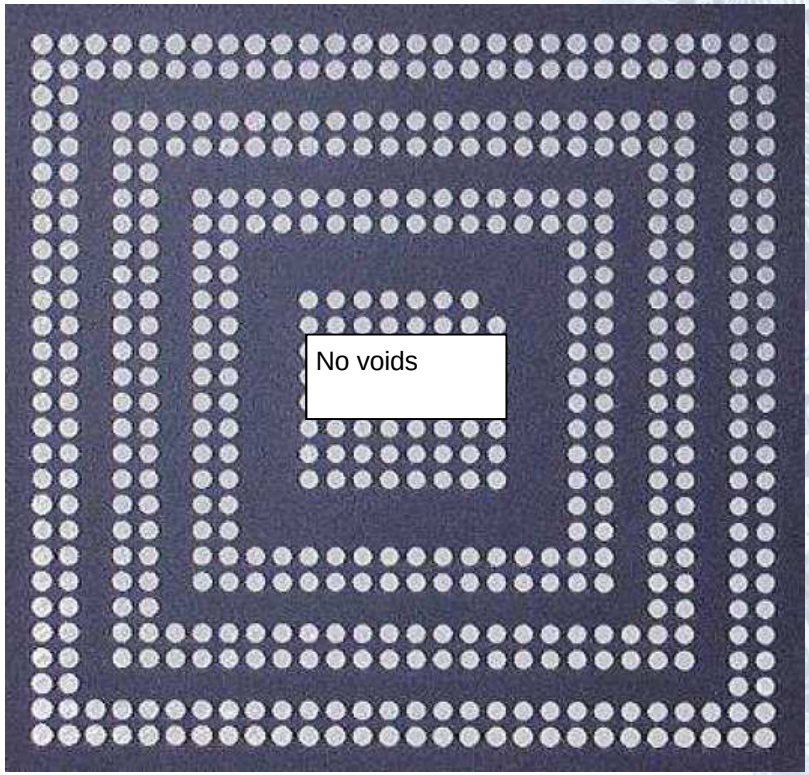
What is Included in the Documented Material?

- Ideal
- The component requiring underfill is completely underfilled with a good fillet all the way around, no encroachment on to components, no overfill and no voiding. Refer to J-STD-030 for fillet acceptability.

No fillet, good fillet, no voids



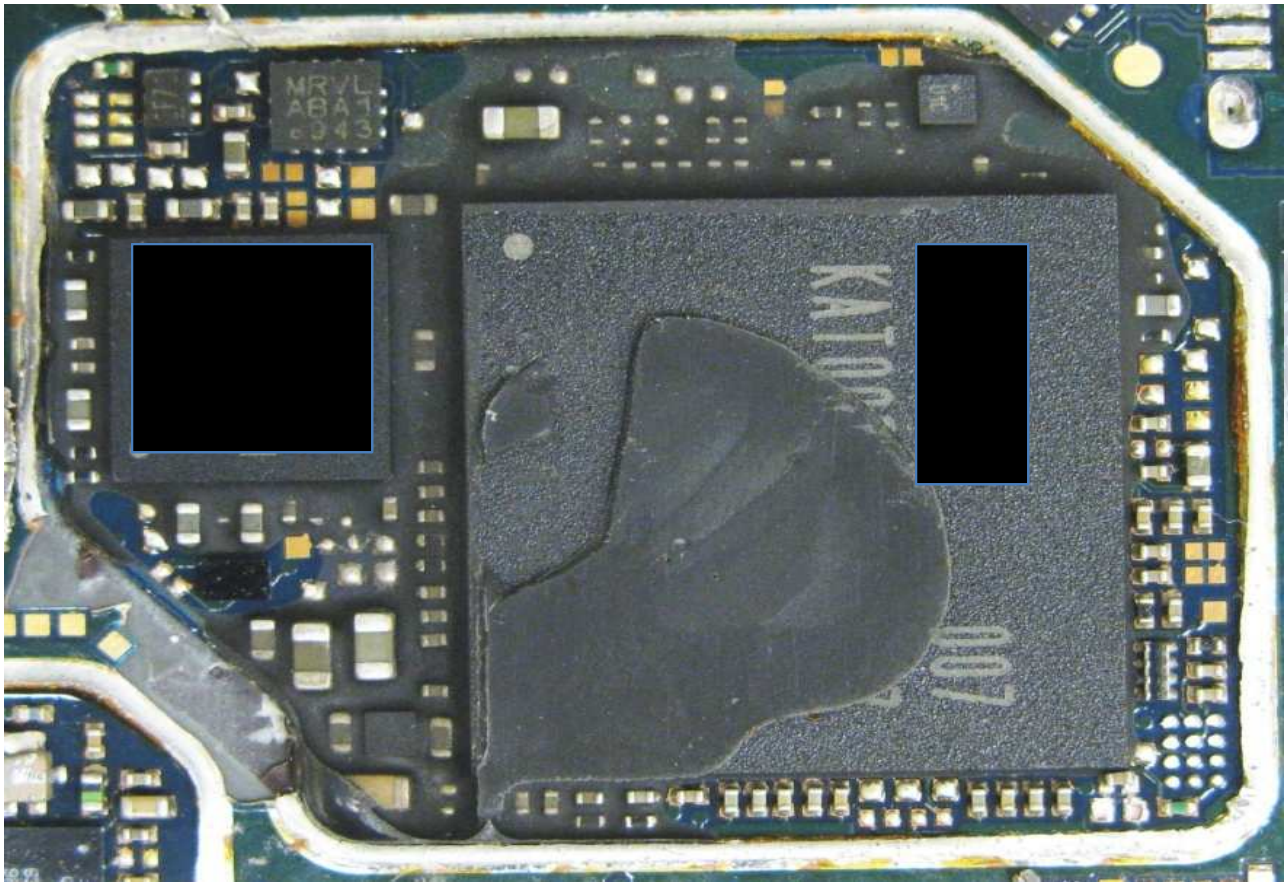




What is Included?

- Underfill on top of underfilled components
  - Several (but not all) Class 3 users told me that underfill allowed to flow up onto the top of components could lead to failure during thermal cycling
  - Underfill allowed to make contact between the top of a component and the inside of an RF can could potentially transmit forces to the component during drops

Underfill between Part and RF Can

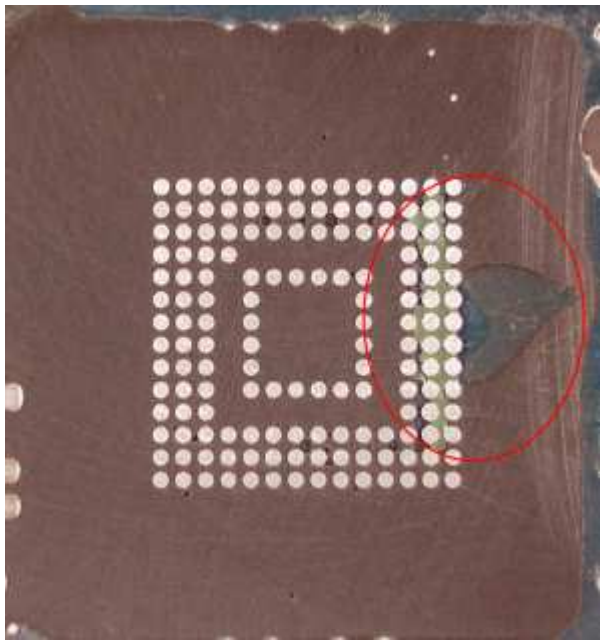


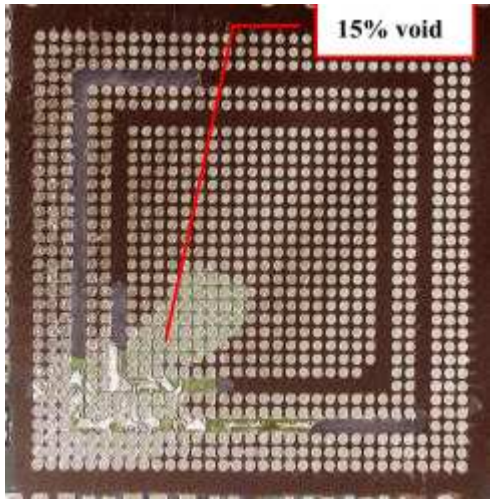
Voids

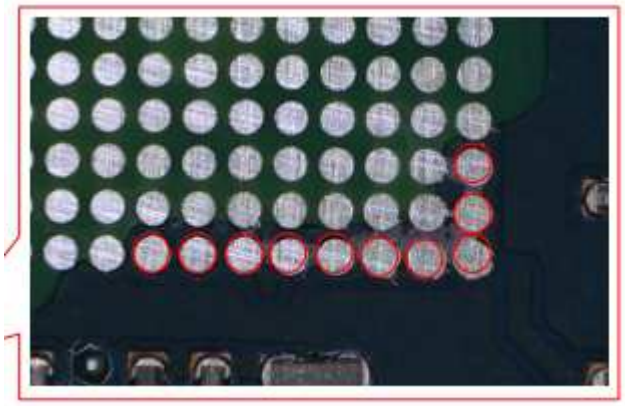
- **Does one really care?**
- **It depends! ©**

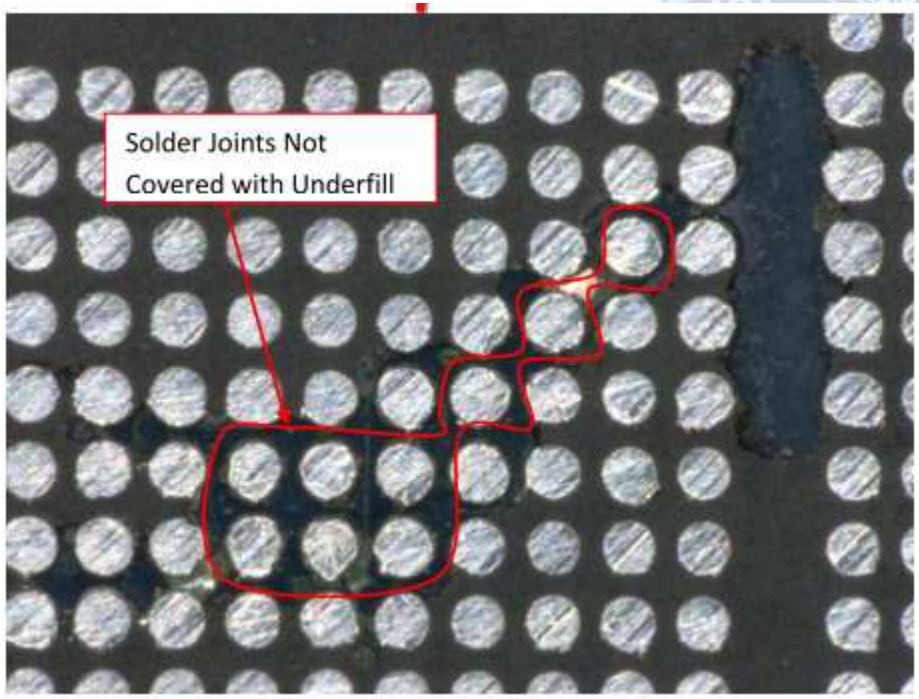
Voids

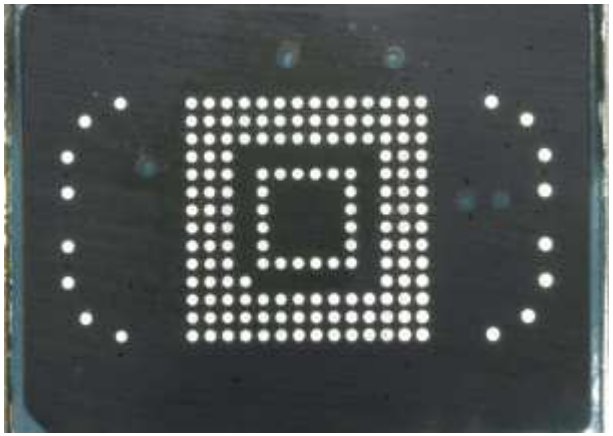
- Expected thermal cycle extremes
- Lifetime of the product
- Class of product
- Type of solder used

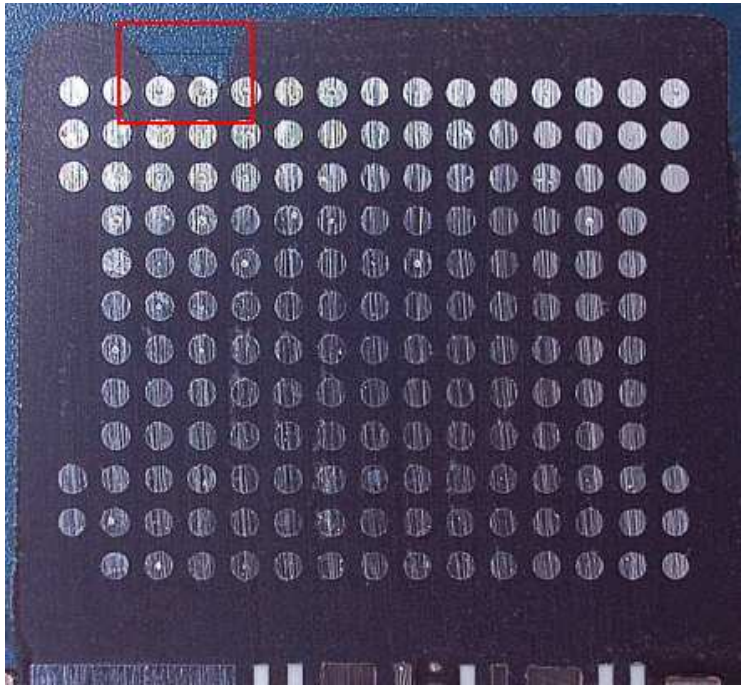


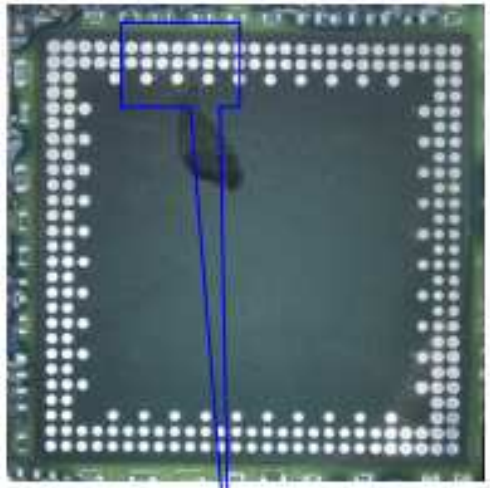

15% void

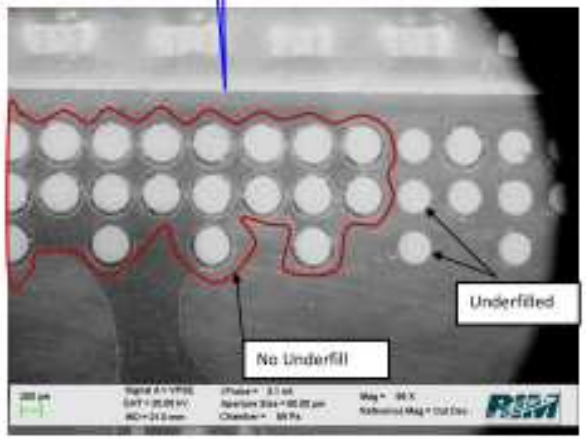


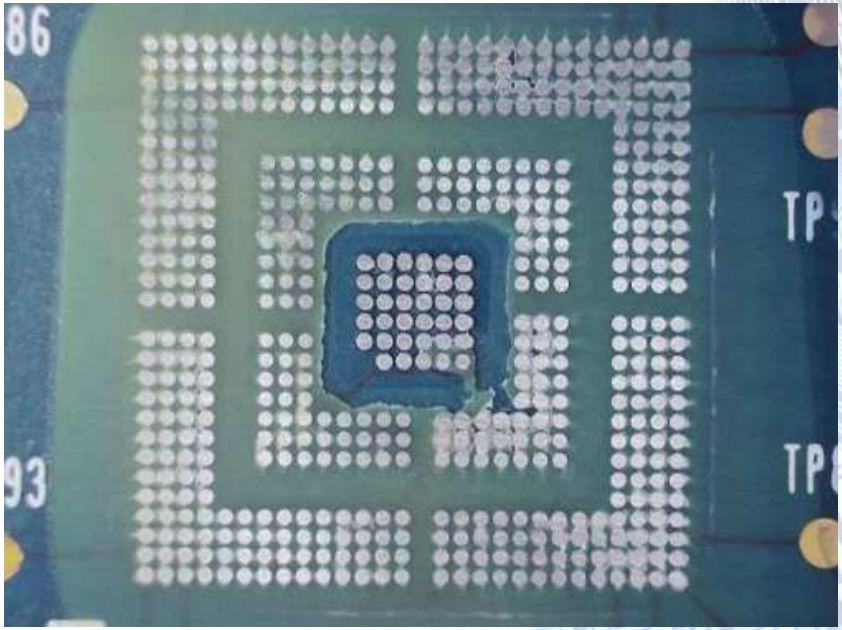

Solder Joints Not
Covered with Underfill








Underfilled
No Underfill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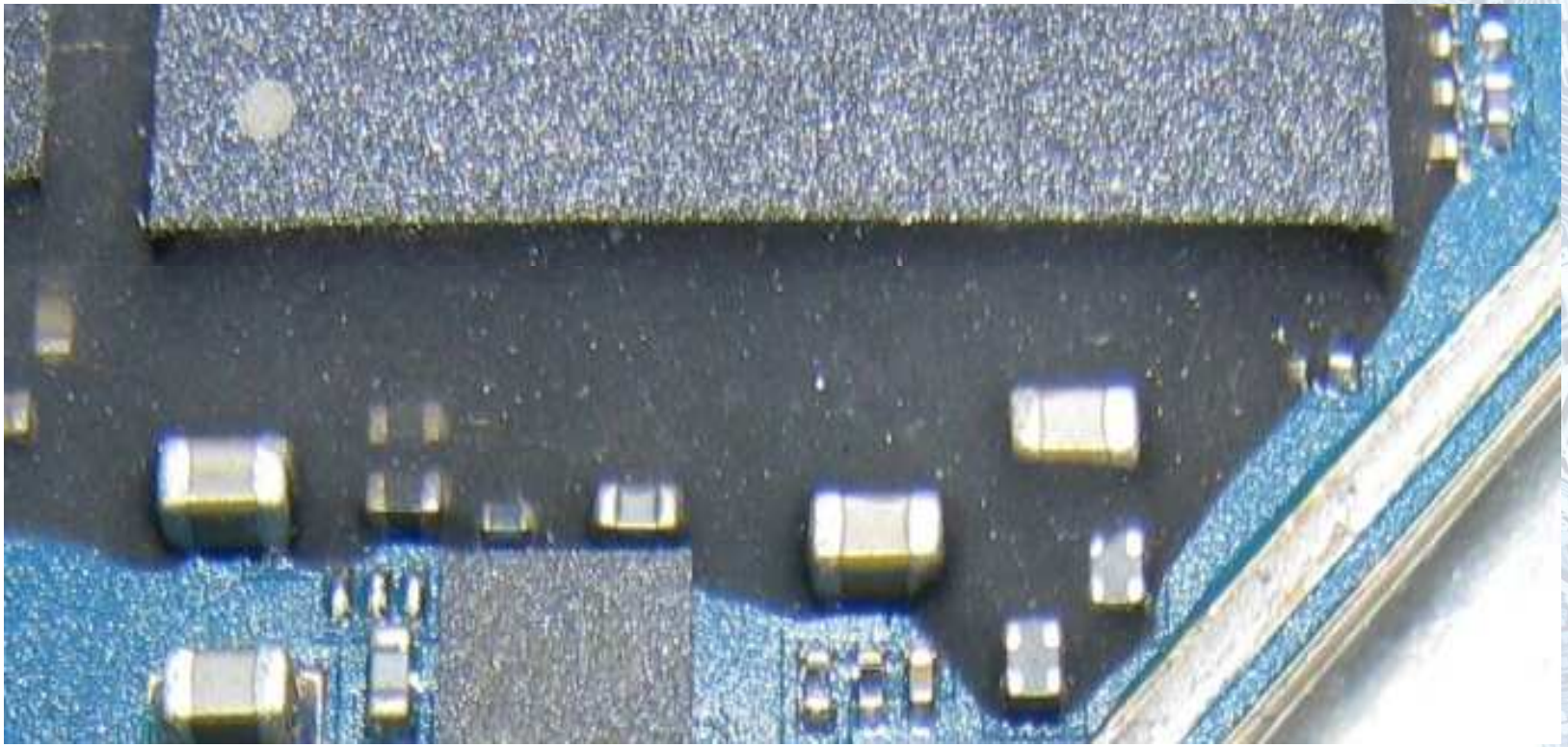
93

Underfill Reaching Unintended Components

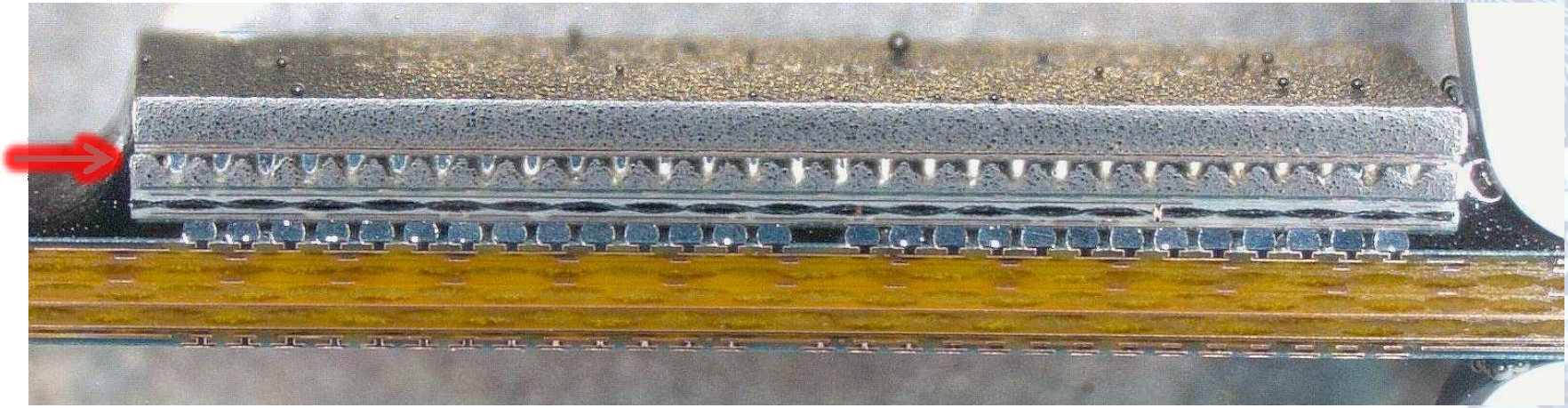
- Is your volume application under control?
- Is you target component starved for underfill?
- Have you half underfilled an adjacent array BGA, CSP or FC?
- Have you embedded chip components that might then be susceptible to damage where they wouldn't have been otherwise?

Embedded Chip Components – Good or Bad?



Miscellaneous

Try adding Underfill!



Summary

- Less overmold = more underfill use
- Application well understood
- Nevertheless, challenges exist
- No magic wand available for examination
- All invited to participate in building a true workmanship standard

Questions?