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Design and Process Implementation Principles for Embedded Components

Vern Solberg
STC-Madison

Biography:
Vern Solberg is an independent consultant specializing in SMT and microelectronics design and manufacturing technology. He has served the industry for more than twenty-five years in areas related to both commercial and aerospace electronic products and is active as an author and educator. Solberg holds several patents for 3D semiconductor packaging innovations and is the author of Design Guidelines for Surface Mount and Fine-Pitch Technology a McGraw-Hill publication and furnishes the 'Designers Notebook' column for SMT magazine. Vern was also awarded the prestigious 'Raymond E. Pritchard Hall of Fame Award' and is currently an active member of IEEE, SMTA, IMAPS and the IPC, the industries standards development organization for electronics. Current IPC activity- Co-Chairman of the task group currently developing the IPC-7092, 'Design and Assembly Process Implementation for Embedded Components'.

Executive Summary
Companies attempting to improve PCB functionality and minimize space are now considering embedding a broad range of components within the circuit structure. Both uncased active and passive component elements are candidates for embedding but the decision to embed components within the multilayer circuit structure must be made early in the design process. Some components are easy candidates for integrating into the substrate while others may be difficult to rationalize because they involve more complex process methodology. Although many of the discrete passive and active devices may remain mounted to the outer surfaces of the multi-layer board, embedding components within the inner layers of the structure will enable greater utilization of the circuit board structure. Additionally, the embedding of uncased semiconductor elements directly in-line with a related semiconductor package mounted on the outer surface significantly reduces inductance and contributes to increasing signal speed. This paper will include design guidelines, material selection and how to utilize micro-via build-up termination methodology for interconnecting both passive and active semiconductor elements. Examples will be furnished to help the product designer and manufacturing specialist in selecting components for embedding and the methodologies typically adopted for developing the circuit board structure.

Design and Process Implementation Principles for Embedded Components

Vern Solberg
STC-Madison
Madison Wisconsin USA

Introduction

- Both uncased active and passive component elements are candidates for embedding but the decision to embed components within the multilayer circuit structure must be made early in the design process.
- Some components are easy candidates for integrating into the substrate while others may be difficult to rationalize because they involve more complex process methodology.

A key issue developers will need to address early on in the design phase of the embedded component product are; what will be the most suitable base material for the substrate and which components will be the best choice for embedding?

1. Substrate Material Selection

- Industry roadmaps consistently point to materials and process refinement as the key enablers for improving product performance and manufacturing efficiency.
- Likewise, the conversion to lead-free solder technologies has forced the laminate industry to make significant refinement to all packaging and substrate related materials.
- The substrate methodologies being used for embedded semiconductor and passive component packaging utilizes one of the following dielectric systems:
  - FR-4 or FR-5 Epoxy/Glass
  - BT Epoxy/Glass
  - Polyimide film (PI)

Epoxy/Glass Composites

- The FR-4 and FR-5 family of substrate materials have been (and will continue to be) the “work-horse” of interconnection technology.
- The materials are widely available, very versatile and they can be altered to accommodate different product functions or applications, including semiconductor packaging, hand held portable products and system level boards.
- Although all epoxy/glass laminates have similar physical attributes, the products that adapt these materials often have very different manufacturing focus and performance requirements.

Improving the Physical Robustness of the Base Material

- Although the Tg is important, more important for assembly processing is-
  - limiting Z-axis expansion
  - increasing decomposition temperature (T_d)
  - improving the inter-laminar adhesion

With a lower expansion ratio, the substrate should not experience damaging stresses during multiple solder process exposures above 240ºC.

Bismaleimide-Triazine (BT)

- BT laminate is one of the preferred substrate materials for array configured semiconductor package applications initially developed by Mitsubishi Gas and Chemical .
- The company discovered that, when compared to standard epoxy resin systems, the blending of bismaleimide / triazine and epoxy provided-
  - Enhanced thermal and mechanical stability
  - Improved electrical performance.
  - Furnishes a higher Tg (180ºC),
  - Lower coefficient of thermal expansion
  - Improved electrical insulation in high humidity and temperature.

Polyimide (PI)

- Polyimide based substrates are composed of high-strength and high-temperature polymer material system engineered with an 'all polyimide resin chemistry' that is suitable for any electronic package application requiring the ultimate performance.
- Thermal stability of the polyimide composition and glass fiber reinforcement makes this material particularly attractive for products with stringent high temperature requirements and a low coefficient of thermal expansion (CTE) to provide excellent plated through-hole reliability.

Material Supply Chain Concerns

- Although many of these material systems can furnish excellent functional capability they do not all have a wide supply base.

Type	Resin	Reinforcement	T_g (ºC)
FR-4	Epoxy	Woven E Glass	130-170+
B-T	Bismaleimide triazine/epoxy	Woven E Glass	170-230
PI	Polyimide	Woven E Glass	250-265

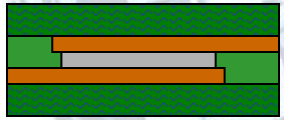
Data source: IPC-4101

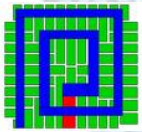
Because BT and PI may have more limited applications, fabrication costs are somewhat higher than the more common FR-4 based substrate.

2. Embedding Passive Components

Formed device integration

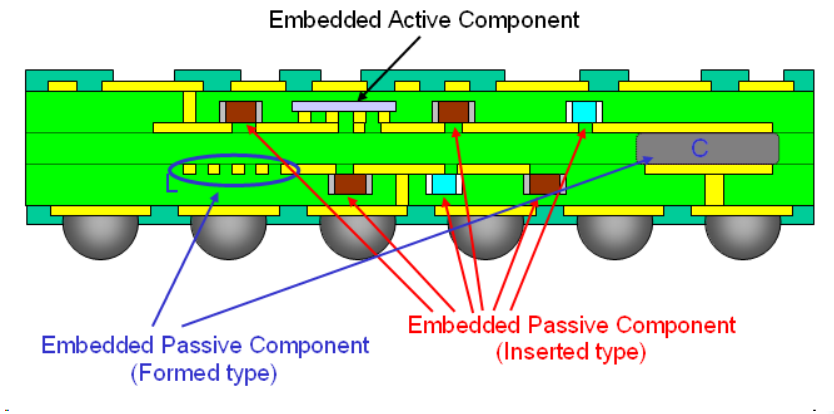
- Formed resistors-
  - Several companies have developed material sets and fabrication processes for thick-film resistors, requiring only a conventional screen-printing process.
- Formed capacitors-
  - The capacitor dielectric separating the copper surfaces of the power and ground plane an organic polymer thick film or ceramic thin film composite.
- Formed inductors-
  - A specific inductance can be developed using thin circuit trace patterns configured in spiral like geometry





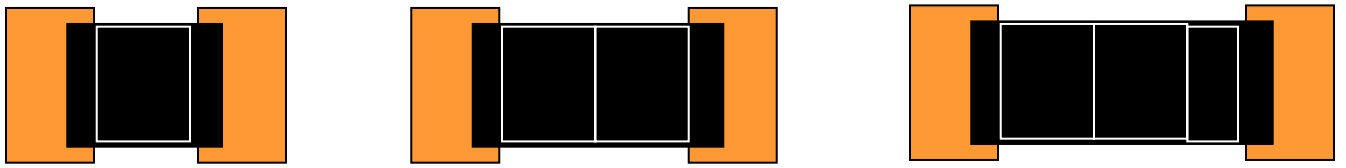
Formed Resistor Variations

- Materials incorporated into the board during
- Manufacture:
  - Part of the PCB structure or substrate
  - Either internal or near surface of board
- Forms –
  - Laminate/foil
  - Paste/liquid
  - Plated
  - Thin-film metal



Formed Resistors Using Conductive Thick Film Materials

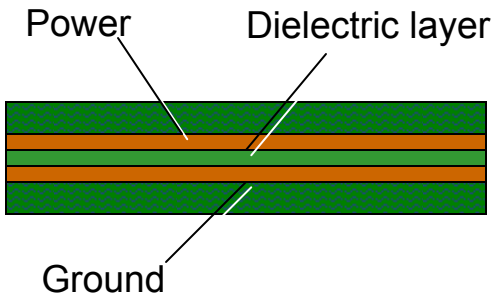
- Polymer thick-film (PTF) and ceramic thick-film (CTF) resistors can also be formed directly onto the laminate surface.
- The application of these materials require only conventional screen printing processing to provide the resistor pattern.
  - The paste-like PTF material is available in resistance values that range between 1 ohm and 1 meg ohm per square while the CTF materials value will range between 10 ohms and 10K ohms.



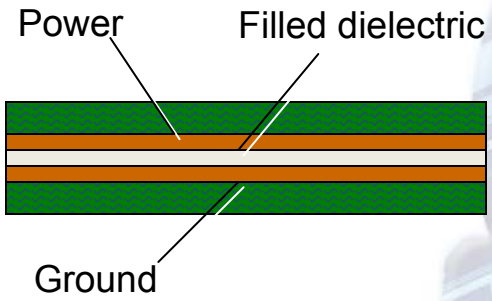
1 sq = 1KΩ | 2 sq = 2K Ω | 2 1/2 sq = 2.5K Ω

Formed resistors using thick film materials

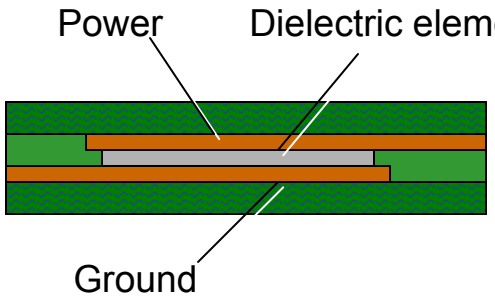
In-laminate Formed Capacitors



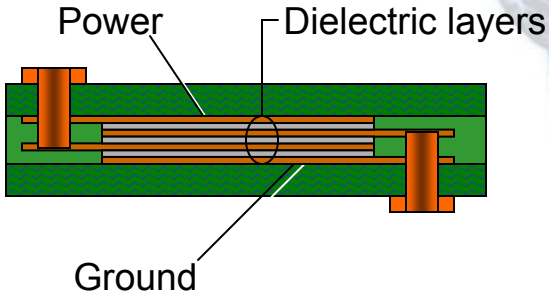
Planar



Planar



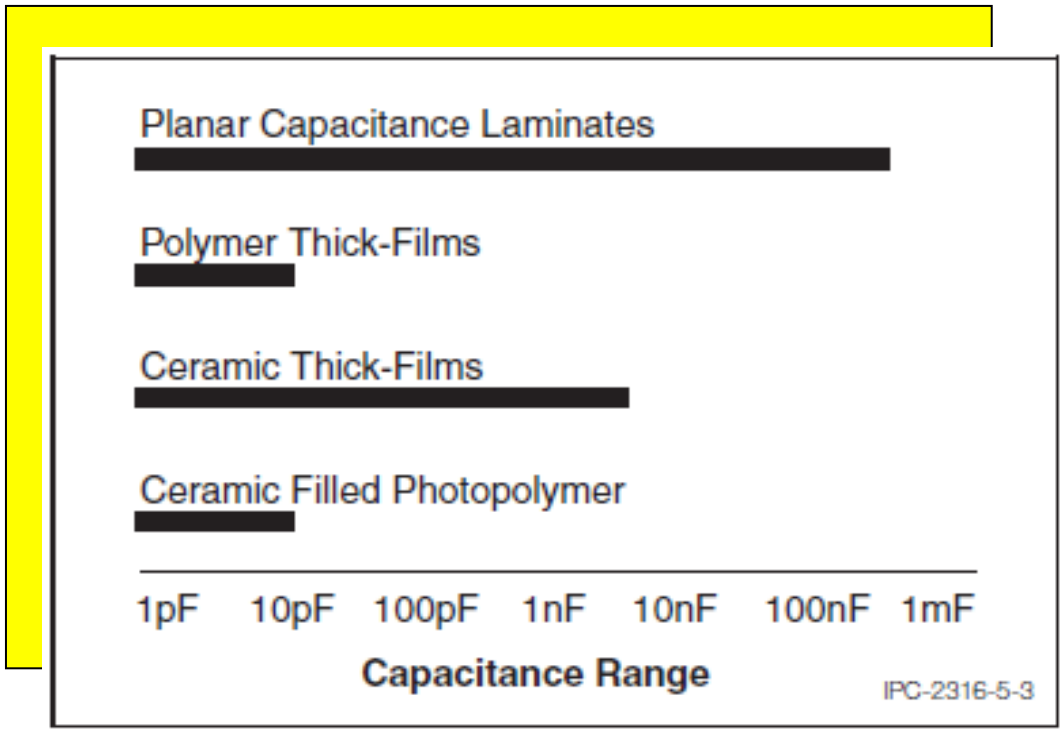
Discrete



Sequential layer

Embedded Capacitor Materials

Formed capacitor materials can be organized in two categories: laminates or pastes/inks.



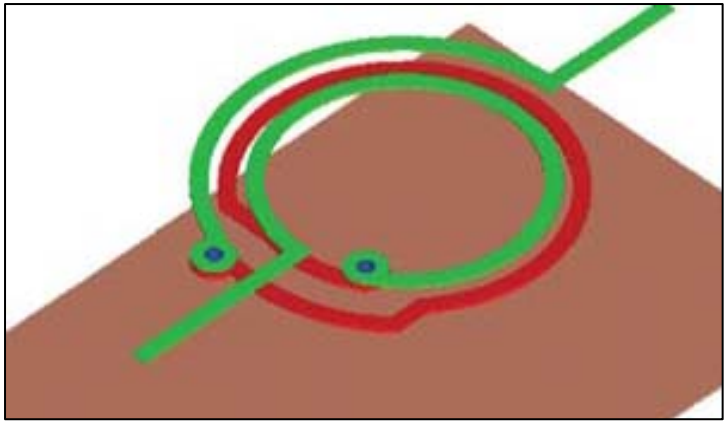
Source: IPC-2316

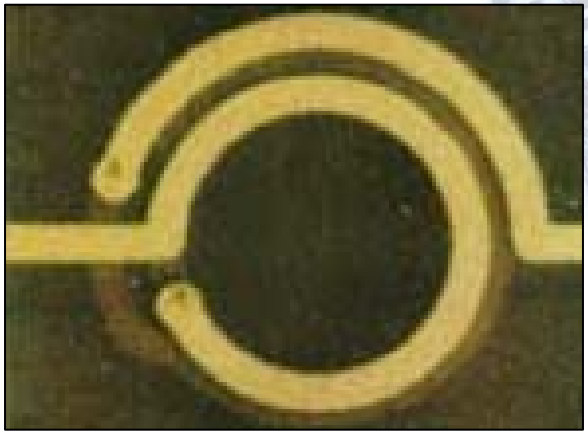
Formed Capacitor Elements

- Process variations-
  - Etched copper planes using unfilled and filled copper clad laminate.
  - Photo-imageable using filled polymer film
  - Photo-print using filled dielectric sheet material
  - Photo-imageable filled dielectric sheet material
  - Dielectric filled copper clad laminate
- Monetary impact-
  - Minimal for all photo-print products
  - Precision screen-printing may be required
  - Precision imaging may be required
  - Some material may need a high temperature furnace
  - Many products and processes will require licensing

Formed Inductors

- Formed inductors are not new elements in printed board designs.
- Formed inductors are current loops configured to induce a magnetic field for storing and controlling inductive energy.

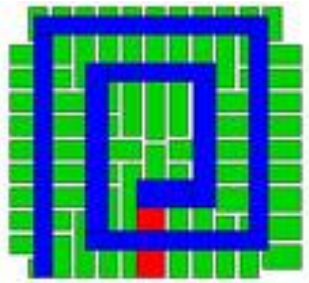




Example source: IPC-2316

Formed Inductor Design

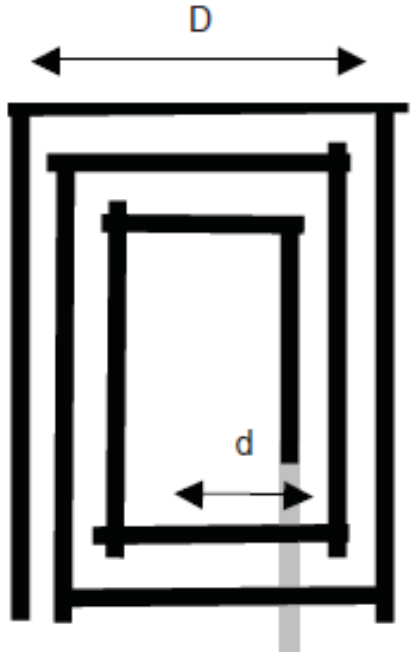
- The inductor commonly designed into a circuit structure is the ‘spiral’ inductor.



  - The inductance is determined by the length of the spiral and number of turns.
  - The spacing between turns will control the resonant frequency of the inductor.
  - A wider spacing will typically reduce capacitance and raise the inductance frequency.

Spiral Inductor Design Principles-

- The sizing of inductors is dependent on a number of parameters-
  - Line width
  - Spacing
  - Geometry
- Single layer copper spirals can only reach about 10nH, however, multi-layer spirals can reach up to 30 nH.



a = (D+d)/4
c = (D-d)/2
N = no. of turns
S = spacing
t = metal thickness
D = outermost dimension
d = innermost dimension

Inductance
$L = 0.0241aN(5/3)\ln[8(a/c)]$

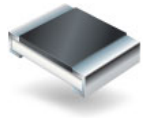
Source: IPC-2316

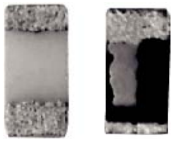
Utilizing a ferromagnetic material either as a core within loops of copper or lying beneath or sandwiching a spiral can possibly extend the inductor value into the 100nH range.

Inserted Passive Components

Discrete device attachment

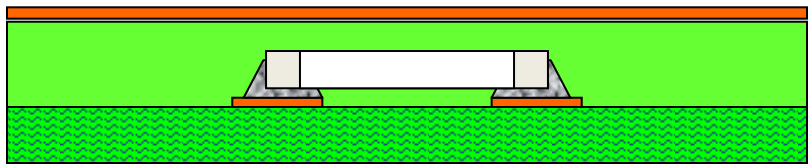
- As an alternative to forming component parts, many companies are inserting discrete passive components within the multilayer circuit.
- Inserted resistors elements-
  - The smallest discrete resistor is furnished in a standard 01005 package outline in all standard values.
- Inserted capacitors-
  - The capacitor family includes the 01005 package outline as well, but value range will be limited.
- Inserted inductors-
  - Small outline inductors are available from limited sources with values ranging up to 100nH.



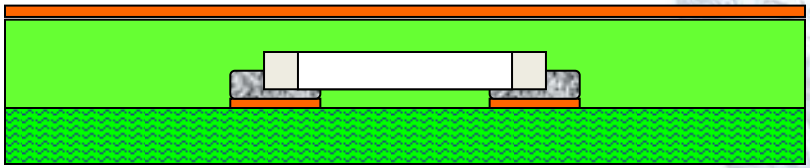


Inserted Passive Component Process

- Miniature passive components can be mounted directly onto the inner layer base substrate but handling and placement will require systems with a high level of positional accuracy.
- Interconnection can be made using deposited solder paste and reflow processing or secured using a anisotropic conductive polymer and a thermal cure process.



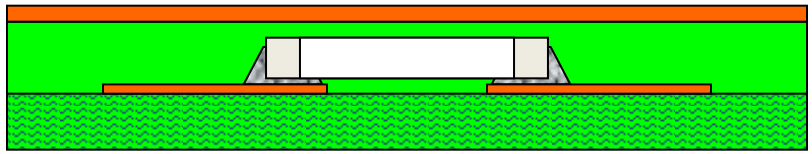
Reflow solder



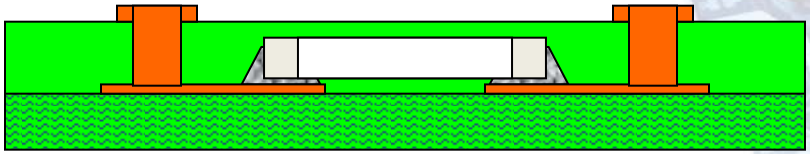
Conductive polymer

Lamination and Circuit Interface Process

- Following component termination a build-up layer of glass reinforced prepreg and copper foil material or resin coated copper (RCC) is laminated over the devices.
- As a result of the lamination process the resin material of the prepreg or RCC will flow in and around the device achieving complete encasement.
- To provide an electrical interface to the outer copper surface layer, small (micro-via) holes are formed using very small diameter drills or laser ablation.



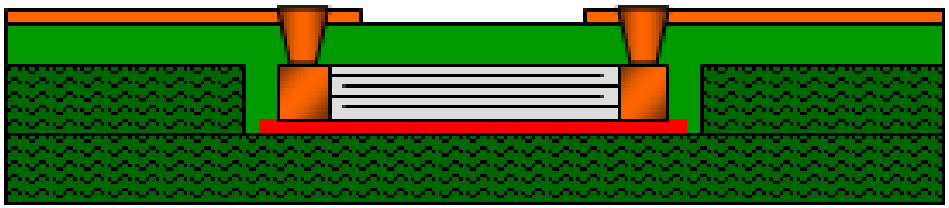
RCC lamination



Micro-via interface

Alternative Termination Process

- Rather than relying on solder or conductive polymer for electrical interface, passive devices can be mounted onto the substrates surface with a non-conductive adhesive.
- Electrical termination can then be made directly onto the component terminals with micro-via ablation and copper plating process.

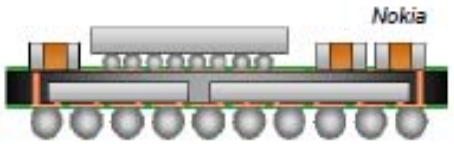


To achieve the most reliable micro-via to component interface the user should specify copper plated terminals.

3. Embedding Active Components

Attachment and interface methodology

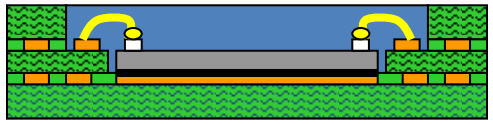
STATs ChipPAC



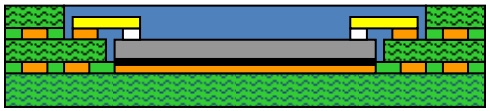
- Progress in developing high density embedded component substrate capability has accelerated through the cooperation and joint development programs between a number of government, industry and technical universities.
- In addition to these joint development programs, several independent laboratories and package assembly service providers have developed a number of proprietary processes for specific applications.

Die Attach and Interface

- There are a number of methods being used for interconnecting uncased semiconductor components.
  - The face-up attachment method traditionally adopts an adhesive material (liquid or film) for initially attaching the die to the substrate interposers' surface.
  - Both wire-bond and ribbon-bond processes may be applied for completing the cavity type die-to-substrate interface.



Face-up in cavity wire-bond

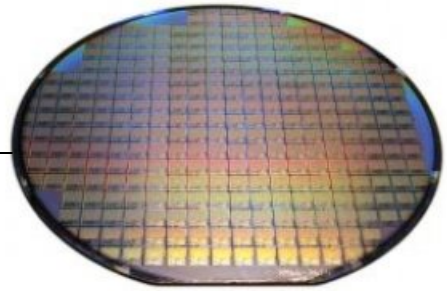


Face-up in cavity ribbon-bond

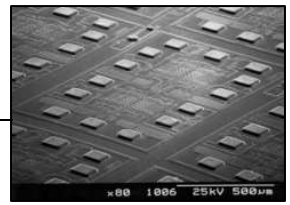
- Following the die attach and termination process the die element is commonly encapsulated with an epoxy compound that, when cured, becomes a homogeneous part of the substrates structure.

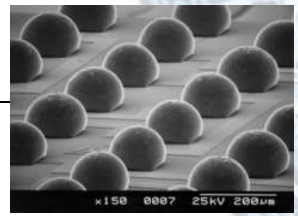
Flip-Chip Interface Preparation

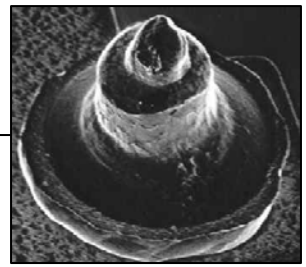
- Mounting the semiconductor in the facedown orientation (flip-chip) requires additional preparation to the die element while in the wafer level format-



  - Prepare aluminum bond sites with UBM process.
  - Deposit or print solder bump for reflow solder processing.
  - Or, provide a gold ball bump for conductive polymer or gold-to-gold interface.



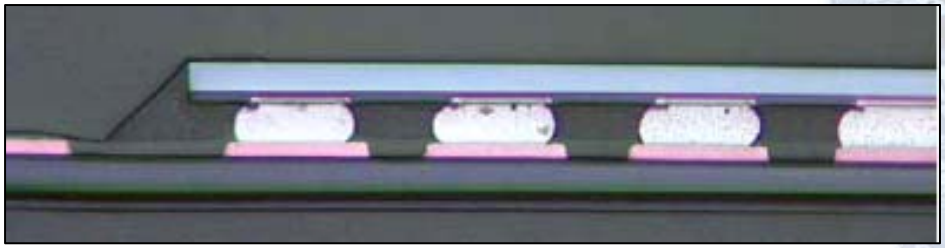




Example sources: Semiconductor Design And Pac Tech

Flip-Chip Attachment

- Reflow solder processing is the most common technique for flip-chip assembly and a substantial infrastructure already exists for supplying systems for both high and low volume manufacturing.
- Common methods for mass reflow soldering include:
  - Hot Air/Gas Convection
  - Infrared
  - Conduction
  - Vapor Phase



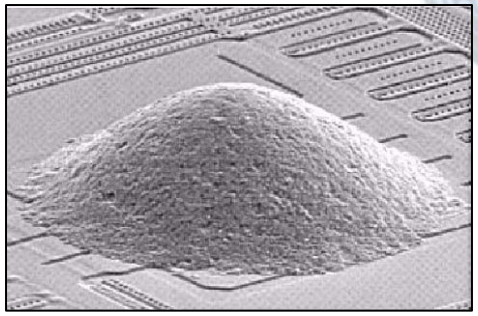
Example source: Auburn University

Conductive Polymer Adhesives

- Most polymer adhesives used in flip-chip semiconductor assembly contain a large percentage of silver alloy particles for electrical conductivity.
- The polymer adhesives initially contain solvents that allow easy dispensation, and are cured by exposure to high temperature in the presence of catalysts.
- Curing consists of two steps:

  1) outgassing of the solvents

  2) polymerization of the paste into a cross-linked thermoset condition.

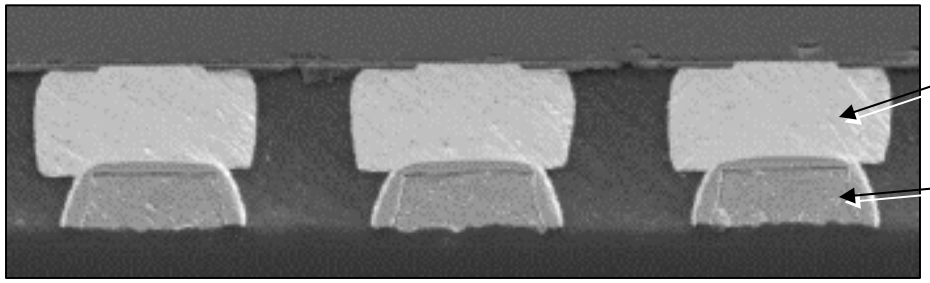


Stencil printed, conductive epoxy bump (~150µm dia.)

Example source: KSW Microtec

Gold-to-Gold Interface (GGI)

- An alternative bumping process furnishes a gold contact on each bond site utilizing the same basic system developed for wire-bond assembly.
- The GGI attachment technique utilizes heat, pressure and ultrasonic or thermosonic energy, to form a welded interconnection from the gold bumped die to the substrates gold-plated land pattern.

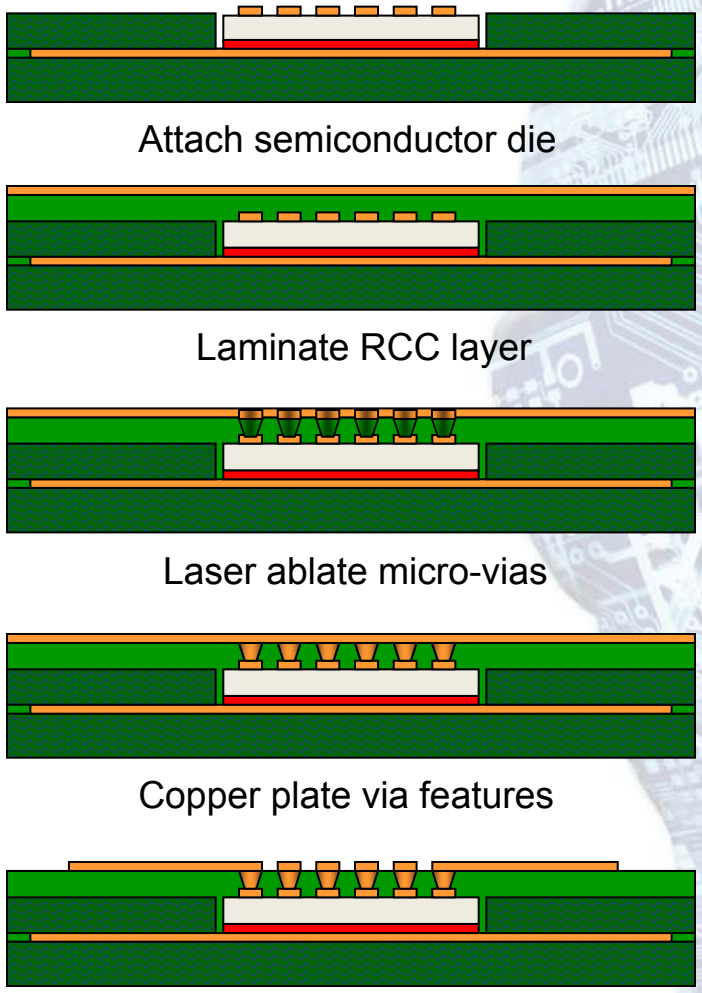


The GGI process eliminates the need for flux and cleaning prior to applying the prepreg laminate or RCC material.

Example source: Nippon Avionics

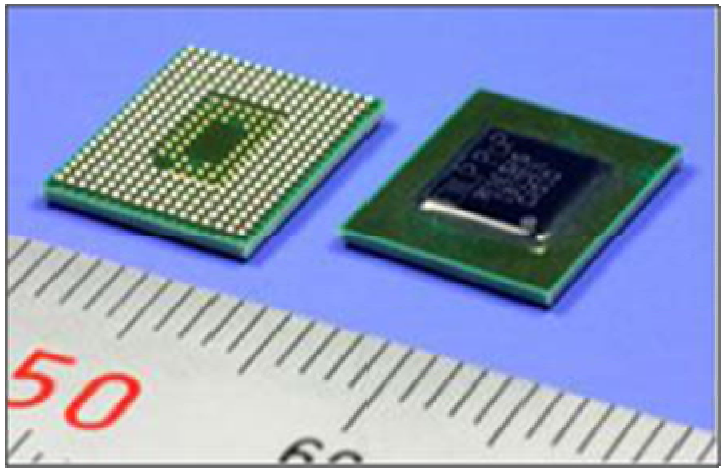
Face-up Micro-via Interface

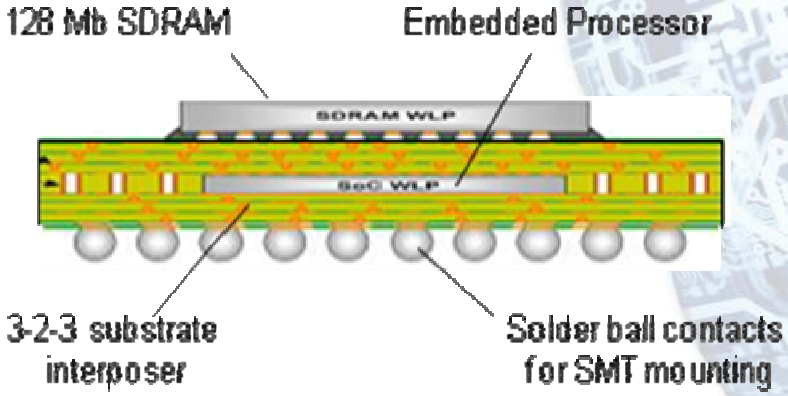
- In preparation for direct micro-via to die bond pad interface the bond sites on the die element will be furnished with a compatible Cu alloy contact surface.
- When micro-via plate and etch processes are complete the substrate is made ready for additional build-up layering.



4. 3D Semiconductor Package Development

- Embedding one or more silicon based semiconductor elements within the inner layers of the structure will enable greater utilization of the circuit board or interposers outer surfaces.

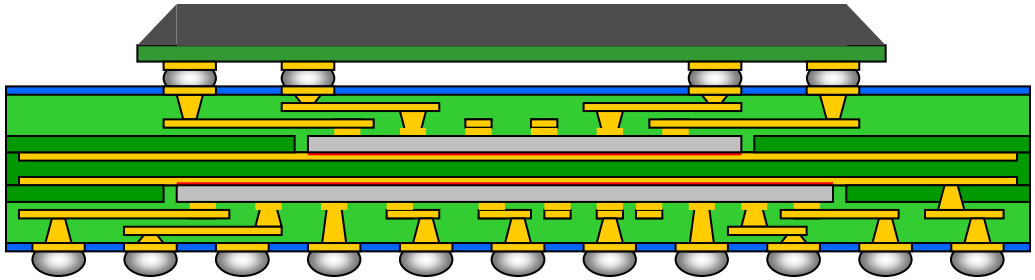




Example source: Casio Micronics

Performance

- Designers are well aware that the shorter the circuit interface between the individual die elements the greater the signal transmission speed.
- By embedding the semiconductors on an inner layer directly in line with a related semiconductor package mounted on the outer surface, the conductor interface between die elements will be minimized.



The shorter interface between die elements will significantly reduce inductance and increase signal speed.

Summary and Conclusion

- Several PCB suppliers with experience in build-up circuits are already heavily involved in embedding both passive and active components.
- Although 'formed' resistor and capacitor processes are very mature processes, a number of users are not satisfied with their physical stability and wide tolerance range.
- With the availability of smaller passive device outlines from a wide supply base, many companies recognize the practical advantage for embedding discrete passive elements.
  - Less restrictive value selection
  - Wide resistor and capacitor value range
  - Tolerance stability

Economic Concerns

Positive factors-

Increase	Decrease
Number of printed boards fabricated on a panel due to decreased board size.	Printed board area can be smaller due to a reduction in the number of surface mounted passive components.
Surface mounted component density resulting in shorter coupling between devices.	Wiring density simplified due to the integration of resistors and bypass capacitors within the substrate.
Potential for higher second level assembly process yields	Reduction in overall assembly costs, solder process defects and rework

Economic Concerns cont.

Negative factors-

Increase	Decrease
Printed board cost per unit area due to process complexity.	Printed board fabrication throughput impacted by process variables.
Wiring density requirements due to the reduced printed board area.	Overall printed board fabrication yield due to process related defects.

- Embedding the semiconductor is where many companies may find a significant roadblock-
  - Procurement of semiconductors in a wafer format
  - Outsourcing metallization and thinning
  - Testing embedded mixed function assemblies
- The PCB fabricator cannot perform a full functional electrical test of the end product at the substrate level-
  - So how to test and what to test and what features are needed to enable test?
- Ideally, the originating companies will bring together the two primary suppliers; the circuit board fabrication specialist and the assembly service provider.
  - These partnerships must be willing to adjust their portion of the generated revenue against the overall process yield. That includes the sharing of losses from fabrication process defects and damaged components.

Thank you