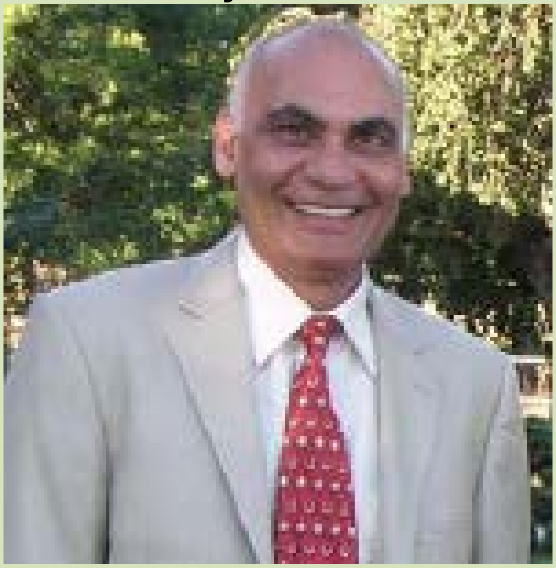
IPC Midwest 2011

Key Issues in Bottom Termination Component (BTC) Design and Assembly for Improved Reliability and Yield

Ray Prasad

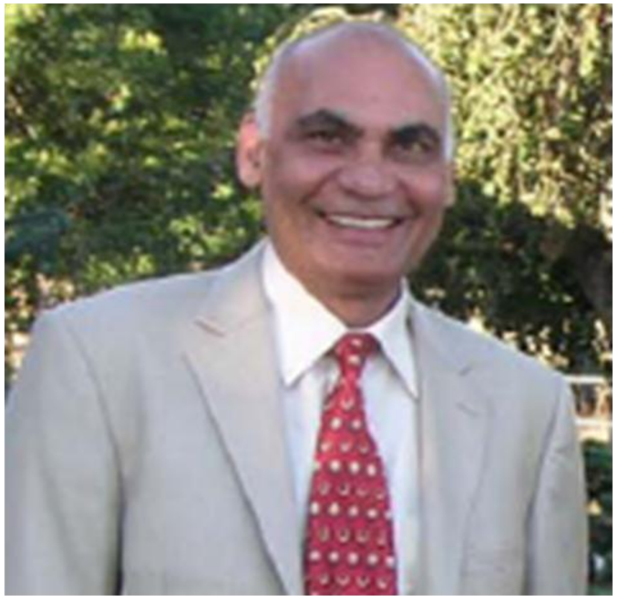


Ray Prasad Consultancy Group

Executive Summary

With the release of IPC 7093, "Design and Assembly Process Implementation for Bottom Termination SMT Components," earlier this year, the term BTC is the newest acronym to enter the world of SMT. BTCs are very much like the BGAs but without the balls. Excellent electrical and thermal performance combined with lowest package cost has made this package very popular especially in mobile products. However, the absence of balls changes practically all aspects of design and manufacturing SMT assemblies using BTCs. The connection between the package and PCB is essentially like a postage stamp which poses challenges in both design and assembly of BTCs to achieve acceptable reliability. And achieving good yield is also a challenge since both the package and PCB must be perfectly flat. Any warpage in package and PCB has to be compensated by solder paste but too much paste creates voids and package floating and too little paste causes opens and insufficient solder resulting in premature failure. Based on the design and assembly guidelines in IPC 7093 co-chaired by the author, this presentation will focus on key issues in design and assembly to reduce defects and improve reliability.

Key Issues in BTC Design & Assembly for Improved Reliability and Yield



By

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Brief Professional Profile of Ray P. Prasad

Ray Prasad is the founder of Ray Prasad Consultancy Group. Before and starting his consulting practice in 1994, Mr. Prasad held key technology positions at Boeing and Intel for 15 years. He was the SMT Program Manager at Intel responsible for developing and implementing SMT for the system products. He also developed and taught in-house and design and manufacturing courses to Intel engineers. For establishing the SMT infrastructure at Intel he was recognized by Intel CEO Andy Grove. He also managed the Intel PentiumPro™ package program for Intel and introducing SMT into Boeing airplanes when he served as a lead engineer at that company.

Author of the text book *Surface Mount Technology: Principles and Practice* *published by Walter Kluwer Academic Publishers* and over 100 papers, Mr. Prasad holds two patents in BGA and is a popular workshop leader for in depth SMT, BTC, BGA/CSP and Lead free professional courses at national and international conferences and major OEM and EMS companies.

A long time member of IPC, he is currently the chairman of BGA committee IPC-7095 "Design and Assembly Process Implementation for BGA". He is also the Co-Chairman of IPC-7093 "Design and Assembly Process Implementation for Bottom Terminations surface mount Components (BTCs) such as QFN, DFN and MLF. He is the past chairman of the Surface Mount Land Pattern (IPC-SM-782, now IPC 7351) and Package Cracking (J-STD-020) committees.

Mr. Prasad is the recipient of SMTA's Member of Distinction Award and IPC President's award for his contribution to the advancement of electronics industry and recipient of Intel's highest award – Intel Achievement Award. He is a columnist for the SMT magazine and also serves on its advisory board.

Mr. Prasad received his BS in Metallurgical Engineering from the Regional Institute of Technology, Jamshedpur in India and MS in Materials Science and Engineering and MBA from the University of California at Berkeley, USA. He is a registered Professional Metallurgical Engineer.

Outline

- Types of BTCs their Manufacturing Processes
- Pros and Cons of BTCs
- Land Pattern and Stencil Design Considerations
- BTC Solder Joint Quality and Reliability Considerations
- Summary

BTC: Bottom Termination Components

- The term BTC represents industry descriptive package names such as
  - QFN (Quad Flat Pack No-Lead package)
  - LGA (Land Grid Array)
  - SON (Small Outline No-Lead – leads on two sides)
  - PQFN (Plastic Quad Flat No-Lead)
  - MLFP (Micro Lead Frame Plastic)
  - MLP (Micro Lead-Frame Package) etc.

BTC Definition

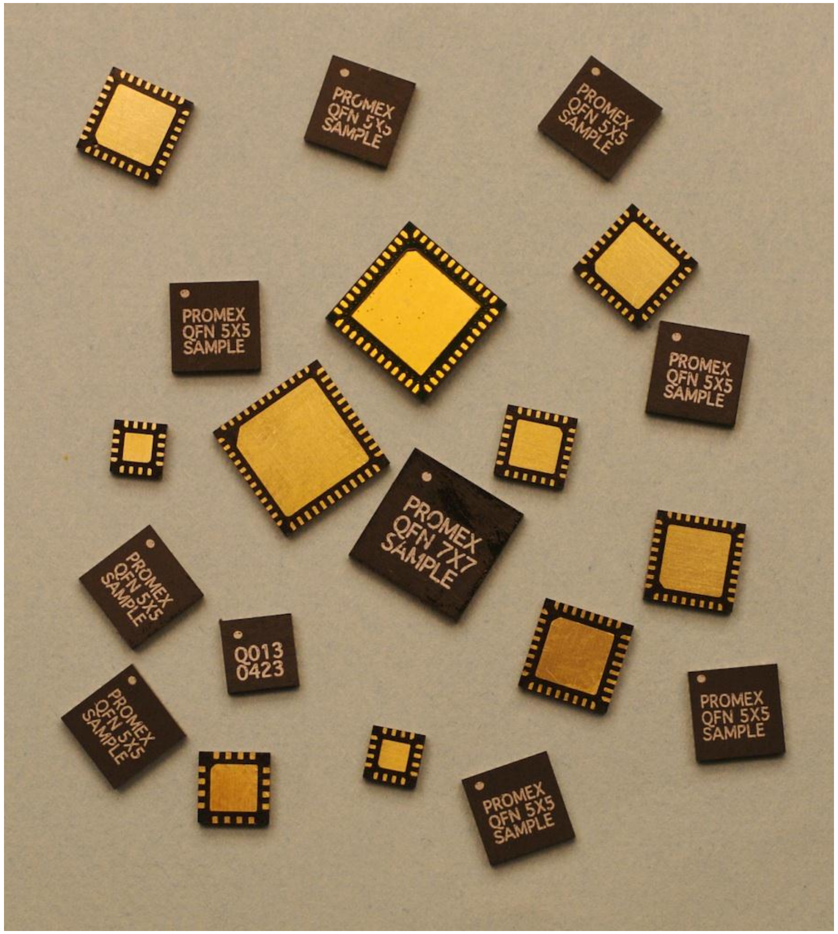
- BTCs in some ways are similar to BGAs and even called by some as poor man's BGA which also have hidden terminations, but they are also very different. They do not have spheres but rather metallized terminations or pads underneath the package.
- This minor difference in I/O shape makes all the difference in design, assembly and rework between BTCs and BGAs
- BTC is a relatively new packaging technology. So expect changes in design and assembly of BTCs as we all learn about this technology with passage of time

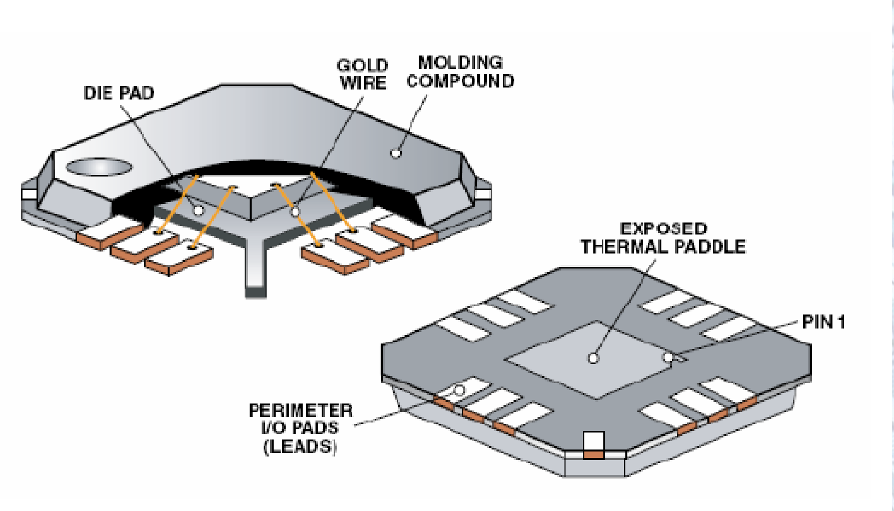
BTC Lead Configuration Vs Other Package Types- Pros & Cons

SHAPE OF TERMINAL / ITEM	GULL-WING	J-LEAD	BTC	B.G.A.
Compatibility with High Pin Package Trend	◆	●	●	◉
Package Thickness	◆	●	◉	◉
Lead Rigidity	△	◆	◉	◉
Repair/Rework	●	◆	●	△
Electrical & Thermal Perf	△	●	◉	◆
Solder Joint Inspection	●	◆	△	△
Ease of Cleaning	△	◉	△	◉
Package Cost	◆	●	◉	△

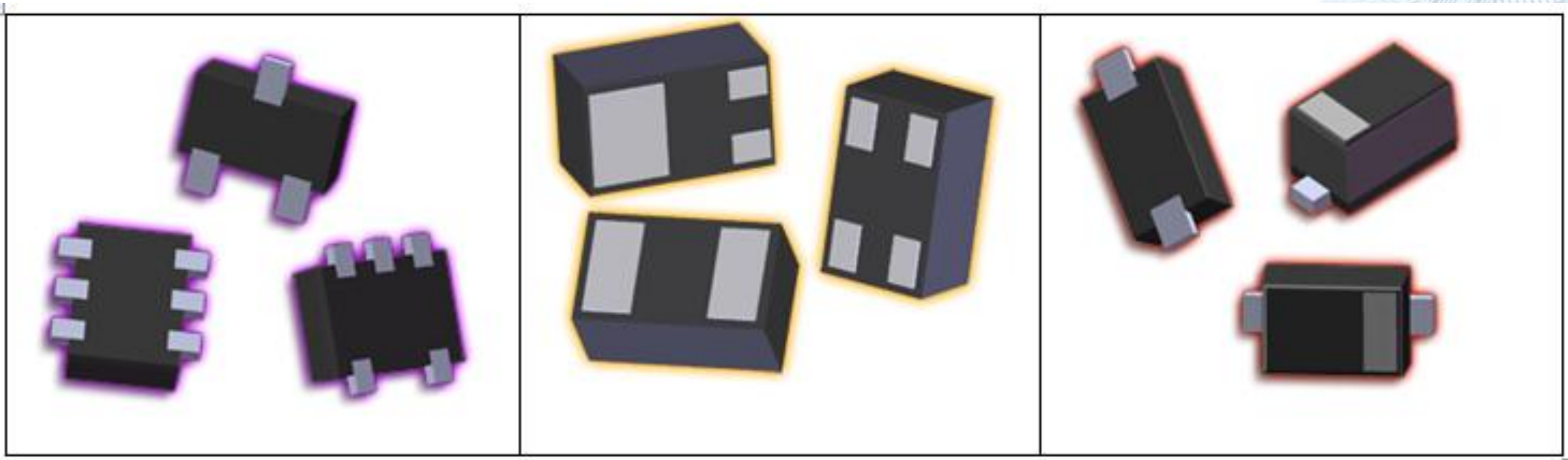
◉ = EXCELLENT ◆ = VERY GOOD ● = GOOD △ = POOR

Examples of BTC: Bottom Termination Components Family: IPC 7093





Examples of Discrete BTCs



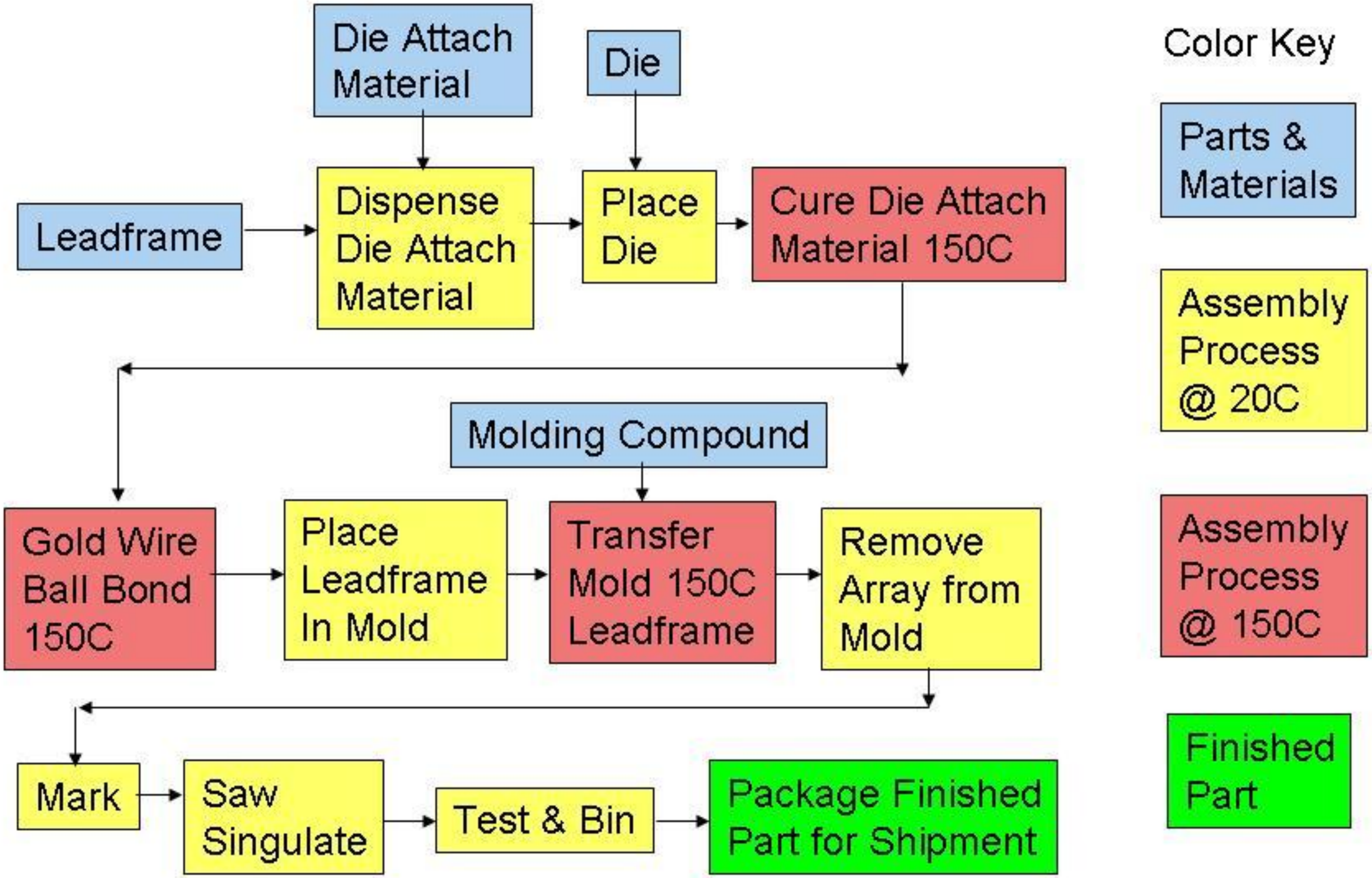
(a) Saw Singulated, Full Lead

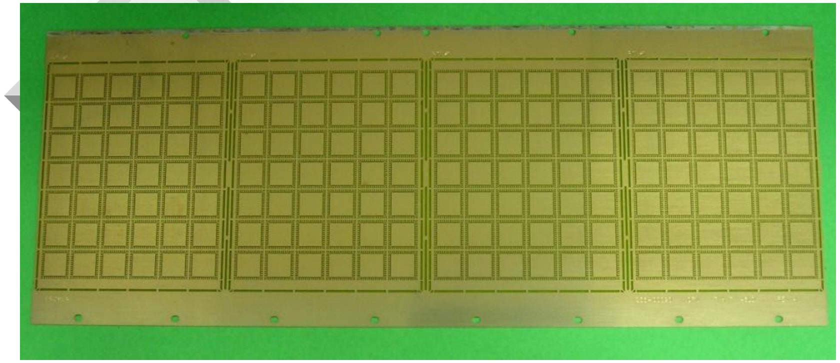
(b) Saw Singulated, Lead Pullback

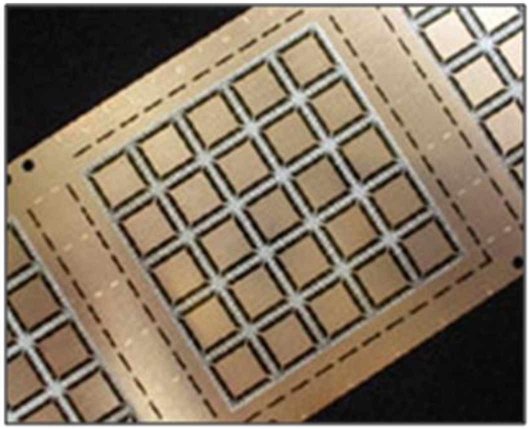
Pullback

No-Pullback

QFN Fabrication with Saw Singulation

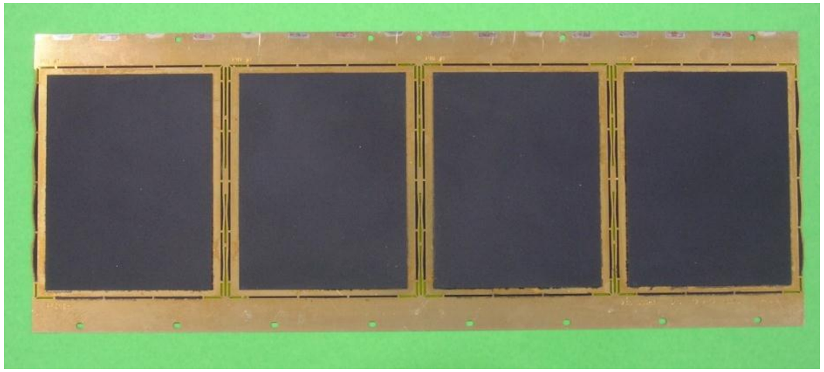




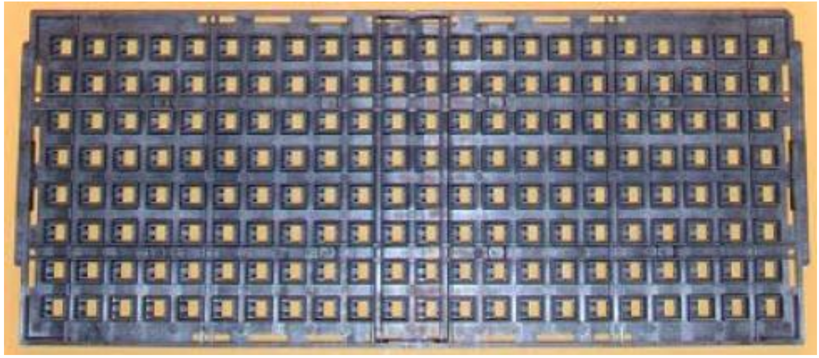


Example source: QPL Group

QFN Lead frame
Before Molding



QFN Lead frame
After Molding



QFN after Sawing
In JEDEC Tray

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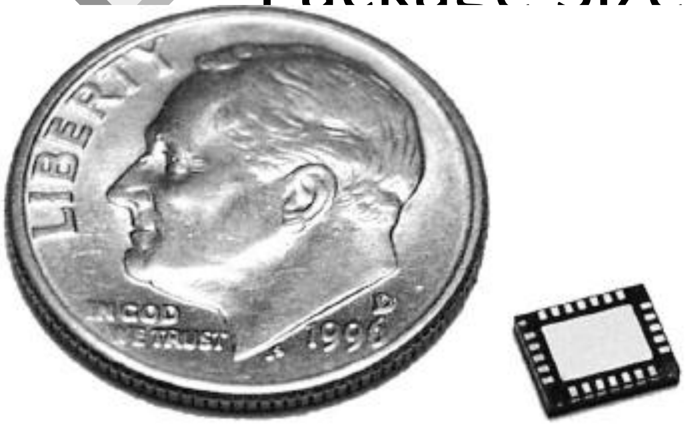
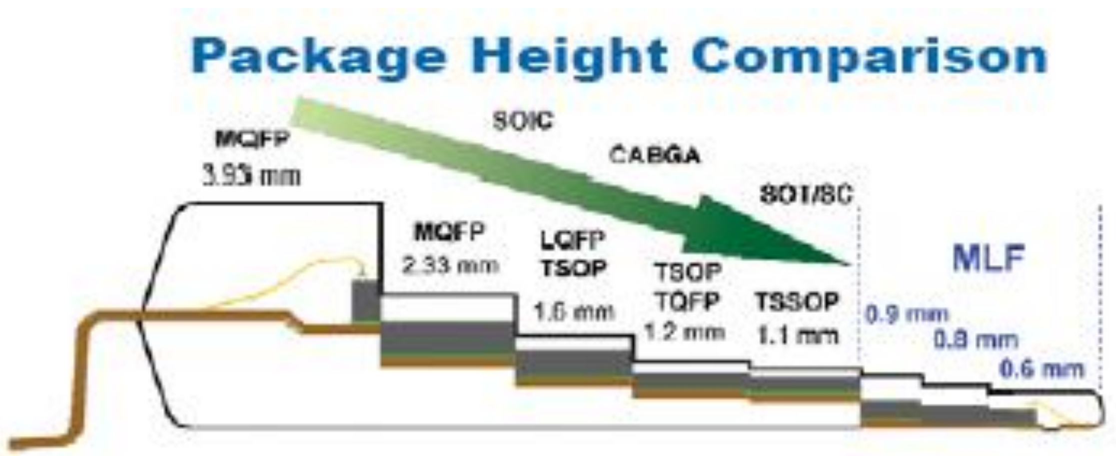
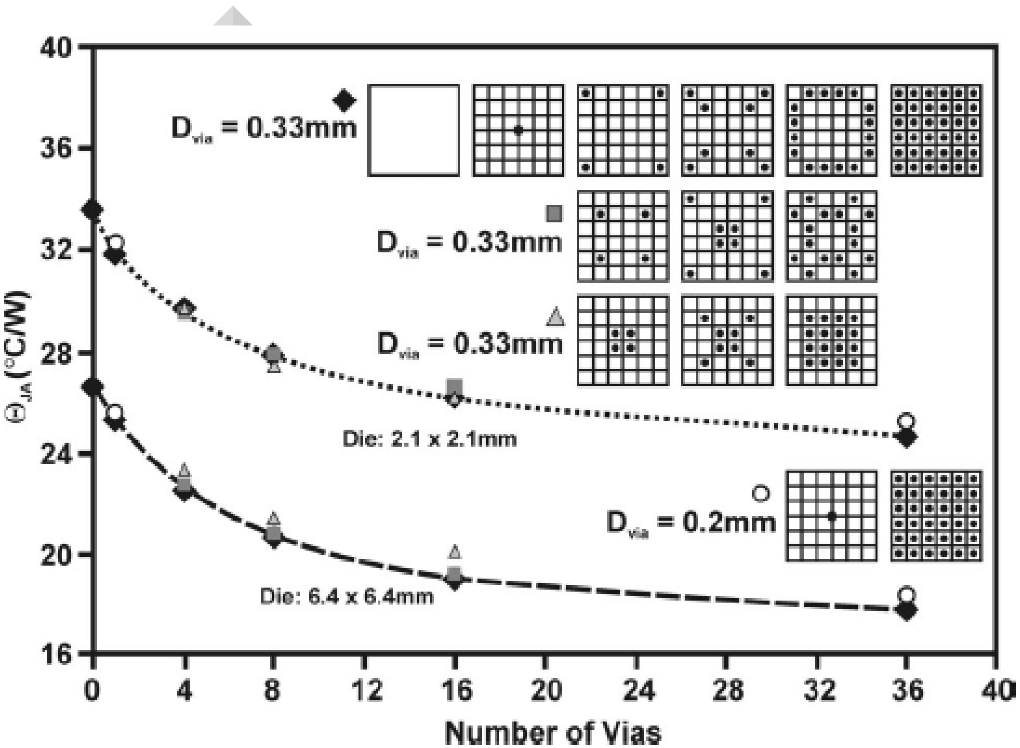
Benefits of BTC Packages

- The basic driver for BTCs is the cost. It is a package with the lowest per pin cost, as low as half a cent per pin.
- To put this in a proper perspective, if a package costs less than one cent per pin, it is considered a very low cost package.
- So BTCs become an ideal package especially in high volume applications such as cell phones or other mobile products
- In addition to cost advantage they offer superior electrical performance and improved thermal management, critical in today's smart mobile products.

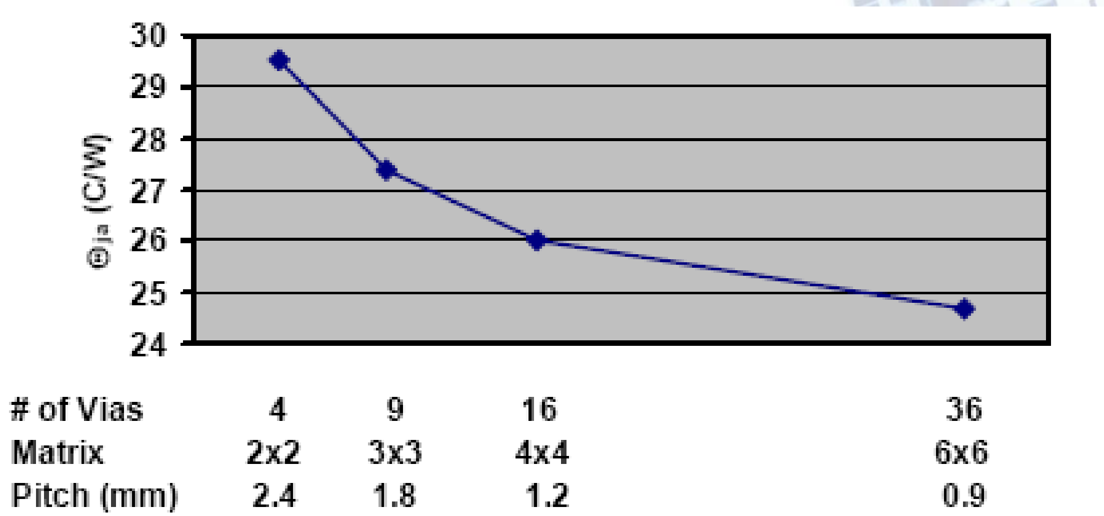
Package Size & Height Comparison



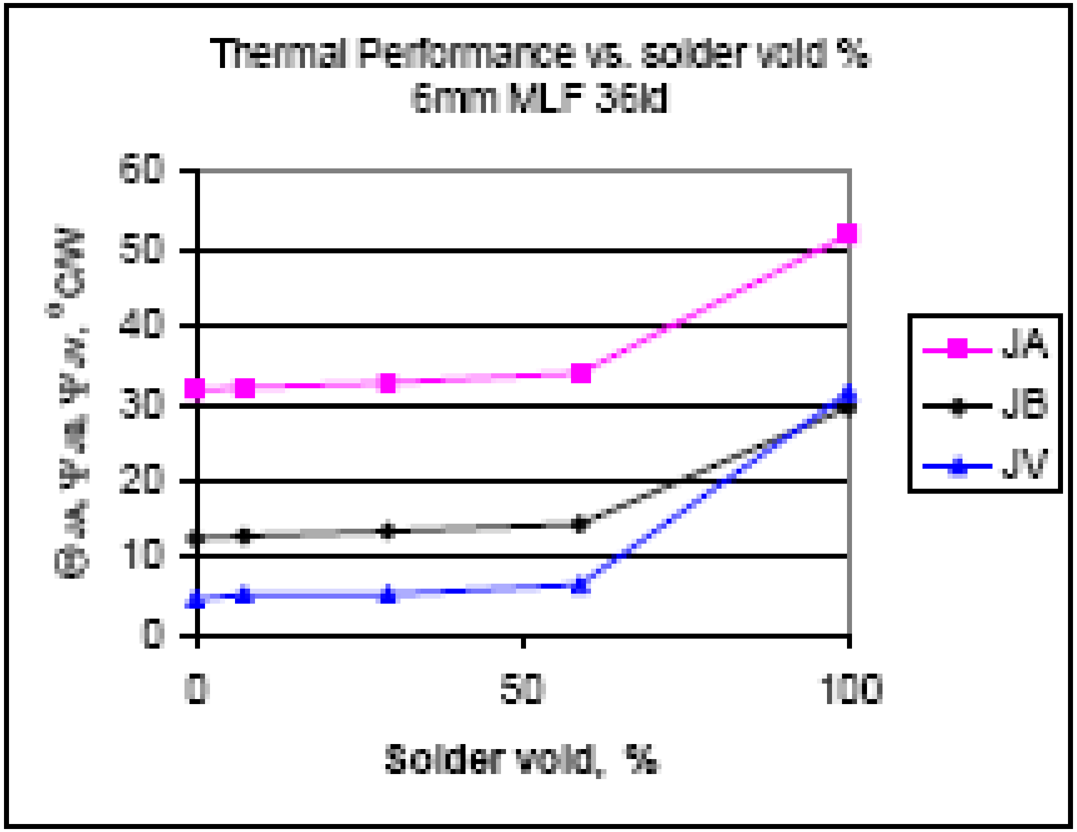




Impact of Thermal Vias on Package Thermal Performance



Impact of Voids on Thermal Performance of QFNs



Concerns in BTC Packages

- Excessive or unevenly deposited solder paste volume may cause the package to float, resulting in poor land pattern alignment, random solder bridging, voiding and opens.
- Too little solder volume may compromise product reliability. Even minimal warping in the package or PWB can result in solder joint opens.
- Because the terminal features may not protrude beyond the package body, visual inspection and uncompromised verification of the solder interface will be difficult
- The low package cost may not immediately translate into overall low assembly cost since this package presents many challenges in assembly, inspection, and rework.

Concerns in BTC Packages Contd.

- Due to reliability concerns, QFN is “next generation” product only in consumer applications. Limited use in long life high reliability applications
- Prone to floating and excessive voids with too thick paste
- Prone to opens/insufficient if paste is too thin
- High potential for both bridges and opens. So need perfection in package, PCB flatness, printing and reflow
- Toe fillet may not be possible even with extended pad (for example pull back leads) because of exposed copper

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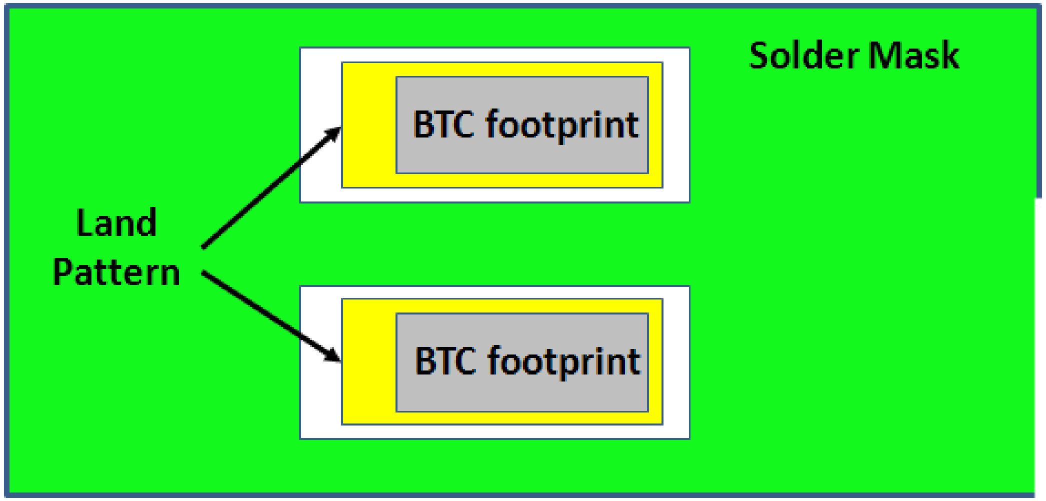
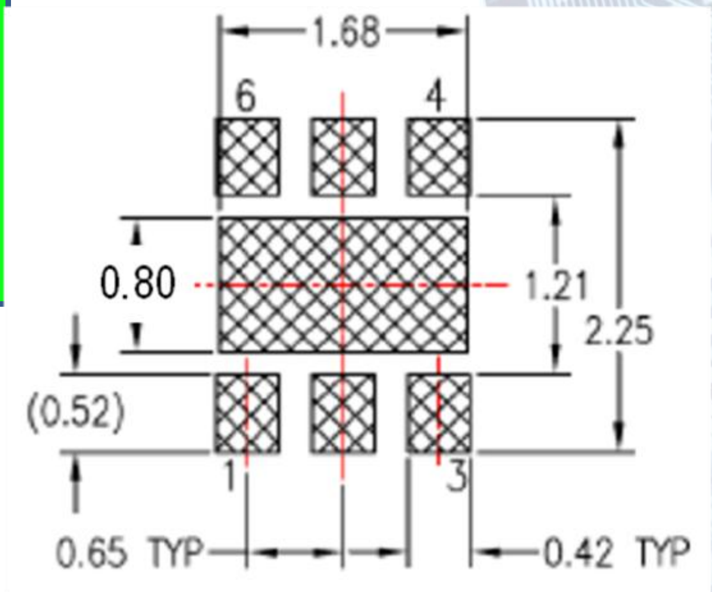
BTC Land Pattern Design

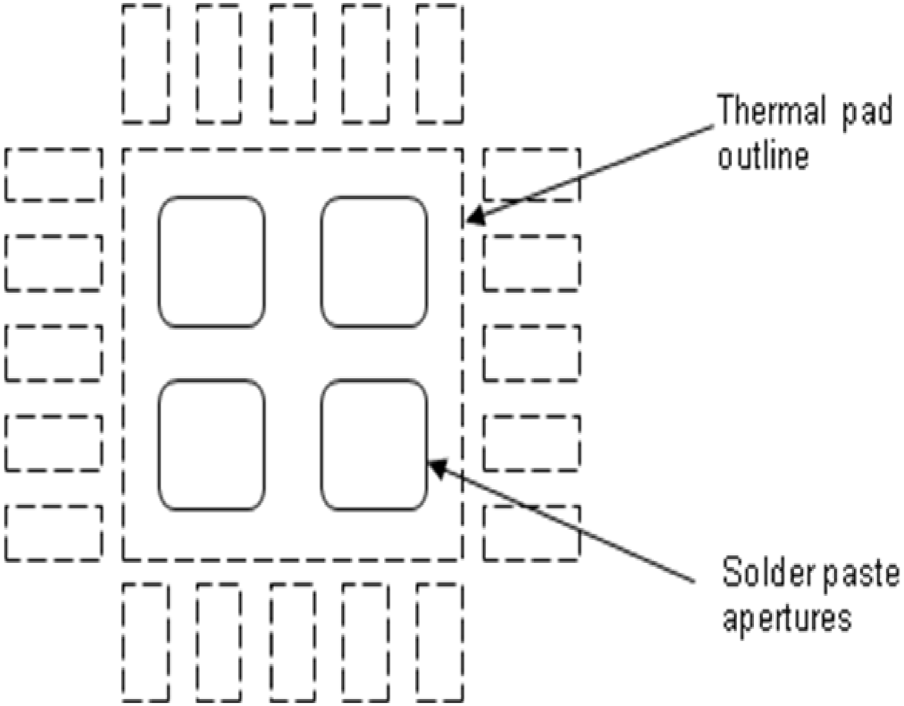


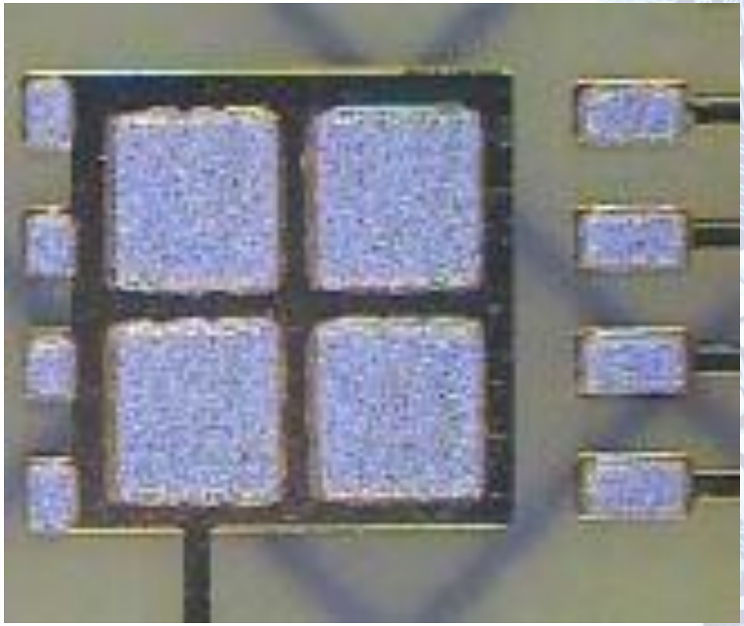


Three Key Guidelines

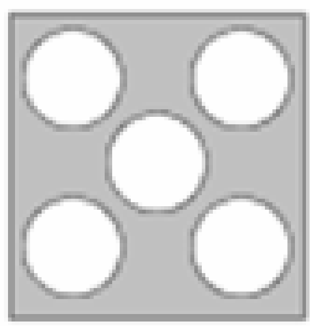
1. Pads are slightly larger than the terminal
2. Pad is extended for toe fillet
3. Allow sufficient space between thermal pad and perimeter pads to prevent bridging

Stencil Aperture Design Guideline for QFN Thermal/Ground Plane

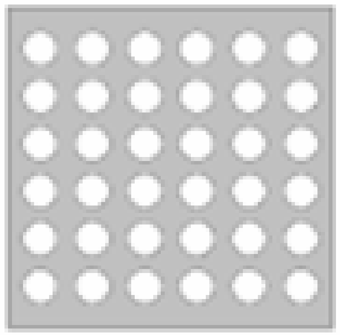




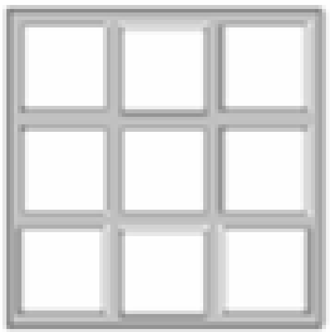
Other Ideas for QFN Stencil Design of Thermal/Ground Plane



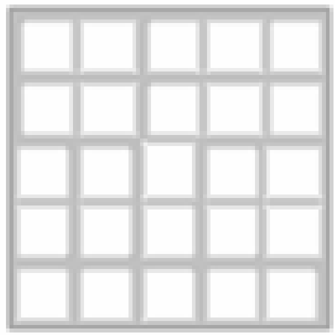
1.5 mm dia. aperture
@1.6 mm pitch
37% coverage



1.0 mm dia. aperture
@1.2 mm pitch
50% coverage

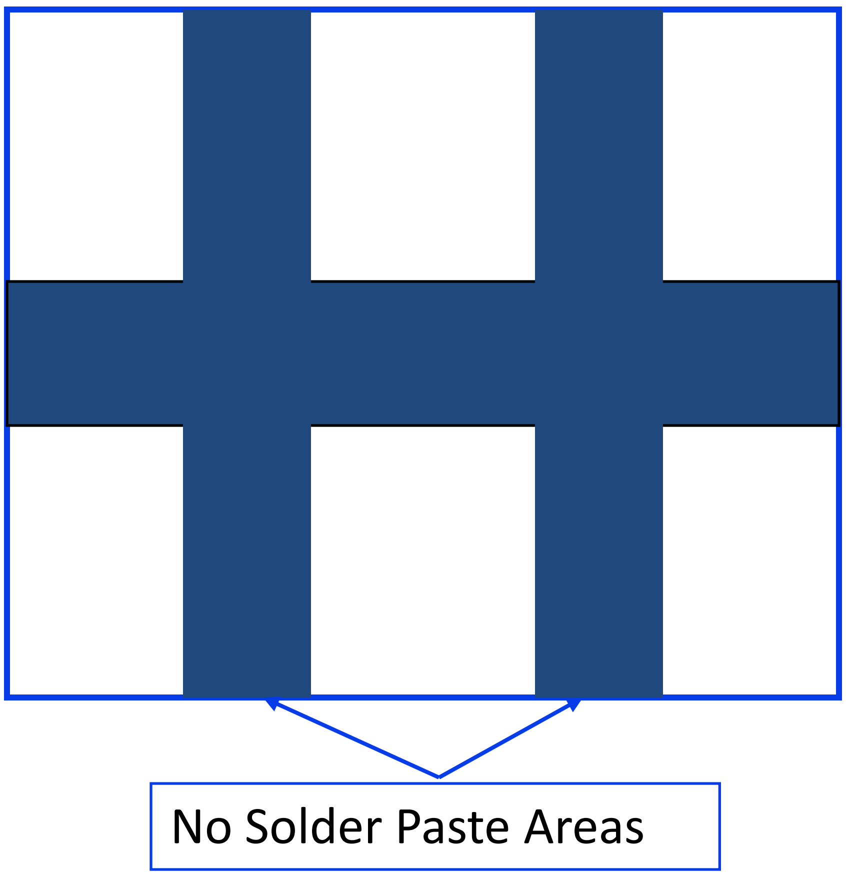


1.3 x 1.3 mm aperture
@1.65 mm pitch
68% coverage



1.3 x 1.3 mm aperture
@1.5 mm pitch
81% coverage

Other Ideas for QFN Stencil Design of Thermal/Ground Plane, Contd..



- Use smaller multiple apertures instead of one large aperture
- Only 60 to 70% Paste Coverage on Center Pads
  - Reduce voids
  - Reduce out-gassing (spatter, solder balling)
  - Reduce open joints (large paste will form a dome and may raise the peripheral leads resulting in opens)

Paste Printing Around Vias in BTC Thermal Pads

- Can lose solder through vias in thermal pad
- Solder bump on the opposite side can create printing and placements problems on the secondary side
- Capping and tenting is used to prevent this problem but adds to cost and chemical entrapment in vias
- Best way to deal with leakage of solder is to avoid printing around vias in thermal pad (next slide)