IPC Midwest 2011

Physics-of-Failure Approach to Integrated Circuit Reliability

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Executive Summary:

Modern electronics typically consist of microprocessors and other complex integrated circuits (ICs) such as FPGAs, ADCs, and memory. They are susceptible to electrical, mechanical and thermal modes of failure like other components on a printed circuit board, but due to their materials, complexity and roles within a circuit, accurately predicting a failure rate has become difficult, if not impossible. Development of these critical components has conformed to Moore's Law, where the number of transistors on a die doubles approximately every two years. This trend has been successfully followed over the last two decades through reduction in transistor sizes creating faster, smaller ICs with greatly reduced power dissipation. Although this is great news for developers of high performance equipment, including consumer products and analytical instrumentation, a crucial, yet underlying reliability risk has emerged. Semiconductor failure mechanisms which are far worse at these minute feature sizes (tens of nanometers) result in higher failure rates, shorter device lifetimes and unanticipated, early device wear out.

Physics-of-Failure (PoF) knowledge and an accurate mathematical approach which utilizes semiconductor formulae, industry accepted failure mechanism models, and device functionality can access reliability of those integrated circuits vital to system stability. Currently, four semiconductor failure mechanisms that exist in silicon-based ICs are analyzed: Electromigration, Time Dependent Dielectric Breakdown, Hot Carrier Injection and Negative Bias Temperature Instability. Mitigation of these inherent failure mechanisms, including those considered wear out, is only possible when reliability can be quantitatively calculated. Algorithms have been folded into a software application to not only calculate a failure rate, but also give confidence intervals and produce a lifetime curve, using both steady state and wear out failure rates, for the integrated circuit under analysis. Furthermore, the algorithms have been statistically verified through testing, employ data and formulae from semiconductor materials (to include technology node parameters), circuit fundamentals, transistor behavior, circuit design and fabrication processes. Initial development has yielded a user friendly software module with the ability to address silicon-based integrated circuits of the 130 and 90nm technology nodes.

DfR is now working to extend the capability of the tool into smaller technology nodes (65nm and 45nm) and other material sets such as silicon on insulator (SOI). Several commercial organizations have indicated a willingness to assist with the development and validation of 45nm technology through integrated circuit test components and acquisition of field failure data. Continued development would incorporate this information and would expand into functional groups relevant for analog and processor based integrated circuits.

The initial work was performed by DfR Solutions, and funded by Aero Engine Controls, Boeing, GE, NASA, DoD, and FAA in cooperation with the Aerospace Vehicle Systems Institute (AVSI).

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Reliability of Next Generation Microelectronics

- Ever growing concern in our industry that systems utilizing high performance microelectronics (≤130nm feature size) will not survive their anticipated lifetimes of 10 to 30 years
  - Failure will occur because of the short lifespans of individual transistors caused by intrinsic degradation (aging)
  - It is a fallacy to say that integrated circuits will not fail because they have no moving parts. The sole reason they work is by the movement of charge carriers (electrons and holes) within them.

"The notion that a transistor ages is a new concept for circuit designers," … aging has traditionally been the bailiwick of engineers who guarantee the transistor will operate for 10 years or so…But as transistors are scaled down further and operated with thinner voltage margins, it's becoming harder to make those guarantees… transistor aging is emerging as a circuit designer's problem.

IEEE Spectrum, June 2009

Reliability versus Performance

- Commercial Off the Shelf (COTS) is a term defining the acquisition of commercially sold electronics as an alternative to in-house or one-off government funded developments
  - Example: USAF supercomputer built from 1,760 Sony PlayStation 3 game consoles (10% of the cost of an equivalent system)[1,2]
  - Consumer purchasing drives the COTS marketplace – has followed the trending prediction of Moore's Law for over 40 years
  - Consumers want high performance; yet they are not concerned about the 3-5 year lifetime of these products because they will buy a new when a failure occurs
- Growing need to predict the lifetimes of these components for aerospace, defense and other high performance industries (ADHP)
  - Anticipated lifetimes of these systems is 10-30 years (beyond the designed lifetimes of consumer electronics)

1. http://www.stripes.com/military-life/turning-playstations-into-power-stations-1.99009
2. http://www.airmanonline.af.mil/news/story.asp?id=123228018

Trading Reliability for Performance

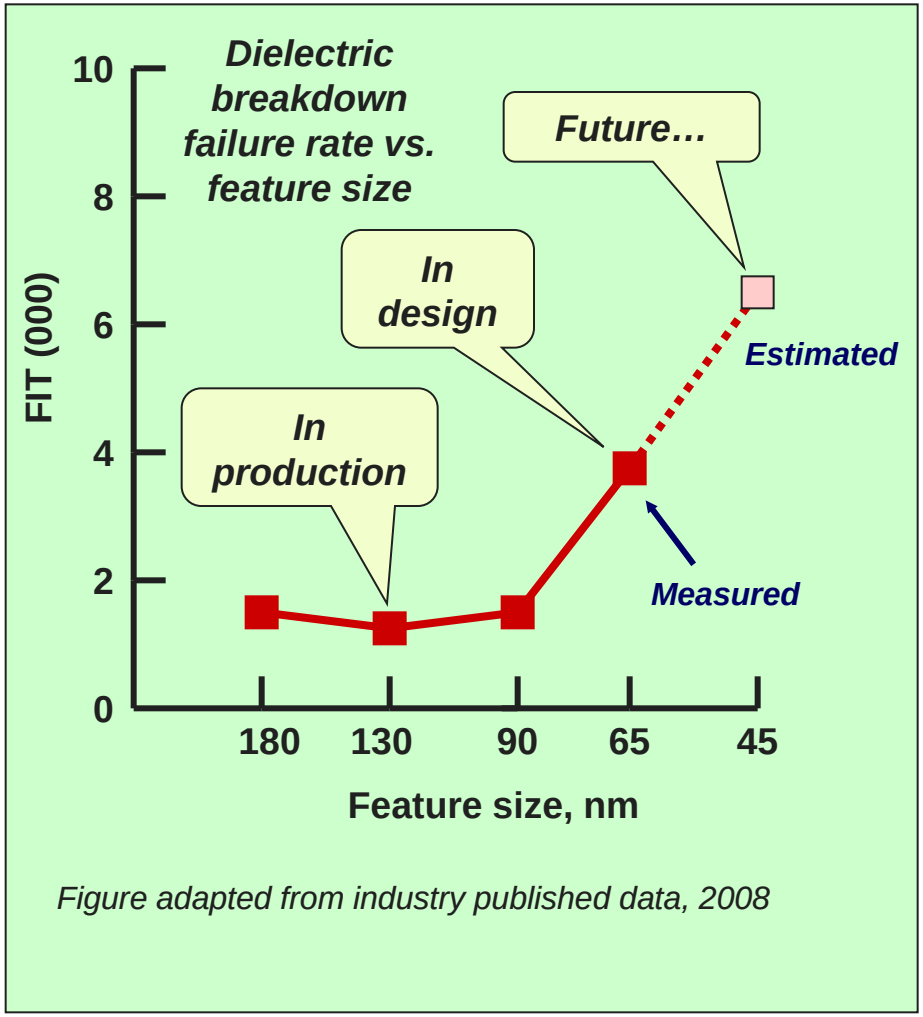


Figure adapted from industry published data, 2008

- Each new generation of technology introduces smaller, faster, more dense circuits
  - *Smaller and Faster circuits cause*
    - *Higher current densities*
    - *Lower voltage tolerances*
    - *Higher electric fields*
  - *Inherent Si-based failure mechanisms are manifested at these minute feature sizes*
- They are faster, but are they as reliable as the last generation?
  - The answer is no!

Failure rate data/projection from the aerospace industry (same application environment at each node)

IC Reliability (Example) - Microprocessors

- 90nm Microprocessors
  - 150-200 FIT over 5 years (0.11% AFR)

Part Number	Description	Node	Field Return Failure Rate (FIT)
MT16LSDF3264HG-10EE4	Micron 2GB SDRAM	130nm	689
M470L6524DU0-CB3	Samsung 512MB SDRAM	130nm	415
HYMD512M646BF8-J	Hynix 1GB DDRAM	130nm	821
MC68HC908SR12CFA	Freescale Microcontroller	90nm	221
RH80536GC0332MSL7EN	Intel 1.8GHz Pentium	90nm	144

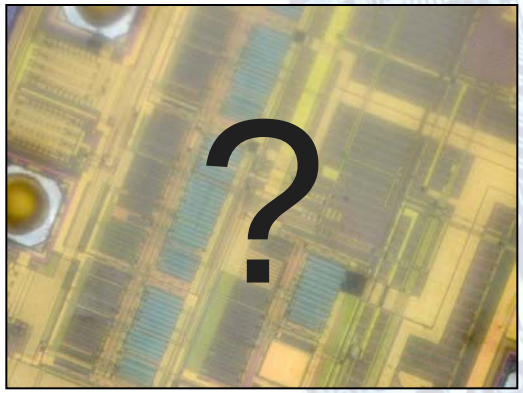
- 65nm Microprocessor
  - 422 FIT over 5 years (0.37% AFR)

	Operating Reliability Goals		
Time in Use →	0 – 1 Year (8760 hrs)	0 – 3 Years (26280 hrs)	0 – 5 Years (43800 hrs)
Cumulative Percent Fail	0.24%	0.85%	1.85%
Average Failure Rate	274 FIT	323 FIT	422 FIT

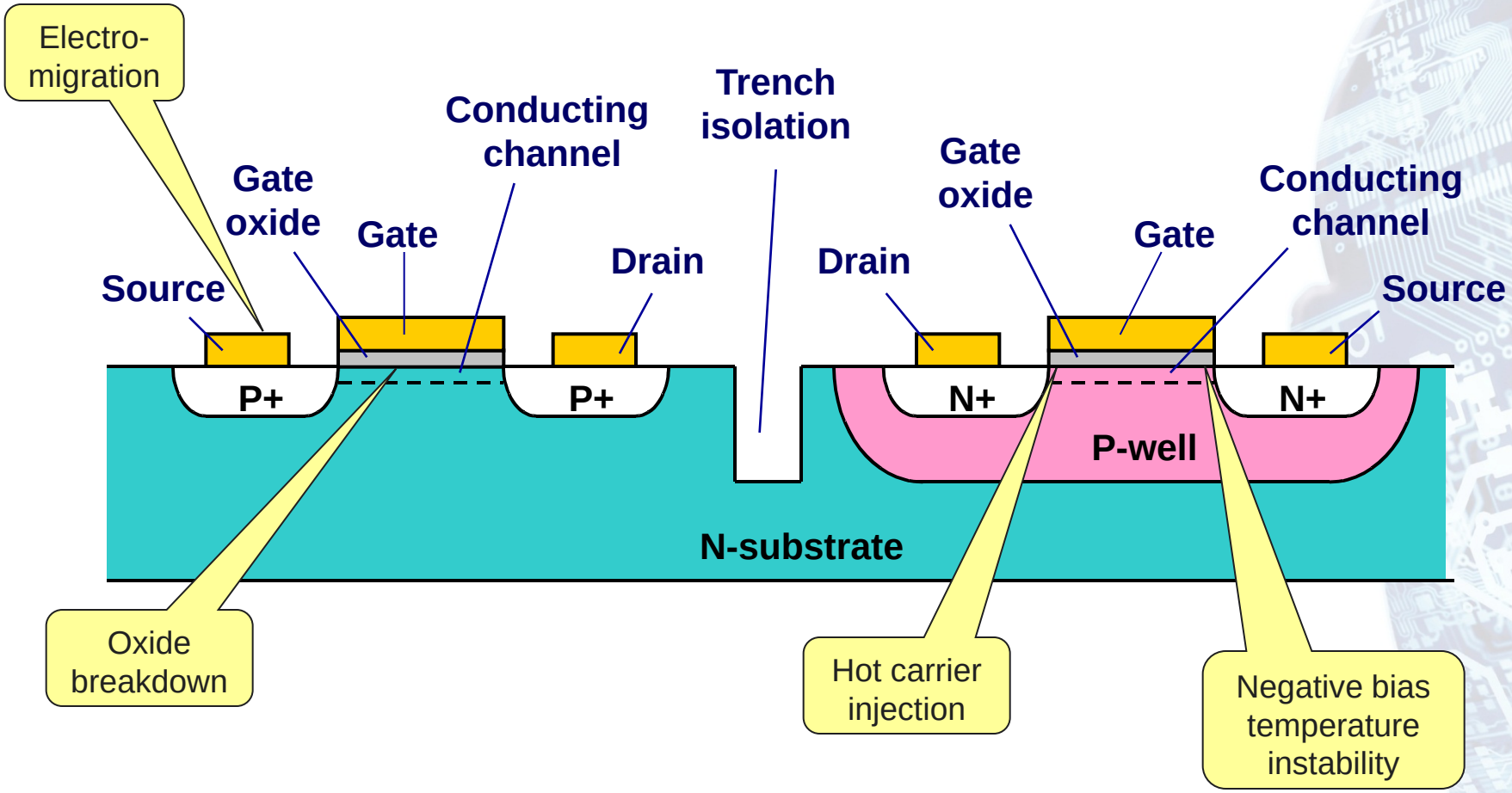
3X increase in AFR with each decrease in node size

Taking a Physics-of-Failure Approach

- Limited resources available on integrated circuit design and reliability
  - Can we perform a prediction with just in-house system design criteria (electrical\thermal data) and component documentation such as its datasheet?
- PoF knowledge of degradation mechanisms
  - Transistor stress states
  - Functional group susceptibility
  - Electrical and thermal conditions
- Integrated circuit materials and complexity
  - Technology node or feature size (i.e. 90nm)
    - Corresponding material set (e.g. Si, GaAs, SiGe, GaN and SOI)
  - Functional complexity
    - Identified as functional groups within a circuit
  - Operating conditions
    - Voltages, frequencies, currents, and temperature

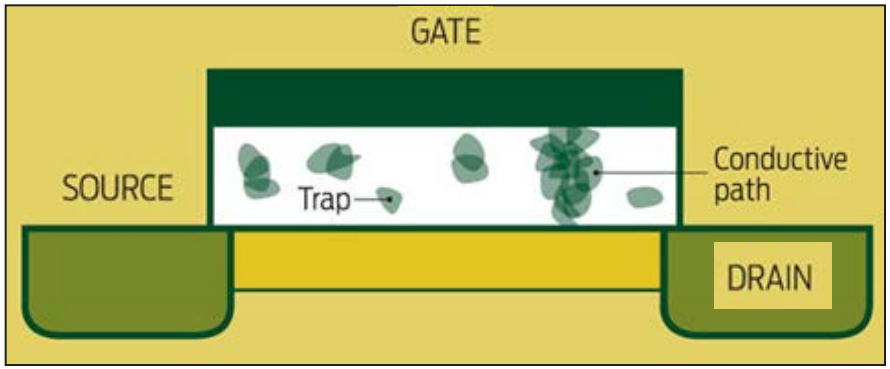


Issues Inherent to CMOS Design



Time Dependent Dielectric Breakdown (TDDB)

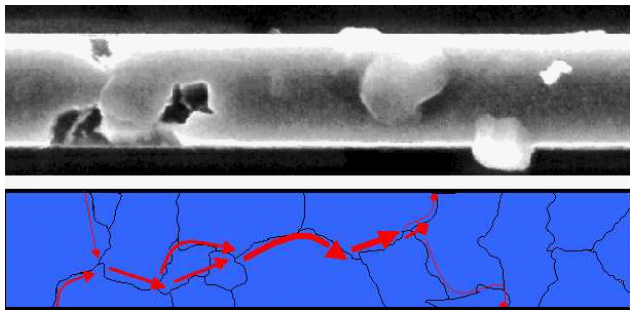
- What is it?
  - Voltage applied to the gate causes electrically active defects to become trapped in the gate oxide. When enough charges are trapped, an electrical short will exist from the gate metallization to the conducting channel
- Problems with feature Scaling:
  - The gate oxide thickness is reduced at each consecutive node
  - Power supply voltage is approximately the same as previous node
  - Increase in electric field on gate dielectric due to smaller thickness
  - What does this mean? *Not so time dependent after all*
    - Instead of cumulative degradation from multiple breakdown sites causing failure after an undefined interval, one breakdown site may cause immediate failure

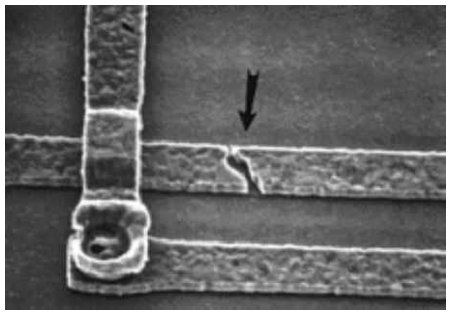


Artist depiction from May 2011 edition of IEEE Spectrum

Electromigration (EM)

- What is it?
  - The molecular displacement of atoms within a conductor caused by the flow of electrons
  - Dependent on conductor materials, their grain boundaries, and grain sizes
- Hasn't it been resolved? Partially.
  - Effects have already been mitigated a few times, but not resolved
    - Black's equation predicts time-to-failure
    - Latest conductor change to a better Al + Cu alloy (~0.13 micron node)

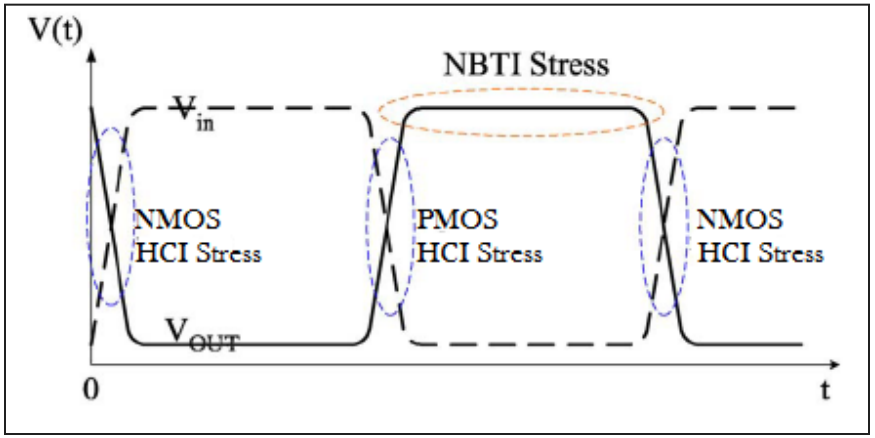




Damaging effects of EM on conductors

Negative Effects from the Electric Field

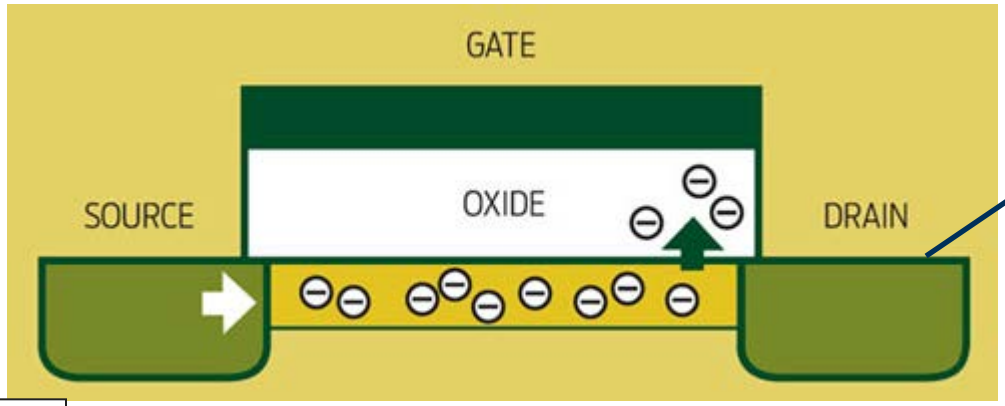
- Wearout *because of* transistor design
  - MOSFETs operate using electric fields ("field effect transistor")
  - Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) are driven by electric fields
  - New architectures experience these modes, i.e. FLASH memories
    - Floating gate transistor makes use of forced HCI and Fowler-Nordheim tunneling to store charge on the floating gate



Transistor stress states relating to HCI/NBTI damage (V_{in}/V_{out} curve)

Hot Carrier Injection (HCI)

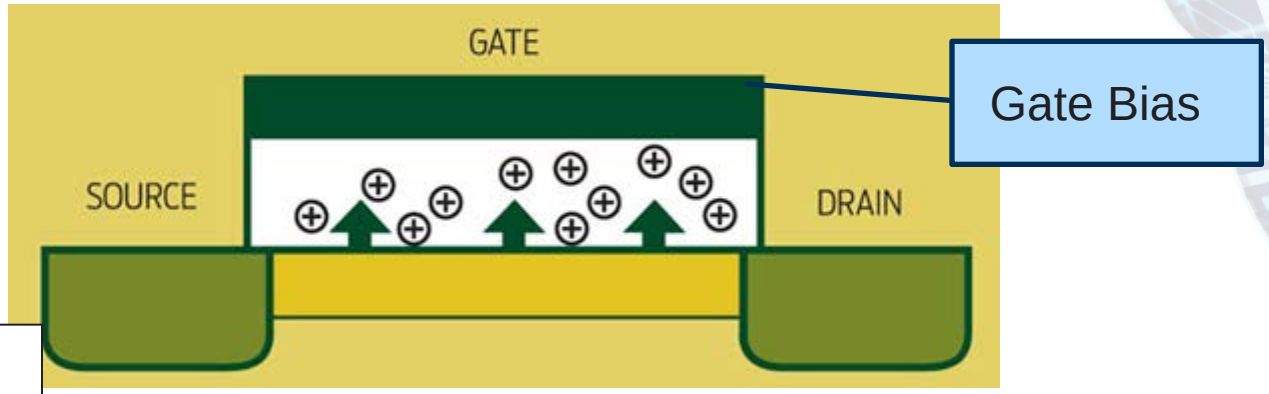
- What is it?
  - Electrical carriers become injected in the gate oxide either by a single carrier gaining sufficient kinetic energy, or Multiple carriers undergoing collisions that force them out of the directional path of electric field (the conducting channel)
- Characteristics
  - HCI has inverse Arrhenius relationship
    - Activation energy -0.2 to -0.1 eV
    - Lower temperatures (~35 to ~55°C) increase vulnerability



Artist depiction from May 2011 edition of IEEE Spectrum

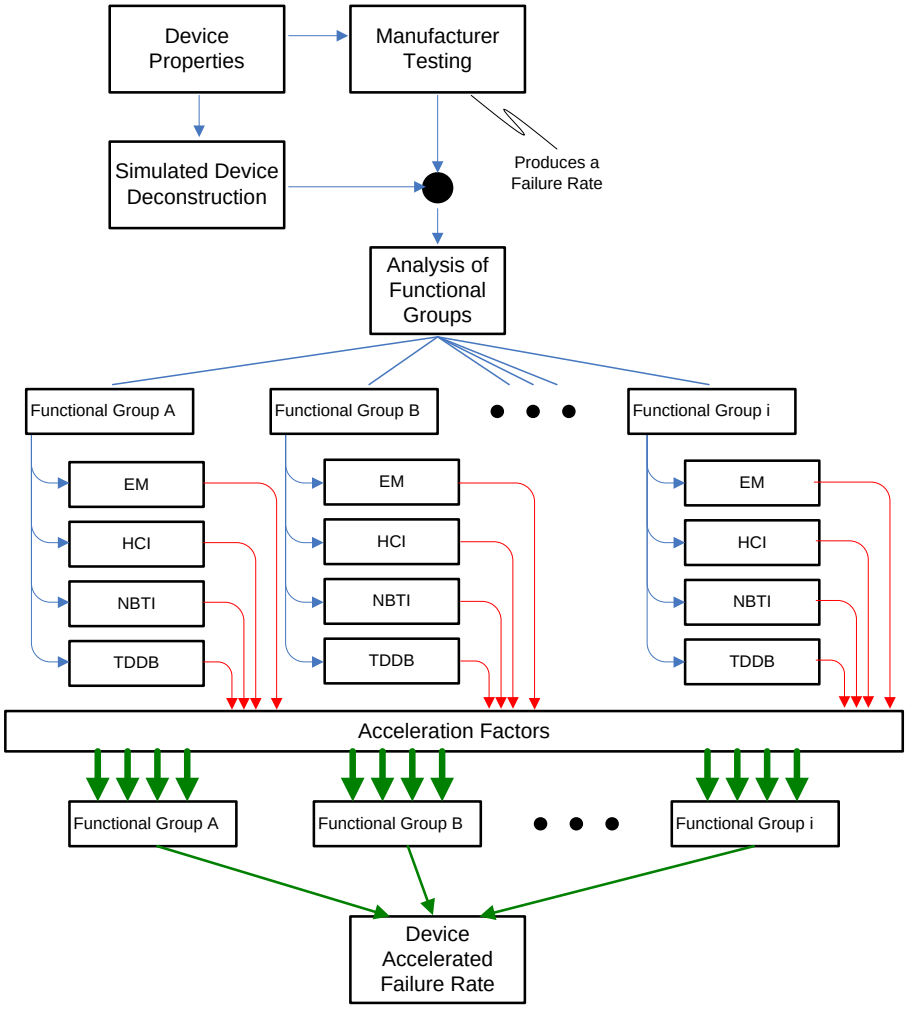
Negative Bias Temperature Instability (NBTI)

- What is it?
  - Charge carriers are attracted to the electric field on the gate even when the conducting channel is not active. Charges migrate into the gate oxide.
- Bias Temperature Instability
  - Combined bias & temperature stresses are required for activation
    - Fluctuations in temperature (overall device + self heating property)
    - High temperatures cause molecular instability
    - Requires much lower electric fields than HCI
  - Trap formation from electric fields are worse under negative bias
    - positive bias temperature instability is ~90%+ recoverable



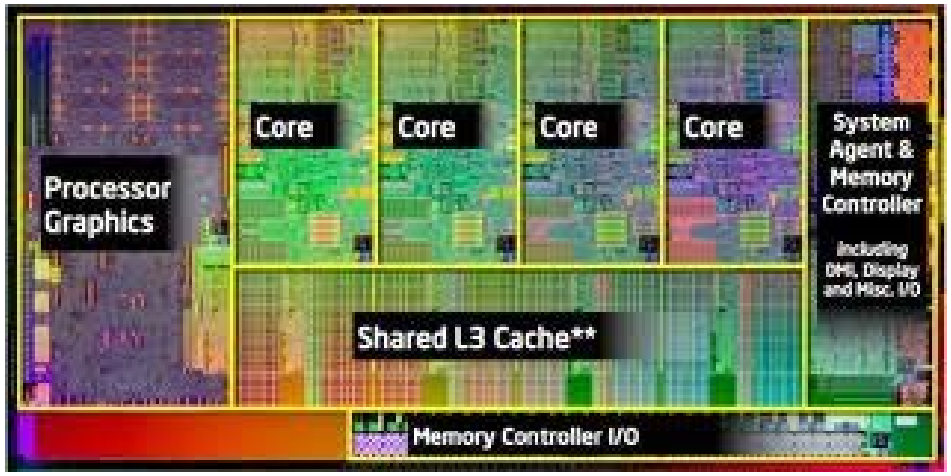
Artist depiction from May 2011 edition of IEEE Spectrum

Integrated Circuit – Lifetime Prediction



- Models the simultaneous degradation behaviors of multiple failure mechanisms on integrated circuit devices
- Devised from published research literature, technological publications, and accepted degradation models from:
  - NASA\JPL
  - University of Maryland
  - Semiconductor Reliability Community
- Easy to use software solution by multiple engineering disciplines

Functional Group Breakdown of an IC

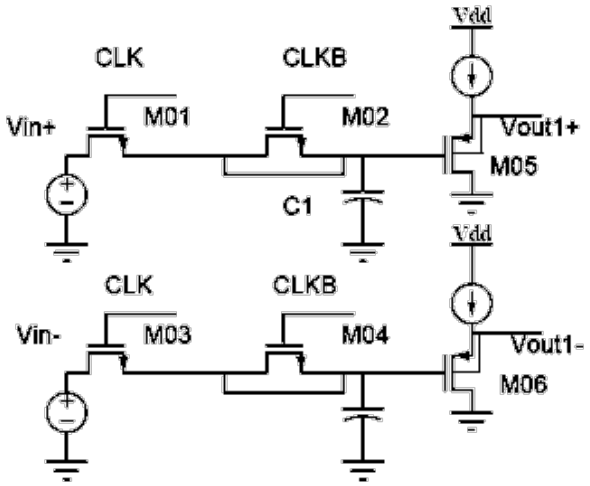


Graphic and overlay of Intel Core i5 Processor

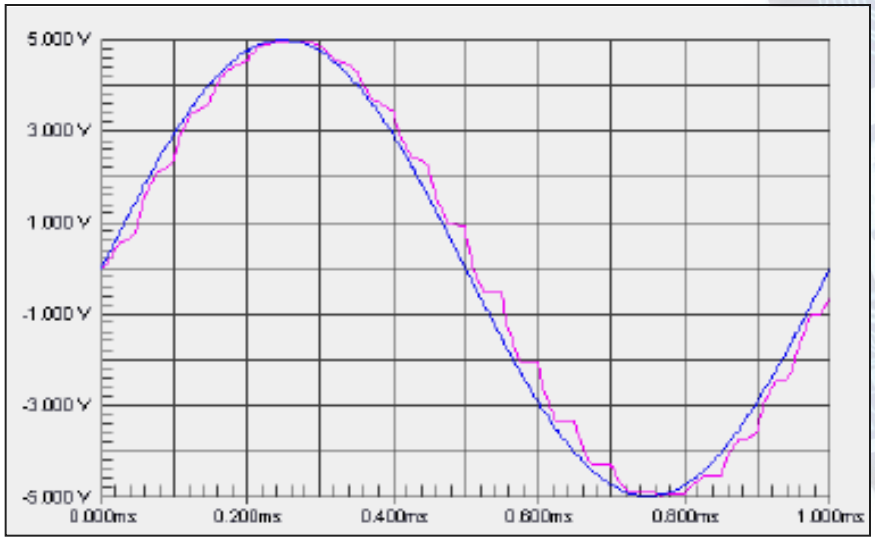
- The complexity of an integrated circuit can be described as a set or multiple sets of smaller sub-circuits called functional groups
  - Each functional group can be comprised of multiple cells which are the basic building blocks of the group, i.e. SRAM bit or processor core
- Each functional group experiences different electrical stresses which can quantified by analyzing transistor stress states
  - Degradation mechanisms come into play under specific transistor stress states such as drain bias for HCI or gate bias for BTI

Analyzing Transistor Stress States

- Establish relevancy of failure mechanisms, weighting factors, and inputs into Physics-of-Failure algorithms based on
  - Quantity and location of transistors within circuit
  - Probabilistic likelihood of applied operation conditions through background simulation of each functional group



Track (sample) & Hold



Transistor stress state analysis on Track and Hold functional group

Industry Testing Falls Short

- Limited degree of mechanism-appropriate testing
  - Only at transition to new technology nodes
  - Mechanism-specific coupons (not real devices)
  - Test data is hidden from end-users

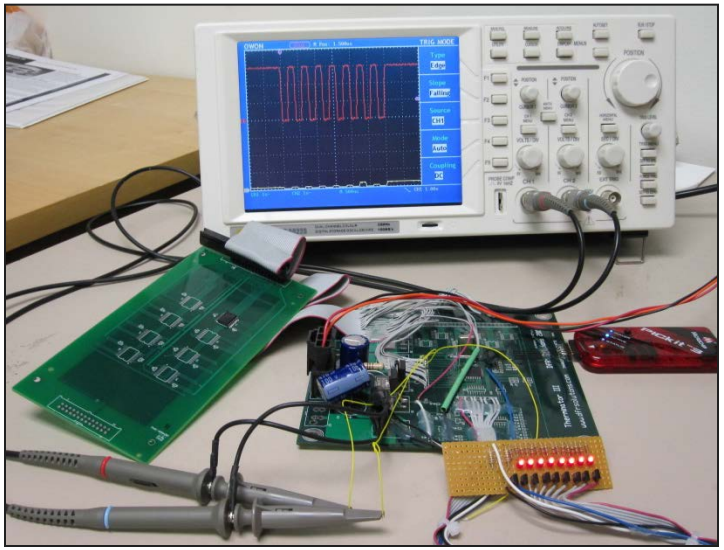
- Questionable JEDEC tests are promoted to OEMs
  - Limited duration (1000 hrs) hides wear out behavior
  - Use of simple activation energy, with incorrect assumption that all mechanisms are thermally activated, can result in overestimation of FIT by 100X or more

Modeling A Solution: From Test to Prediction

- The process flow uses technology node based degradation models which provide the ability to extrapolate from an appropriate accelerated test to anticipated field conditions
  - An appropriate test functionally stresses the integrated circuit just as it would be stressed under field conditions, i.e. FLASH memory bit retention
- Utilizing Physics-of-Failure degradation equations, acceleration factors can be applied at the transistor level for clock frequency, voltages, and temperatures.

$$AF_{EM} = \left(\frac{f_1}{f_2}\right)^n \left(\frac{V_{dd1}}{V_{dd2}}\right)^\gamma e^{\left(\frac{E_a}{k} * \frac{T_1 - T_2}{T_1 T_2}\right)}$$

$$AF_{NBTI} = \left(\frac{V_{gs1}}{V_{gs2}}\right)^\gamma e^{\left(\frac{E_a}{k} * \frac{T_1 - T_2}{T_1 T_2}\right)}$$



$$AF_{HCI} = e^{\left(\gamma * \frac{V_{ds1} - V_{ds2}}{V_{ds1} V_{ds2}}\right)} e^{\left(\frac{E_a}{k} * \frac{T_1 - T_2}{T_1 T_2}\right)}$$

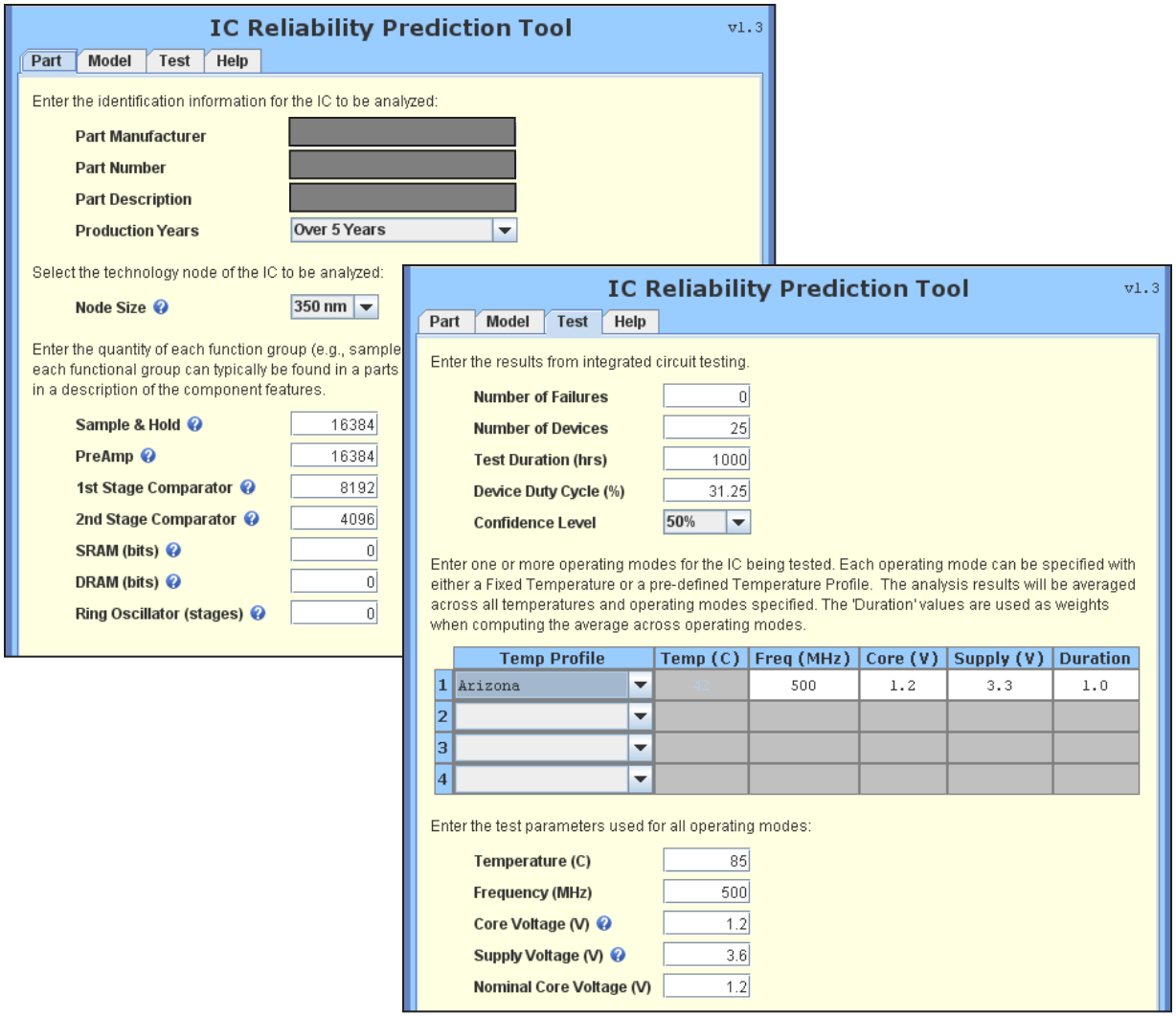
$$AF_{TDDB} = \frac{V_{gs1}^{(a+bT_1)}}{V_{gs2}^{(a+bT_2)}} e^{\left(c * \frac{T_1 - T_2}{T_1 T_2} + d * \frac{T_1^2 - T_2^2}{T_1^2 T_2^2}\right)}$$

Overall Mathematical Theory

- Model of a device's failure rate considering the tiers of system and device level inputs
  - λ_T is the failure rate of the device under analysis
  - λ_i is the normalized failure rate of a failure mechanism within a given functional group
  - $K_{i,F}$ is a constant defined by the weight percentage of functional group F as it is affected by the i^{th} failure mechanism
  - P_F is the probability of functional group failure from one functional group cell
  - N_F is the total number of cells in each functional group
  - N is the total number of functional groups across all types
- Acceleration factors can be applied at the transistor level to extrapolate from known device test conditions to a known system field environment

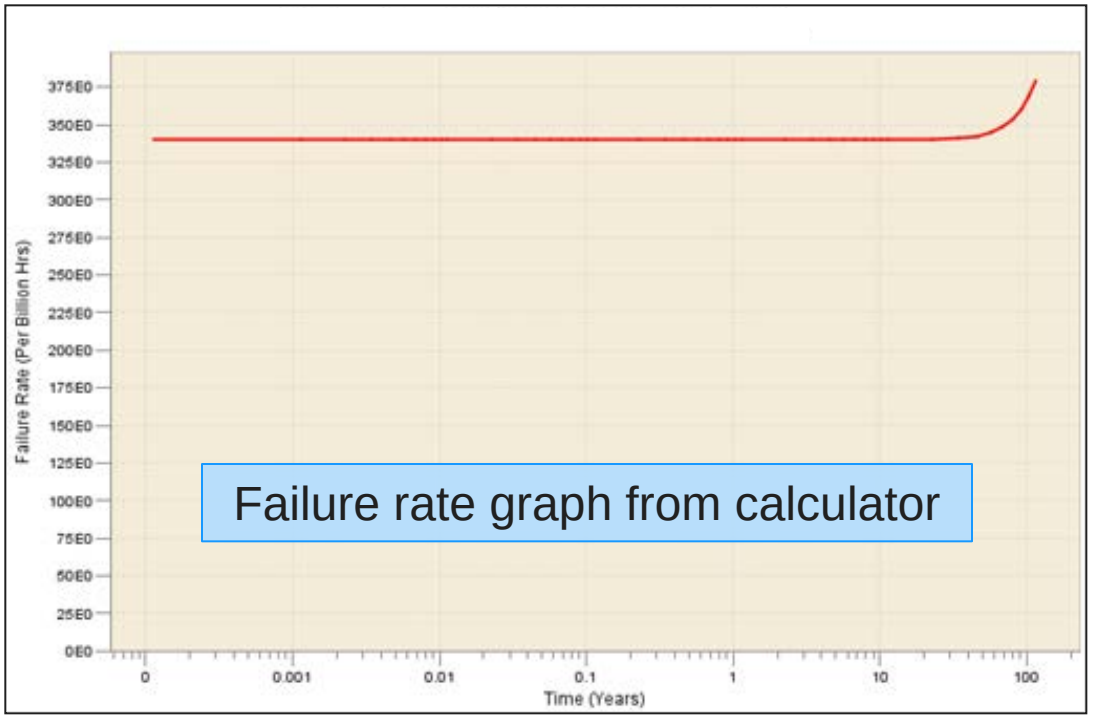
$$\lambda_T = N \times \sum \left(N_F / N \right) \times P_F \times \sum \left(K_{i,F} \times \lambda_i \right)$$

Snapshot of the Software Tool



- **Inputs:**
  - Component information
    - Feature size
    - Complexity
    - Test data
    - Operating modes
    - Electrical conditions
  - System Information
    - Temperature profiles
    - Duty cycle
  - Confidence level
- **Outputs:**
  - Device reliability
  - Device failure rate

Example: 12-bit ADC



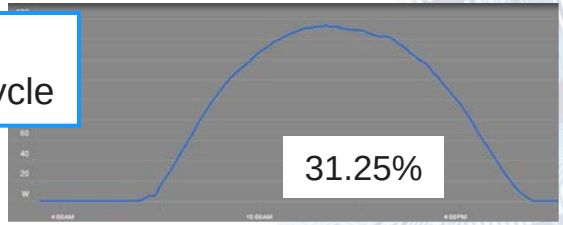
Failure rate graph from calculator

Part Number	Process Technology	Field Voltage (V)	Test Voltage (V)	Field Temperature (°C)	Test Temperature (°C)
ADC	350nm	3.3	3.6	Profile	85.0

Device characterization

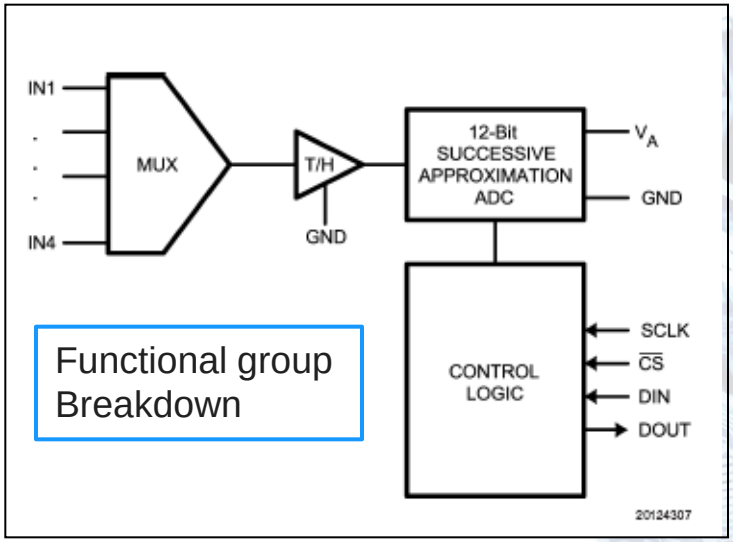
The resultant failure rate is based on full utilization of device features under these specific conditions

System Duty Cycle



System Temperature Profile

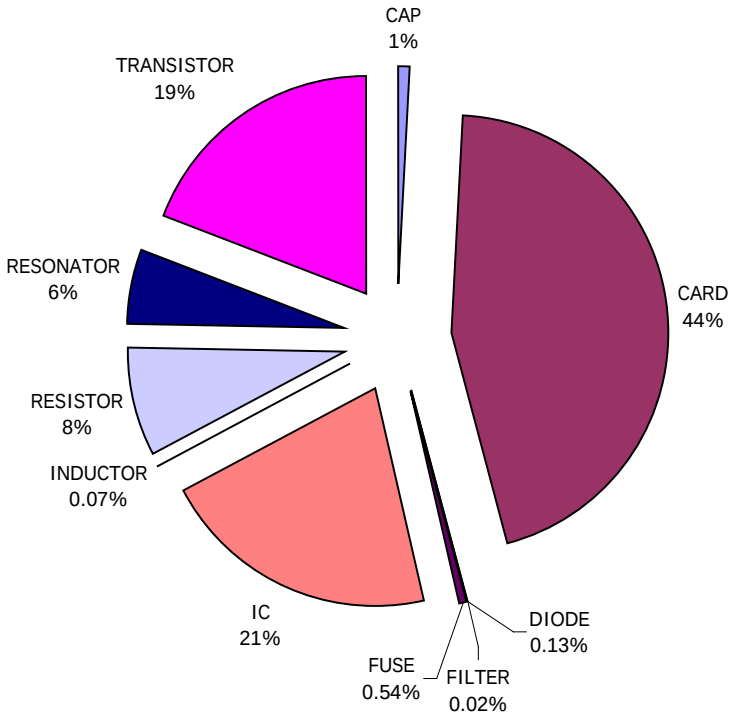
Peak Temperature (°C)	Percentage of Calendar Year
40	4.1%
	17.8%
	21.9%
	12.6%
60	20.8%
70	22.7%



Functional group Breakdown

Validation Study (130nm to 90nm)

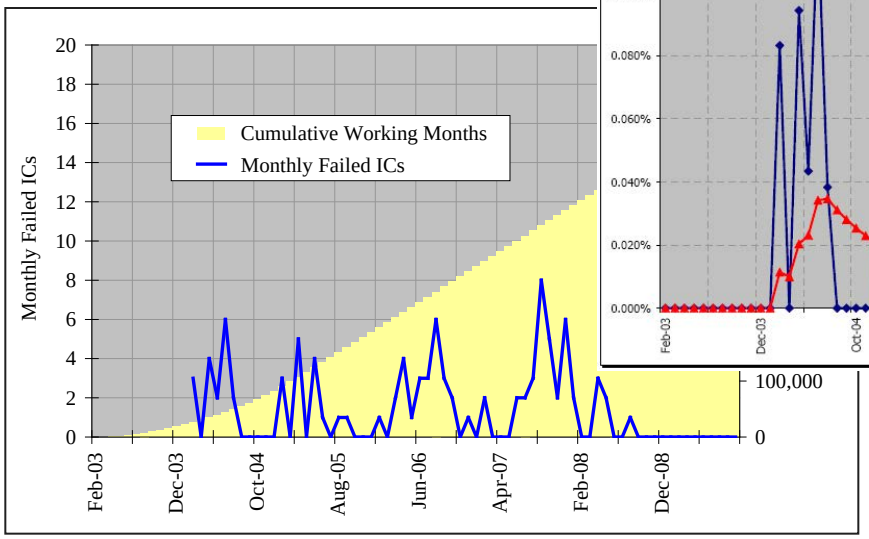
- Field return data was gathered from a family of telecommunication products
  - 56 different ICs comprised 41.5% of the failed part population
- The validation activity was utilized failure data from 5 integrated circuits

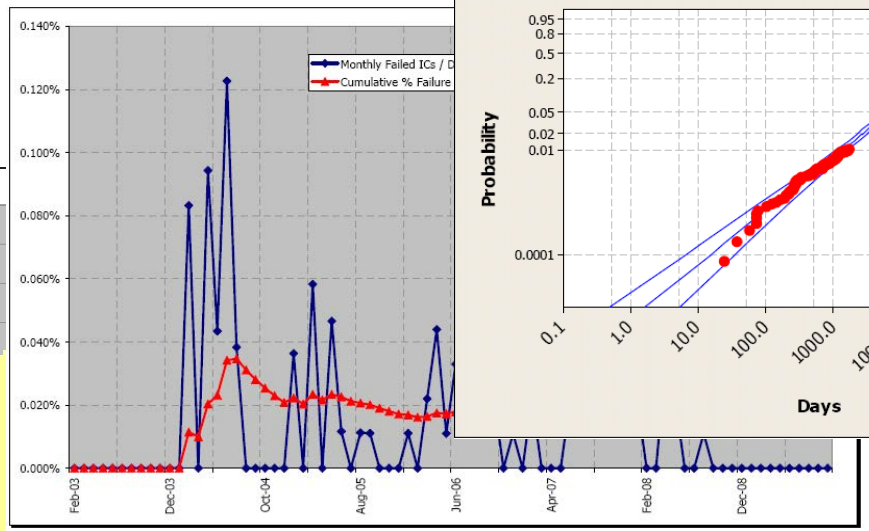


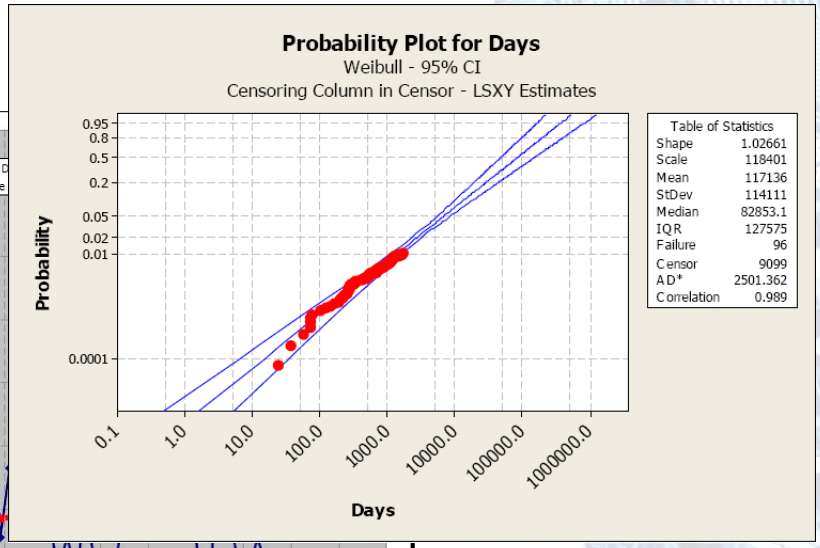
Year	Description	Quantity Replaced
2004	1 GB DRAM	190
2001	256MB DRAM	152
2005	512MB DRAM	161
2002	Microcontroller	114
2005	Microprocessor	18

Statistical Analysis on Field Returns

- Failure rate was calculated from raw data
  - Environmental conditions to determine in-field operating temperature
  - Thermal measurements to determine power dissipation
  - Cumulative failure distributions
    - Weibull
    - Exponential







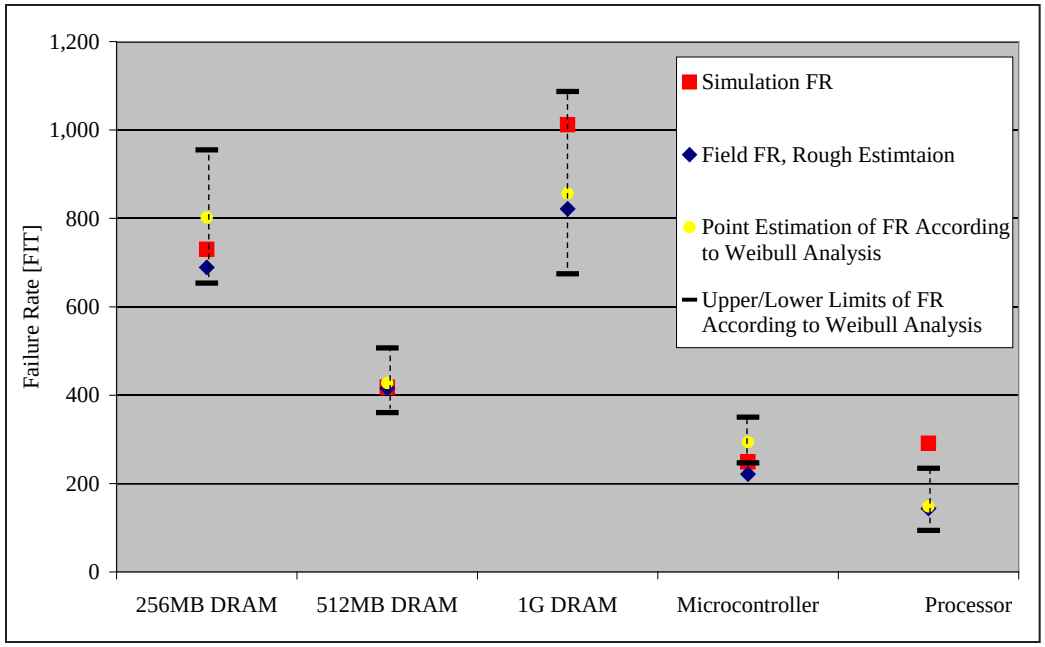
Extracted graphs from statistical analysis of field returns

Lifetime Prediction in Action

Component Information

(Actual calculator inputs)

Description	Node Technology	Field Temp. (C)	Calculated Test Temp. (C)	Vdd Field (V)	Vdd Test (V)
256MB DRAM	150 nm	42	62.28	3	3.3
512MB DRAM	100 nm	42	70.00	2.5	2.7
1GB DRAM	110 nm	42	66.68	2.6	2.7
Microcontroller	90 nm	40	77.40	5	5.5
Microprocessor	90 nm	58	99.70	1.276	1.34



Failure rates and limits

Comparison of Results – JEDEC 47D HTOL and MTBF

- Typical High Temperature Operating Life (HTOL) Test
  - Stated purpose is to simulate many years of operation at ambient, by testing at elevated temperatures and voltages: Test 77 pieces/qualification lot for 1000 hrs at 125°C (junction) to achieve zero failures
    - Accelerate via Arrhenius model with E_a=0.7 eV
    - For 3 lots (231 pcs) and operating temp of 55°C, the field operating time is ~18 million hours. At 60% confidence, *the failure rate is 51 FITs*
- Telcordia SR-332: Reliability Prediction Procedure for Electronic Equipment
  - Last Revision: Issue 6, December 1997
  - Replaced by SR-332, September 2006
- MIL-HDBK-217F (Notice 2): Reliability Prediction of Electronic Equipment
  - Last Revision: February 28, 1995 (per DoD repository)

Description	Failure in Time (FIT) (failures per billion operating hours)				
	Field	Predicted	JEDEC (Ea = 0.7eV)	SR-332	MIL-HDBK-217F
DRAM (256MB)	689	730	51	15	18
DRAM (512MB)	415	418	51	15	18
DRAM (1GB)	821	1012	51	15	18
Microcontroller	220	249	51	27	18
Microprocessor	144	291	51	67	2691

Application of Results

- Industry Standards
  - *VITA 51.2, Physics of Failure Reliability Predictions*
  - *MIL-HDBK-217J, Reliability Prediction of Electronic Systems*
    - *Addition of Physics-of-Failure requirements*
  - *IEC TS 62239, Preparation of an Electronic Component Management Plan*
    - *Addition of a wearout requirement*
- Certification requirements
- Platform customer requirements

Further Development

- Current Development (partnerships)
  - 65nm\45nm Si and 45nm SOI technologies
  - 12 additional functional groups to include processor circuitry
- Future roadmap of existing features:
  - 32nm, 22nm technologies
  - Additional functional groups
    - Digital including logic and conditioners (e.g. gates)
    - Analog for signal processing (e.g. opamps)
    - Processor based (DSP, FPGA, etc)
- Customizable equivalent circuits and automated functional group analysis for ASIC design
- "Expert mode"
  - Modification of all default parameters
- Tradeoff analysis
  - Performance vs. Reliability