Expanding IEEE Std 1149.1 Boundary-Scan Architecture Beyond Manufacturing Test of Printed Circuit Board Assembly

Jun Balangue
Keysight Technologies
Singapore
Jun_balangue@keysight.com

Abstract

This paper will discuss the expanded use of boundary-scan testing beyond the typical manufacturing test to capture structural defects on a component/devices in a printed circuit board assembly (PCBA).

The following topics will be discussed to demonstrate the capability of boundary-scan test system on how we can extend beyond typical manufacturing test:

1. Boundary-scan as a complete manufacturing test system – A boundary-scan test system should be able to cover all the needs of a manufacturing test to be an effective solution.
2. Boundary-scan implementation during PCBA design stage – This topic will discuss the importance of design for test (DFT) at the early stage of PCBA design to maximize the use of boundary-scan to lower the cost of test while increasing the test coverage.
3. Implementation of boundary-scan beyond typical structural testing – While capturing structural defects are important during manufacturing test, the need for boundary-scan to include other areas beyond PCBA structural testing is now necessary.

Introduction

IEEE Std 1149.1 (Boundary-scan)

The IEEE Std 1149.1 is an IEEE Standard for Test Access port and boundary-scan Architecture which was first released in 1990 to address the printed circuit board increasing density and manufacturing faults - such as open and shorts. The boundary-scan devices are specifically designed with internal shift registers placed between each device pin and the internal logic as shown in Figure 1. The shift registers are known as boundary-scan cells that are allowed to be controlled and observed at each input and output of the device pin. When these boundary-scan cells are connected together they form a data register chain called the Boundary Register and when the boundary-scan devices are connected, it is called the boundary-scan chain. These boundary-scan chain of boundary-scan cells provide the ability to drive/receive digital voltage levels (representing 0 and 1 values) to enable multiple forms of testing, programming, measurement and control that can be automated into special purpose test equipment, from just the 4-5 signals of the boundary-scan interface, called the Test Access Port (TAP) which consist of Test Data Input (TDI), Test Data Output (TDO), Test Clock (TCK), Test Mode Select (TMS) and the optional Test Reset (TRST).

The 1149.1 standard had gone through many improvements and enhancements. The last one in 2013 included major improvements to access function inside the device core which were only available previously through a Built-In Self-Test (BIST) execution. The next standards that garnered a lot of support from the network communication PCBA was the IEEE 1149.6 high-speed differential interconnects which was approved in 2005. It has just gone through ratification in 2015 to support the same PDL function in 1149.1-2013 but addressing the functions related to high speed differential.

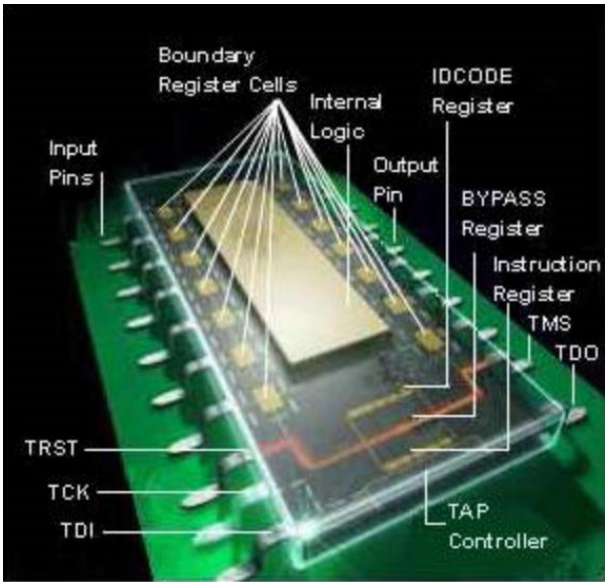


Figure 1 An Illustration of a Boundary-Scan Device

The following topics will be discussed to show the expanding capability of the boundary-scan test system to extend beyond typical manufacturing test and address the coverage challenges of current and future PCBAs:

1. **Boundary scan as part of the manufacturing test system –** With the increasing density of the PCBA due to the proliferation of high speed differential signal especially on network communication and servers, the boundary-scan test becomes an integral part of ICT strategy to ensure the high test coverage and quality of every board. Boundary-scan also helps to balance the ICT system cost and at the same time retains the coverage needed, while ensuring those failed boards are repaired. Figure 2 shows a typical PCBA manufacturing line where the In-circuit test (ICT) system and functional test system are placed after the SMT line to capture structural and functional defects. Figure 3 also shows the stations where boundary-scan can be implemented as follows:
    - **Boundary Scan at In-Circuit Test (ICT)**
      The ICT is the most favored manufacturing test system because of its ability to detect structural failures - such as opens, shorts, analog unpowered, and analog/digital powered testing including boundary-scan test with accuracy and speed. Modern ICT has the native software to execute boundary-scan test which includes both the IEEE Std 1149.1 and IEEE Std 1149.6 while those ICT that do not have the native boundary-scan software have an option to integrate a 3rd party boundary-scan box.

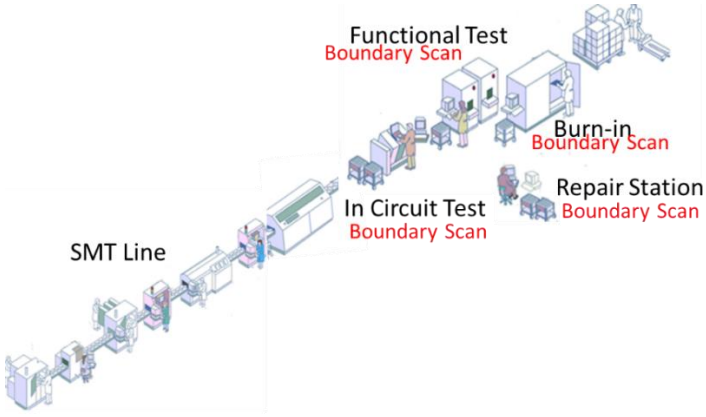


Figure 2 – Typical PCBA Manufacturing line shows the stations where boundary scan can be implemented

The Benefits of integrating boundary scan test in ICT are as follows:

1. Coverage on nodes/device pins that have no test point due to high speed signal, such as - 1149.6 and DDR(Double Data Rate).
2. Lower cost of ICT system by using less hybrid cards. A 10,000 nodes can be reduced to fit into a 5,000 node ICT resource.
3. Lower cost of fixture by having less test probes.
4. Better production failure message including device pin level for ease of repair versus a block failure on functional. (Refer to Figure 3 on ICT failure message vs functional message)

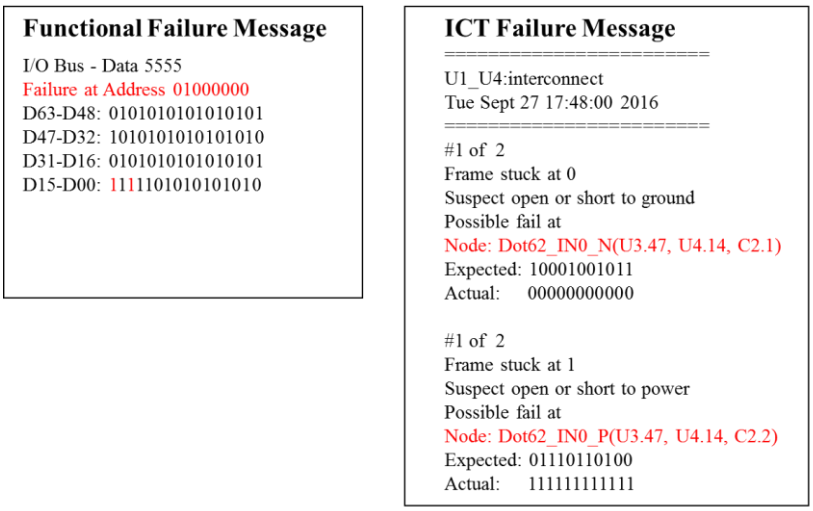


Figure 3 – Functional failure versus ICT failure message

- **Boundary Scan at Functional Testing (FT) and Burn In**
  The implementation of boundary-scan as part of functional test and burn in or another test station before functional test station is now slowly being adopted in manufacturing as it helps to screen the boards that have structural defects. PCBAs that failed at functional testing are normally challenging to diagnose/or repair as it does not give a specific component pin failure compared to the ICT and boundary-scan failure message. In addition, the implementation of boundary-scan in functional test addresses the coverage gap that is not possible to be implemented in ICT such as:

- 1149.1/1149.6 Loopback test on connectors and backplane
- 1149.1/1149.6 Interconnect test between board under test and plug in cards such as daughter boards, DIMM etc.
- Built-in self-test (BIST) targeting specific ASIC/CPU and functional block such as memories, PCI interface etc.
- Implementation of IEEE Std 1687 and industry chip company validation, debug and test technology which are being embedded into advanced processors and chipsets.

  The other advantage of integrating boundary-scan before functional and/or burn in is that it is able to immediately see a failure before the functional and/or burn in test is executed which normally takes a longer time, thus, wasting more time.

- **Boundary Scan at Repair station**
  The use of boundary-scan to verify ICT/Functional and Burn-In failed boards is recommended as a single repair tool station due to the following reason:

- The boards after ICT are assembled with heatsinks and might not be able to do a re-test in ICT. This will mean more work to remove the heatsink and cost issues as some of the heatsinks need to be scrapped.

2. Boundary scan implementation during PCBA design stage

The successful implementation of boundary-scan into manufacturing test lies in the effort by the designer to include boundary-scan at schematic design and PCB layout stage (See Figure 4). The ability of the boundary-scan software tool has improved tremendously today to help assist the designer and NPI Test engineer to review the design. The following reports are available:

- A DFT report (See Figure 5) that lists boundary-scan design constraint, such as boundary-scan devices which are in chain and proper buffering is done, compliance bias as per BSDL declaration. This will help the designer and NPI engineer to enable them to correct the constraints before the PCB layout is done which will ensure boundary-scan's successful implementation during Prototype Run, NPI and Production/Manufacturing run. The DFT report also list the 1149.6 device/pin that are properly connected with AC coupling to the other 1149.6 boundary-scan device/pin.

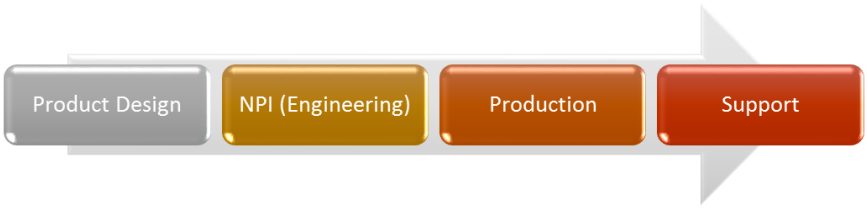


Figure 4 – Product Design and Manufacturing flow

- The next important report to generate is the test coverage and test point reduction list to ensure that the right coverage strategies are implemented on the board. The test coverage will help the NPI engineer to review the manufacturing test strategy to ensure higher coverage on the PCBA.

Chain Name	1~U1_1~U4
Scan Chain	*1~J8* -> 1~U1 -> 1~U2 -> 1~U3 -> 1~U4 -> *1~J8*

JTAG Headers

Port	Pin	Net	Remark
TDI	1~J8.7	1~ANGELA_TDI	
TDO	1~J8.9	1~ANGELA_TDO	
TMS	1~J8.3	1~ANGELA_TMS	
TCK	1~J8.1	1~ANGELA_TCK	
TRST	1~J8.5	1~ANGELA_TRST_L	

Fan Out Report

Port	Pin	Fanout	Connected Devices	Remark
TMS	-	-	-	No Fan Out of more than 7 is found
TCK	-	-	-	No Fan Out of more than 7 is found
TRST	-	-	-	No Fan Out of more than 7 is found

Device	1~U1 (BSDL File = scan92lv090_mode1.bsdl)

Test Port

Port	Pin	Node	Trace
TDI	1~U1.8	1~ANGELA_TDI	1~J8(7)-> (8)1~U1
TDO	1~U1.11	1~$2N784	1~U1(11)-> (8)1~U2
TMS	1~U1.38	1~ANGELA_TMS	1~J8(3)-> (38)1~U1
TCK	1~U1.1	1~ANGELA_TCK	1~J8(1)-> (1)1~U1
TRST	1~U1.39	1~ANGELA_TRST_L	1~J8(5)-> (39)1~U1

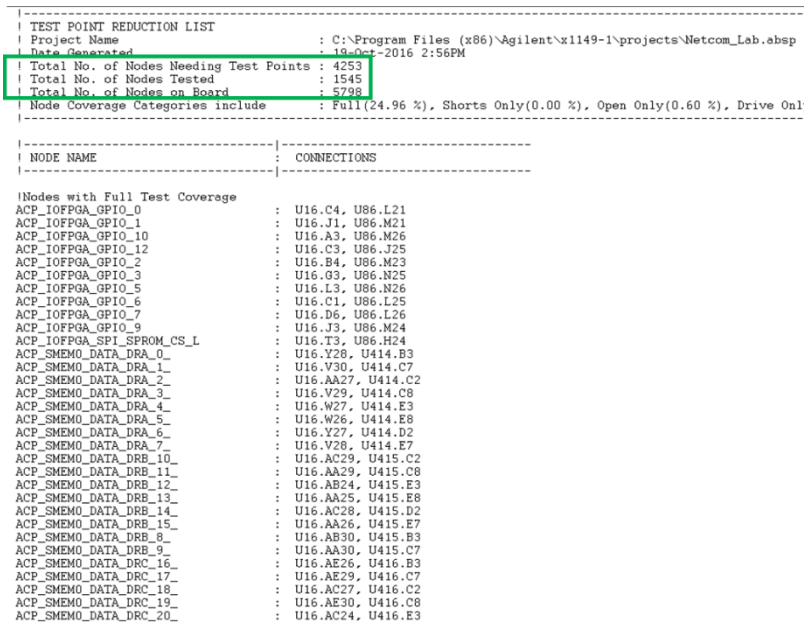
Compliance: None

AC Scan Cell(s)

Pin	Node	Dot6 Rx Cell	Capacitor	To Pin	Node	Dot6 Tx Cell
1~U1.21	1~DOT12_DIN7	11	1~RP2%r8_9	1~U2.20	1~DOT11_RO7	20
1~U1.19	1~DOT12_DIN6	12	1~RP2%r7_10	1~U2.18	1~DOT11_RO6	21
1~U1.13	1~DOT12_DIN5	13	1~RP2%r6_11	1~U2.12	1~DOT11_RO5	22
1~U1.7	1~DOT12_DIN4	14	1~RP2%r5_12	1~U2.6	1~DOT11_RO4	23
1~U1.3	1~DOT12_DIN3	15	1~RP2%r4_13	1~U2.2	1~DOT11_RO3	24
1~U1.63	1~DOT12_DIN2	16	1~RP2%r3_14	1~U2.62	1~DOT11_RO2	25
1~U1.61	1~DOT12_DIN1	17	1~RP2%r2_15	1~U2.60	1~DOT11_RO1	26
1~U1.59	1~DOT12_DIN0	18	1~RP2%r1_16	1~U2.58	1~DOT11_RO0	27

Figure 5 - Boundary Scan Design for test (DFT) report

- The test point reduction (TPR) lists all the nodes that are covered by boundary-scan test and will help the NPI Engineer and PCB layout designer to properly allocate the test point on the board to nodes that are not covered (See Figure 6). This will also help ensure the cost of the ICT system and fixture are reduced since boundary-scan test does not need to have access to the nodes except to the TAP pins (TDI, TMS, TCK, TDO and optional TRST).



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| TEST POINT REDUCTION LIST
| Project Name                          : C:\Program Files (x86)\Agilent\x1149-1\projects\Netcom_Lab.absp
| Date Generated                        : 19-Oct-2016 2:56PM
| Total No. of Nodes Needing Test Points : 4253
| Total No. of Nodes Tested             : 1545
| Total No. of Nodes on Board           : 5798
| Node Coverage Categories include      : Full(24.96 %), Shorts Only(0.00 %), Open Only(0.60 %), Drive Onl
|-------------------------------------------------------------------------------------------------------------

|-----------------------------------|-----------------------------------
| NODE NAME                         :  CONNECTIONS
|-----------------------------------|-----------------------------------

!Nodes with Full Test Coverage
ACP_IOFPGA_GPIO_0                   :  U16.C4, U86.L21
ACP_IOFPGA_GPIO_1                   :  U16.J1, U86.M21
ACP_IOFPGA_GPIO_10                  :  U16.A3, U86.M26
ACP_IOFPGA_GPIO_12                  :  U16.C3, U86.J25
ACP_IOFPGA_GPIO_2                   :  U16.B4, U86.M23
ACP_IOFPGA_GPIO_3                   :  U16.G3, U86.N25
ACP_IOFPGA_GPIO_5                   :  U16.L3, U86.N26
ACP_IOFPGA_GPIO_6                   :  U16.C1, U86.L25
ACP_IOFPGA_GPIO_7                   :  U16.D6, U86.L26
ACP_IOFPGA_GPIO_9                   :  U16.J3, U86.M24
ACP_IOFPGA_SPI_SPROM_CS_L           :  U16.T3, U86.H24
ACP_SMEM0_DATA_DRA_0_               :  U16.Y28, U414.B3
ACP_SMEM0_DATA_DRA_1_               :  U16.V30, U414.C7
ACP_SMEM0_DATA_DRA_2_               :  U16.AA27, U414.C2
ACP_SMEM0_DATA_DRA_3_               :  U16.V29, U414.C8
ACP_SMEM0_DATA_DRA_4_               :  U16.W27, U414.E3
ACP_SMEM0_DATA_DRA_5_               :  U16.W26, U414.E8
ACP_SMEM0_DATA_DRA_6_               :  U16.Y27, U414.D2
ACP_SMEM0_DATA_DRA_7_               :  U16.V28, U414.E7
ACP_SMEM0_DATA_DRB_10_              :  U16.AC29, U415.C2
ACP_SMEM0_DATA_DRB_11_              :  U16.AA29, U415.C8
ACP_SMEM0_DATA_DRB_12_              :  U16.AB24, U415.E3
ACP_SMEM0_DATA_DRB_13_              :  U16.AA25, U415.E8
ACP_SMEM0_DATA_DRB_14_              :  U16.AC28, U415.D2
ACP_SMEM0_DATA_DRB_15_              :  U16.AA26, U415.E7
ACP_SMEM0_DATA_DRB_8_               :  U16.AB30, U415.B3
ACP_SMEM0_DATA_DRB_9_               :  U16.AA30, U415.C7
ACP_SMEM0_DATA_DRC_16_              :  U16.AE26, U416.B3
ACP_SMEM0_DATA_DRC_17_              :  U16.AE29, U416.C7
ACP_SMEM0_DATA_DRC_18_              :  U16.AC27, U416.C2
ACP_SMEM0_DATA_DRC_19_              :  U16.AE30, U416.C8
ACP_SMEM0_DATA_DRC_20_              :  U16.AC24, U416.E3
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Figure 6 – Test Point Reduction list

3. **Implementation of boundary-scan beyond structural testing**

Although the boundary-scan structural defect coverage is still important during manufacturing test, the needs for a boundary-scan coverage to include other areas beyond typical structural testing is now necessary due to increasing complexities of tPCBA design. Several standards are ratified and introduced to address this growing needs:

IEEE Std 1149.1-2013 and IEEE Std 1149.6-2015 Procedural Description Language (PDL)

The 1149.1 standard was revised and published in 2013 while the 1149.6 was revised and published in 2015. Both standards include the PDL as part of the BSDL to be available for functional usage. The use of PDL on 1149.1/1149.6 is to document the boundary-scan device controls of data, instructions and the target registers such as IP packages. This new feature will allow the implementation of boundary-scan beyond the typical structural testing such as I/O functions, memory BIST of the device which will have significant test coverage on the PCBA that were only available previously on system functional testing.

IEEE 1687 Std 2014

The IEEE Std 1687 is commonly known as instrument JTAG (iJTAG). The objective here is to develop a methodology and rules to access the instrumentation embedded into a semiconductor device without the need to define the instruments or their features using IEEE Standard 1149.1.

The proposed standard would includes a description language that specifies an interface to help communicate with the internal embedded instrumentation and features within the semiconductor device, such as - built-in self-test (BIST), embedded instruments that are normally accessible only to chip designers, as well as other internal functions of the device (see Figure 7). IEEE Std 1687-2014 or iJTAG permits usage of IEEE 1149.1 test access port (TAP) interface, which is prevalent on a majority of devices to manage the configuration, operation and collection of data, from the embedded instrumentation circuitry inside the target device.

The automatic test equipment (ATE) providers will be able to access the embedded instruments, logic BIST and IPs inside the device for chip, board or system testing purposes. The electronics manufacturer will be able to regain test coverage with minimal cost impact by integrating this solution into their current testing processes. The adoption of IEEE Std 1687-2014 into mainstream testing will depend on how the industry responds. Each business segment is now waiting for a compliant device that will support the standards, and adoption will be based on their specific needs.

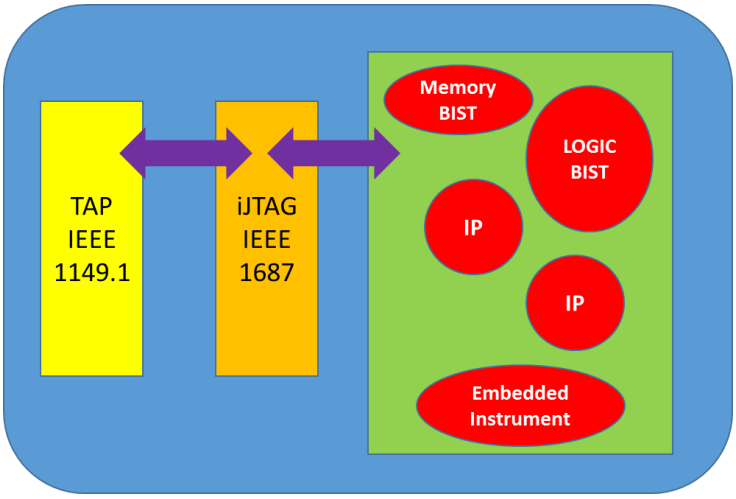

Figure 7 IEEE Std 1687-2014 connection to IPs and accessible through IEEE 1149.1 test access port (TAP).

Example of industry chip company validation, debug and test technology

Industry chip company validation, debug and test technologies are being embedded into advanced processors and chipsets which enable the test for the company CPU designs with this technology if test access is constrained by PCBA real estate or high-speed signal integrity. The execution of the test requires access to the CPU debug port2 and uses the chip company design abstraction layer to access the CPU core to verify its function and that of surrounding devices. The technology requires the motherboard BIOS to be set up according to the company BIOS writer Guide3, reserving a designated register to host the results of the test technology. During the manufacturing test, the PCBA under test has to be powered up safely to run the BIOS and the test technology will post the results of its test into the designated register. The content of the register is then compared to the known good board (KGB) values to determine if the PCBA passes or fails the set of tests.

The test technology will test the company test technology enabled CPU (and BIOS) for the following functions:

- Platform hub controller (PCH)
- Memory (On Board DDR)
- Graphics eg VGA, HDMI, eDP
- High speed I/O(HSIO) eg PCIe, SATA, USB3
- Communication interfaces eg LAN, USB2
- I/O Peripherals eg keyboard, audio

BIST using JEDEC STAPL/ IEEE SVF/Custom proprietary Language/ Conclusions

Boundary-scan tools are now capable to interpret and convert the binary files or configuration (CFG) files supplied by the ASIC designer or vendor to execute Built-in self-test (BIST) such as memory BIST, Logic BIST and other custom function test that will help extend the coverage of a board during boundary-scan testing.

The boundary-scan 1149.1 along with the new enhancements and standards such as - IEEE 1149.6 and IEEE 1687 will redefine the testing strategy for PCBA, not only in the In-Circuit Test but including various areas of manufacturing such as - functional test, burn in and repair as well as the prototype and NPI stages of the product which will help the industry in ensuring testability of the next generation of PCBAs and streamlining the efficiency of the test systems.

References

1. 1687-2014 IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device
2. 1149.1-2013 IEEE Standard Test Access Port and Boundary-Scan Architecture-- http://standards.ieee.org/findstds/standard/1149.1-2013.html

3. 1149.6-2015 IEEE Standard for Boundary-Scan Testing of Advanced Digital Network-- http://standards.ieee.org/findstds/standard/1149.6-2015.html
4. Kenneth P. Parker, “The Boundary-Scan Handbook, 4th Edition” 2015
5. Jun Balangue, “New IEEE Standards for board and system tests” Circuits Assembly, Printed Circuit Design and Fab, April, 2015
6. “Boundary Scan DFT Guidelines for good chain integrity and test coverage” Application note, Keysight Technologies

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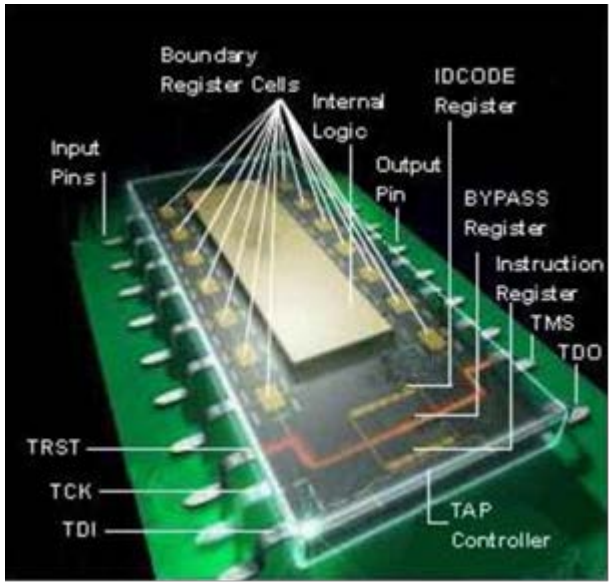
Introduction

- IEEE Std 1149.1 (Boundary-scan)



The IEEE Std 1149.1 is an IEEE Standard for Test Access port and boundary-scan Architecture

Agenda:

1. Boundary-scan as a complete manufacturing test system
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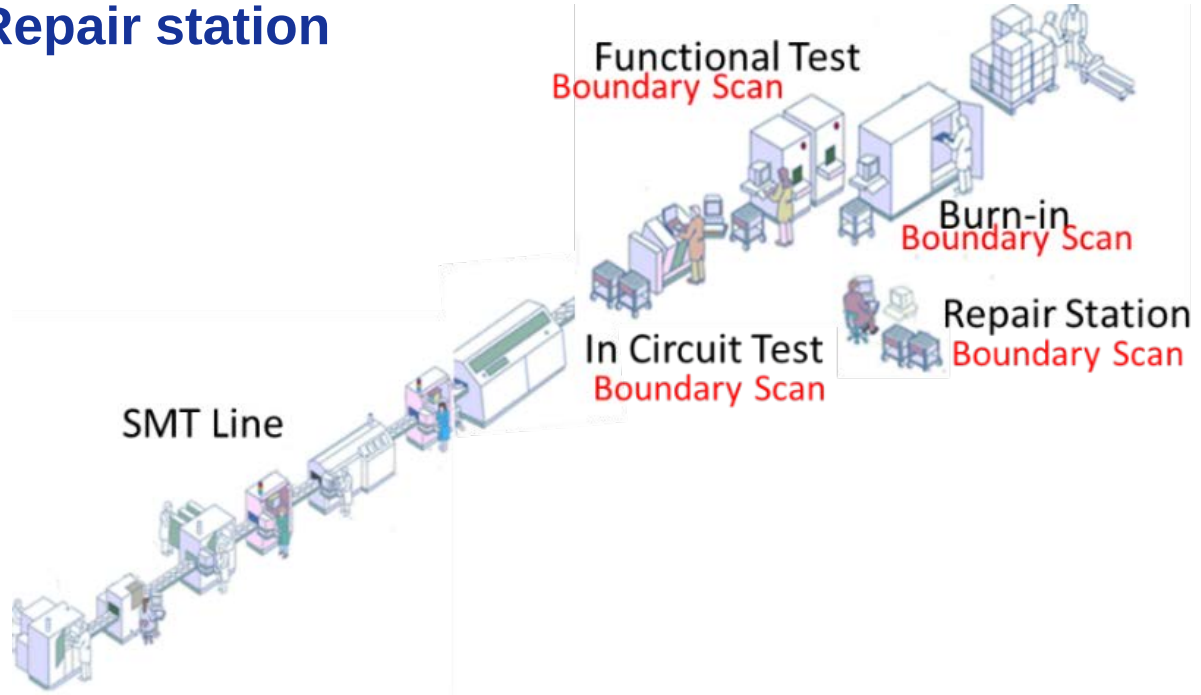
Boundary-scan as a complete manufacturing test system

- Boundary Scan at In-Circuit Test (ICT)
- Boundary Scan at Functional Testing (FT) and Burn In
- Boundary Scan at Repair station



Boundary-scan as a complete manufacturing test system

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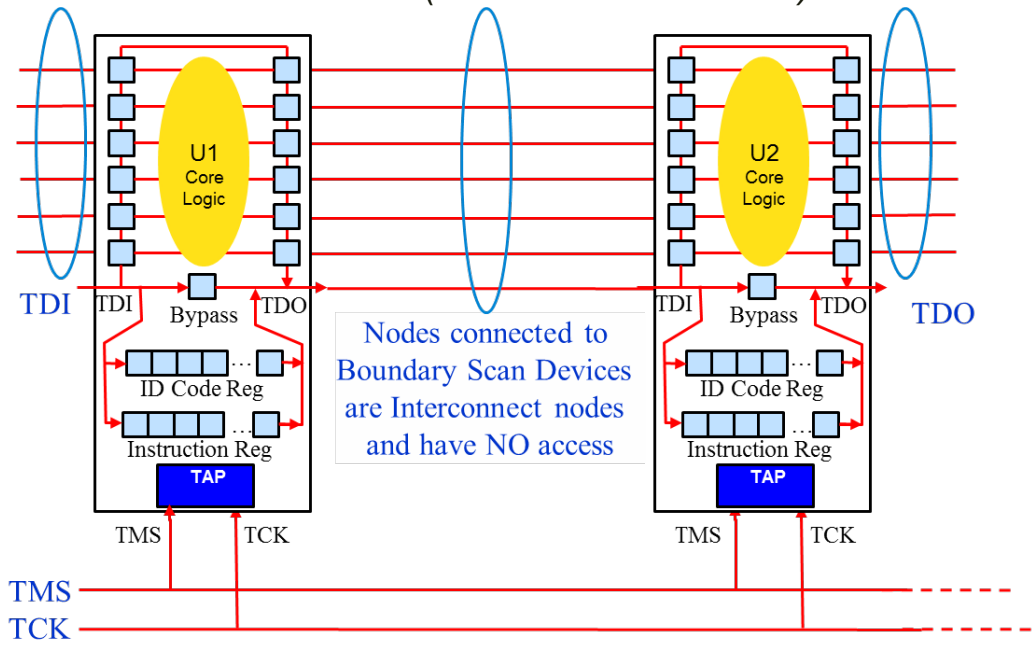

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```
!-------------------------------------------------------------------------------------------------------
! TEST POINT REDUCTION LIST
! Project Name                              : C:\Program Files \x1149\projects\project.absp
! Date Generated                            : 5-Jan-2017 10:08AM
! Total No. of Nodes Needing Test Points : 4952
! Total No. of Nodes Tested                 : 4752
! Total No. of Nodes on Board               : 9704
! Node Coverage Categories include       : Full          3496    (36.03 %)
!                                           Short Only    448     (4.62 %)
!                                           Open Only     0       (0.00 %)
!                                           Drive Only    0       (0.00 %)
!                                           Partial       808     (8.33 %)
!                                           None          4952    (51.03 %)
!-------------------------------------------------------------------------------------------------------
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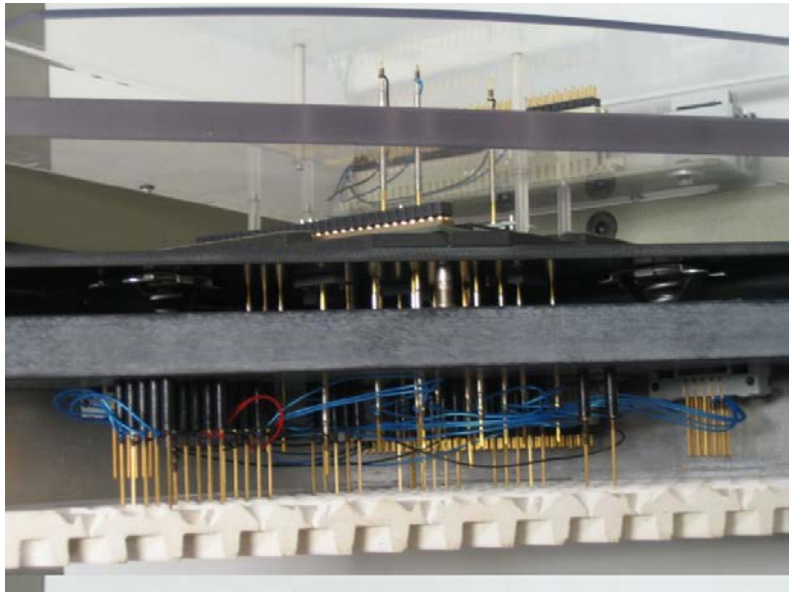

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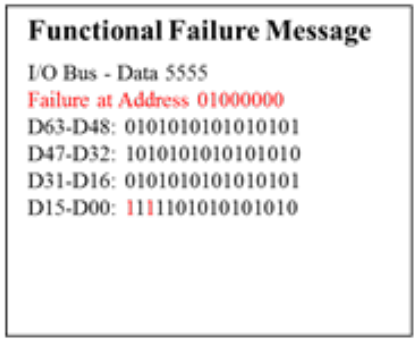

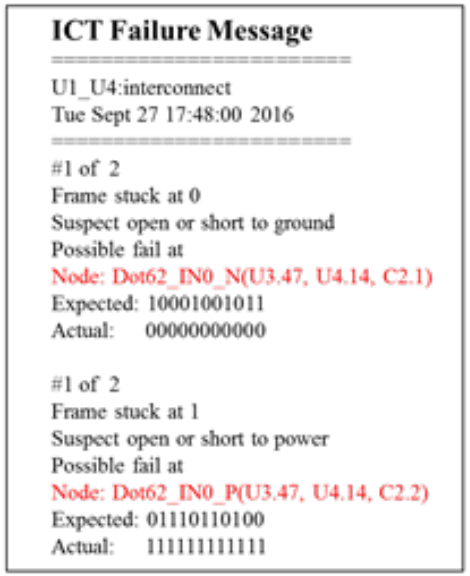

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4. Implementation of IEEE Std 1687 and industry chip company validation, debug and test technology which are being embedded into advanced processors and chipsets.

Boundary-scan as a complete manufacturing test system

- **Boundary Scan at Repair station**

The Benefits of integrating boundary scan test at repair station:

1. *Able to verify the board on bench repair station that failed boundary scan*
2. *Functional failed boards don't need to return to ICT for verification*

Agenda:

1. Boundary-scan as a complete manufacturing test system
2. **Boundary-scan implementation during PCBA design stage**
3. Implementation of boundary-scan beyond typical structural testing

Boundary-scan implementation during PCBA design stage

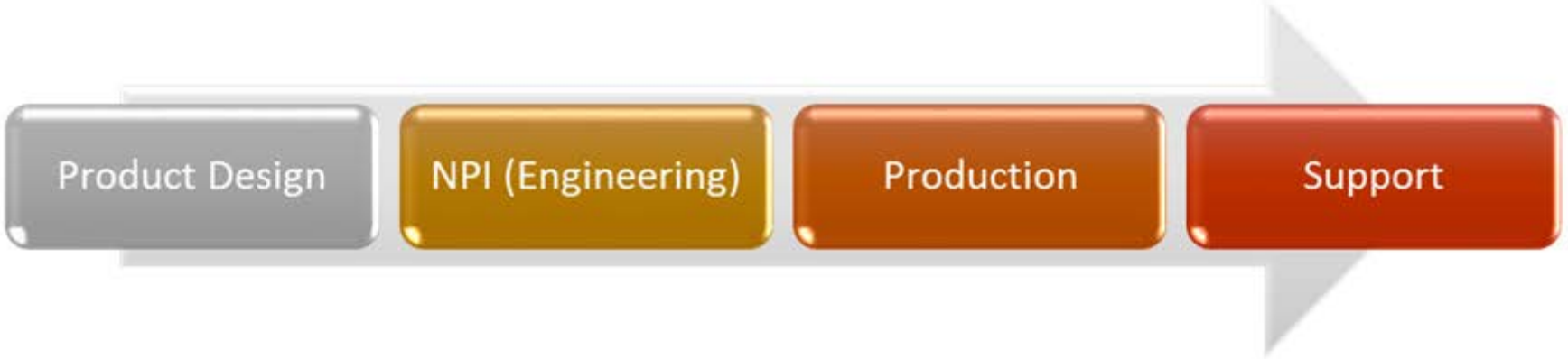


Figure 4 – Product Design and Manufacturing flow

Boundary-scan implementation during PCBA design stage

- **Design for test report**

Chain Name	1~U1_1~U4
Scan Chain	*1~J8* -> 1~U1 -> 1~U2 -> 1~U3 -> 1~U4 -> *1~J8*

JTAG Headers

Port	Pin	Net	Remark
TDI	1~J8.7	1~ANGELA_TDI	
TDO	1~J8.9	1~ANGELA_TDO	
TMS	1~J8.3	1~ANGELA_TMS	
TCK	1~J8.1	1~ANGELA_TCK	
TRST	1~J8.5	1~ANGELA_TRST_L	

Fan Out Report

Port	Pin	Fanout	Connected Devices	Remark
TMS	-	-	-	No Fan Out of more than 7 is found
TCK	-	-	-	No Fan Out of more than 7 is found
TRST	-	-	-	No Fan Out of more than 7 is found

Device	1~U1 (BSDL File = scan92lv090_mode1.bsdl)

Test Port

Port	Pin	Node	Trace
TDI	1~U1.8	1~ANGELA_TDI	1~J8(7)-> (8)1~U1
TDO	1~U1.11	1~$2N784	1~U1(11)-> (8)1~U2
TMS	1~U1.38	1~ANGELA_TMS	1~J8(3)-> (38)1~U1
TCK	1~U1.1	1~ANGELA_TCK	1~J8(1)-> (1)1~U1
TRST	1~U1.39	1~ANGELA_TRST_L	1~J8(5)-> (39)1~U1

Compliance: None

AC Scan Cell(s)

Pin	Node	Dot6 Rx Cell	Capacitor	To Pin	Node	Dot6 Tx Cell
1~U1.21	1~DOT12_DIN7	11	1~RP2%r8_9	1~U2.20	1~DOT11_RO7	20
1~U1.19	1~DOT12_DIN6	12	1~RP2%r7_10	1~U2.18	1~DOT11_RO6	21
1~U1.13	1~DOT12_DIN5	13	1~RP2%r6_11	1~U2.12	1~DOT11_RO5	22
1~U1.7	1~DOT12_DIN4	14	1~RP2%r5_12	1~U2.6	1~DOT11_RO4	23
1~U1.3	1~DOT12_DIN3	15	1~RP2%r4_13	1~U2.2	1~DOT11_RO3	24
1~U1.63	1~DOT12_DIN2	16	1~RP2%r3_14	1~U2.62	1~DOT11_RO2	25
1~U1.61	1~DOT12_DIN1	17	1~RP2%r2_15	1~U2.60	1~DOT11_RO1	26
1~U1.59	1~DOT12_DIN0	18	1~RP2%r1_16	1~U2.58	1~DOT11_RO0	27

Figure 5 - Boundary Scan Design for test (DFT) report

Boundary-scan implementation during PCBA design stage

- **Test Point Reduction**

```
|-------------------------------------------------------------------------------------------------------------
| TEST POINT REDUCTION LIST
| Project Name                                : C:\Program Files              \x1149-1\projects\Netcom_Lab.absp
| Date Generated                              : 19-Oct-2016 2:56PM
| Total No. of Nodes Needing Test Points : 4253
| Total No. of Nodes Tested                   : 1545
| Total No. of Nodes on Board                 : 5798
| Node Coverage Categories include            : Full(24.96 %), Shorts Only(0.00 %), Open Only(0.60 %), Drive Onl
|-------------------------------------------------------------------------------------------------------------

|-----------------------------------|-----------------------------------
| NODE NAME                         :  CONNECTIONS
|-----------------------------------|-----------------------------------

!Nodes with Full Test Coverage
ACP_IOFPGA_GPIO_0                   :  U16.C4, U86.L21
ACP_IOFPGA_GPIO_1                   :  U16.J1, U86.M21
ACP_IOFPGA_GPIO_10                  :  U16.A3, U86.M26
ACP_IOFPGA_GPIO_12                  :  U16.C3, U86.J25
ACP_IOFPGA_GPIO_2                   :  U16.B4, U86.M23
ACP_IOFPGA_GPIO_3                   :  U16.G3, U86.N25
ACP_IOFPGA_GPIO_5                   :  U16.L3, U86.N26
ACP_IOFPGA_GPIO_6                   :  U16.C1, U86.L25
ACP_IOFPGA_GPIO_7                   :  U16.D6, U86.L26
ACP_IOFPGA_GPIO_9                   :  U16.J3, U86.M24
ACP_IOFPGA_SPI_SPROM_CS_L           :  U16.T3, U86.H24
ACP_SMEM0_DATA_DRA_0_               :  U16.Y28, U414.B3
ACP_SMEM0_DATA_DRA_1_               :  U16.V30, U414.C7
ACP_SMEM0_DATA_DRA_2_               :  U16.AA27, U414.C2
ACP_SMEM0_DATA_DRA_3_               :  U16.V29, U414.C8
ACP_SMEM0_DATA_DRA_4_               :  U16.W27, U414.E3
ACP_SMEM0_DATA_DRA_5_               :  U16.W26, U414.E8
ACP_SMEM0_DATA_DRA_6_               :  U16.Y27, U414.D2
ACP_SMEM0_DATA_DRA_7_               :  U16.V28, U414.E7
ACP_SMEM0_DATA_DRB_10_              :  U16.AC29, U415.C2
ACP_SMEM0_DATA_DRB_11_              :  U16.AA29, U415.C8
ACP_SMEM0_DATA_DRB_12_              :  U16.AB24, U415.E3
ACP_SMEM0_DATA_DRB_13_              :  U16.AA25, U415.E8
ACP_SMEM0_DATA_DRB_14_              :  U16.AC28, U415.D2
ACP_SMEM0_DATA_DRB_15_              :  U16.AA26, U415.E7
ACP_SMEM0_DATA_DRB_8_               :  U16.AB30, U415.B3
ACP_SMEM0_DATA_DRB_9_               :  U16.AA30, U415.C7
ACP_SMEM0_DATA_DRC_16_              :  U16.AE26, U416.B3
ACP_SMEM0_DATA_DRC_17_              :  U16.AE29, U416.C7
ACP_SMEM0_DATA_DRC_18_              :  U16.AC27, U416.C2
ACP_SMEM0_DATA_DRC_19_              :  U16.AE30, U416.C8
ACP_SMEM0_DATA_DRC_20_              :  U16.AC24, U416.E3
```

Figure 6 – Test Point Reduction list

Agenda:

1. Boundary-scan as a complete manufacturing test system
2. Boundary-scan implementation during PCBA design stage
3. **Implementation of boundary-scan beyond typical structural testing**

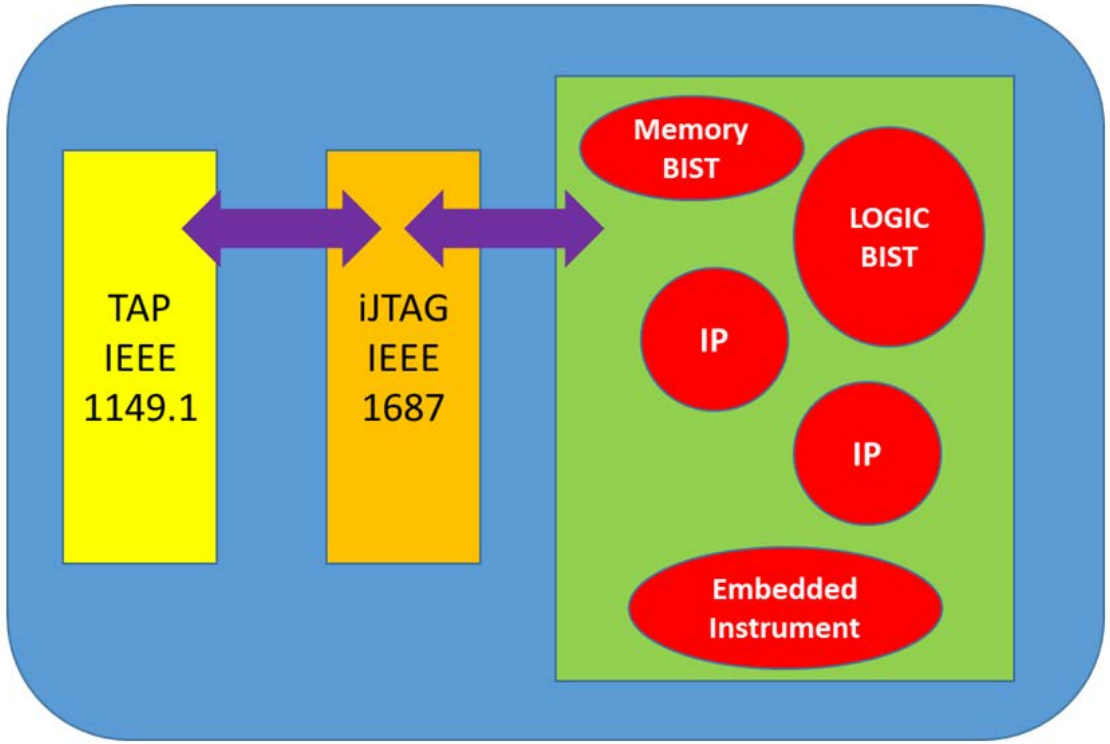
Implementation of boundary-scan beyond typical structural testing

- IEEE Std 1149.1-2013 and IEEE Std 1149.6-2015
- IEEE Std 1687-2014
- Industry chip company validation, debug and test technology
- BIST using JEDEC STAPL/ IEEE SVF/Custom proprietary Language

IEEE Std 1149.1-2013 and IEEE Std 1149.6-2015

- Test Mode Persistence
- New Instructions (INIT_SETUP, INIT_CLAMP, and INIT_RUN, IC_RESET)
- Dynamic DATA registers
- Support PDL as part of the BSDL for functional usage

IEEE Std 1687-2014

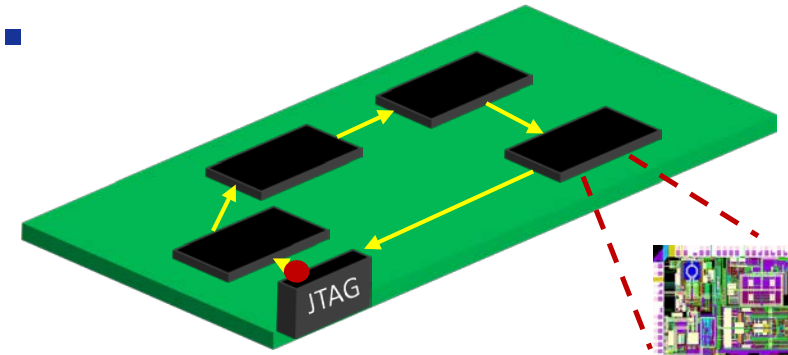


IEEE Std 1687-2014 connection to IPs and accessible through IEEE 1149.1 test access port (TAP).

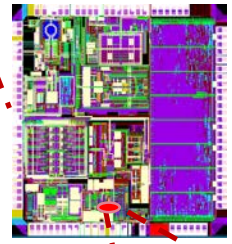
Industry chip company validation, debug and test technology

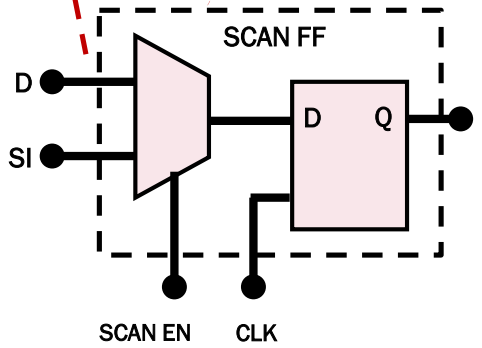
- *Platform hub controller (PCH)*
- *Memory (On Board DDR)*
- *Graphics eg VGA, HDMI, eDP*
- *High speed I/O(HSIO) eg PCIe, SATA, USB3*
- *Communication interfaces eg LAN, USB2*
- *I/O Peripherals eg keyboard, audio*

BIST using JEDEC STAPL/ IEEE SVF/Custom proprietary Language



1149.1





ASIC BIST tests are created for a board containing the ASIC under test using Company's Insert Source Language (ISL)

BIST vectors are converted to ISL custom tests

x1149 Hardware and Software fully capable to handle all complexities of various BIST – LBIST, MBIST, etc. with clear diagnostics.

Conclusions

- Boundary Scan as part of structural test (In Circuit Test) has been adopted for many years.
- Further enhancement to the IEEE 1149.1-2013 and IEEE 1149.6-2015 will broaden the structural and functional coverage of boundary scan into manufacturing.
- DFT, Test Coverage analysis and In Circuit Testtest point planning during design and prototype stage will further enhance the value of boundary scan.
- Boundary Scan beyond structural test such as Burn In, Board and System Functional, and Repair will further help broaden the proliferation of boundary scan while lowering the cost of test.