Managing the Diminishing Supply and Obsolescence of PCBs for Legacy Systems

William (Bill) Loving
ScanCAD International, Inc.
Littleton, Colorado

Abstract

Diminishing Material Supply (DMSMS) is defined as the loss or impending loss of manufacturers or suppliers of items or raw materials. Obsolescence refers to a lack of availability due to statutory and process changes, as well as new designs. DMSMS and Obsolescence adversely affect Total Life Cycle Management (TLCM).

As DMSMS and Obsolescence relate to printed circuit boards (PCB), there is an ever increasing need for maintaining spare and replacement boards for legacy systems that are operating well past their intended lifecycle. This is especially true in the transportation, medical, automotive, aerospace and military industries. Many times, the original manufacturer is no longer in business or no longer has the fabrication data. In these cases, there is the urgent need to precisely regenerate this manufacturing data from existing remaining parts, film, paper drawings, etc. Exact "Form, Fit and Function" is required so newly fabricated PCBs will "handshake" or integrate properly with existing systems and to avoid costly environmental or functional testing. Replacement parts that are not identical in all ways to the original parts must be treated as a new design, which is a very expensive and time consuming proposition.

There are many techniques that have been used to re-engineer PCB's. Each has distinct advantages and disadvantages. Some of the techniques covered in this paper are:

- Manual hand probing for Bill of Materials (BOM) and Net list generation,
- Optical and X-ray imaging systems for capturing connectivity and PCB geometry information.
- Flying Probe Test (FPT) and Bed of nails test systems for obtaining and validating connectivity information
- Techniques that create data in usable formats, and even permit information to be imported into Computer Aided Design (CAD) systems, etc.

Optical and X-ray images of internal PCB layers will be presented along with discussion about the pros and cons of each image acquisition process. Destructive and non-destructive techniques used for obtaining inner layer PCB information will be discussed.

The required manufacturing data formats such as Gerber/Drill data, IPC-2581, etc. can be generated using some of the PCB Re-engineering techniques that are presented in this paper. Other data formats required for board testing and repair, such as Net list (IPC-D-356A) and Schematics, will be covered in detail. In some cases, replacement components may no longer be available and some redesign may be needed which requires moving the data back into a CAD system. In addition, some organizations use these processes to "miniaturize" existing PCBs while maintaining existing functionality.

This paper provides a basic understanding of the various techniques for PCB Reengineering that are available today in support of addressing DMSMS and Obsolescence as they related to TLCM.

Introduction

A real life DMSMS story will clearly define why this topic is very relevant to our world today. A large power plant supplying power to the California grid tripped off line one day recently, the maintenance staff quickly isolated the problem and determined that the cause was the failure of a small insignificant PCB (one of many) in one of their control systems. They went to pull a replacement PCB from their local stores inventory at the plant. No stock. They immediately contacted their company wide stores… No stock. They initiated the emergency fall back strategy of contacting external suppliers and the original manufacturer. No stock and the OEM was no longer in business. What choices did they have? They must replace or repair the PCB quickly. Imagine actual cost of each minute that this plant was down. This scenario is playing out every day in most industries around the world and this is why it is important to share the information in this paper.

As DMSMS and Obsolescence relate to printed circuit boards (PCB), there is an ever increasing need for maintaining or repairing spare and replacement boards for legacy systems that are operating well past their intended lifecycle. This is especially true in the transportation, medical, automotive, aerospace and military industries. Many times, the original manufacturer is no longer in business or PCB repair or fabrication data can no longer be located. In these cases, there is a need to precisely reengineer (RE) this manufacturing data from existing remaining parts, film, paper drawings, etc. In some cases, the schematic is required in order to repair existing PCBs. In other cases, exact "Form, Fit and Function" is required in order to fabricate new replacement PCBs that will "handshake" or integrate properly with existing legacy systems. These replacement parts must be identical in all ways to the original parts.

There are many techniques that have been used to successfully extract working schematics and/or reengineer legacy PCB's. Some are destructive processes which require the original part to be destroyed as it is processed. Other processes are non-destructive. There are advantages and disadvantages to each technique.

- Manual hand probing to generate net lists
- Optical and X-ray imaging systems for capturing connectivity and PCB geometry information, and therefore net lists.
- Flying Probe Test (FPT) and Bed of nails test systems for obtaining net lists and validating connectivity information
- Data Interfaces to Computer Aided Design (CAD) and Computer Assisted Manufacturing (CAM) systems that permit schematic regeneration from net lists

In many cases, it is a combination of these techniques that provides the most thorough, cost effective and productive PCB RE solution.

The Need

It is without question that there is an ever increasing need for repairing and/or replacing PCBs in legacy systems. The fact is that many systems are being run long beyond their original design life. This reality is then combined with many factors that impact the ability to source spare parts. Each time the world experiences another economic roller coaster, more manufacturers and electronic suppliers file for bankruptcy or are absorbed into other companies. Many times the critical manufacturing and repair information for PCBs are forever lost. Data loss also occurs due to computer viruses, accidental or intentional data loss, incomplete disaster recovery scenarios, or simply technological evolution and obsolescence.

The fact is, the need for recreating or Reengineering or reverse engineering manufacturing and repair data from existing parts is rapidly growing. Each industry has third party companies that are dedicated to repairing and supporting obsolete legacy systems such as:

- Maintaining old switch equipment for telecommunications
- Test equipment for the semiconductor industry that is no longer supported
- Transportation systems (air traffic control systems, train and subway switch equipment, etc.)
- Aging nuclear and fossil fueled power plants
- Avionics going back over a half century
- Medical equipment that is being shipped to developing countries without support (X-ray, CT scan and MRI Imaging systems, etc.)
- Marine and automotive electronics
- Military and Defense systems of all sorts, etc.

Surprisingly, the problem includes even more simple systems such as sound systems and amplifiers for rock concerts, musical instruments, sprinkler control modules for irrigation systems… wherever you look, you will see aging electronics and the potential need to repair or replacement electronics. Electronics are at the core of most of the world's complex systems that are critical for daily operations.

Even the term "legacy" can sometimes be surprising. Some systems may be considered legacy or back level just a few short years after release, leaving the end user in a difficult predicament. Massive investments in equipment must be supported with spare parts, yet, the parts may not be available. What options are there for organizations in this situation?

When possible, legacy systems are retired and replaced prior to running out of spares. In some cases, it is possible to replace or upgrade a portion of a legacy system to "buy time". Many times, none of this is possible, and equipment must be repaired and maintained exactly as it is.

Most complex systems consist of a variety interrelated and interconnected PCBs. A collection of PCBs that must "hand shake" perfectly together for a system to operate properly. Over time, one or more of these PCBs fails and needs to be repaired or replaced. In many cases, a single component out of hundreds or thousands of components on a PCB may fail, causing a massive system to stop. In other cases, the substrate holding the components may have failed or have been damaged during a repair process. Components and boards can be damaged for many reasons including temperature, humidity, vibration, power fluctuation, insects/rodents, mistreatment, aging, accidents, etc. Regardless of the reason, a PCB has failed and it is now time to repair or replace.

If a new replacement PCB is desired, it is important to create an exact replica of the existing part. This is called "Precise Form, Fit and Function". The original performance characteristics must be precisely duplicated. The replacement board must have the identical electrical characteristics… Cross talk, RFI, EMI, SI, Delay, etc. All must be identical in order for the PCB to handshake properly with other PCBs in the system. In many cases, the replacement must even include original manufacturing "defects", drilled out traces (even down in inner layers), jumper wires or other oddities that impact electrical characteristics. Organizations must resist the urge to "improve" the board design. Any changes to the PCB, and therefore these characteristics, may or may not, create problems.

In the long run, it is best to exactly duplicate the original PCB for many reasons, including:

1. Lower total cost
2. Time savings
3. No need to recertify (UL, CE, FCC, FAA, etc.)
4. No need to perform environment testing
5. No need for system testing
6. No need for expensive and time consuming complete system redesign
7. Improve success rate and reduce risk of failure

These benefits are derived from the fact that a PCB can be recreated that is IDENTICAL in all ways to the original PCB, provided the same components can be identified and sourced. This is true for single, double sided and multilayer PCBs. It is critical that all other elements of the PCB remain identical as well including substrate materials, substrate thickness, conductor thickness, etc.

In some cases, organizations wish to improve on existing PCBs or to miniaturize or modify the PCB to accommodate new functions or handle problem areas, etc. In other cases, the design must be modified to utilize new component packages, for example changing from a through hole device to surface mount package, or allowing for a new style connector, new tooling/mounting holes, etc. Sometimes, it is even possible to eliminate jumper wires and other patches that were added to PCBs over the years, without changing the electrical characteristics of the PCB. Each situation is different and must be carefully managed.

Even if a PCB is to be modified, it is always best to reverse engineer the PCB all the way back to its original design. Perfect form, fit and function. Only then should the modifications begin, based on a foundational PCB that is 100% functional, tested and working which would give a predicable base line.

If an existing PCB is to be repaired, it is still advisable to perform a 100% reverse engineering process on the PCB. This process provides all of the data needed to repair or create a 100% identical replacement PCB. When this is not possible due to time or budget constraints, then techniques discussed in this paper will permit a Bill of Material (BOM) and schematic to be generated, which are the minimum requirements needed for PCB repair. In many cases, a replacement PCB cannot be fabricated from only BOM and schematic information, but existing PCBs can be repaired because the failing component can now be identified and replaced.

Why not just redesign a PCB for a legacy system from scratch? In many cases, the newly designed PCB will not play well with the other components or PCBs complex systems. Again, the PCB must be exact form, fit and function. It must be an exact replacement and behave 100% exactly like the original PCB.

The processes discussed in this paper do just that. Eliminating the need for recertification, system testing, etc. The goal is to be able to install the replacement PCB into the aircraft, automobile, medical device, nuclear power plant… and know with certainty that it will work as before… perfectly.

Is this being done today? Absolutely yes. As an example, if the reader of this paper has flown in the last 20 years, please know that the global air traffic control system is, for the most part, "legacy" equipment, and it is being maintained by the techniques covered in this paper!

The telephone switch equipment around the world that we all use today is kept running with these techniques. All techniques shared in this paper are in use today. The newest techniques include X-ray, CT scan and other nondestructive techniques.

The Inputs

What types of inputs are being used to reengineer PCBs today? Organizations must do with whatever is available for PCB reengineering. These include:

Design and/or Manufacturing Data:

Sometimes older or incomplete revisions of CAD, BOM or other manufacturing data (such as the Gerber data shown in Figure 1 below) are available. This can be a helpful start.

```
%FSLAX24Y24*%
%MOIN*%
%ADD11C,.0080*%
%ADD19C,.0400*%
%ADD70C,.0450*%
%ADD71C,.0500*%
%ADD22C,.0600*%
%ADD43R,.0600X.0300*%
%ADD45R,.0550X.0250*%
%ADD46R,.0250X.0550*%
%ADD92R,.0500X.0500*%
%ADD95R,.0600X.0600*%
%ADD96R,.0650X.0650*%
%ADD105R,.1000X.1000*%
G54D70*
X4300Y32300D02*
X31800D01*
Y4050D01*
X4300D01*
Y32300D01*
G54D11*
X12835Y31453D02*
Y31803D01*
X13085D01*
```

Figure 1: Gerber Data in text format

For example, a graphical image of Gerber data listed above can look like the following image in Figure 2 below:

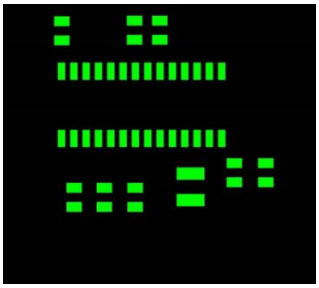


Figure 2: Gerber image

Phototools, Paper Drawings, Microfiche, etc.:

In some cases, PCB data can be found in the form of diazo, silver halide film or chrome glass that are all used as photo tools for PCB fabrication. There are still massive temperature and humidity controlled film archives located around the world where some PCB data is stored, some dating back 30 years or more. Also, PCB data has been recovered from paper drawings and has even been recovered from archived microfiche. Figure 3 below depicts what a photo tool might look like.

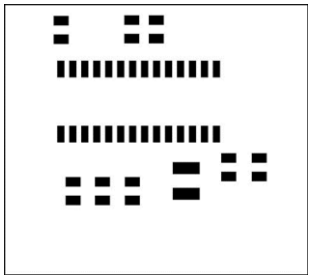


Figure 3: Photo tool image

Actual Printed Circuit Board:

In most cases, the actual legacy PCBs can be found. Even non-functioning PCBs can be very useful for reengineering. Ideally, more than one PCB remains, permitting some additional post re-engineering validation and verification processes to confirm the new data is correct.

The intent is to take the board and "re-engineer" it or take it back to the original manufacturing data, then, if desired, even move this data back up into a CAD system. Maybe the term reverse engineering is even more appropriate. Figure 4 below shows a picture of an actual populated PCB.

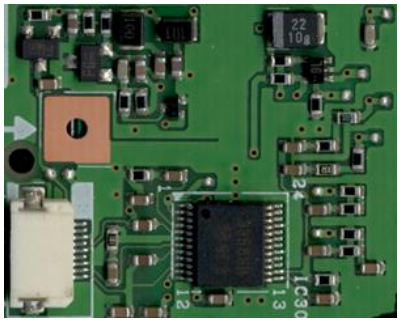


Figure 4: Populated PCB image

In some cases, bare PCBs may be located as well. Bare PCBs do not have components placed on them as shown in Figure 5 below.

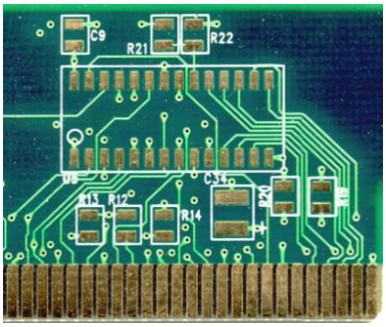


Figure 5: Bare PCB image

Solder Paste or Glue Stencils/Screens:

Other PCB manufacturing steps can include solder paste or glue stencils, component inspection templates or other aids and documentation used for PCB manufacturing. If any of these exist, they can also be used as complimentary INPUTS for reengineering. See Figure 6 image below:

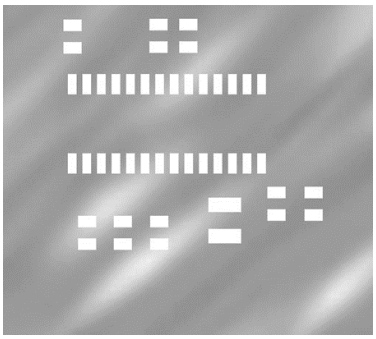


Figure 6: Solder Paste Stencil image

X-ray or X-ray CT scan:
Some organizations have access to sophisticated X-ray or X-ray CT (Computed tomography) scan technology that can be applied to PCBs. These images can also be combined with the other PCB RE INPUTS above to help reengineer a PCB. Please see Figure 7 and 8 below showing multilayer X-ray images.

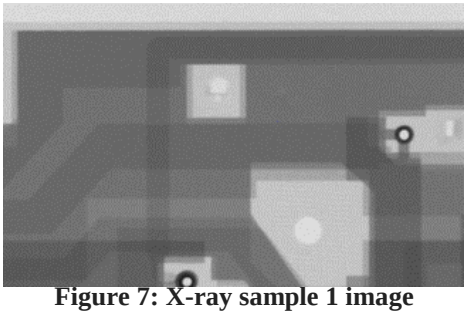


Figure 7: X-ray sample 1 image

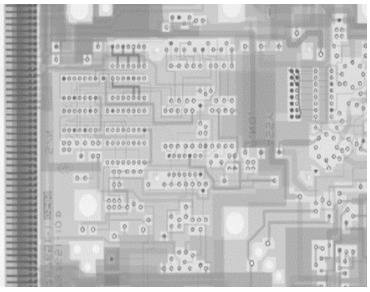


Figure 8: X-ray sample 2 image

The Process

A. Reengineering Technique: Nondestructive, Manual
The first technique discussed is the manual probing of the top and bottom of a PCB using basic test equipment.

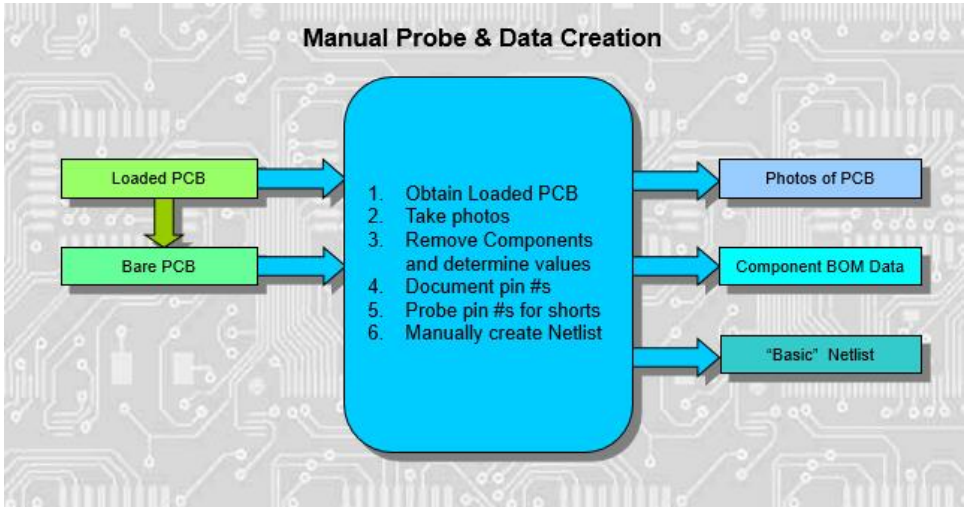


Figure 9: Manual Probe Flowchart

The above Figure 9 is a graphical or flow chart of a manual probe scenario. Note the process flow from loaded board to data which is top down and left to right in this flow chart. This can be highly error prone and time consuming. A complex board could take many man months of work. The resulting data is typically placed in spreadsheet software format. Validation using the resulting netlist on an electrical FPT or Bed of Nails tester is highly recommended, if not mandatory. The resulting data of this process is strictly a BOM and a Netlist. This data cannot be used to create fabrication data for a PCB that guarantees the same form, fit and function. The resulting netlist and BOM data can be used to create a schematic, and therefore as a PCB repair tool.

+ Low capital cost, ability to create basic netlist and BOM

- Very slow, high labor cost, error prone, no Form/Fit/Function

B. Reengineering Technique: Destructive, Automatic, Optical Imaging

This process is able to handle PCBs of all layer counts, from 1 to 20+ layers.

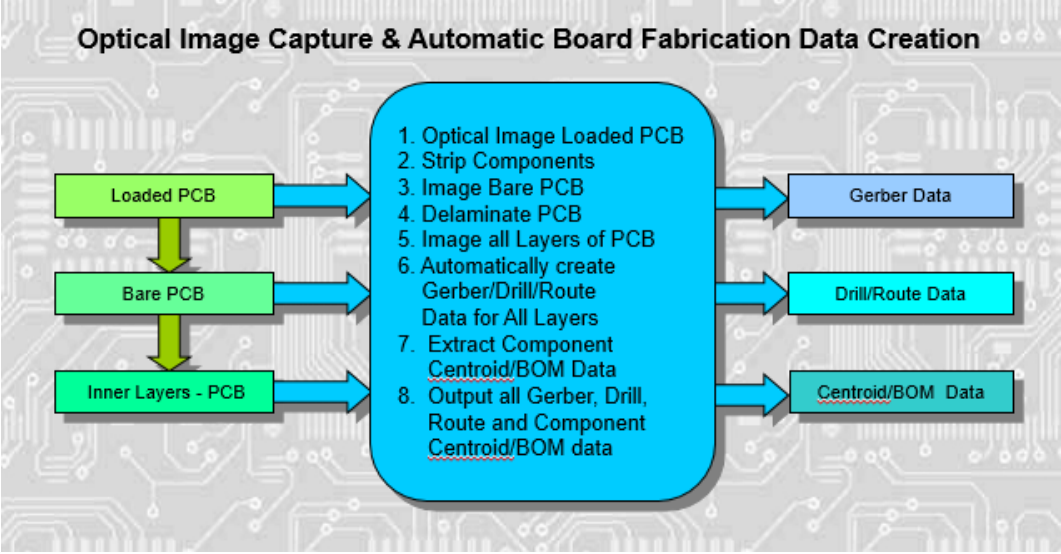


Figure 10: Optical Image Capture Flowchart

Output data from this process can be used to manufacture PCBs to exact form, fit and function, or it can be converted into Netlist data and on to a Schematic, as needed.

Figure 10 above is a graphical flow chart representation of the DESTRUCTIVE automated optical process, from populated PCB to form, fit and function PCB fabrication data using optical techniques. All features on and in the PCB are reproduced to the exact same physical characteristic. Using this process, creates exact Gerber Data and Drill and Route Files for Multilayer PCB's, supporting blind/buried vias, differential pairs, RF designs, microwave, etc. This is because the optical process recreates the data that was used to fabricate the PCB in the first place. Literally making an exact duplicate, right down to any original manufacturing defects.

With this technique, it is possible to take a visual tour down through a PCB using the images taken from each layer as the PCB was delaminated… one layer at a time. The following images show the process in action… the final image shows bright GREEN Gerber/CAD data generated for an inner layer automatically from the color image… this is a six-layer memory board for a laptop. Note the "differential pairs" needed for Signal Integrity (SI): these are 75 um (three mil) traces and spaces. Note the color imaging that this technique uses to look deep into a PCB.

Figure 11 below shows an image of the top of a bare PCB.

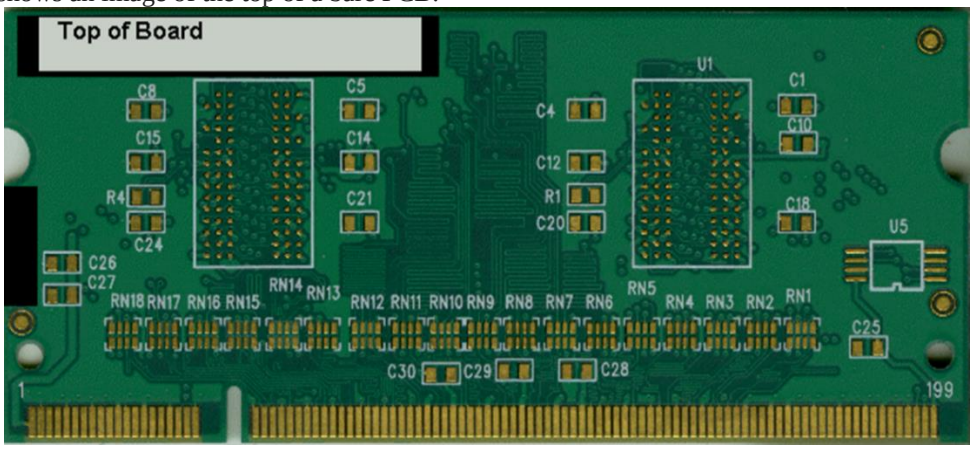


Figure 11: Bare PCB image

Figure 12 below shows an image of the same board with legend (silk screen) mechanically removed

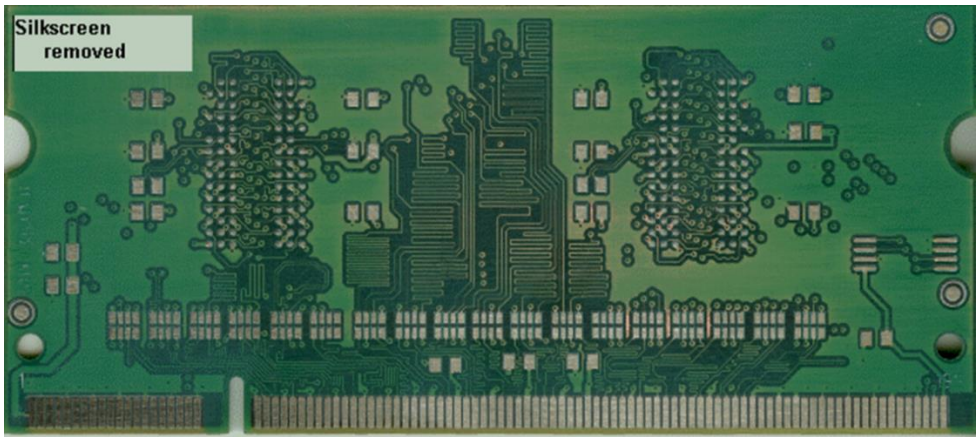


Figure 12: Bare PCB legend removed image

Figure 13 below shows an image of the same board with the solder mask mechanically removed showing the top circuit/signal layer.

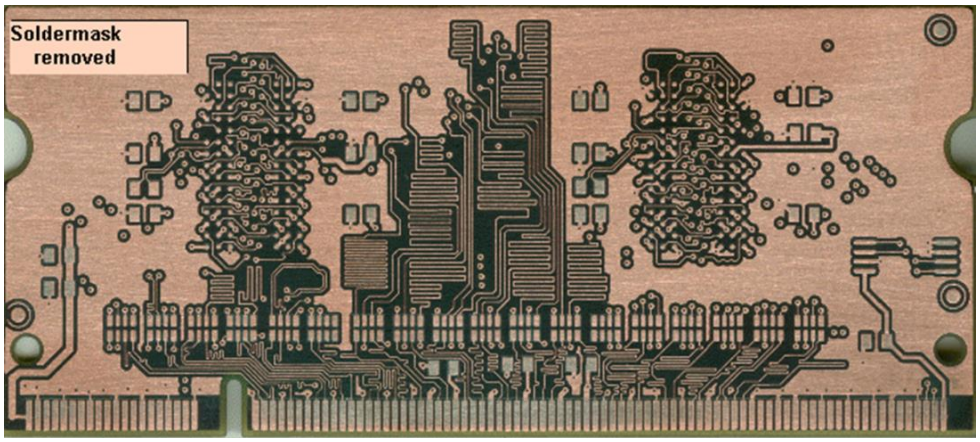


Figure 13: Soldermask Removed showing Top Circuit image

Figure 14 below shows an image of the same board with the top circuit layer mechanically removed showing the second layer of the PCB, in this case a power plane. Note the vias, isolated and otherwise.

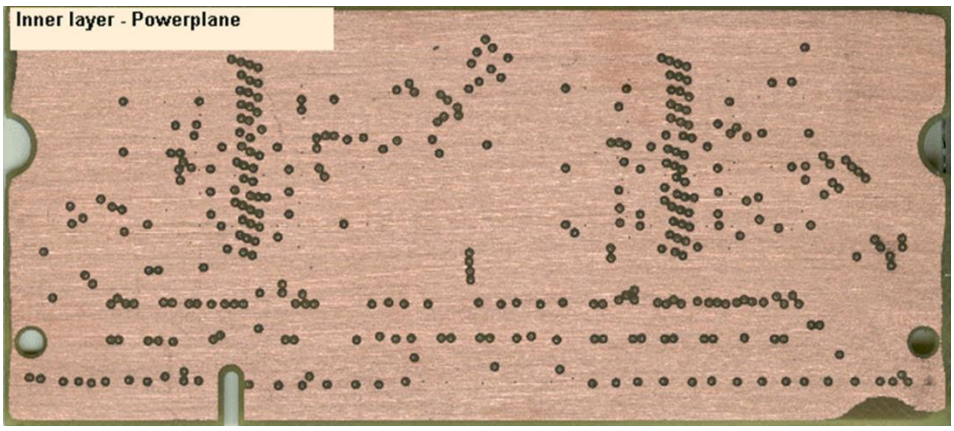


Figure 14: Top circuit removed showing Power plane image

Figure 15 below shows an image of the same board with the power plane mechanically removed showing the third layer of the PCB, in this case another signal layer.

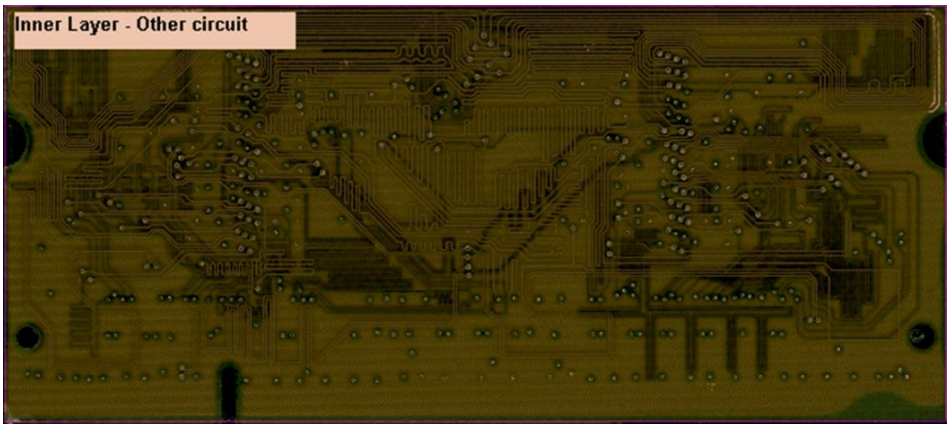


Figure 15: Power plane removed showing inner circuit layer image

Figure 16 below is an image of the same board with the inner signal layer mechanically removed showing the 4th layer of the PCB, yet another signal layer. Note the light color of the conductor.

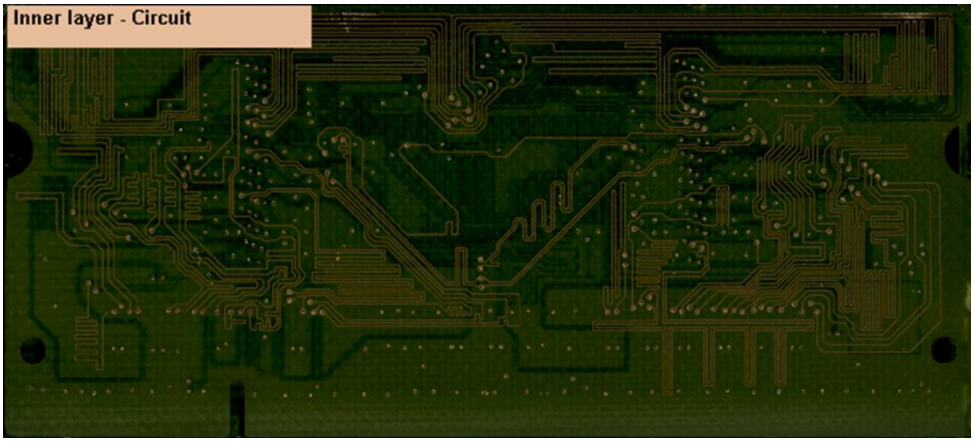


Figure 16: Next inner circuit layer image

Figure 17 below shows an image of the same inner layer with an overlay of CAD/Gerber data shown in bright green that was automatically generated for this image to cover the light colored conductor. The new CAD data identically matches the bitmap image.

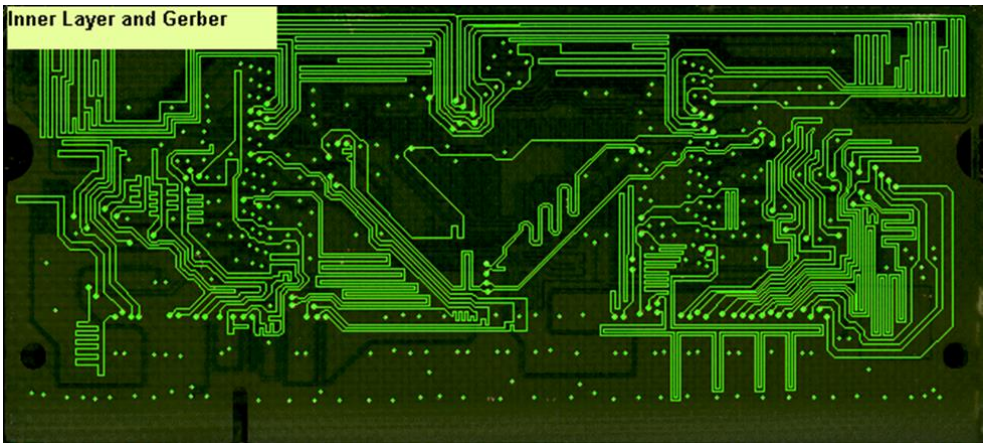


Figure 17: Inner Layer showing Gerber overlay image

There are a variety of delamination processes that can be used to delaminate a PCB such as the one shown in the images above. These include 100% mechanical techniques such as mechanical sanding and polishing, either manually or using orbital or detail sanders, automated CNC milling machines, chemical etching processes including ferric chloride as an etchant or micro milling machines specially designed for this type of delamination work. It is estimated that 90+% of the PCBs that are delaminated for reengineering globally are done using mechanical techniques. There are a variety of tools on the market that provide this capability.

+ Fast, low cost, low skill level operator, Form/Fit/Function, accurate

- PCB is destroyed

C. Reengineering Technique: Nondestructive – Bare Board FLYING PROBE TESTER

This technique uses a bare board Flying Probe Tester (FPT). The flow chart in Figure 18 below shows a representation of this process.

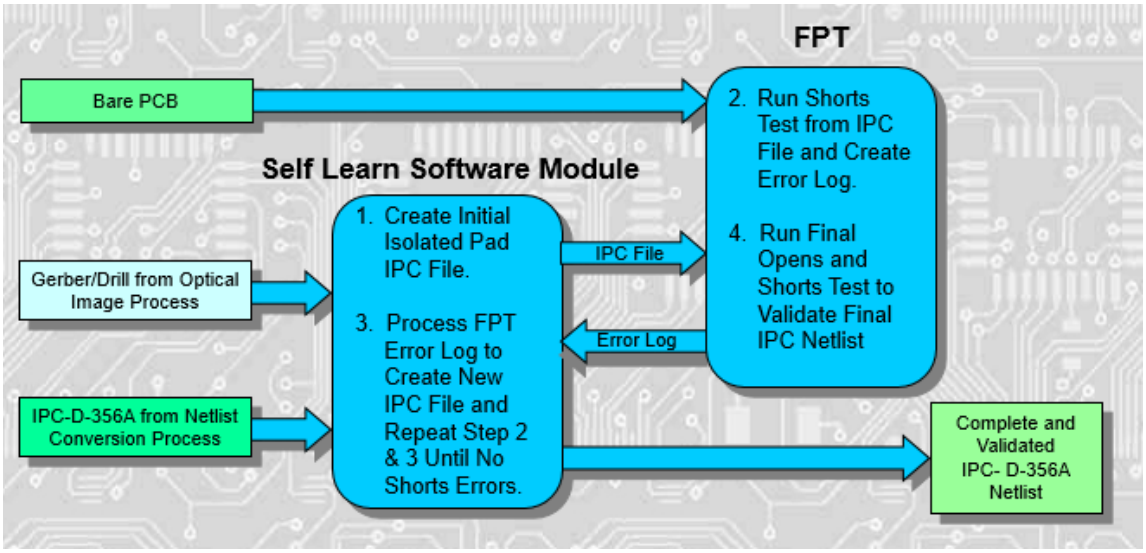


Figure 18: Bare Board FPT Self Learn Software Module Flowchart

A bare board FPT can be used to validate Gerber/Drill data created from the other PCB Re techniques (Hand Probe, Optical, X-ray, etc.) It is also possible to use the top and bottom Gerber and Drill data created from the optical technique to then run a self-learn process that will generate a Netlist without destroying the bare PCB.

There are three PCB reengineering techniques that use PCB electrical test equipment, bare board and populated board flying probe testers and bed of nails testers.

This first technique involves the use of a bare board Flying Probe Tester (FPT). FPT systems DO NOT NEED test fixtures. FPT systems use probes that move in three axis to carefully touch points on a PCB. The FPT does need to know where and what the test points are on both sides of the PCB. The bare board FPT can be used in a couple of different ways.

It can be used to create a netlist from the bare PCB using the four numbered steps shown on this flow chart. The FPT extracts the netlist from a bare PCB in a step by step process by performing a SHORTS ONLY or CAPACITANCE test on the bare PCB of all of the "isolated" pads, while allowing for drill diameters generated in the earlier processes. The probe must touch the conductor on the PCB and not drop into a hole. The resulting test data is then translated into a netlist. (Essentially the list of shorts indicates which pads are connected or, likewise, the list of isolated pads of similar capacitance may indicate that they are on the same net.)

The bare board FPT can also be used to independently validate the netlist created in earlier PCB RE scenarios. To do this, a complete IPC-D-356A netlist is loaded on the bare board FPT and the system is run as if the PCB was a new PCB being tested after fabrication, checking for both shorts and opens. (It is important to note that test adjacency must be set to size of the PCB to ensure that all test points are checked against all other test points. Adjacency is a standard FPT test parameter that indicates the maximum distance between nets for a test to be run.)

All three electrical tester techniques have a potential source of error when performing PCB RE on failed PCBs. It is possible that the PCB has experienced internal delamination. If this is the case, then plated through hole barrels may be broken creating an open that will translate to a net not detected by the tester. It is for this reason that it is recommended that these

electrical test techniques be complimented by the "optical" PCB RE techniques. Internal opens from damaged boards are detected using the optical technique and this type of error is avoided.

+ PCB is not destroyed

- Slow, capital expensive, error prone, no Form/Fit/Function

D. Reengineering Technique: Nondestructive – Bed of Nails Tester

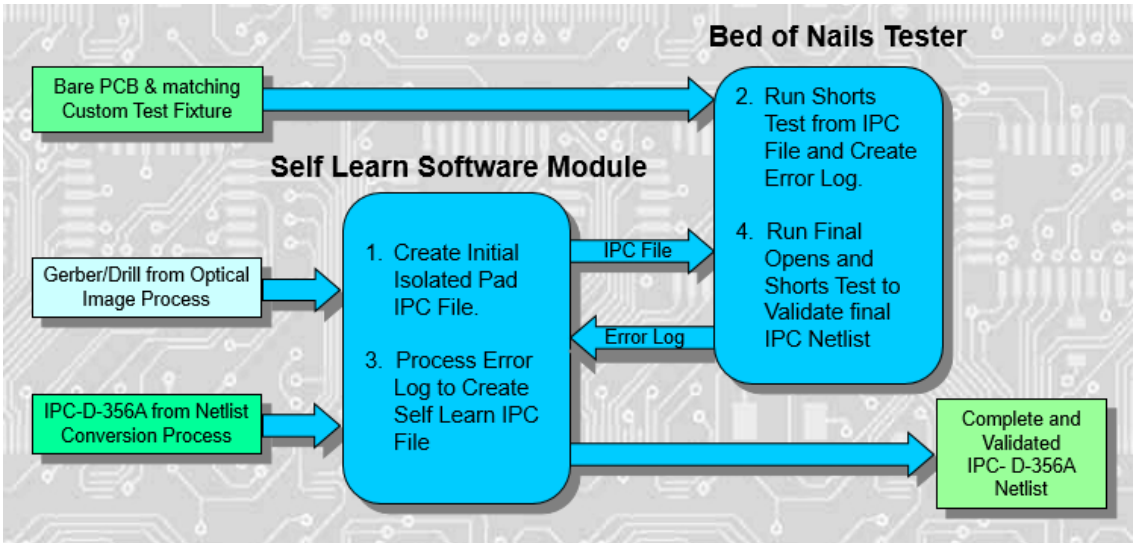


Figure 19: Bare Board Bed of Nails Tester Self Learn Flowchart

The second electrical test technique is similar to a FPT. It is called a bare board Bed of Nails (BON) electrical tester. The Figure 19 above shows a graphical representation of this process.

As with the FPT, it can be used to validate Gerber/Drill data or to generate a self-learn netlist (shorts and/or capacitance). The top and bottom Gerber and Drill data from the other techniques can be used to fabricate a custom test fixture that is required for the Bed of Nails Tester. The PCB is not destroyed.

It is important to note that BON systems REQUIRE test fixtures to be built for each PCB. This is an additional cost that must be considered with this technique.

+PCB is not destroyed

- Fast, if the user has access to a test fixture, capital expensive, error prone, no Form/Fit/Function

E. Reengineering Technique: Nondestructive, Populated Board Flying Probe Tester

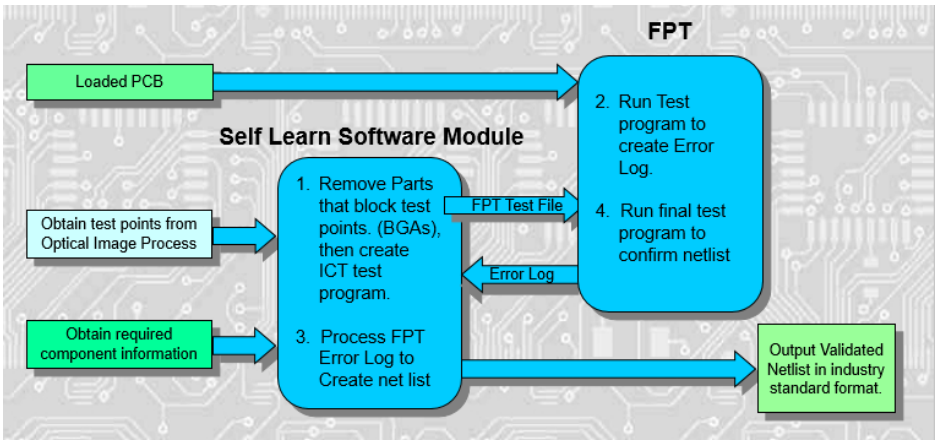


Figure 20: Populated Board FPT Self Learn Flowchart

The third electrical test technique using a populated or loaded board FPT. As with the other two electrical test solutions, it can be used to either validate netlist data, or to run a self-learn process that will generate a Netlist without destroying the populated PCB. See Figure 20 above for a graphical representation of this process.

This technique involves the use of a populated board Flying Probe Tester (FPT). Again, FPT systems DO NOT NEED test fixtures. This tester can be used two different ways... First, the FPT can be used to create a netlist from a populated or a bare PCB. Using the four numbered steps shown in this Figure, the process is able to use a FPT to extract the netlist from a populated or bare PCB in a step by step process by executing a custom created test program that understands all of the component characteristics on the PCB, including using special techniques to isolate certain devices or provide power to other devices, etc. When testing populated PCBs, the probes must be able to carefully come in contact with component leads or test points that provide access to all hidden leads. Probing populated PCBs can be extremely time consuming and expensive, but, it is possible in many cases, provided there is access to all device leads. NOTE: This can be a problem for BGA packages where all leads are hidden from the tester. A netlist can be generated from the resulting test data. Next, as with the earlier tester scenarios, the FPT can also be used to independently validate the netlist created in earlier scenarios as well as be used as a test machine for PCBs after repair.

+ PCB is not destroyed; system can be used to test populated PCBs after repair

- Slow, very capital expensive, error prone, no Form/Fit/Function

F. Reengineering Technique: Destructive, Automatic Optical with X-ray

Output data from this process can be used to manufacture PCBs to the exact form, fit and function, or be converted into Netlist data and on to Schematic, as needed. It could be difficult or impossible to create data for inner layers, based on the quality and dimensional integrity of X-ray images. Electrical test data validation is strongly recommended.

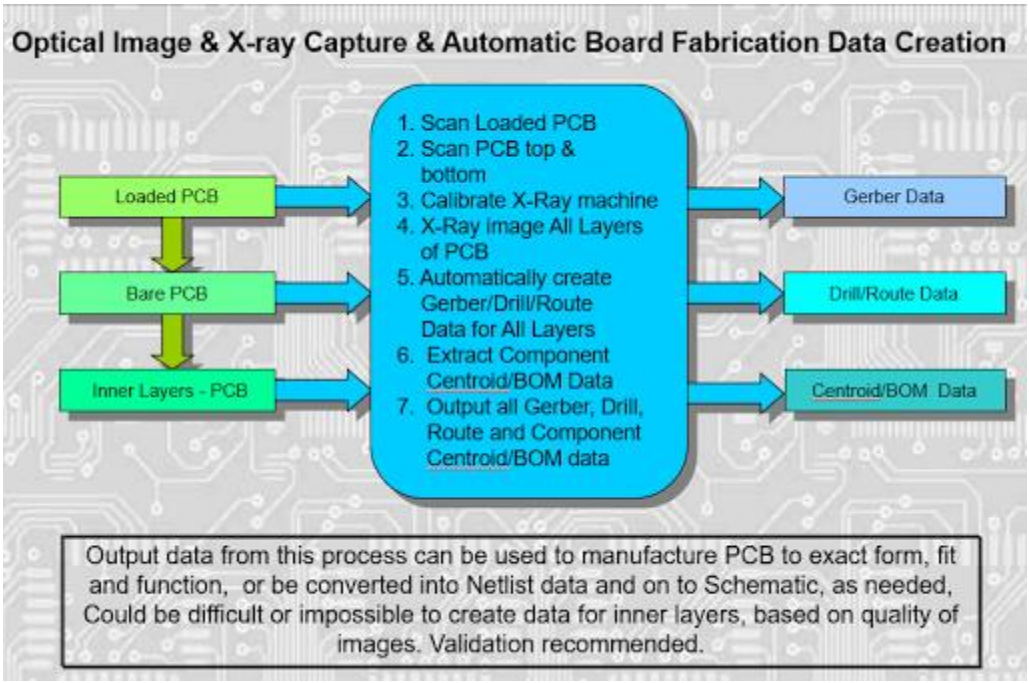


Figure 21: Optical and X-ray Combination Flowchart

Figure 21 above is a graphical or flow chart representation of integrating X-ray and the Optical method. X-ray for the inner layers, Optical for the top and bottom layers of the PCB. By doing so, the legend, silk screen, solder mask, and non-plated through hole information is captured as well as the dimensional integrity of the RE process is locked in. X-ray systems typically do not hold tight dimensional tolerances, so the inner layer X-ray images are then "referenced" to the top and bottom layer images that are dimensionally correct. The benefit of this approach is that the PCB does not need to be destroyed.

X-ray has inherent issues regarding lead. Populated PCBs can have lead solder which absorbs the X-ray energy and creates "blind" areas in the images. It may be necessary to complement this strategy with some manual probing to confirm what is

taking place in the blind areas. This is one reason that we share that this technique is error prone and requires careful validation.

+ PCB is not destroyed, Form/Fit/Function

- Slow, most expensive, new technology, error prone

G. Independent Validation Technique: Optical + PROBING Scenario with two PCBs

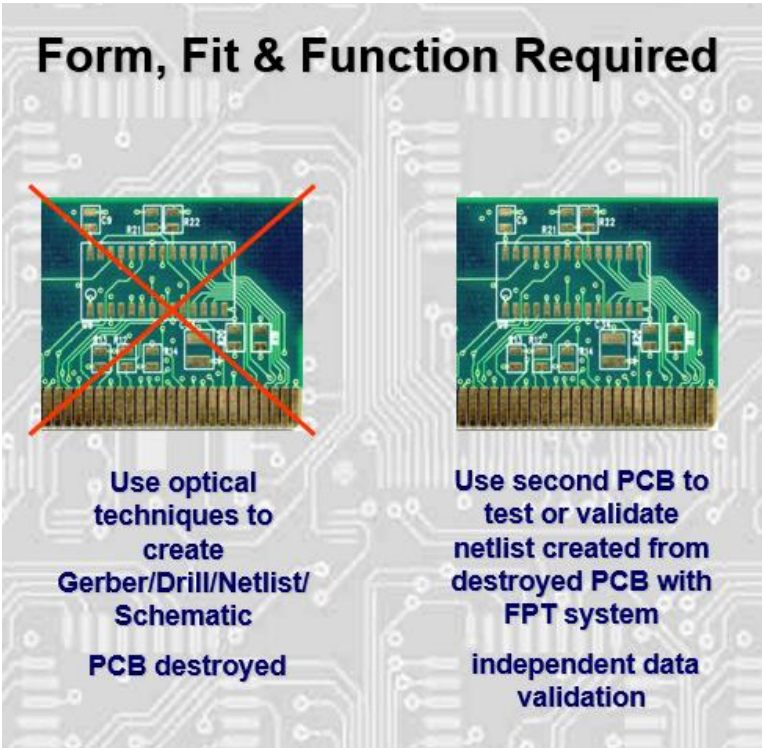


Figure 22: Two PCB with Independent Validation Scenario

PREFERRED SCENARIO… If the organization is able to obtain two PCBs, this is the most desired combination PCB RE and VALIDATION scenario. Again, the first PCB is used to create all of the needed data. The second PCB is used to independently validate the netlist that was created from the first PCB. If there are any discrepancies, the process permits the ability to research the connections in question and identify the error in the high quality optical images that have been captured for every layer of the PCB.

Advantages

- **Preferred method**
- **Quickest**
- **Least effort required**
- **Safe, Accurate Independent Data validation**
- **Supports correct form, fit and function**

Disadvantages

- **Requires minimum of 2 PCB's if validation is desired**
- **1 PCB is destroyed**

H. Independent Validation Technique: Optical + PROBING Scenario with one PCB

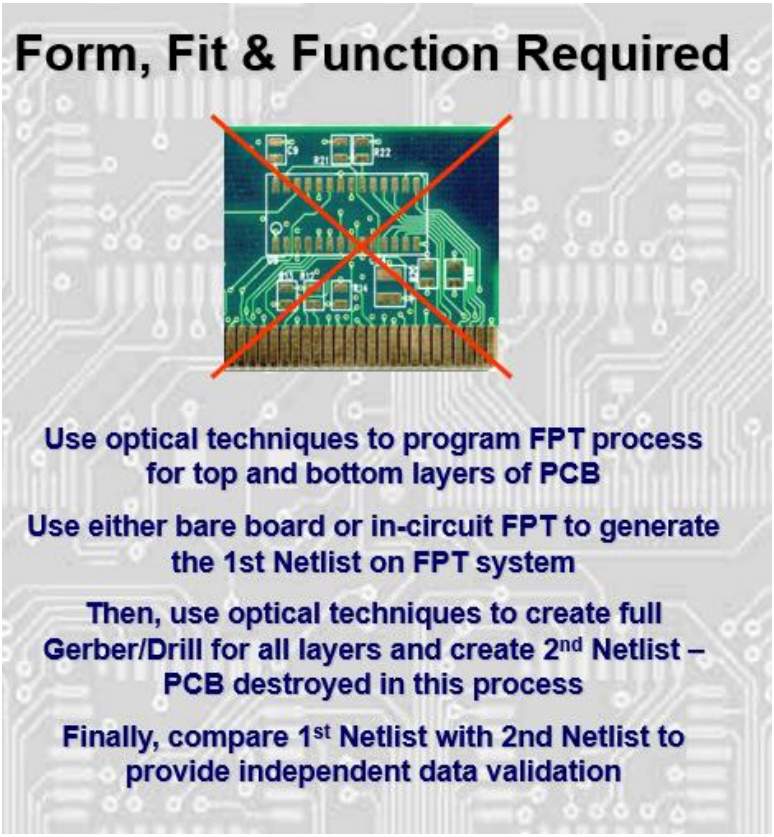


Figure 23: Single PCB with Independent Validation Scenario

The scenario shown in Figure 23 above provides for independent netlist validation, when there is only 1 PCB. It takes time, but the quality and peace of mind knowing that there is an independent netlist validation can be worth it, especially if there is only one remaining PCB in existence. Two independently created netlists are used to validate the data for a single PCB.

Advantages

- **Works with one PCB**
- **Independent validation of Netlist data**
- **Supports correct form, fit and function**
- **Life saver for "last board in the world" situation**

Disadvantages

- **Potentially long processing time**
- **PCB is destroyed**
- **Most effort required**

I. Independent Validation Technique: Optical + X-ray + Probing Scenario with one PCB

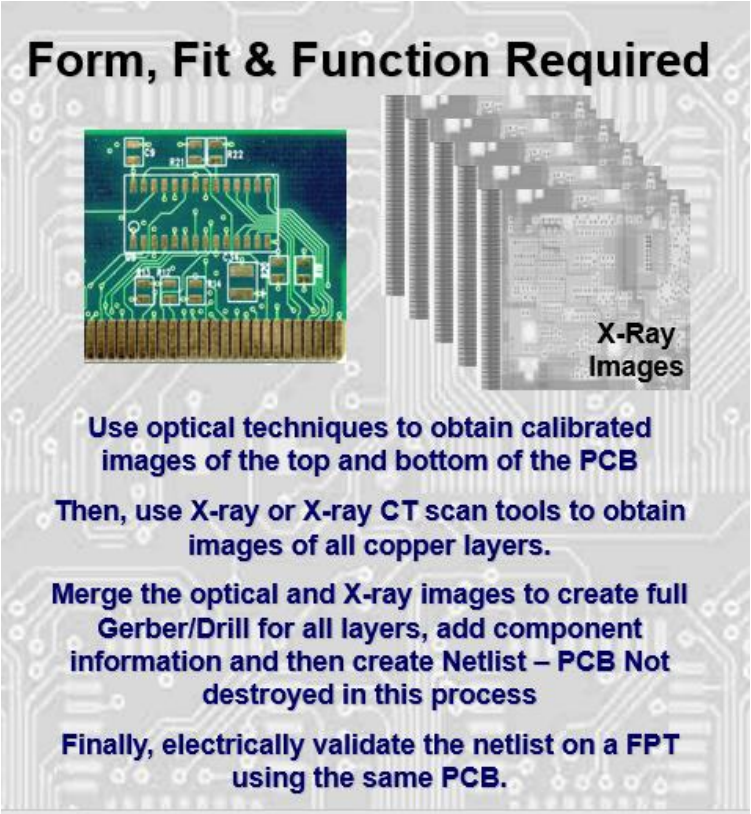


Figure 24: Single PCB with Optical, X-ray with Independent Validation

Advantages

- **Works with one PCB**
- **Validation of Netlist data**
- **Supports correct form, fit and function, if images are high quality**
- **PCB is not destroyed**

Disadvantages

- **Most expensive**
- **Image quality issues**
- **Form, Fit and Function may be error prone, if images are not high quality or if X-ray has dimensional issues**

J. Verification Technique: Optical + PROBING Scenario with one PCB

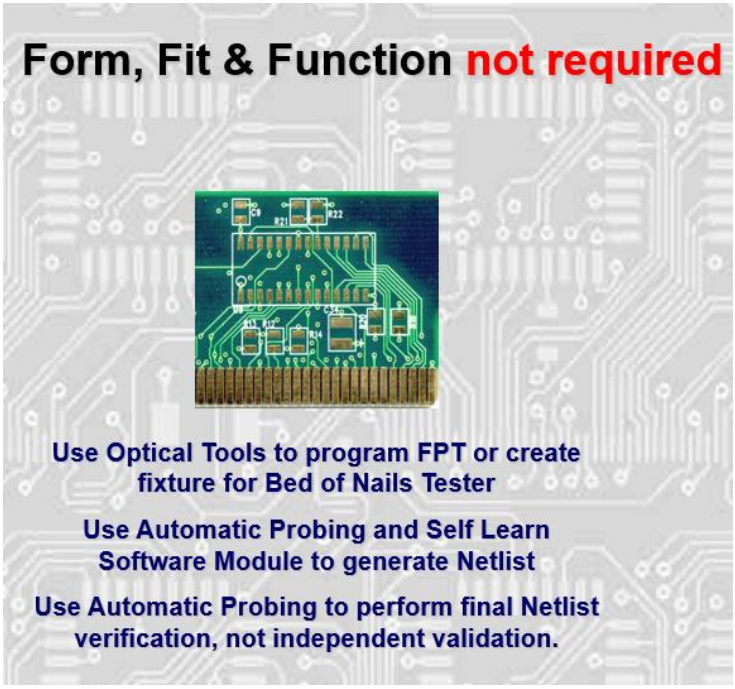


Figure 25: Single PCB without Independent Validation

Advantages
- **Works with one PCB**
- **PCB is not destroyed, but can be damaged if using FPT for probing**

Disadvantages
- **If FPT, possible long processing time, BON or capacitance testing is faster**
- **Possible errors (broken PTH barrels, damaged pads, test errors, etc.**
- **No independent data validation as with two PCB's**
- **No internal form, fit, shape information available**

K. Reengineering Technique: Net list Data Conversion

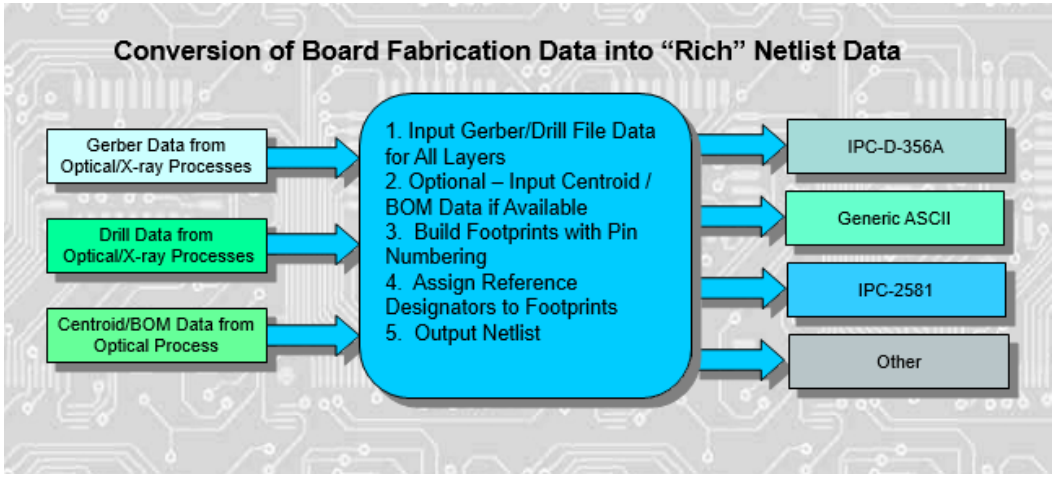


Figure 26: Net List Data Conversion Flowchart

Output data from the Image process can be converted into "rich" netlist formats to be used for form, fit and function PCB Fabrication, input for Schematic Generation and/or be used as input for the nondestructive Automated Probing process. (Off line programming for either bare board or in circuit FPT testers or fixture fabrication data for Bed of Nails tester.)

This flow chart shares how data from earlier processes are enhanced using Data Conversion to add pin numbering, footprint creation and netlist outputs as shown. There are a variety of tools on the market that provide this capability.

NOTE: The IPC-2581 format is the relatively new IPC industry standard for a comprehensive rich netlist format. This was released as a vendor neutral option to the previous proprietary formats that are in common use today.

L. Reengineering Technique: Schematic Data Conversion

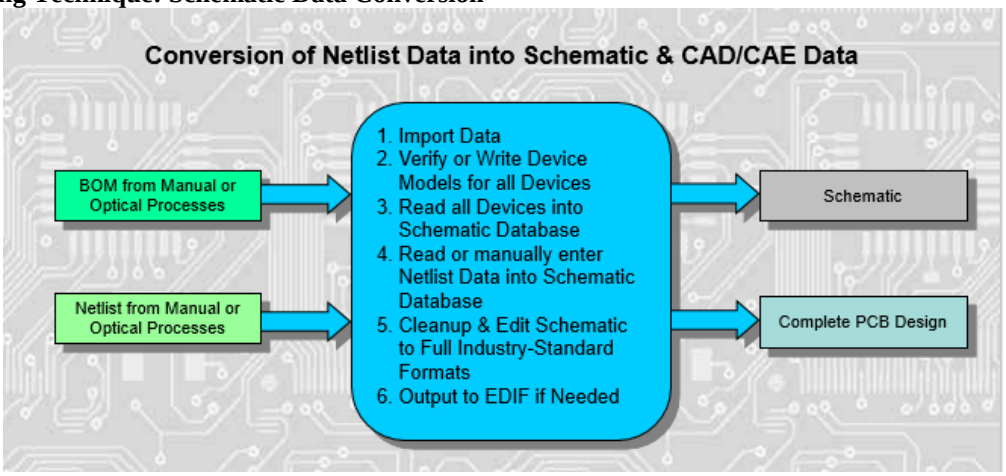


Figure 27: Conversion Schematic Data Conversion Flowchart

Netlist and BOM data can then be used to generate the schematic and possibly even the complete PCB layout in a CAD/CAE environment.

If schematics are needed, this flow chart shows how data from earlier steps are merged and manipulated to create high quality schematics. There are a variety of tools on the market that provide this capability.

The following examples of schematics show what is possible using these techniques:

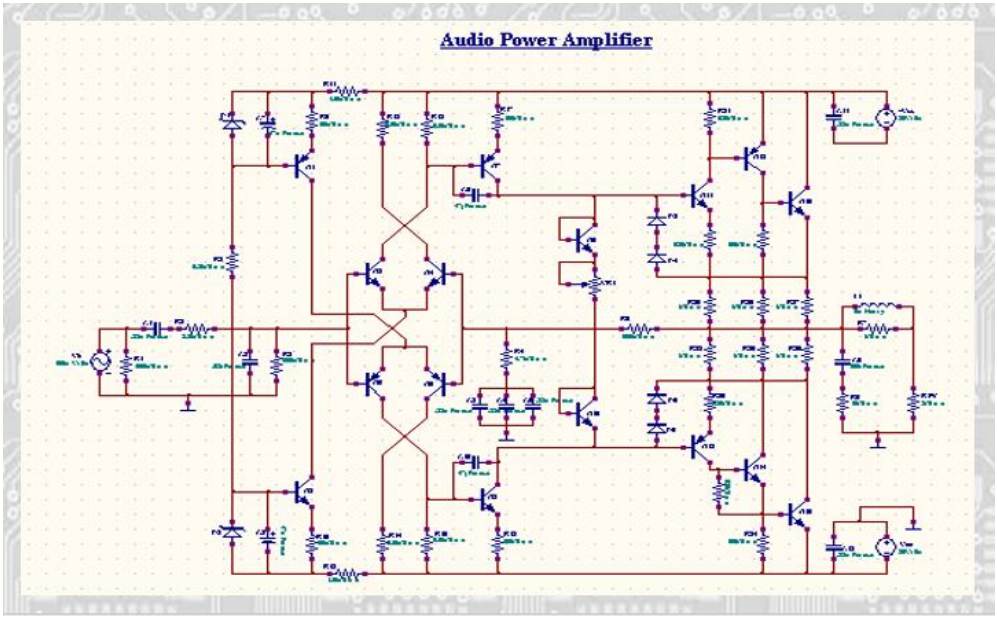


Figure 28: Schematic sample 1 image

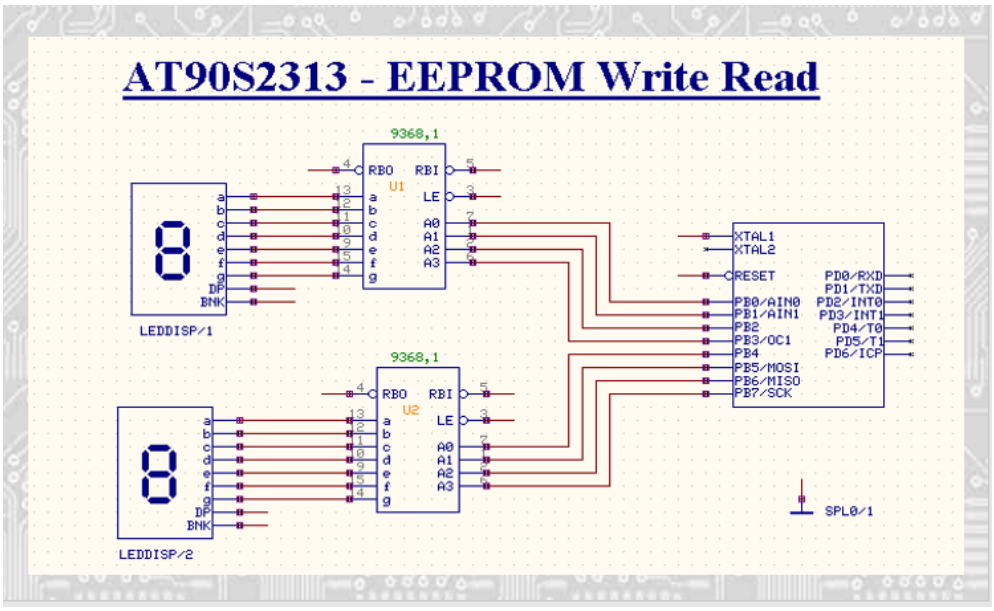


Figure 29: Schematic sample 2 image

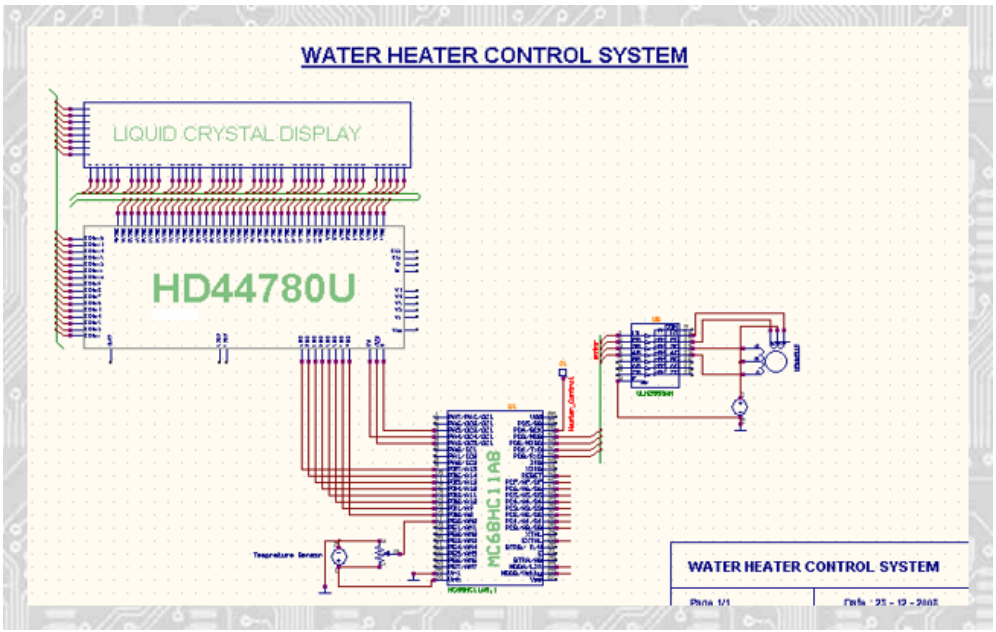


Figure 30: Schematic sample 3 image

Conclusions

The need for managing (repairing and/or replacing) PCBs in legacy systems is increasing globally at a rapid rate given the fact that these systems are being operated well past their intended lifecycle and spare parts and designs are no longer available.

Fortunately, there are a number of proven techniques that precisely regenerate or reengineer manufacturing data from the existing remaining PCBs, photo tools and/or other input sources. Both destructive and nondestructive techniques were covered. The resulting high quality schematics and CAD data permit the repair of remaining existing PCBs, and/or, the ability to fabricate new PCBs that have the exact "Form, Fit and Function" needed to "handshake" or integrate properly into these critical legacy systems. The new replacement parts can be fabricated to be identical in all ways to the original parts, since they are exact replicas of the original parts.

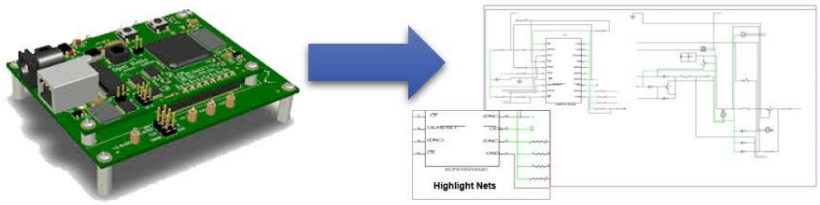


Figure 31: PCB to Schematic image

The following techniques were covered:

- Manual hand probing for net list generation
- Optical and X-ray imaging systems for capturing connectivity, net list and PCB geometry and manufacturing information
- Flying Probe Test (FPT) and Bed of nails/ ICT test systems for obtaining net list and validating connectivity information
- Data Interfaces to Computer Aided Design (CAD) and Computer Assisted Manufacturing (CAM) systems that do schematic regeneration from net lists

As discussed, it is a combination of these techniques that provides the most thorough, cost effective and productive solution.

Finally, the strong recommendation that electrical testers be used to VALIDATE or VERIFY the reengineered data is correct. There are a variety of methods for performing this validation, based on the number of available PCBs and access to electrical testers. In all cases, it is recommended that there be an INDEPENDENT validation of the data. Surprisingly, this is even possible with a single remaining PCB. As discussed, using clever techniques, the single PCB can be used to create two independent netlists that can be compared and used for data validation.

Organizations can move forward with confidence when maintaining and supporting PCBs for their mission critical legacy systems. If we go back to the story of the power plant in the introduction, they used a combination of the techniques described in this paper and were up and running again in less than 72 hours. They, and maybe your organization, do not have a choice. They must repair or replace the PCB, period, no matter the cost.

Managing The Diminishing Supply & Obsolescence Of Pcbs For Legacy Systems

William (Bill) Loving

ScanCAD International, Inc.

Diminishing Material Supply (DMSMS) *is defined as the loss or impending loss of manufacturers or suppliers of items or raw materials.*

Obsolescence *refers to a lack of availability due to statutory and process changes, as well as new designs.*

DMSMS and Obsolescence adversely affect Total Life Cycle Management (TLCM).

Why is this relevant today for PCBs…? The real life story of the California Power Plant…

The NEED:

- **Legacy Product Challenges**
- **Why Re-Engineer Legacy Products**

The PROCESS (INPUT – PROCESS – OUTPUT)

- **Non-Destructive**
- **Destructive**
- **Combination of both**
- **Pros & Cons**

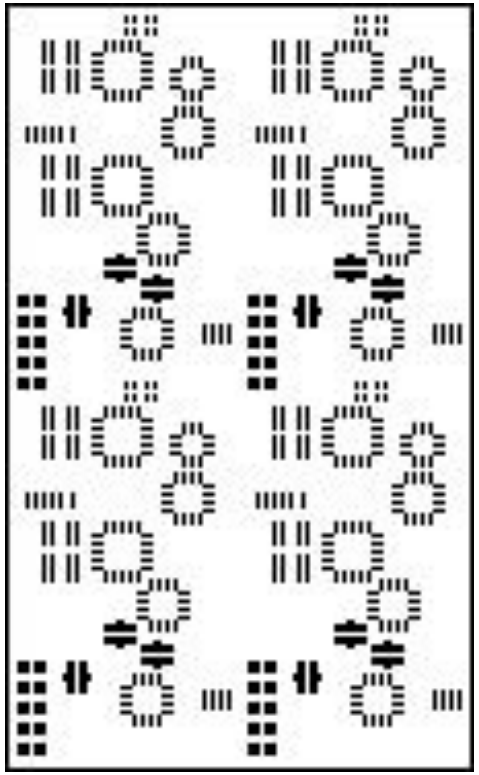
Validation & Verification

Conclusion

Q&A

THE NEED:

- **Missing Manufacturing Data (CAD, Gerber, Drill, PCBA, Test, etc.)**
  - **Lost, corrupt or partial data**
  - **Old photo tools, drawings, microfiche, etc.**
  - **No test data**
  - **No schematics for repair**
- **Original supplier not available**
  - **Out of business, merged**
  - **Discontinued product or components**
- **Diminishing inventories of spare parts**
  - **Products are being run beyond their planned life cycle**
- **Growing demand for maintaining Legacy products & systems**
  - **Must keep legacy systems operating…**



Need Exact Replica of Existing part

- Precise Form, Fit and Function
- Duplicate original performance characteristics
  - Cross talk, RFI, EMI, SI, Delay, etc.

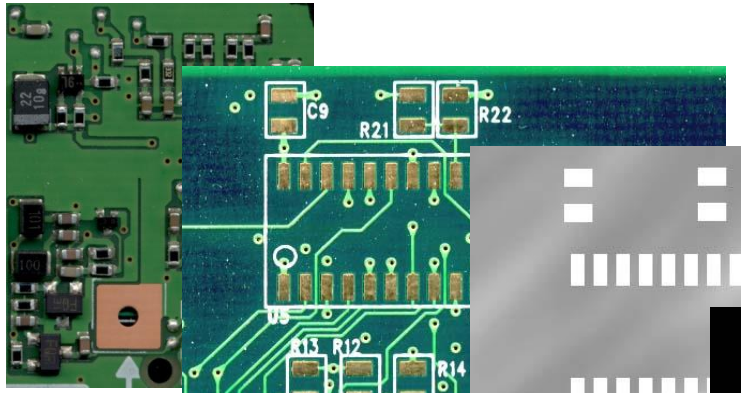
Lower Cost & Save Time

- No need to re-certify (UL, CE, FCC, FAA, etc.)
- No need to perform environment testing
- No need for system testing
- No need for expensive complete redesign

Repair or Improve on existing part

- Need for accurate schematic & Bill of Material
- Miniaturize, Modify and/or improve design
- Utilize new components, substrates, etc.

INPUT:



PCB

Bare PCB

Gerber

Stencil

Film / Paper

X-ray or CT scan

```
%FSLAX24Y24*%
%MOIN*%
%ADD11C,.0080*%
%ADD19C,.0400*%
%ADD70C,.0450*%
%ADD71C,.0500*%
%ADD22C,.0600*%
%ADD43R,.0600X.0300*%
%ADD45R,.0550X.0250*%
%ADD46R,.0250X.0550*%
%ADD92R,.0500X.0500*%
%ADD95R,.0600X.0600*%
%ADD96R,.0650X.0650*%
%ADD105R,.1000X.1000*%
G54D70*
X4300Y32300D02*
X31800D01*
Y4050D01*
X4300D01*
Y32300D01*
G54D11*
X12835Y31453D02*
Y31803D01*
X13085D01*
```

Gerber-274X Output

PROCESS:

Manual Probing of top & bottom of PCB

+ Low capital cost, ability to create basic Netlist & BOM
- Very slow, high labor cost, error prone, no Form/Fit/Function

Destructive Optical Imagining of PCB (all layers)

+ Fast, low cost, low skill level operator, Form/Fit/Function, accurate
- PCB is destroyed

Non-Destructive Automated Probing of top & bottom of PCB

+ PCB is not destroyed
- Slow, capital expensive, error prone, no Form/Fit/Function

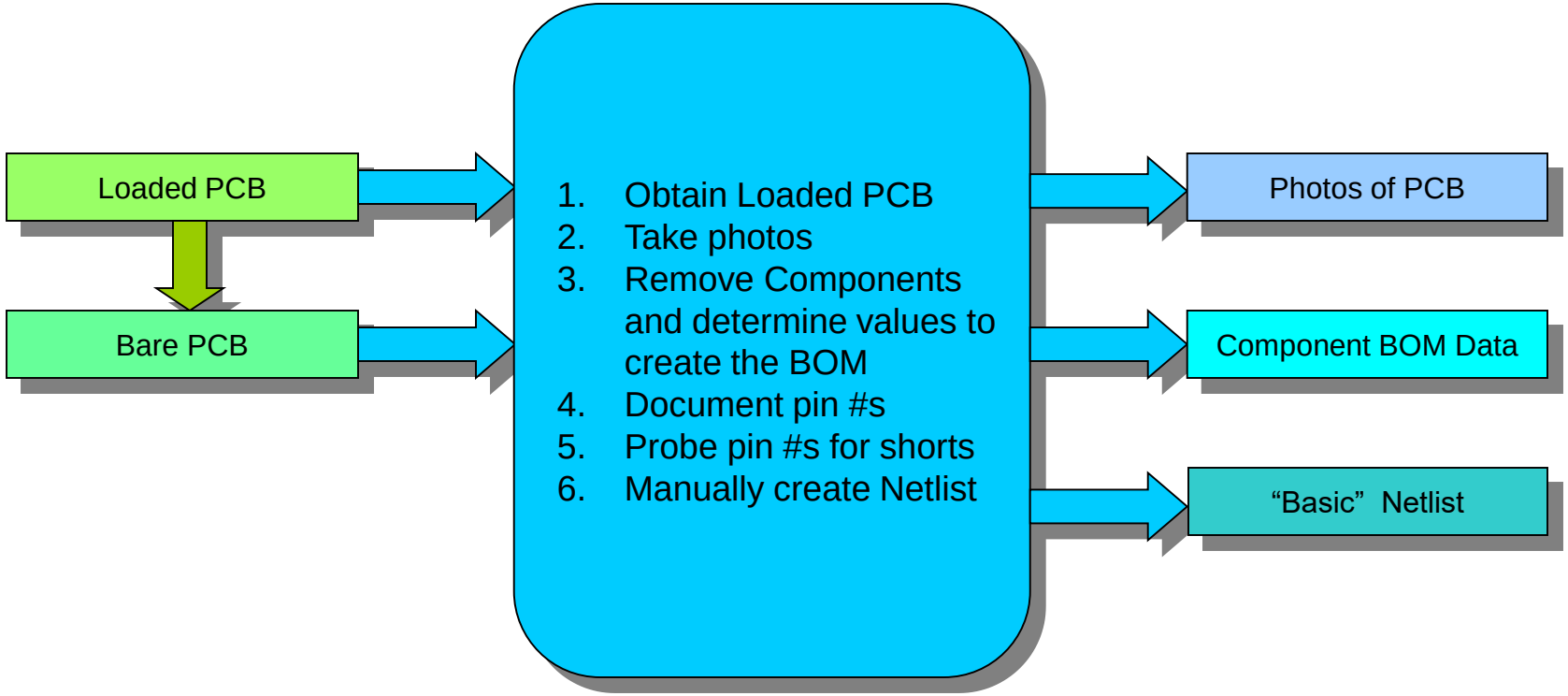
Non-Destructive X-Ray imaging of PCB (all layers)

+ PCB is not destroyed, Form/Fit/Function if paired with optical
- Slow, most expensive, new technology, error prone

Combination of above

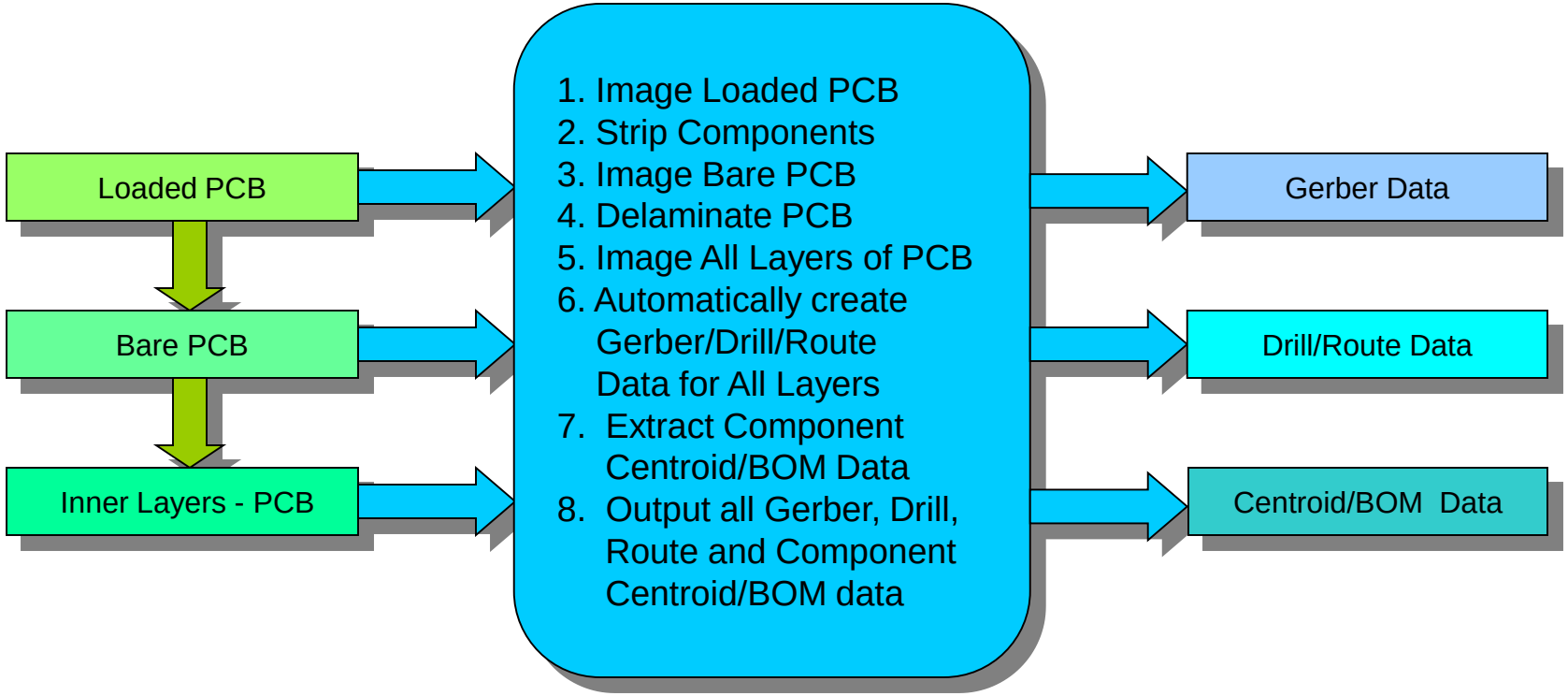
- Must have optical imaging for offline programming & accuracy
- Permit independent data validation from two sources

Manual Probe & Data Creation



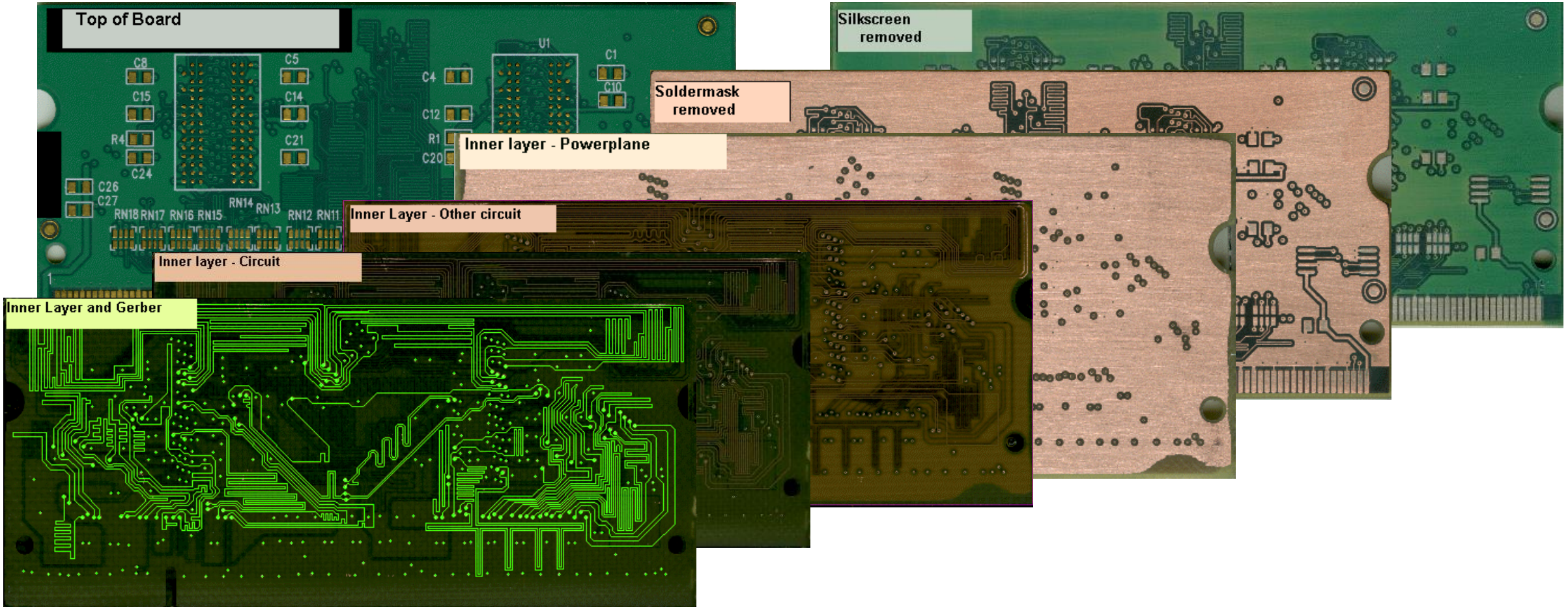
Basic pin # to pin # Netlist data from this manual process can be used to manually build a BOM and a schematic.

Optical Image Capture & Automatic Board Fabrication Data Creation



Output data from this process can be used to manufacture PCB to exact form, fit and function, or be converted into Netlist data and on to Schematic, as needed

- **Create Gerber Data and Drill Files for Multilayer PCB's**
- **Supports blind/buried vias, differential pairs, etc.**



PCB De-Lamination Techniques for PCB RE

Stand-alone Integrated Workstations:

- **Delaminates PCB's – Destroys dielectric with no damage to copper**
- **Can also be used to remove conformal coatings**
- **Quick, quiet, safe and easy to install and use**

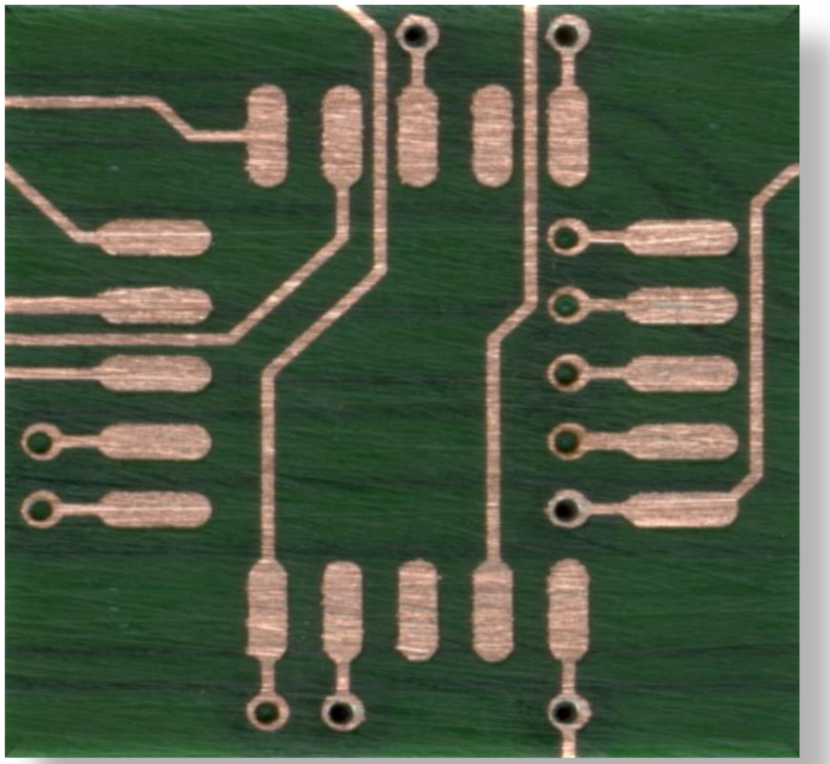
Manual Processes

- **Sanding using block or electric detail sanders**
- **Low cost, effective, easy to learn**

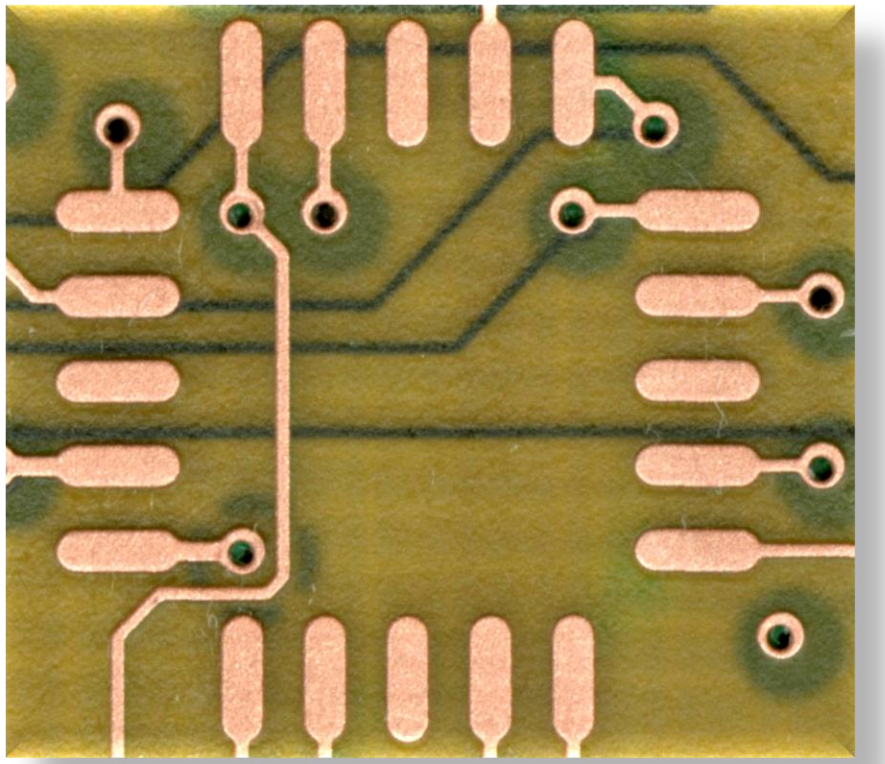
Chemical Processes

- **Stripping and etching processes**
- **Operational & disposal considerations**

Comparison of two Delamination Techniques

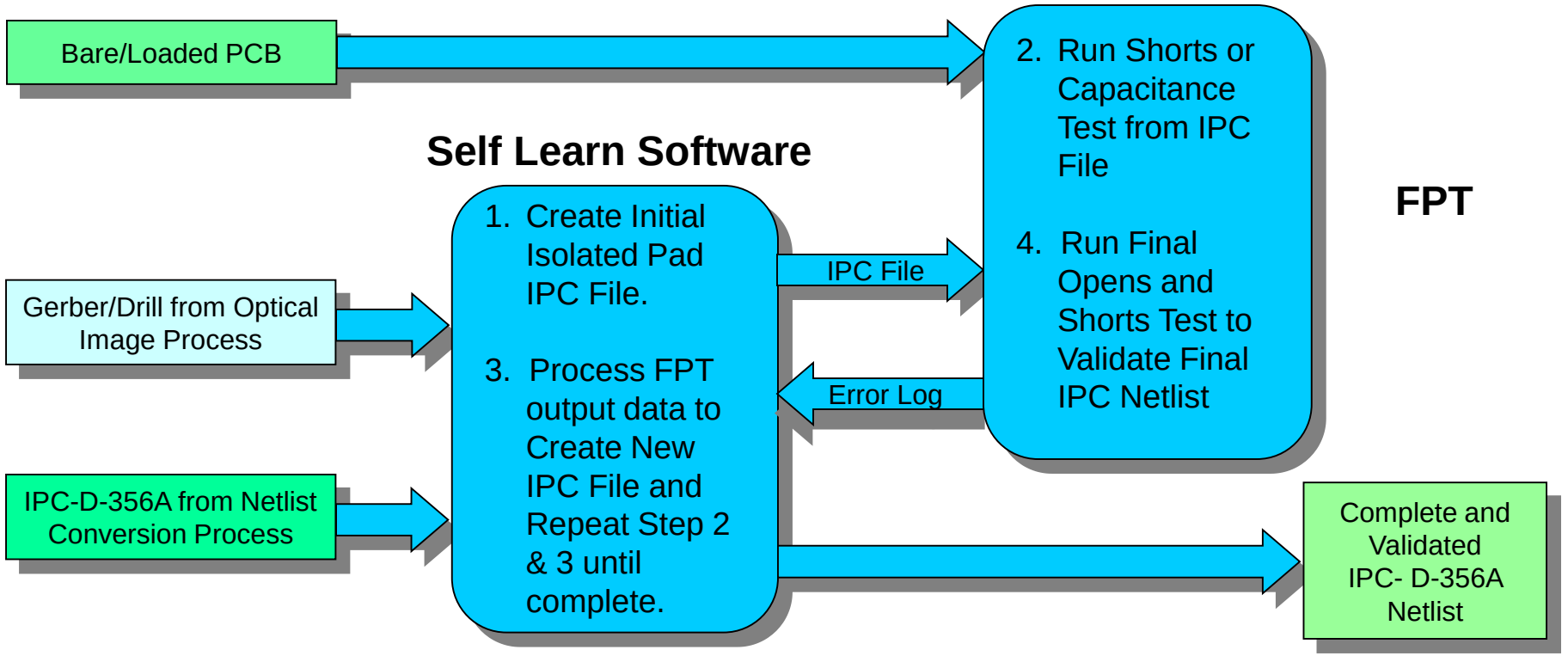


Manually Sanded Board



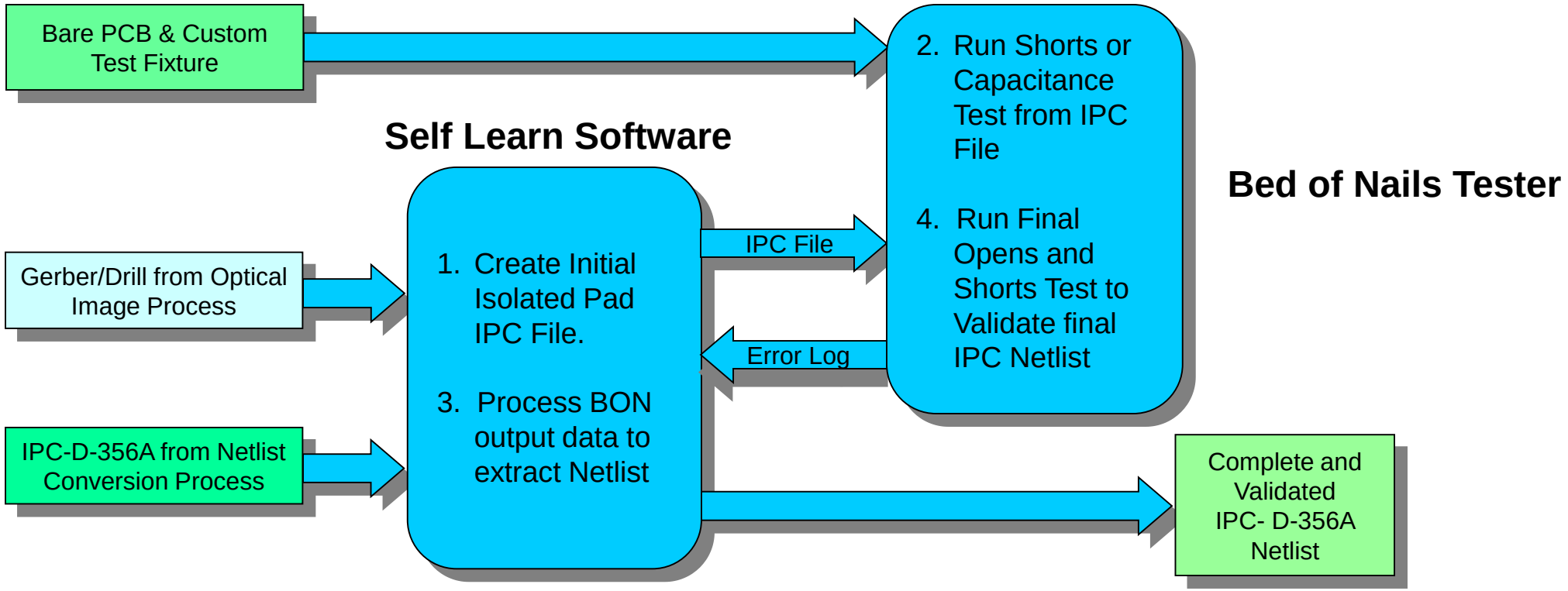
Chemical or Integrated Workstation Board

Non-Destructive – Self Learn on Flying Bare Board Probe Tester (FPT)



An FPT can be used to either validate Gerber/Drill data from the Optical process is correct, or to use the top and bottom Gerber & Drill data from the Optical Process to run a self learn process that will generate a Netlist without destroying the PCB.

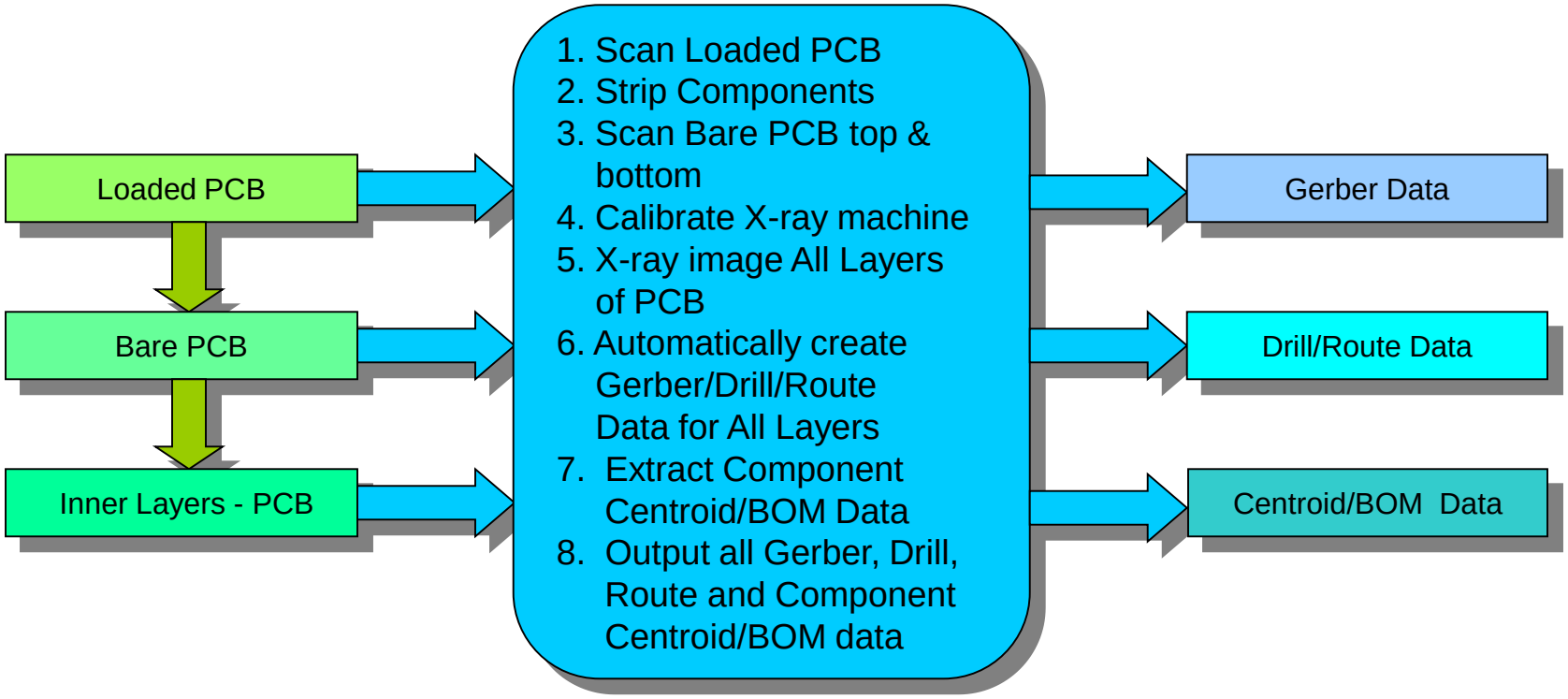
Non-Destructive – Self Learn on Bed of Nails Tester



A Bed of Nails Tester can be used to validate Gerber/Drill data from the Optical process or to generate a self-learn Netlist. The top and bottom Gerber & Drill data from the Optical Process can be used to fabricate a custom test fixture that is required for the Bed of Nails Tester. The PCB is not destroyed.

Non-Destructive – Automatic Optical with X-Ray

Optical Image Capture & Automatic Board Fabrication Data Creation



Output data from this process can be used to manufacture PCB to exact form, fit and function, or be converted into Netlist data and on to Schematic, as needed, Could be difficult or impossible to create data for inner layers, based on quality of X-ray images. Validation recommended.

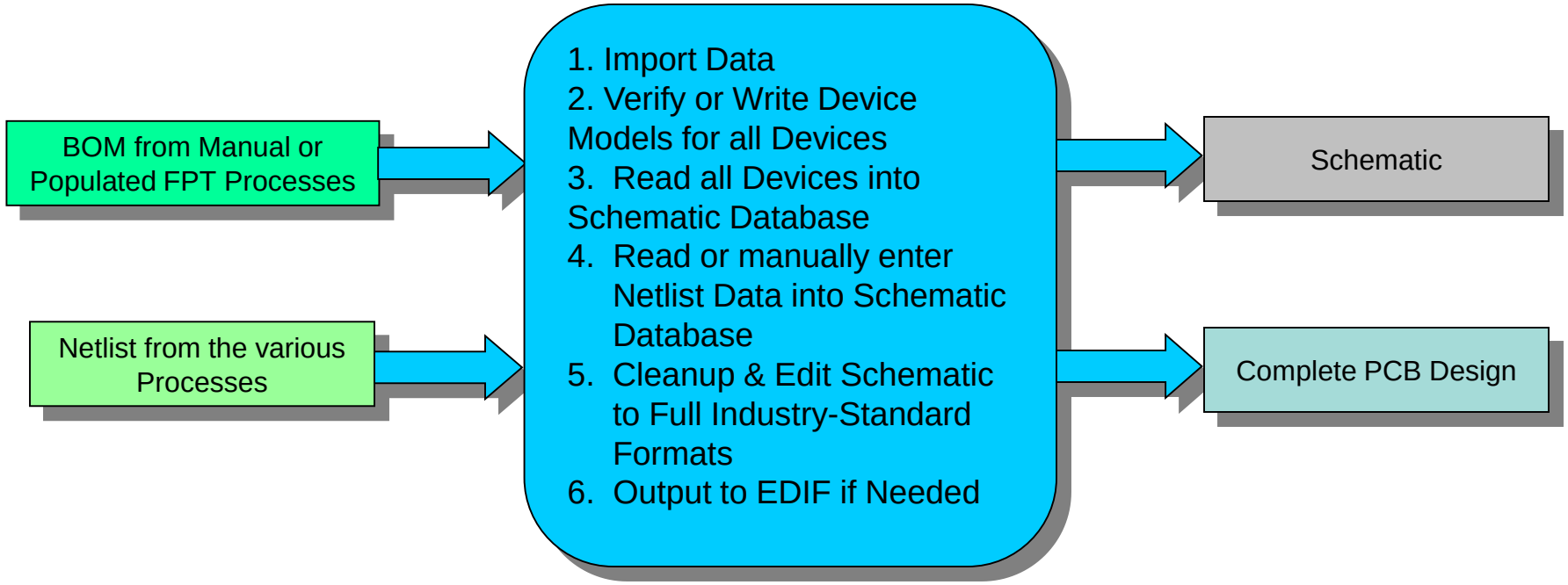
OUTPUT:

Conversion of Board Fabrication Data into "Rich" Netlist Data

Output data from the Image process can be converted into "rich" Netlist formats to be used for form, fit and function PCB Fabrication, input for Schematic Generation and/or be used as input for the non-destructive Automated Probing process. (Off line programming for FPT or fixture fabrication data for Bed of Nails tester.)

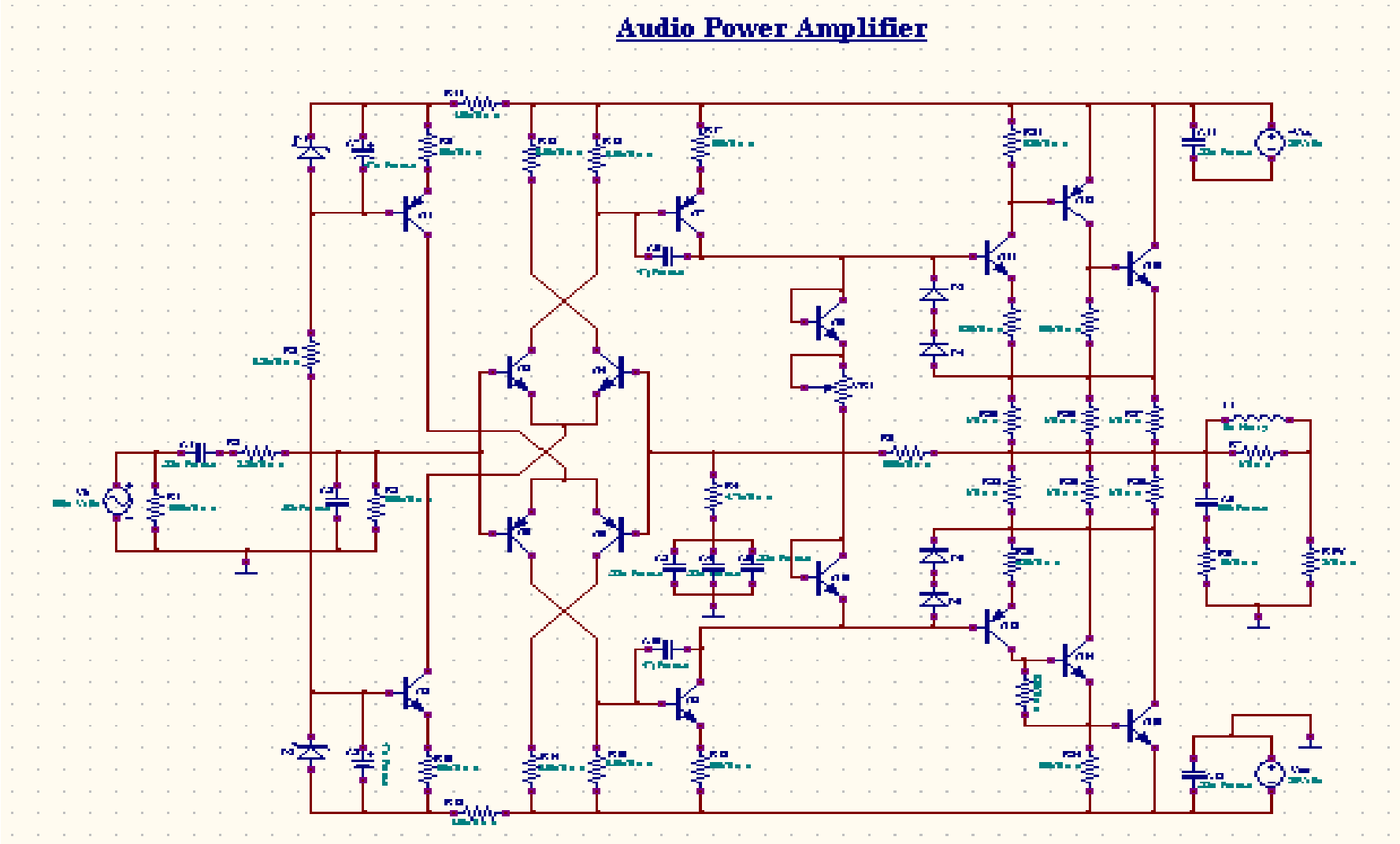
OUTPUT:

Conversion of Netlist Data into Schematic & CAD/CAE Data

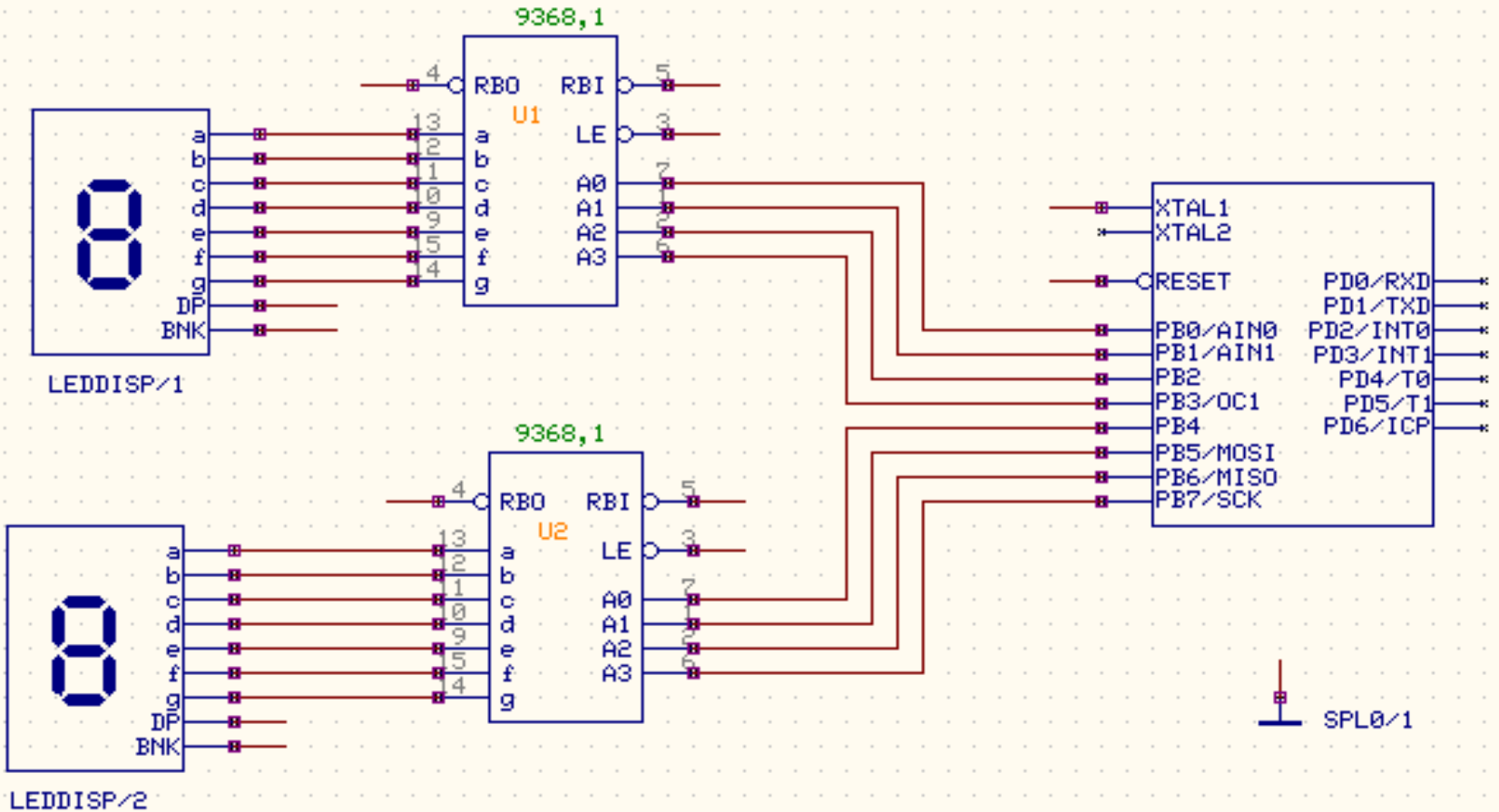


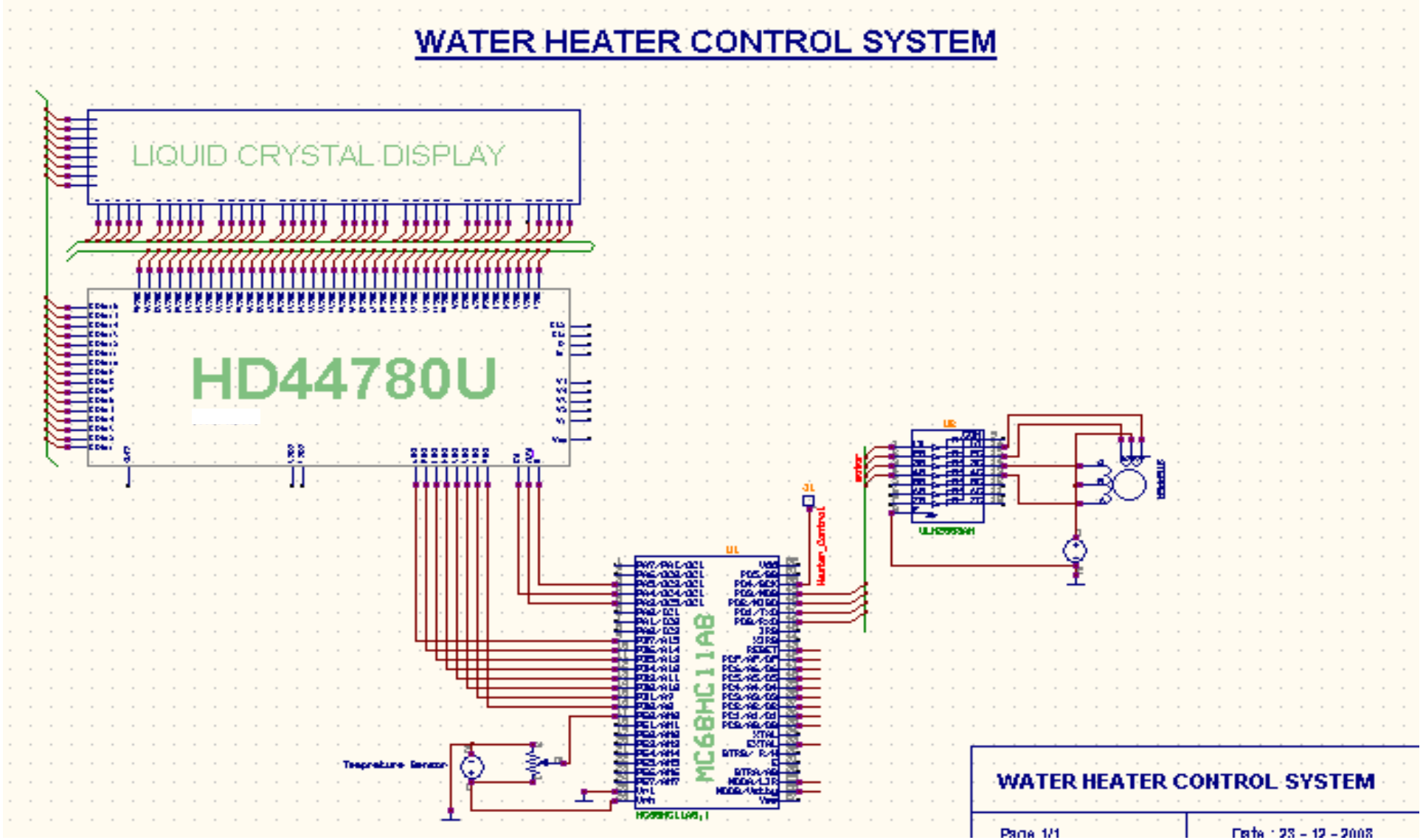
Netlist & BOM data can be used to generate the schematic and possibly even the complete PCB layout in a CAD/CAE environment.

Audio Power Amplifier



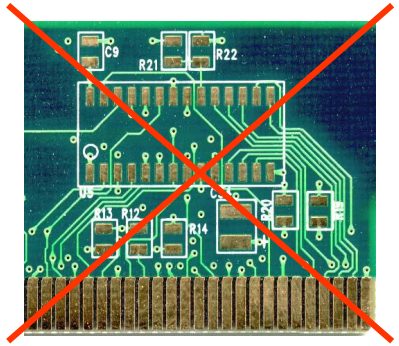
AT90S2313 - EEPROM Write Read



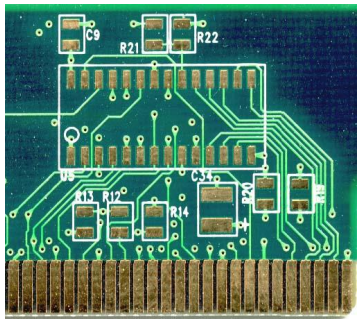

WATER HEATER CONTROL SYSTEM
LIQUID CRYSTAL DISPLAY
HD44780U
MC68HC11A8
Temprature Sensor
WATER HEATER CONTROL SYSTEM
Page 1/1
Date : 23 - 12 - 2008

Combination Techniques - Optical + Probing Scenario with two PCBs

Form, Fit & Function Required



Use Optical tools to create Gerber/Drill/Netlist/ Schematic – PCB destroyed



Use second PCB to test or validate data created from destroyed PCB with probing – independent data validation

Advantages

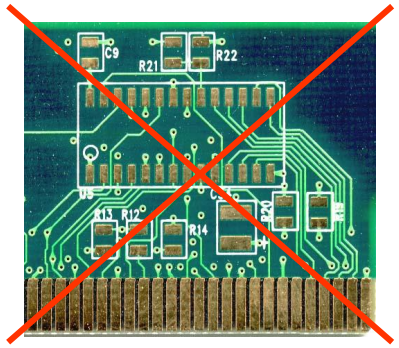
- Preferred method
- Quickest
- Least effort required
- Safe, Accurate Independent Data validation
- Supports correct form, fit and function

Disadvantages

- Requires minimum of 2 PCB's if validation is desired
- 1 PCB is destroyed

Combination Techniques - Optical + Probing Scenario with one PCB

Form, Fit & Function Required



Use Optical Tools to program Automatic Probe process for top and bottom layers of PCB

Use Optical Tool data in Self-Learn software Module to generate 1st Netlist on Tester

Then, use Optical Tools to create full Gerber/Drill for all layers and create 2nd Netlist – PCB destroyed in this process

Finally, compare 1st Netlist with 2nd Netlist to provide independent data validation

Advantages

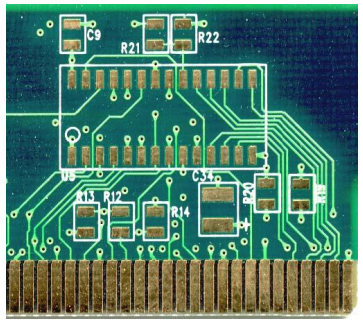
- Works with one PCB
- Independent validation of Netlist data
- Supports correct form, fit and function
- Life saver for "last board in the world" situation

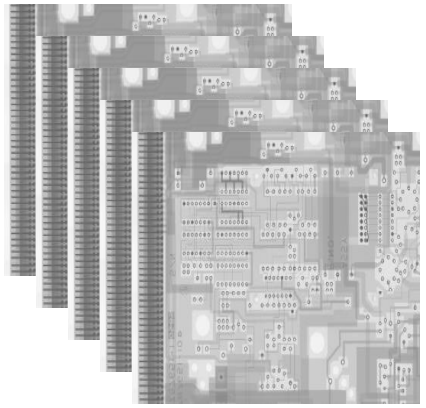
Disadvantages

- Long processing time
- PCB is destroyed
- Most effort required

Combination Techniques - Optical + X-ray + Probing Scenario with one PCB

Form, Fit & Function Required





Use Optical Tools to program Automatic Probe process for top and bottom layers of PCB

Use Optical Tool data in Self Learn software Module to generate 1st Netlist on Tester

Then, use X-ray Tools to create full Gerber/Drill for all layers and create 2nd Netlist

Finally, compare 1st Netlist with 2nd Netlist to provide independent data validation

Advantages

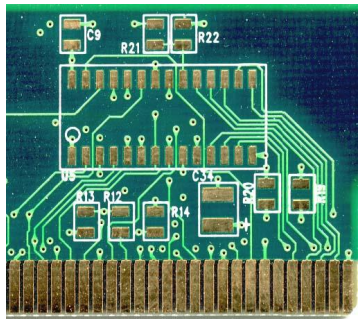
- Works with one PCB
- Independent validation of Netlist data
- Supports correct form, fit and function, if images are high quality

Disadvantages

- Most expensive
- Image quality issues
- Form, Fit & Function may be error prone, if images not high quality or X-ray has dimensional issues

Combination Techniques - Optical + Probing Scenario with one PCB

Form, Fit & Function not required



Use Optical Tools to program FPT or create fixture for Bed of Nails Tester

Use Automatic Probing and Self Learn Software Module to generate Netlist

Use Automatic Probing to perform final Netlist verification, not independent validation.

Advantages

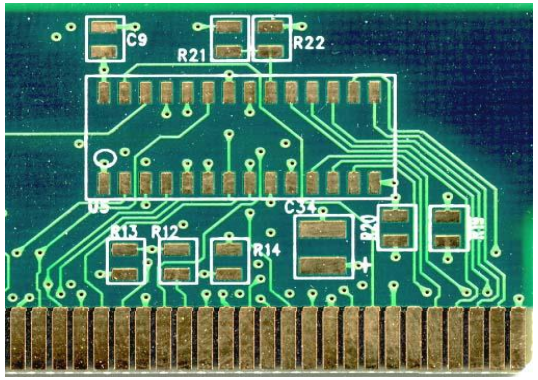
- Works with one PCB
- PCB is not destroyed

Disadvantages

- If FPT, much longer processing time than #1
- No independent data validation as with two PCBs , i.e: broken barrels, damaged pads, test errors, etc.
- No internal form, fit, shape information available

Side Benefit - Detect Counterfeit Boards

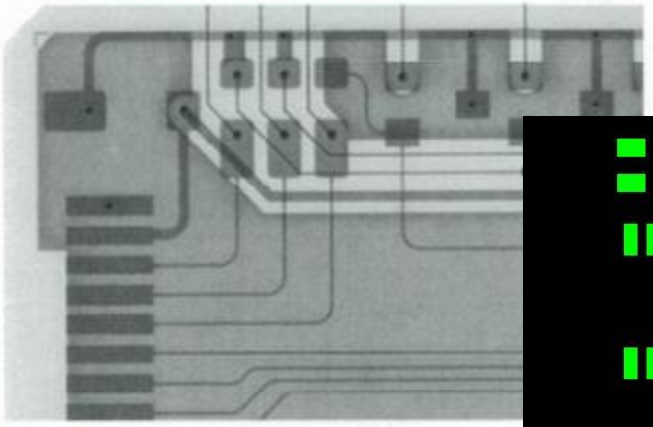
Bare PCB



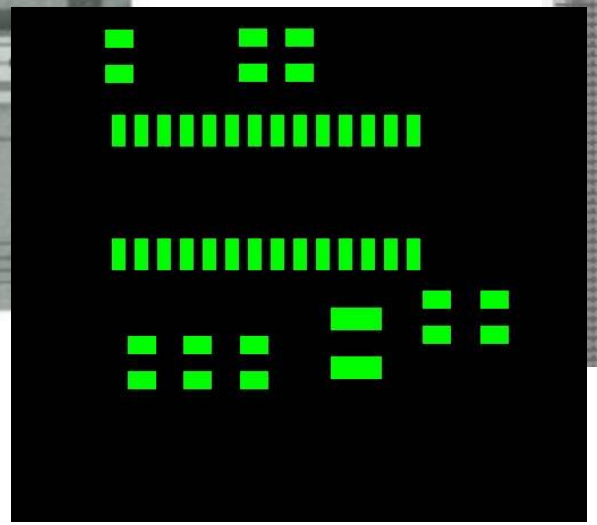
- *Compare actual PCB or X-ray of PCB back to known good Gerber/CAD/Golden Part*
- *Confirm that PCB has not been altered internally - verify trace widths, barrel thickness, ground & power planes, thermals, etc.*

```
%FSLAX24Y24*%
%MOIN*%
%ADD11C,.0080*%
%ADD19C,.0400*%
%ADD70C,.0450*%
%ADD71C,.0500*%
%ADD22C,.0600*%
%ADD43R,.0600X.0300*%
%ADD45R,.0550X.0250*%
%ADD46R,.0250X.0550*%
%ADD92R,.0500X.0500*%
%ADD95R,.0600X.0600*%
%ADD96R,.0650X.0650*%
%ADD105R,.1000X.1000*%
G54D70*
X4300Y32300D02*
X31800D01*
Y4050D01*
X4300D01*
Y32300D01*
G54D11*
X12835Y31453D02*
Y31803D01*
X13085D01*
```

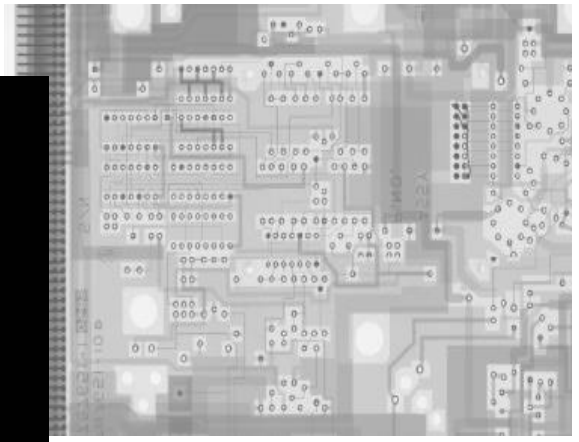
Gerber-274X Data



Ceramic X-ray



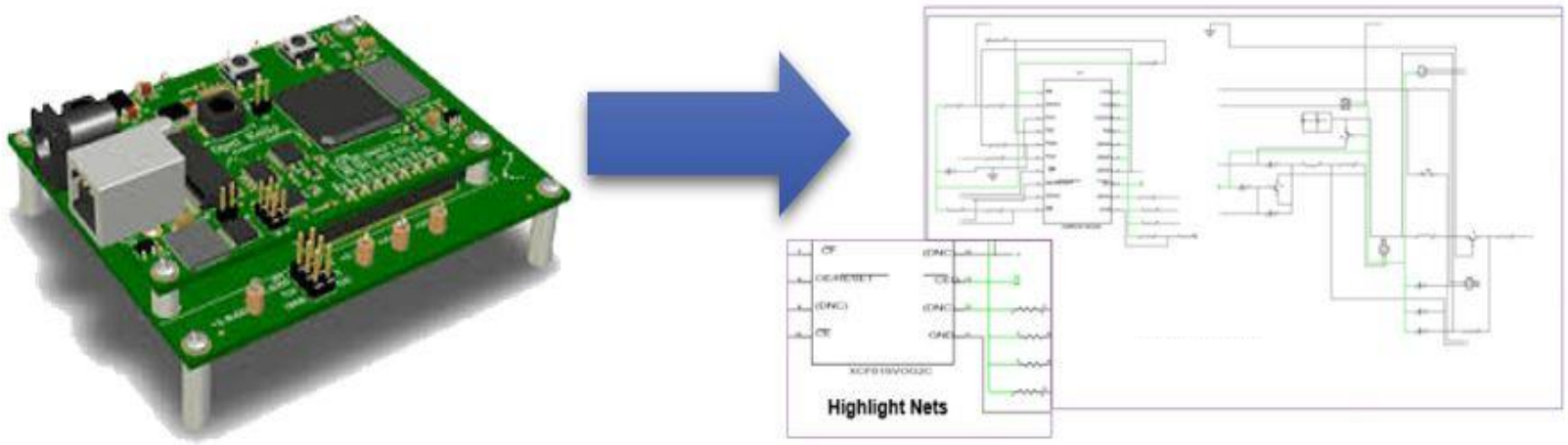
Gerber



PCB X-ray

Conclusion:

- A choice of options based on the desired result…
  - Form, Fit & Function if new PCBs are needed
  - Independent Netlist validation to confirm correct
  - Ability to just create schematic, if only for PCB repair
- Variety of price points
  - From 100% manual to very automated
  - From Non-destructive to Destructive to a combination
- Solutions avoid full re-design and test cycles… SAVE TIME & $$$
  - Faster replacement of product vs complete re-design and related testing & certification processes
- DATA IS PRESERVED..!
  - Data now saved in reliable format for future use
  - Ability to modify designs in the future



Thank you

Q&A