Assessing the Effectiveness of I/O Stencil Aperture Modifications on BTC Void Reduction

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Abstract
Bottom terminated components, or BTCs, have been rapidly incorporated into PCB designs because of their low cost, small footprint and overall reliability. The combination of leadless terminations with underside ground/thermal pads have presented a multitude of challenges to PCB assemblers, including tilting, poor solder fillet formation, difficult inspection and – most notably – center pad voiding. Voids in large SMT solder joints can be difficult to predict and control due to the variety of input variables that can influence their formation. Solder paste chemistries, PCB final finishes, and reflow profiles and atmospheres have all been scrutinized, and their effects well documented. Additionally, many of the published center pad voiding studies have focused on optimizing center pad footprint and stencil aperture designs. This study focuses on I/O pad stencil modifications rather than center pad modifications. It shows a no-cost, easily implemented I/O design guideline that can be deployed to consistently and repeatedly reduce void formation on BTC-style packages.

Introduction
Bottom terminated components (BTC) represent a particular challenge to printed circuit board (PCB) assemblers due to the formation of solder voids in their center pad solder joints. Center pads can serve as electrical grounds, heat sinks, or thermal pathways for heat dissipation (Figure 1). If the electrical and thermal conduction of the joint do not function as specified due to solder voids, premature component failure will likely result.

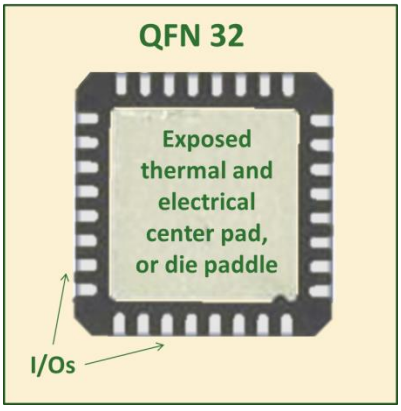

Figure 1 - QFN Package

Solder paste consists of metal powder and flux medium in a blend of 85-90% metal by weight, but only about 50% by volume. After reflow, only 50% of the printed deposit remains as solid solder which presents the challenge of volatilizing as much of the flux as possible to minimize solder voids. A myriad of ground pad solder mask and stencil aperture designs have been tested to provide outgassing pathways to evacuate volatized flux. Most of these designs produce somewhat variable outcomes with limited success, because padstack design is not the biggest factor in voiding.

The two primary variables in void formation are solder paste chemistry and reflow profile. The effect of thermal vias is also a significant consideration; however, it is not evaluated in this study because it is not a variable that can be addressed during the assembly process. Other process techniques available to reduce void formation include vacuum air and vapor phase reflow, but these require considerable capital investment and are not widely available to the typical PCB assembler.

Background

While performing in-depth solder paste print studies and reflowing sample boards, the company's Applications Lab staff noticed that when I/O perimeter pads were left unpasted, solder voids were dramatically reduced. On components that typically exhibited 10-20% voiding, the rate dropped to nearly zero.

The engineers theorized that the absence of solder paste on the I/Os allowed the component to float on the surface of the molten solder and flux gasses could be expelled more readily as a result. They believed that the as molten solder eventually wetted to the component's die paddle the component was pulled down, likely further displacing trapped volatiles on the way, and then finally froze upon cooling. Repeated experiments showed consistent outcomes: when the pads were left unprinted voids were practically eliminated; when the I/O pads were printed 1:1, the voids returned.

The reproducibility of the results led to further discussion and postulation**:** if the witnessed phenomena was rooted in I/O pads' paste deposits limiting the component's ability to float on the surface of the molten solder, effectively shutting down the volatile evacuation pathways, then increasing the volume of paste on the perimeter I/O pads – which should reach their liquidus phase before the center pad underneath the component - would essentially prop the component up and create similar outgassing paths for flux volatiles.

Hypothesis

Increasing the volume of solder paste on the I/O pads temporarily elevates the component as it enters the liquidus phase of the reflow process, thereby improving opportunities for flux volatile outgassing from the center pad.

The hypothesis is based on the concept that the I/O pads achieve a liquidus state slightly before the ground pad due to their locations on the edges of the package and their much lower thermal mass than the package itself. As the paste deposits melt, they coalesce on the solder pad, lifting the BTC package. The extra height temporarily provided by the solder on the I/O pads is believed to be the mechanism that drives the reduction of ground plane voiding. As the solder wets to the terminations and die paddle, the wetting forces pull the package back down. The rapid drawing down of the component body as the solder wets may also force more volatiles out of the molten solder on the center pad. (Figure 2)

In this study, no bridging or shorts were observed, even with the largest increase of I/O solder volume, an overprint of 30mils. However, excessive joints were observed when too much solder paste was applied.

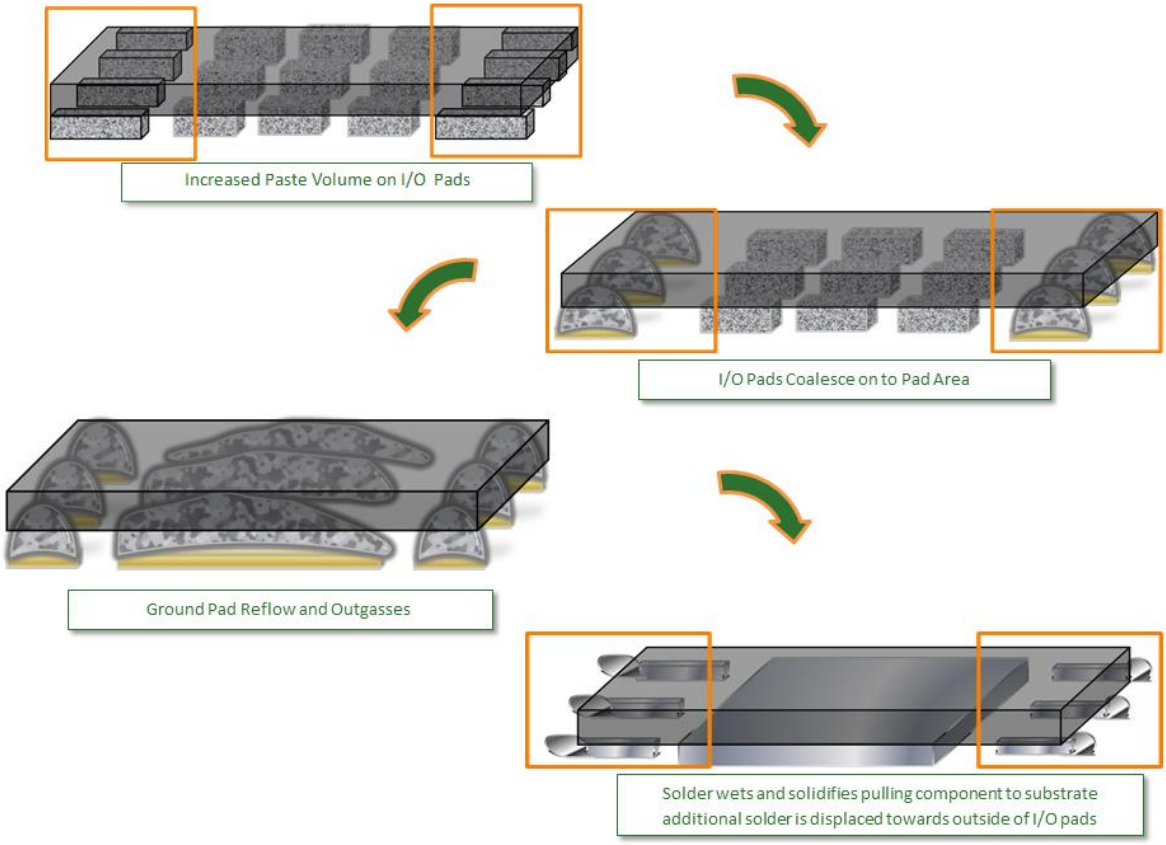

Figure 2 - The Effect of I/O Print Volume on Ground Pad Voiding

Experimental Method

All testing was performed in the company applications laboratory in Juarez, Mexico. The tests were performed by two SMTA-Certified Process Engineers with over 50 years of combined SMT experience.

Test Vehicle

The test PCB design was a commercially available print test board with twelve BTC footprints (Figure 3). The 8.5"x 6" PCBs were constructed of high T_g laminate, used an electroless nickel immersion gold (ENIG) final finish, and were all new and unused.

Twenty test printed circuit board assemblies (PCBAs) were assembled consecutively, all using the same materials and process parameters providing 240 QFNs for study, with 60 of each type.

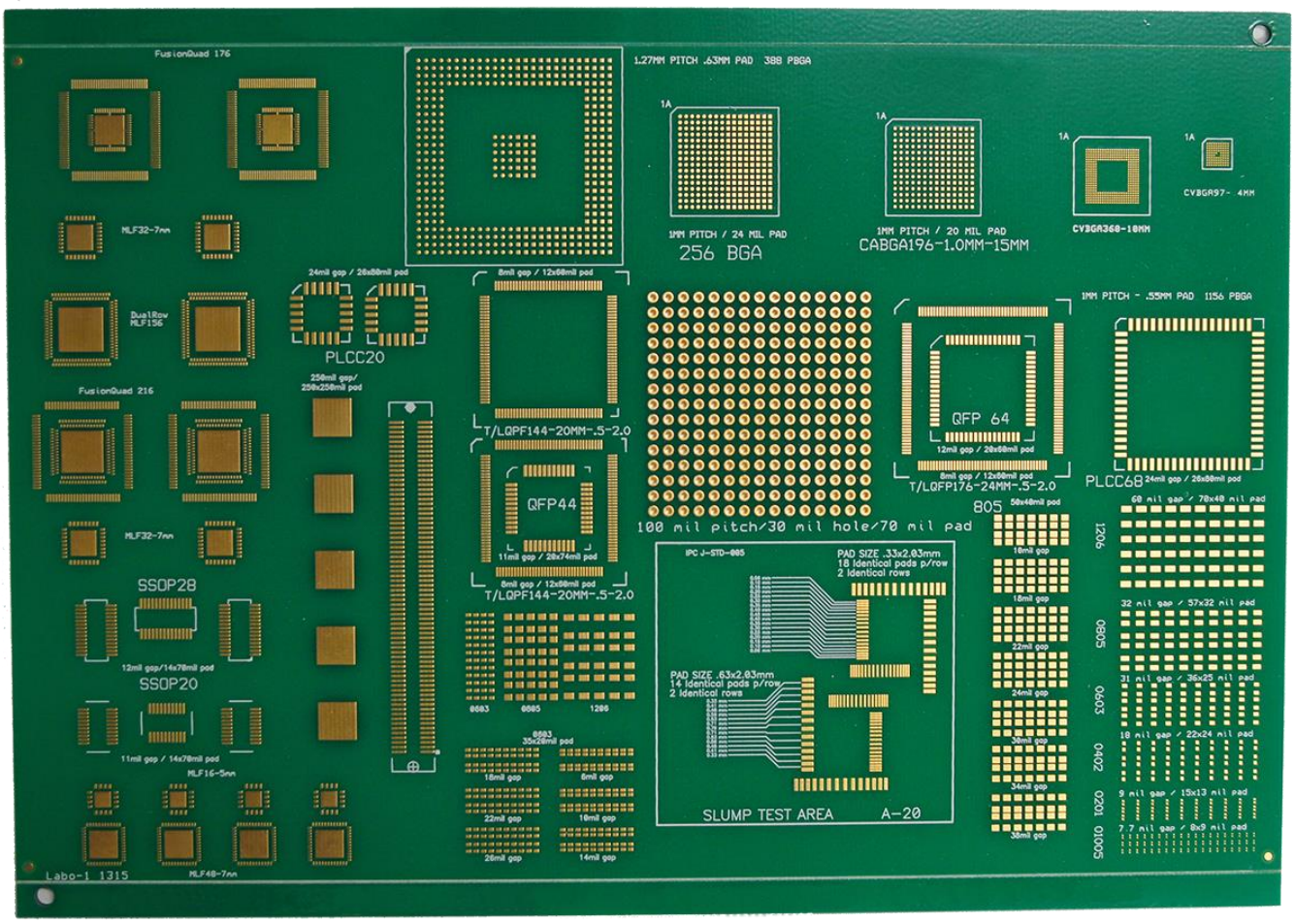

Figure 3 – Test Vehicle

Component Selection

Three packages were analyzed in the study. They are shown left-to right in Figure 4: MLF48, 7X7mm; MLF32, 7x7mm; and MLF16, 5x5 mm. All MLFs were from the same manufacturer and respective lots, with 100% matte tin finish over copper lead frames, and were all procured from the same dummy component supplier as the PCB.

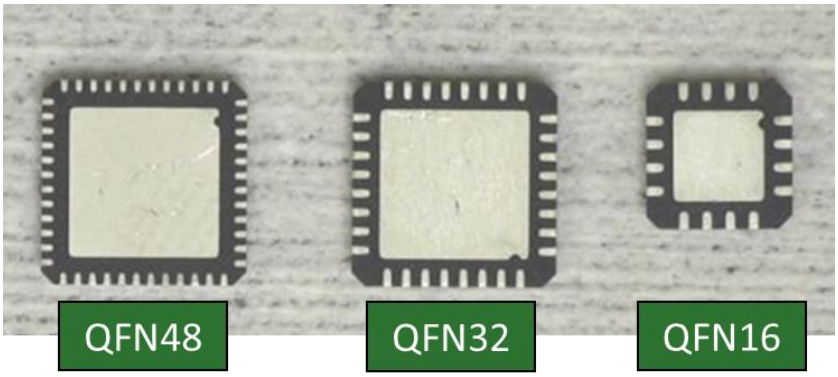

Figure 4 – Components Tested

Table 1 – Types of Components

Component Type	Weight	Pitch
QFN MLF48	0.0585 gr	0.021”
QFN MLF32	0.1275 gr	0.027”
QFN MLF16	0.0585 gr	0.031”

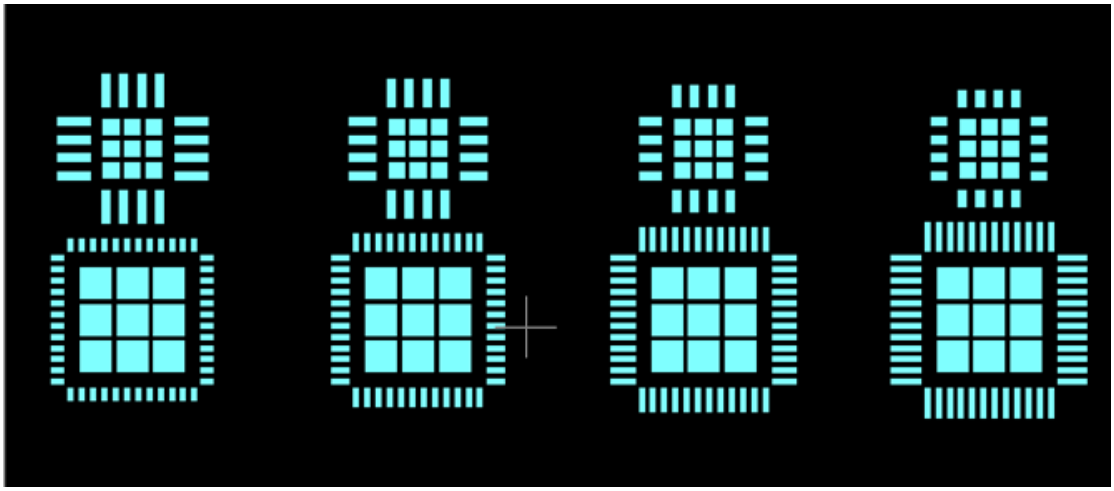

Figure 5 – Experimental I/O Paste Overprint Stencil Design

Solder Paste and Printing

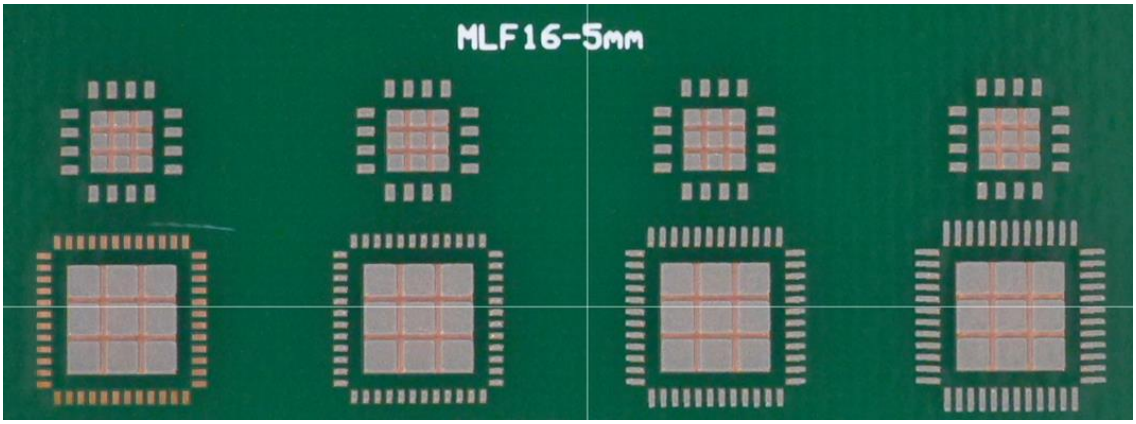

Figure 6 – Original I/O Paste Overprint Technique

The solder paste used was a No Clean SAC305 Type 4 with over 2 years of production history which has consistently exhibited relatively low voiding performance. The stencil used was premium stainless steel, diode laser cut with fluoropolymer nanocoating. The test area was climate controlled; with temperature typically 25.4°C (78°F) and 54%RH.

Reflow Profile/Oven

Assemblies were reflowed in a new, commercially available ten-zone convection oven using an ambient air reflow environment. Figure 7 shows the selected profile. A ramp-to spike (RTS) profile was chosen because:

- Linear profiles generally produce more voids than soak profiles. A common approach to void reduction in profiling is to incorporate a soak zone to increase volatilization of the flux chemistry prior to the alloy becoming molten. The RTS profile is often considered the worst case scenario for voiding.
- Many packages that are void-prone and void-sensitive are often thermally sensitive to reflow process peak temperatures. Therefore, a profile with less heat exposure is usually preferred for BTC and similar miniaturized plastic packages.
- The study's goal was to isolate the effect of the aperture design and minimize the effect of profiling on the results.

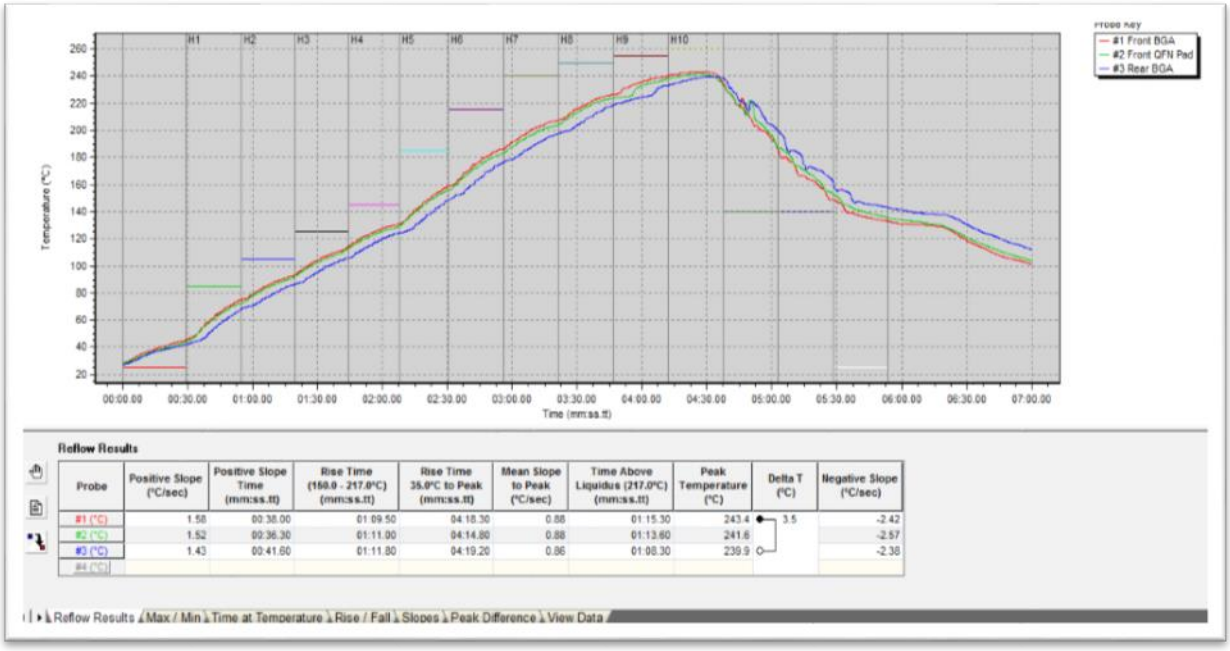

Figure 7 – Selected Profile

Reflow Profile - Long RTS (4.5 min) with Standard Slope (< 2.0) and Standard TAL (~75 sec) Peak Temperature of 240°C

X-Ray Equipment and Settings

An automated high-resolution, transmission X-ray inspection system was used to characterize the voids. The settings used were 75 Kv and .075mA, or 5.6 watts. The results were accumulated and processed using production statistical software.

Results and Discussion

Void Formation:

- Voiding decreased as overprint increased for each package size tested. The results are shown in Figures 8 to 10.

QFN48 Voiding Results

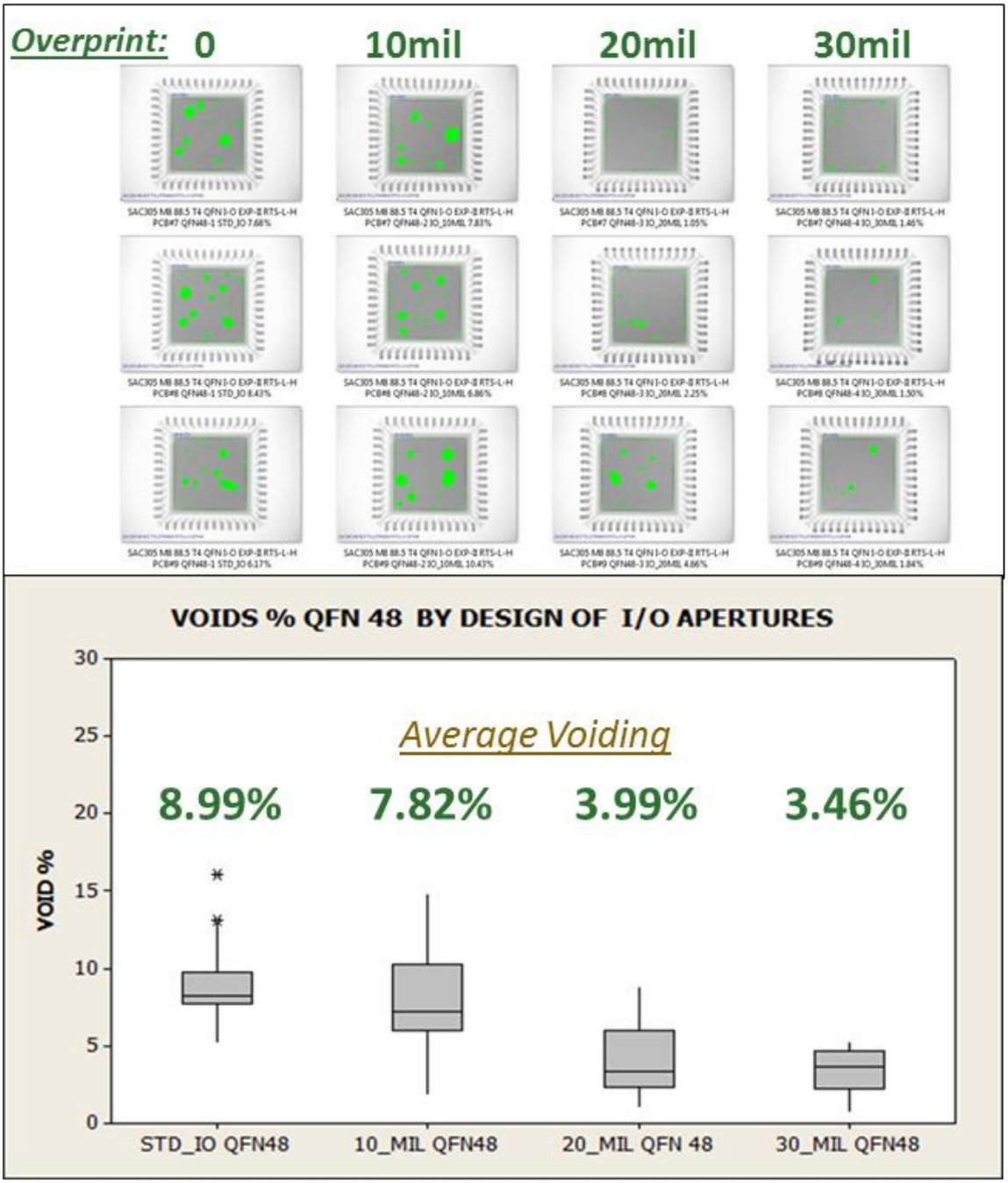

Figure 8 - QFN48 voiding results

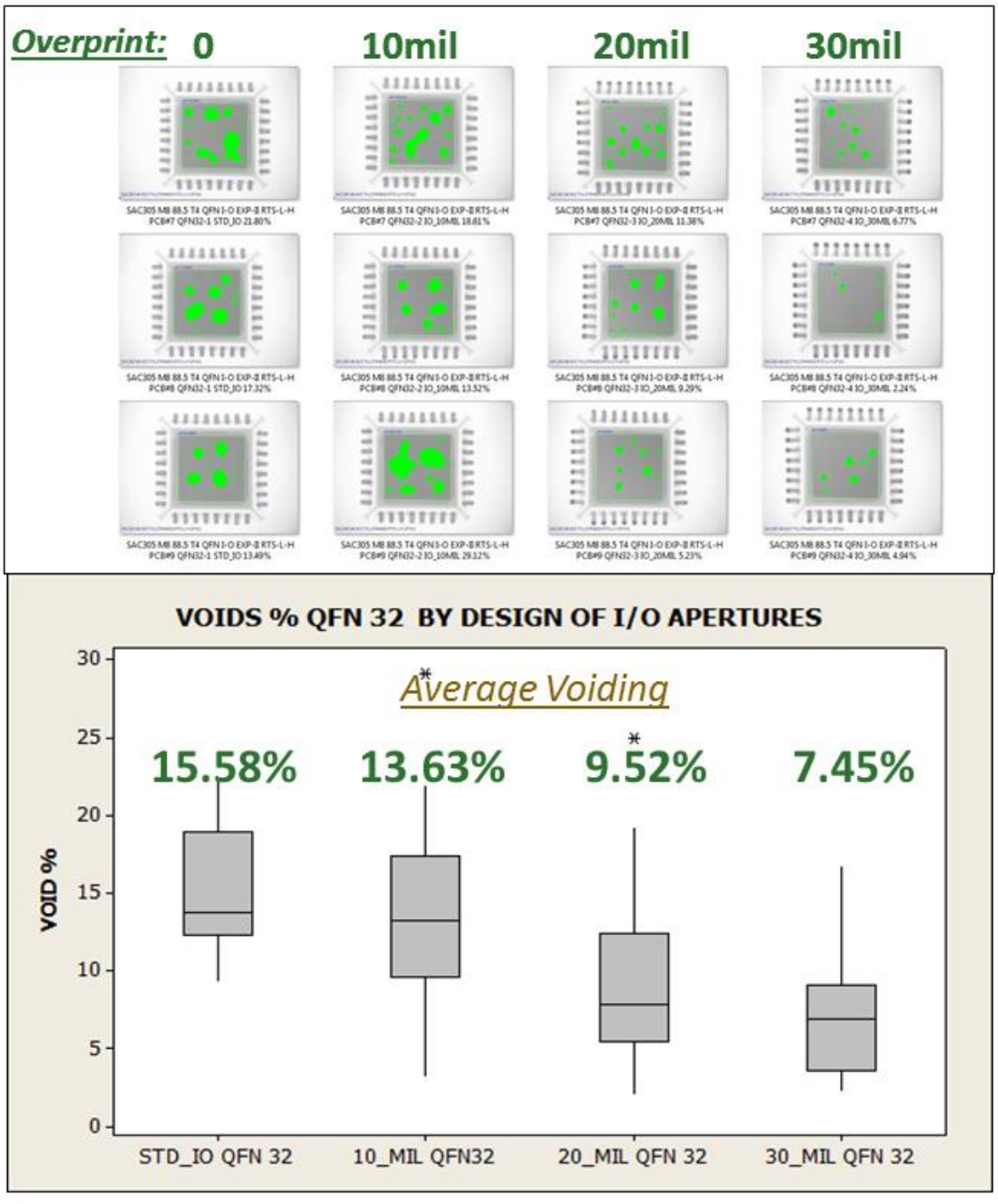

Figure 9 – QFN32 voiding results

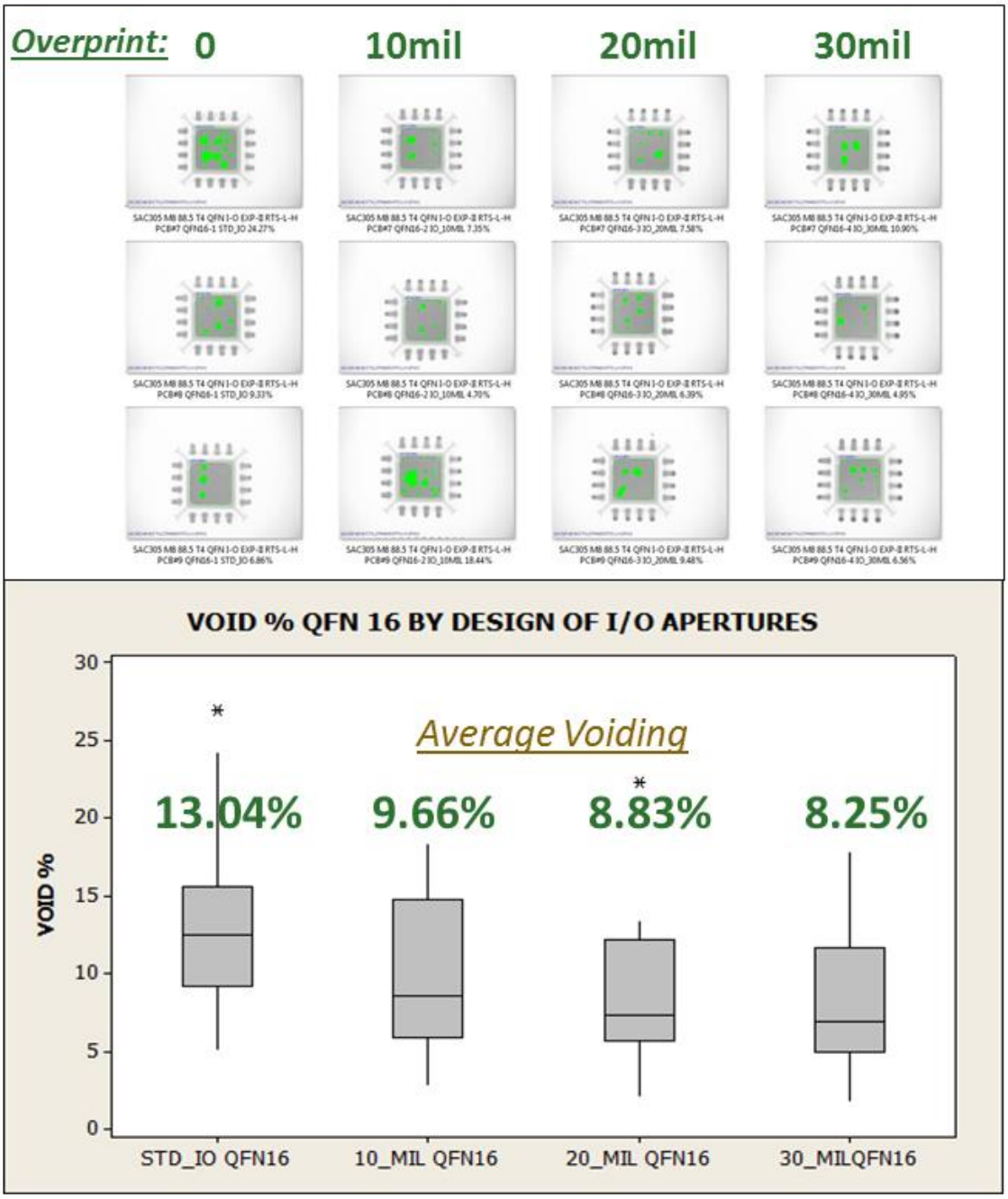

Figure 10 – QFN16 voiding results

The X-ray results from the structured DOE confirmed the earlier results. For each of the 3 devices tested, voids decreased as the overprint increased.

The hypothesis stated that higher volumes of solder paste on the I/O pads help "lift" the component above the center pad's solder paste to enable better outgassing before the center pad paste reaches liquidus temperature. It is impossible to measure the small height differential of the liquidus deposits during the actual reflow process, so they are calculated theoretically using the following assumptions to simplify:

- The volume of the solder (metal) is 50% of the volume of the solder paste overprint
- The overprint coalesces fully onto the pad
- The height is determined by dividing the calculated volume by the I/O pad area

The theoretical height differentials are shown in Table 2.

Table 2 - Theoretical Standoff Differentials Caused by Overprint

Component Size	Extra Standoff from I/O Overprint (mils)			
	0mill	10mil	20mil	30mil
MLF 16	0	0.93	1.85	2.78
MLF 32 & 48	0	0.73	1.45	2.18

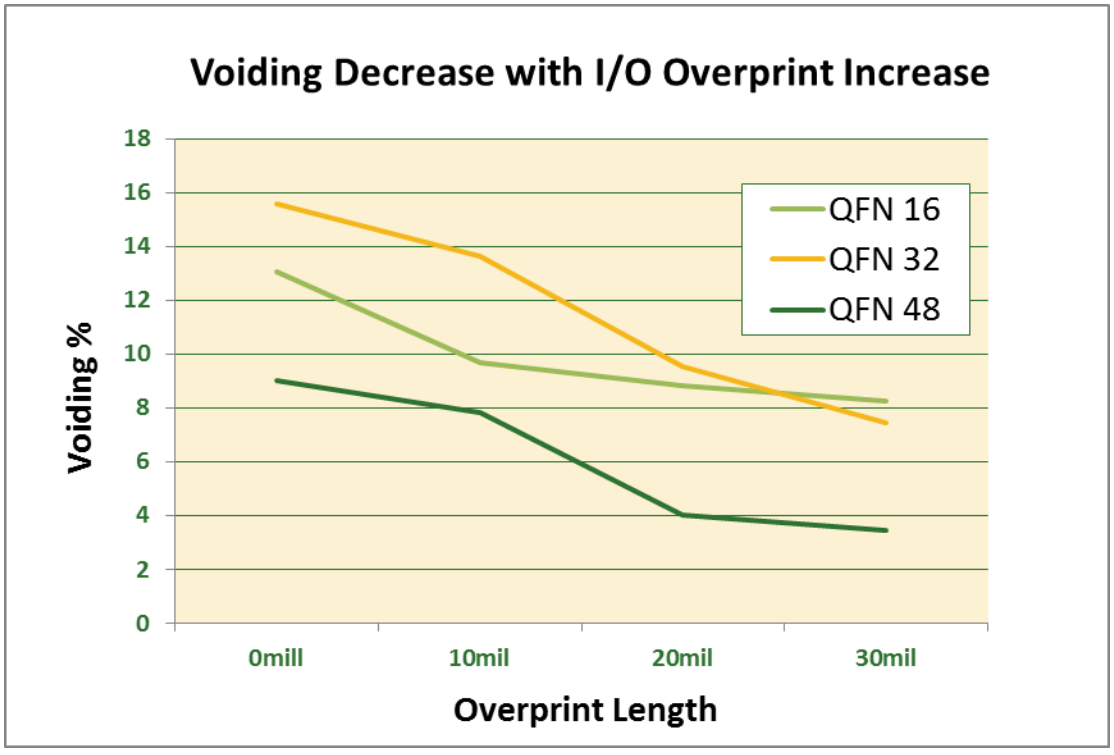

Figure 11 – Voiding Summary

The three packages tested all showed decreased voiding as overprint increased. The combined summary in Figure 11 shows the two larger devices exhibited similar trends with respect to decreased voiding, but the smaller package did not exhibit as much void reduction as the two larger ones when the overprint distance was increased.

Three possible reasons for the different behavior in the smallest package are offered:

1) The smaller package outline and lower thermal mass result in a shorter outgassing time between the I/O pads reaching liquidus and the center pad reaching liquidus. This can be further investigated with advanced profiling techniques and/or thermal cameras.
2) The I/O pads are smaller on the 16-pin device than the 32 and 48 pin devices. Therefore, less overprint is needed to lift the package to the height necessary to achieve the improved outgassing.
3) A mathematical relationship may exist between the ratio of areas of the I/O pads and center pad, the I/O prints and the center pad print, or the perimeters of the I/O and center pads, based on buoyancy forces prior to wetting or surface tension during wetting.

These three potential explanations will be explored in further detail as the project progresses, and will be reported in a future publication.

Solder Joint Formation

After the assemblies were X-rayed, samples were cross-sectioned to examine the solder joint formation on both the I/O pads and the center pad. Samples consisted of 2 section views each of the smallest and largest components, QFN16 and QFN48, at overprints of 0 and 30mils. The first section view was through a row of leads to measure multiple I/O joint heights; the second was through the leads and center pad to measure both perimeter and center solder joint heights and evaluate solder fillet formation. Figure 12 shows the locations on the MLF48, and Figures 13 through 15 show the actual sections for comparison.

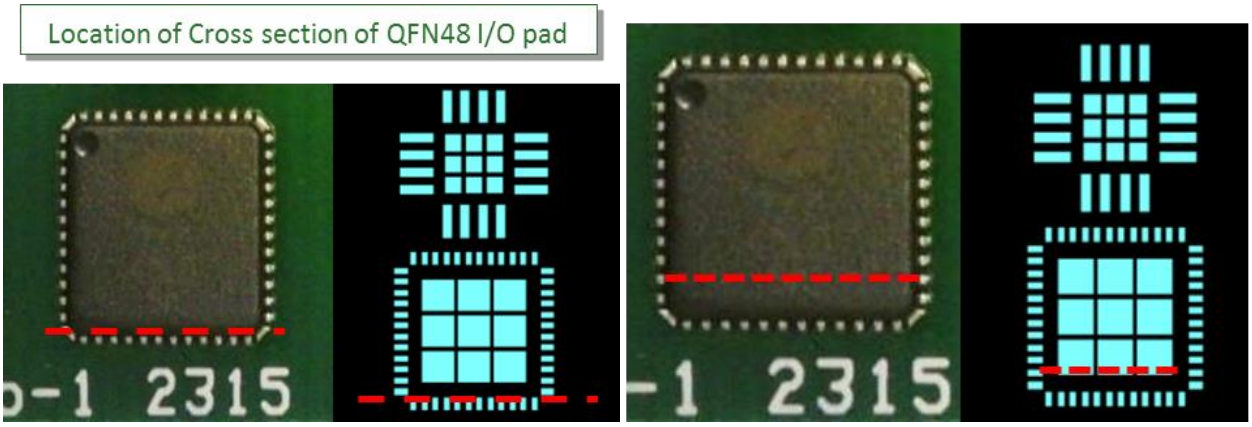

Figure 12 – Locations of Cross-sections on MLF48

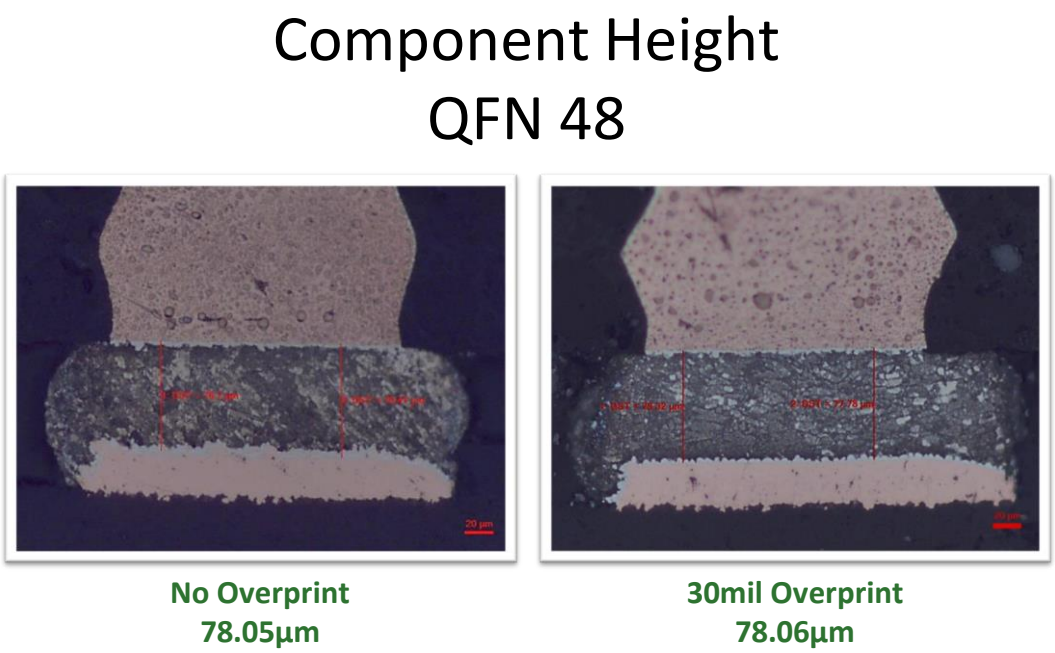

Figure 13 - Cross Sections of QFN48 I/Os at 0 and maximum (30mil) overprints

The images in Figure 13 show similar I/O solder joint heights, despite the difference in solder paste volume, even though the joint from the overprint had nearly 2.5 times the solder paste volume that the joint printed at 1:1 had. The second set of cross-sections – the ones through the center pad - show the extra solder on the I/Os went out to the perimeter.

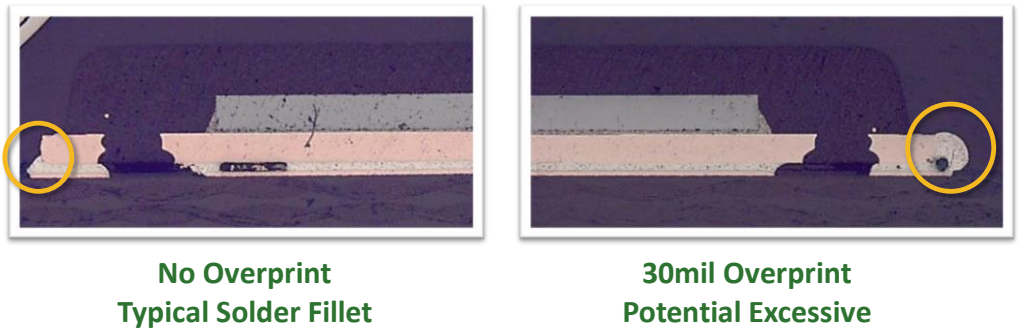

Figure 14 – Cross sections of center and perimeter pads QFN48

In Figure 14, there are notable differences between the solder joints. On the left, where solder paste was printed 1:1 with the I/O pad, a large void is seen in the center joint, and a typical fillet is seen on the perimeter joint. On the right, where the solder paste was printed 30mils beyond the toe of the pad, no voids are seen in the center joint, but the excess solder from the I/O pad is seen squeezing out of the perimeter joint.

The excessive joint seen in Figure 14 is a potential defect. On some bottom-terminated packages, wetting to the sides of the terminations and toe fillets are not required, but even if they are not, many assemblers prefer to see them. If they are inspected at AOI, excessive solder on the terminations could lead to false calls. If they are inspected visually, they could be interpreted as defects due to their negative wetting angle. Figures 15 and 16 show similar images for the QFN16.

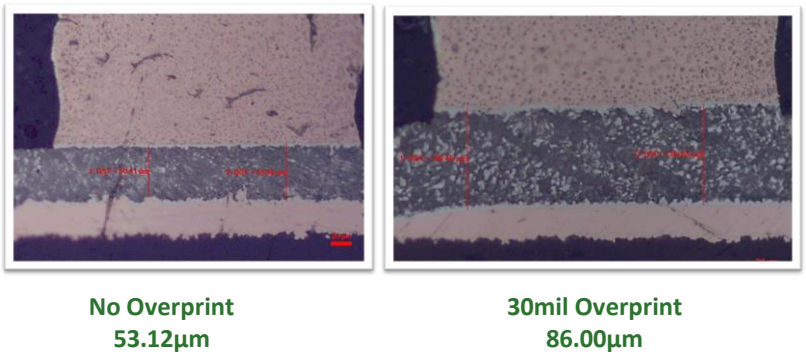

Figure 15 – Cross Sections of QFN16 I/Os at 0 and maximum (30mil) overprints

Solder Joint Formation
QFN16

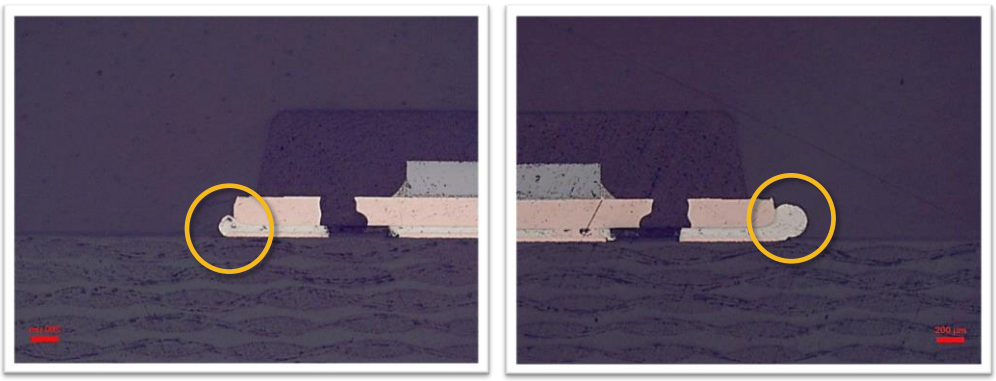

Figure 16 – Cross sections of center and perimeter pads QFN16

The results of the cross-sectional analysis reveal a need to review all the devices at all overprint levels to understand how to balance voiding reduction with perimeter joint formation. Samples of every parameter combination will be complete with the addition of all QFN32s, and QFN16 and QFN48's 10mil and 20mil overprints. The visual images will be combined with the X-ray data to help define an optimum window for overprinting each device.

The ability to dramatically reduce voiding through the overprinting of I/Os has great potential. It is easy, effective, and requires no capital expenditures to implement.

Conclusions

1) Voids were reduced to levels below 10% on all components. On the QFN48 component, the reduction of voids by increasing paste overprint on the I/Os is drastic. The *largest* void measured with +30 mils overprint (5.28%) is approximately the same size as the *smallest* void measured (5.22%) with the standard 1:1 print. The results of the cross-sectional analysis reveal a need to review all the devices at all overprint levels to understand how to balance voiding reduction with perimeter solder joint formation.
2) It appears that the temporary standoff generated by the I/O overprints raise the component to a height which promotes outgassing before wetting and collapse. The data in this experiment show height to be approximately 1- 1.5mils. Increasing the overprint and theoretical height to greater than 2mils does not provide considerable benefit and may result in undesirable outcomes.

3) Each package size responded differently. The smallest package did not appear to benefit from longer overprints as much as the larger packages did.
4) The impact of reflow profile on the void reduction effect is unclear as only one profile was tested. The profile used is considered the most challenging for void reduction and represents a common worst case scenario.

Future Work

This study was a screening test establishing the efficacy of the I/O aperture technique. More data from this study will be obtained, and further testing will assess the impact of other variables on the effect of the I/O overprint technique, including reflow profile, PCB surface finish and component type. Additional testing will focus on refining both I/O and ground pad aperture designs to establish optimal parameters and help build higher standoffs for higher reliability. Field implementation is underway to determine if the lab results are reproducible on the assembly line, and the extent to which this new I/O design can limit voiding in a production environment.

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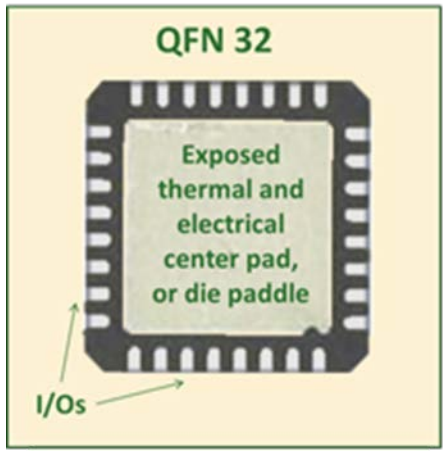
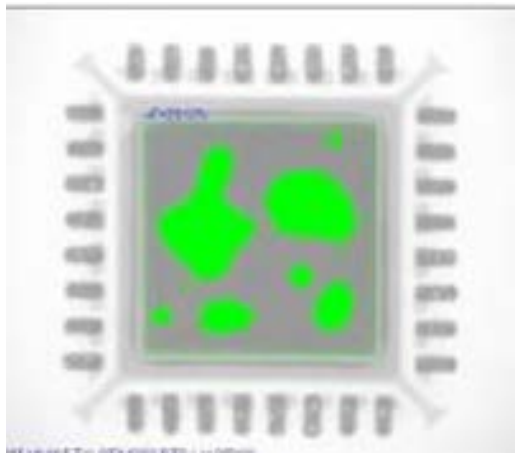
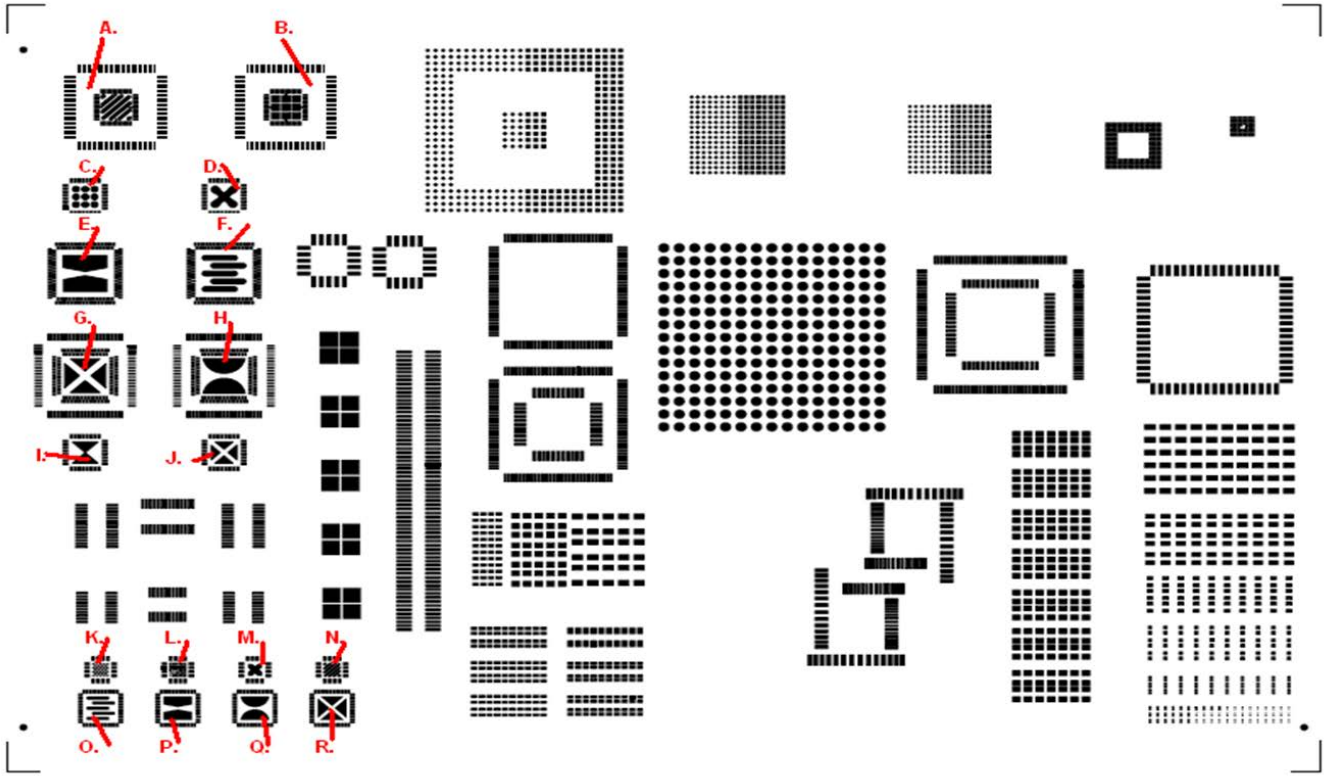




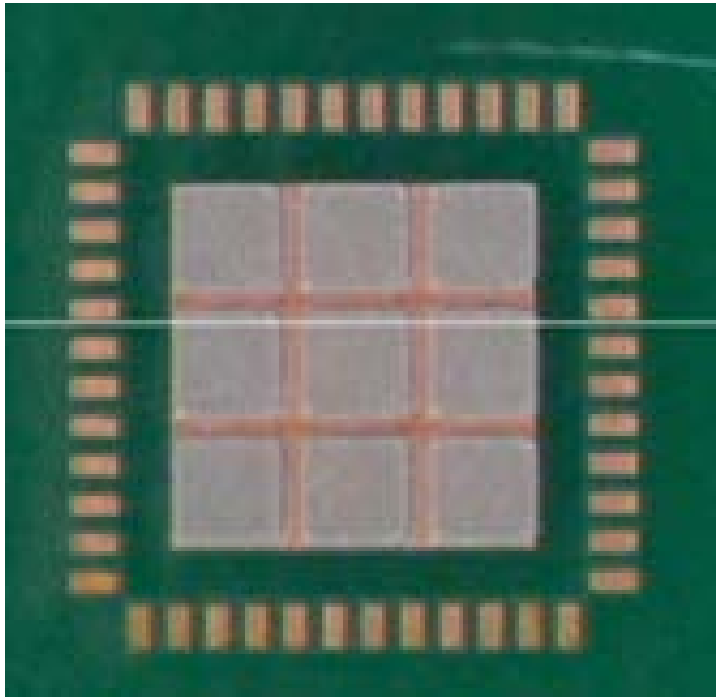
Background

- Most common void reduction techniques include ground pad aperture design and reflow profile modifications having a modest and variable effect.



Background

- Engineers in the company's Applications Lab observed that when I/O pads were left unprinted, solder voids were dramatically reduced. On components that typically exhibited 10-20% voiding, the rate dropped to nearly zero.



Analysis

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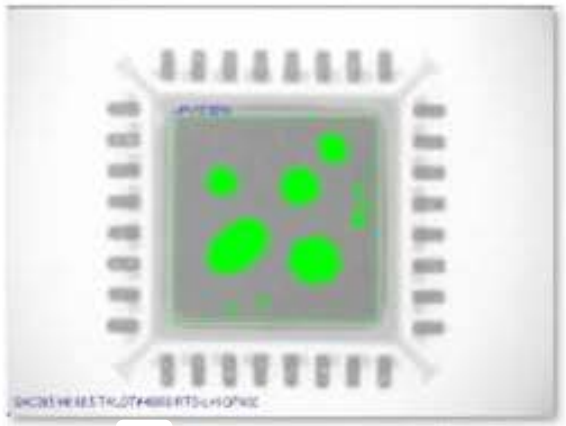
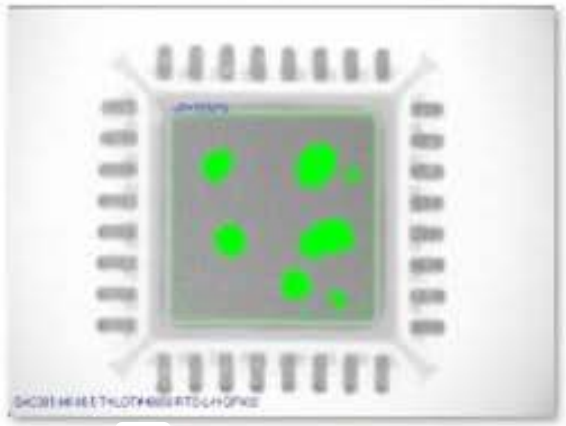
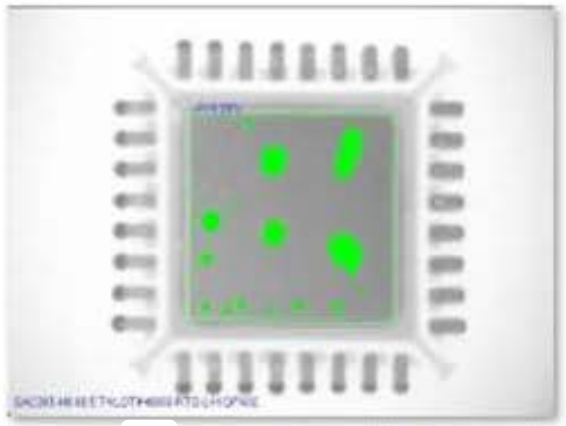
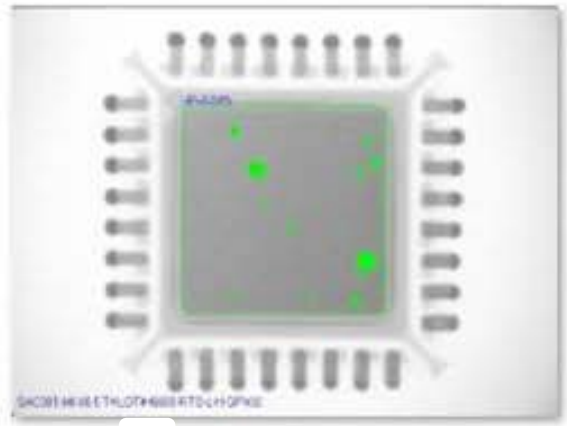

SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#8 QFN32-1 STD_IO 17.32%

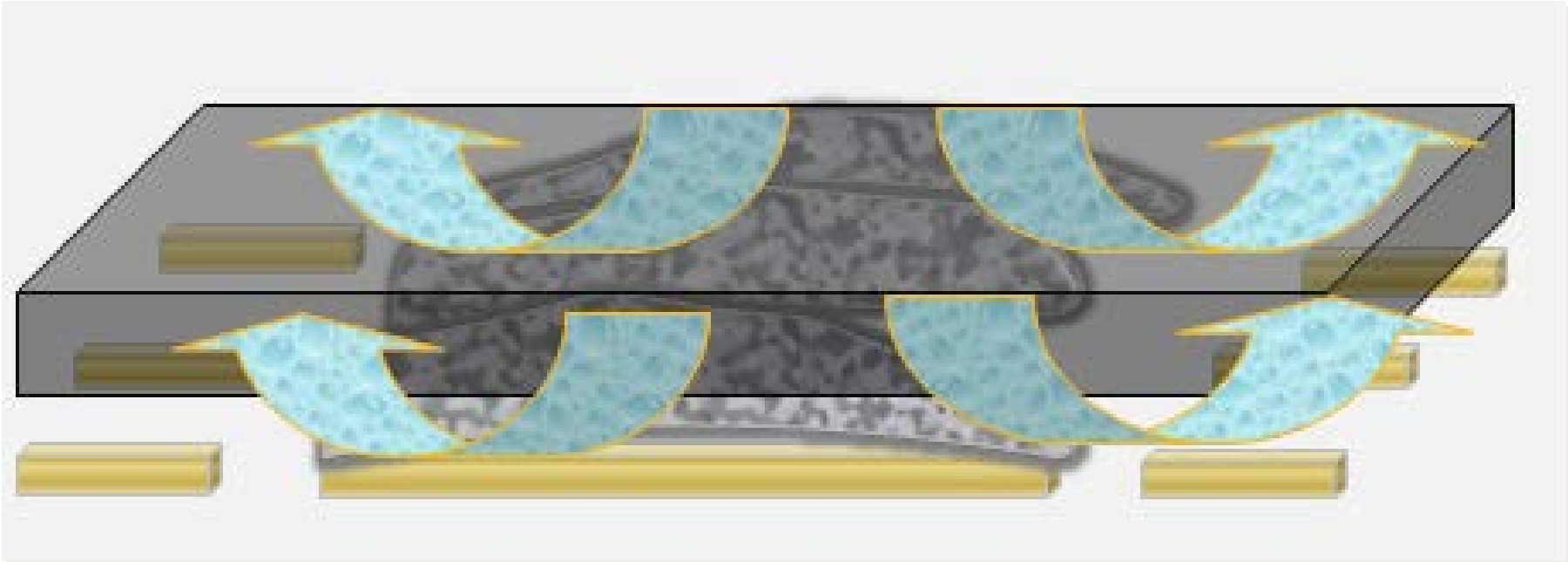

SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#8 QFN32-2 IO_10MIL 13.52%


SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#8 QFN32-3 IO_20MIL 9.29%


SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#8 QFN32-4 IO_30MIL 2.24%

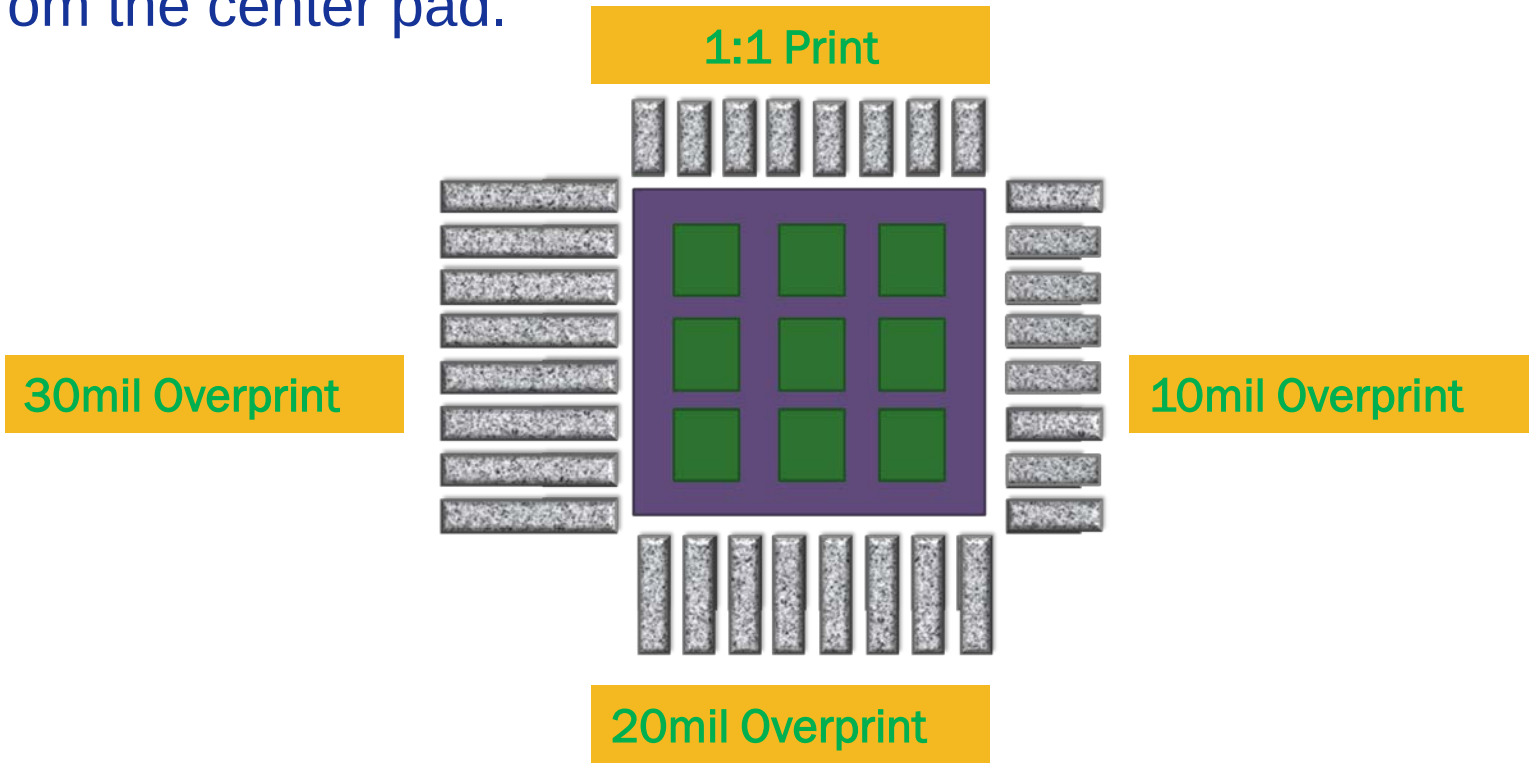
Hypothesis

- The absence of solder paste on the I/O pads allowed the component to float freely on the surface of molten solder improving opportunities for flux volatile outgassing from the center pad.



Test Method

- Increasing the volume of solder paste on the I/O pads allows the component to float freely on the surface of the molten solder, temporarily elevating the component as it enters the liquidus phase of the reflow process, thereby improving opportunities for flux volatile outgassing from the center pad.



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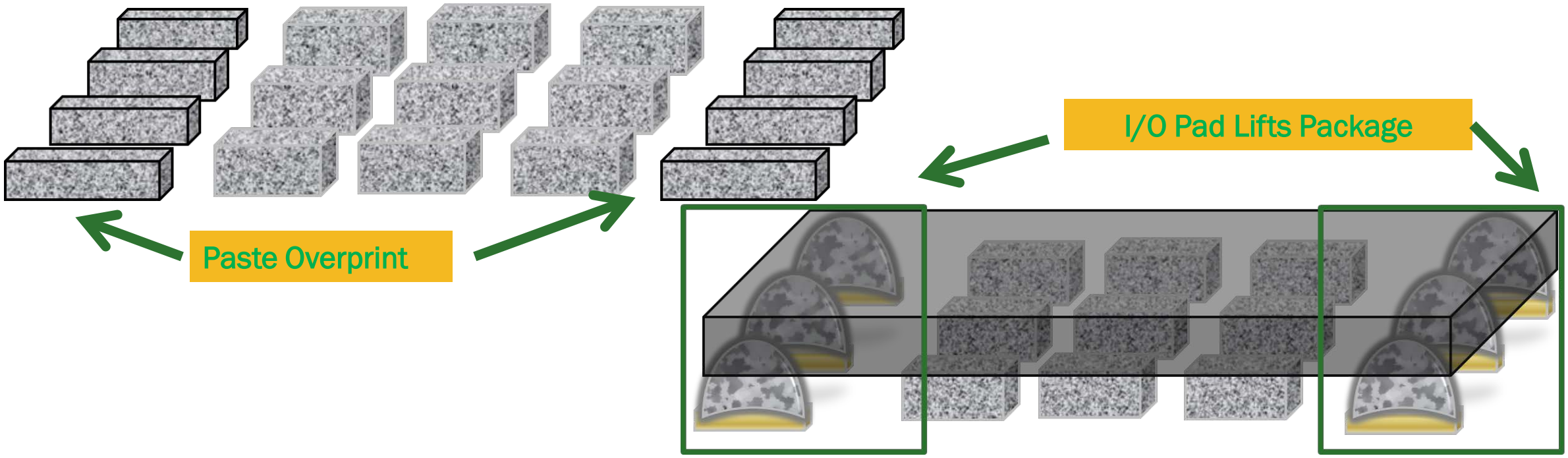
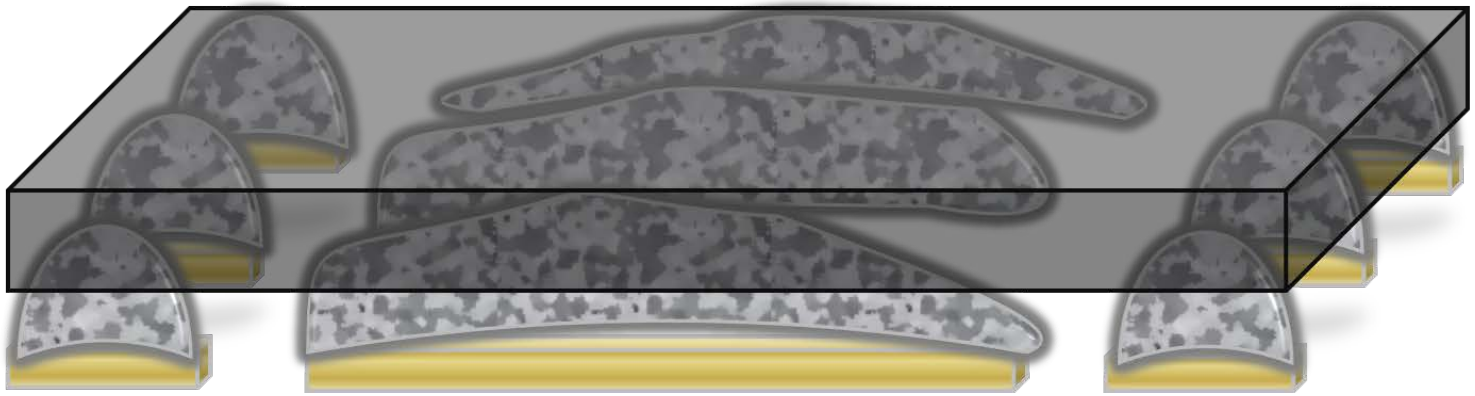
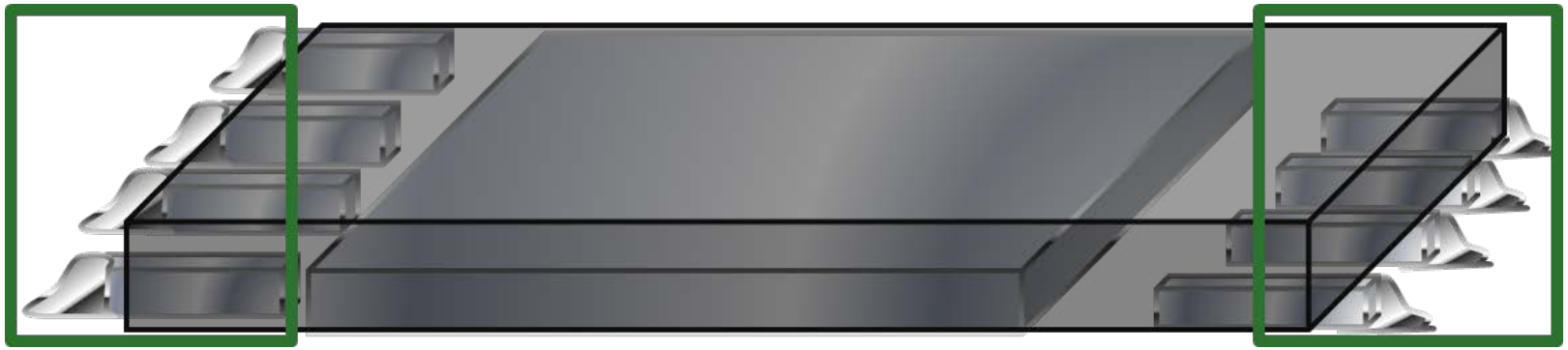


Hypothesis



Solder Wets, Freezes Pulling Package to Substrate – Volatiles Are Displaced

Ground Pad Outgasses Then Reflows



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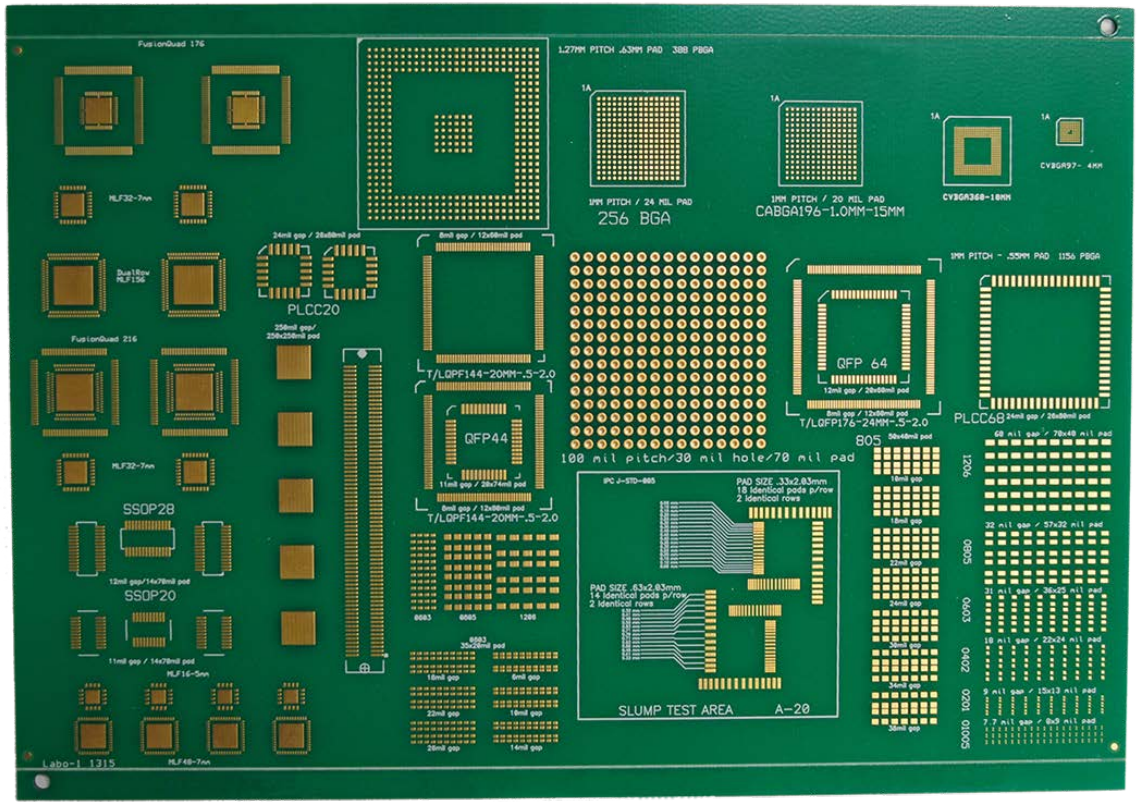
Environment Controlled at

25.4°(C)-77.4°(F) at 59% RH

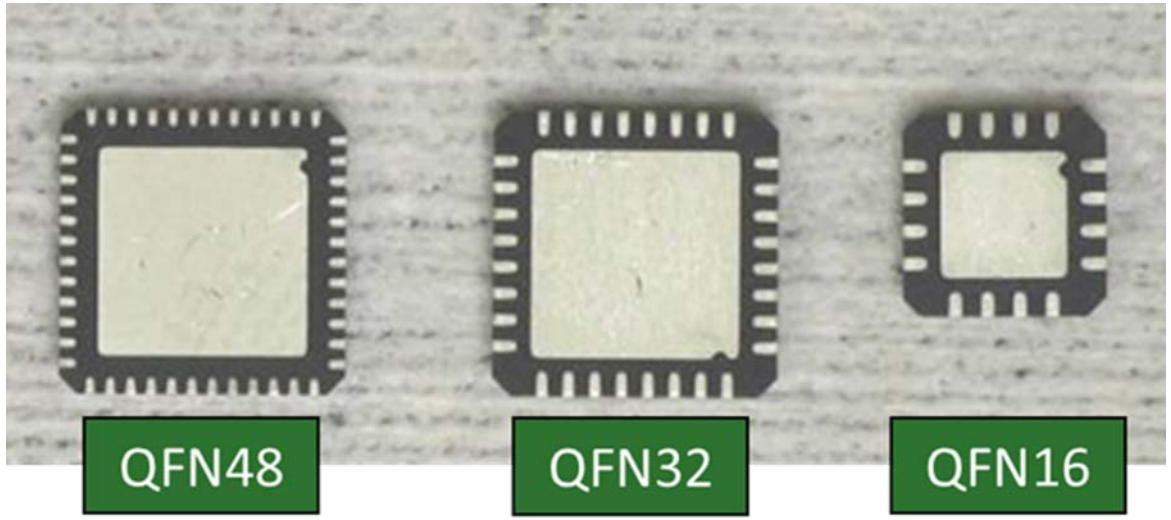
Test Vehicle - PCB

- The test PCB design was a commercially available print test board with four samples of the three components analyzed. The 8.5”x 6” PCBs were constructed of high Tg laminate, used an electroless nickel immersion gold (ENIG) final finish, and were all new.



Test Vehicle – Components

- Three packages were analyzed, shown left-to right - MLF48, 7X7mm; MLF32, 7x7mm; and MLF16, 5x5 mm. All MLFs were from the same manufacturer and respective lots, with 100% matte tin finish over copper lead frames.



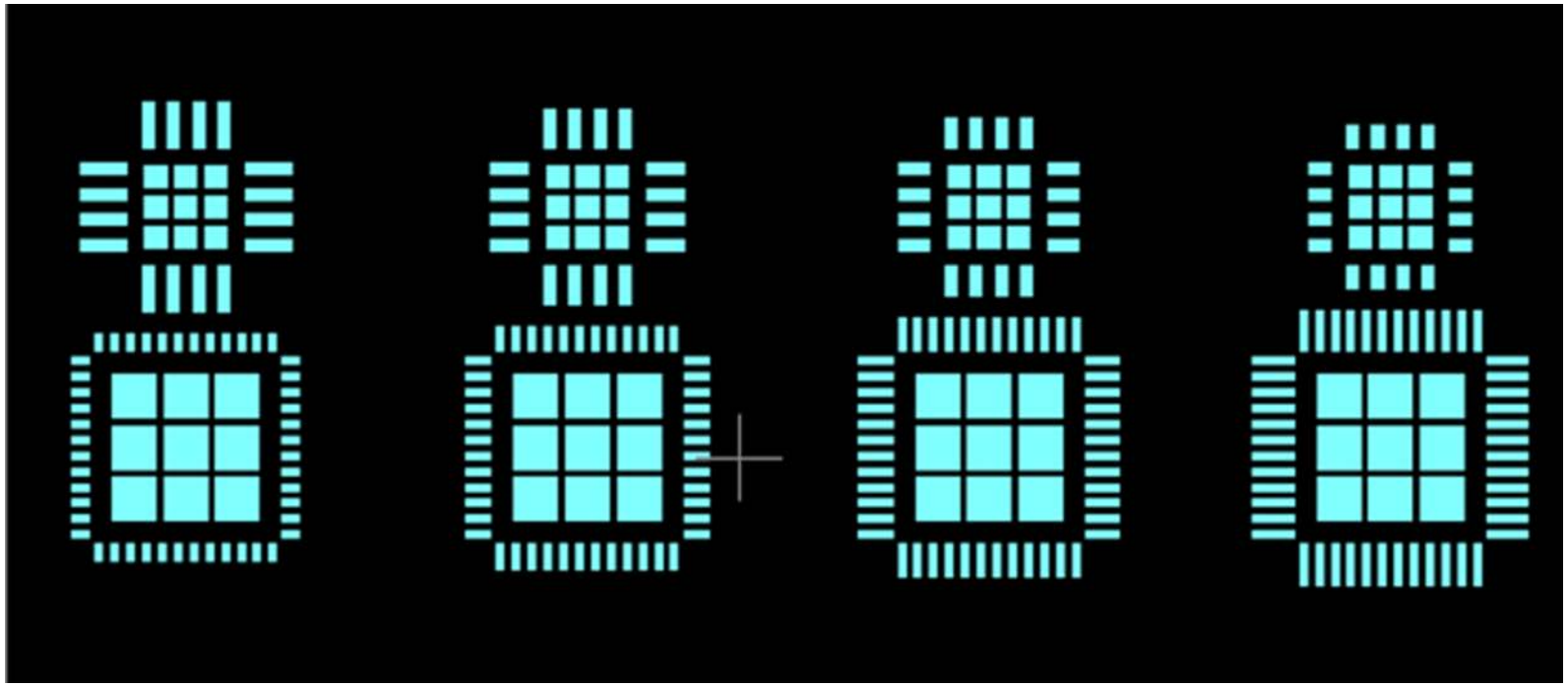
Component Type	Weight	Pitch
QFN MLF48	0.0585 gr	0.021”
QFN MLF32	0.1275 gr	0.027”
QFN MLF16	0.0585 gr	0.031”

Test Vehicle – Solder Paste

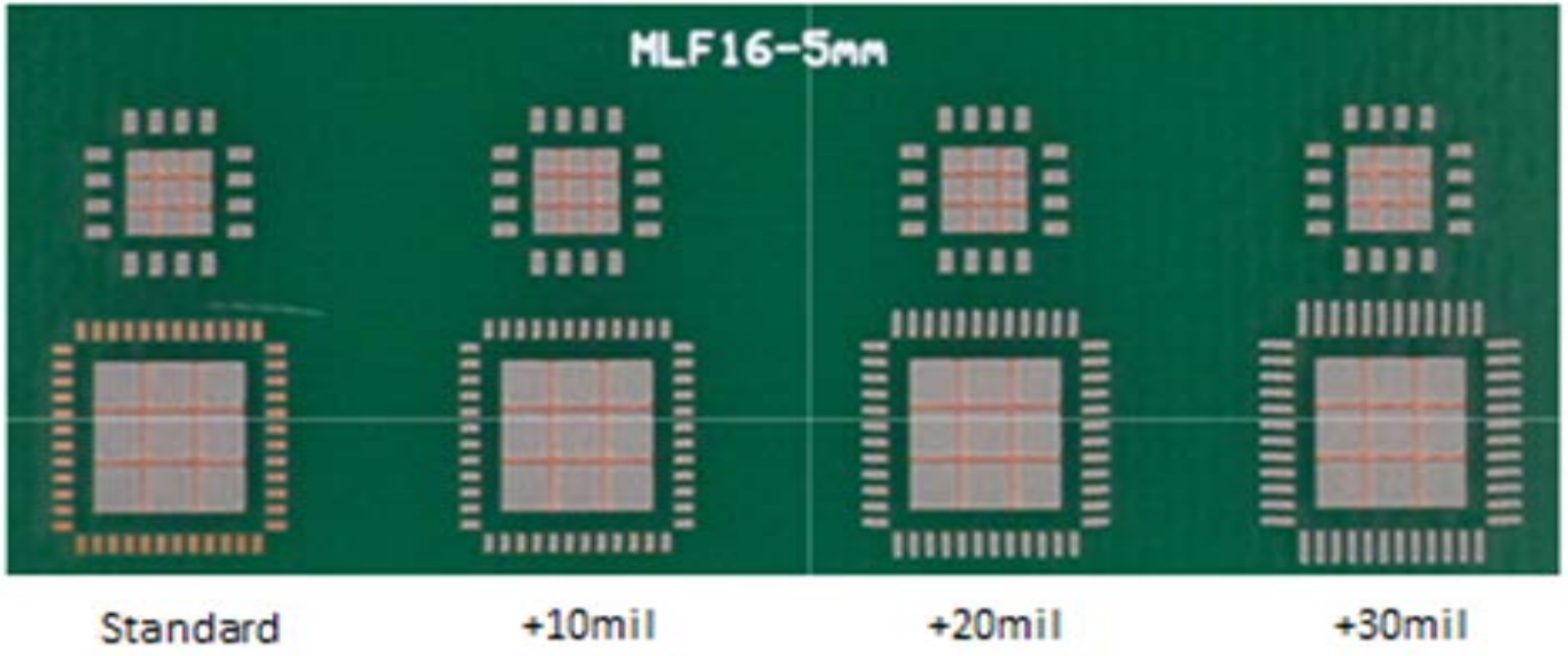
- Established No Clean SAC305 Type 4 which has consistently exhibited relatively low voiding performance.

Test Vehicle - Stencil

- 4mm, premium stainless steel, diode laser cut with fluoropolymer nanocoating.



I/O Overprint Design



1st QFN, I/O apertures as original design 1:1, Standard design

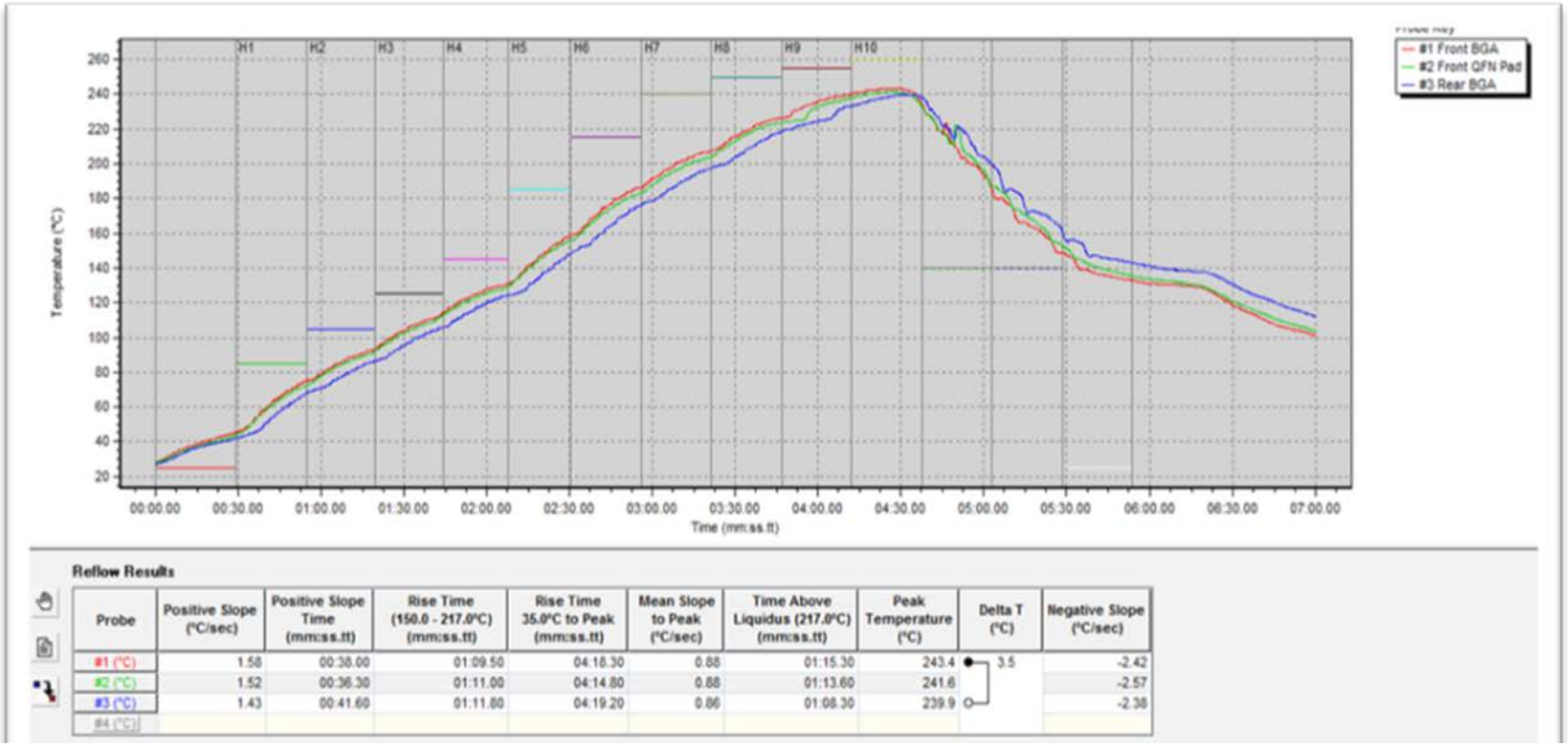
2nd QFN, I/O apertures with 0.010” overprint, +10Mil design

3rd QFN I/O apertures with 0.020” overprint, +20Mil design

4th QFN I/O apertures with 0.030” overprint, +30Mil design

Reflow Profile

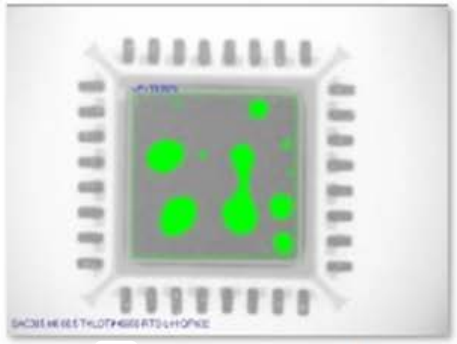
- Ten-zone convection oven in ambient air with linear (RTS) profile selected as they generally produce more voids than soak profiles.

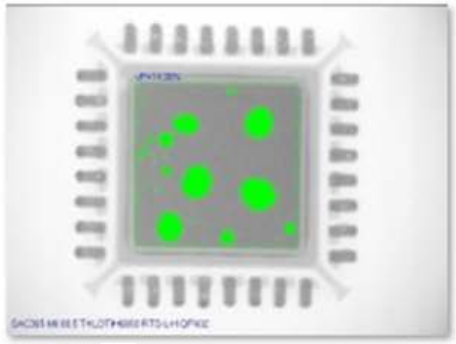


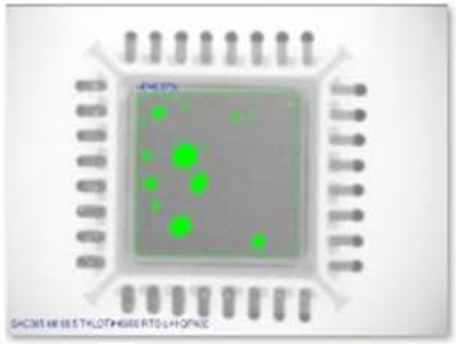
Reflow Profile - Long RTS (4.5 min) with Standard Slope (< 2.0) and Standard TAL (~75 sec)

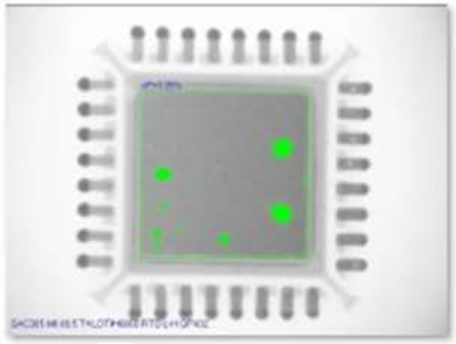
X-Ray

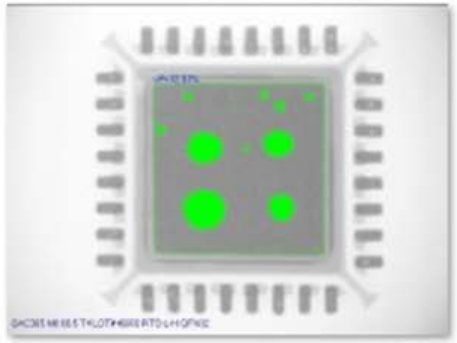
- An automated high-resolution, transmission X-ray inspection system was used to characterize the voids. The settings used were 75 Kv and .075mA, or 5.6 watts. The results were accumulated and processed using production statistical software.

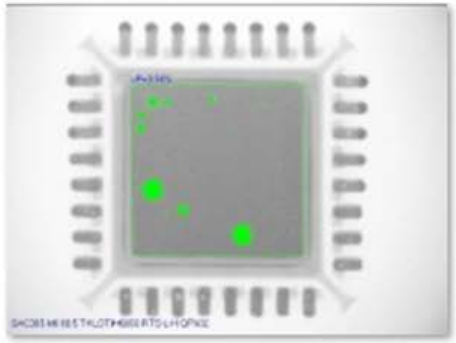

SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#19 QFN32-1 STD_IO 19.06%

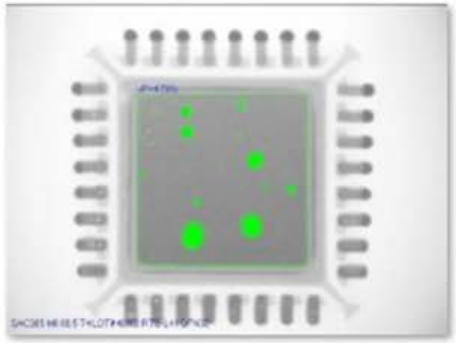

SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#19 QFN32-2 IO_10MIL 14.36%

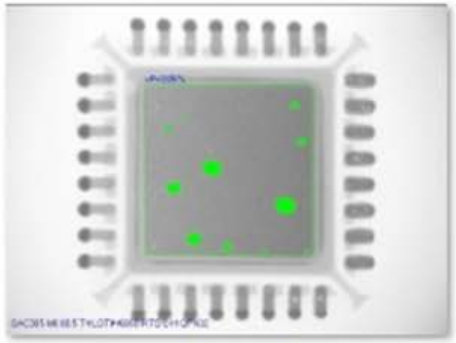

SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#19 QFN32-3 IO_20MIL 6.37%


SAC305 88.5 T4 QFN I-O EXP-II RTS-L-H
PCB#19 QFN32-4 IO_30MIL 3.35%

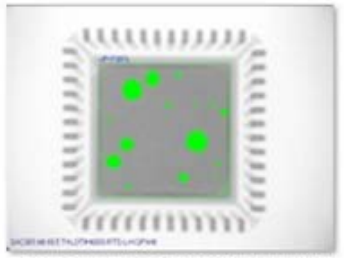
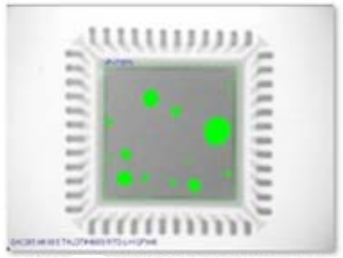
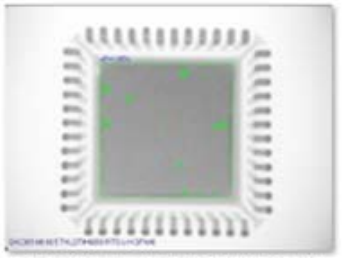
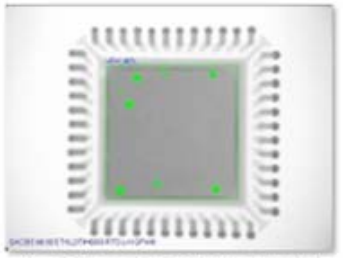
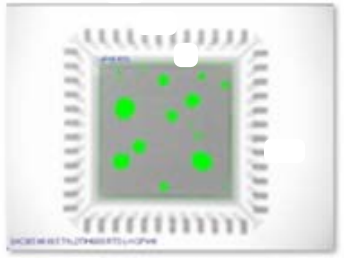
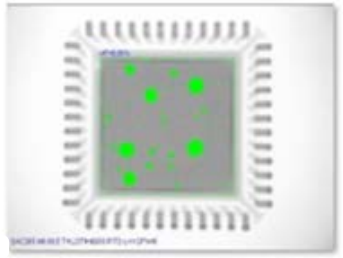
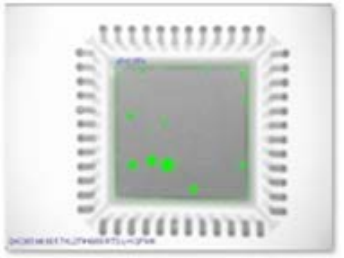
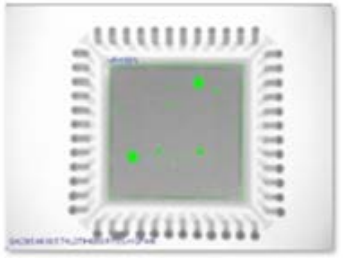
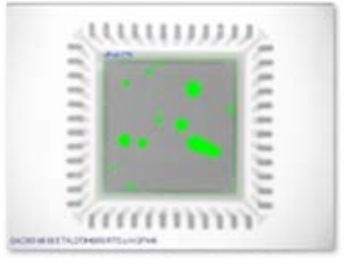
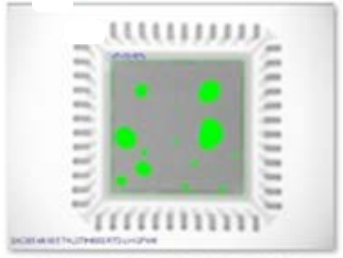
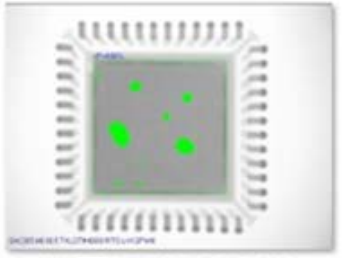
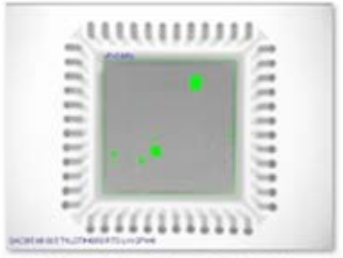




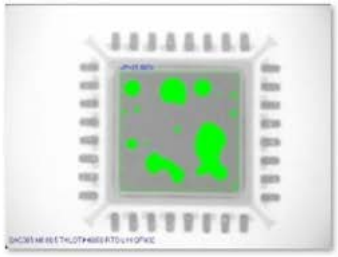
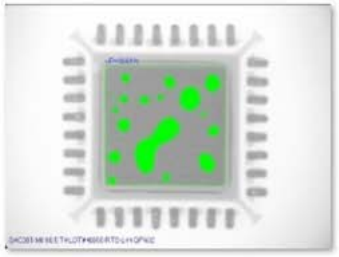
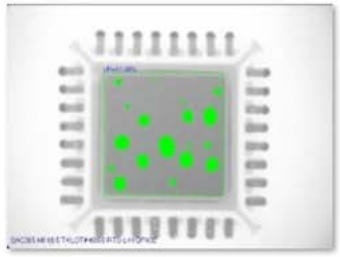
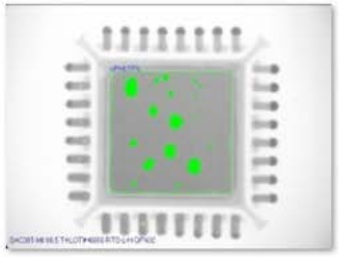
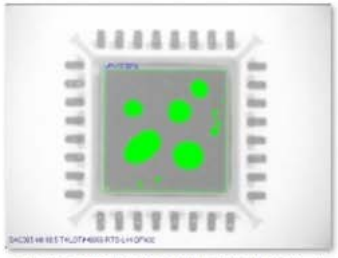
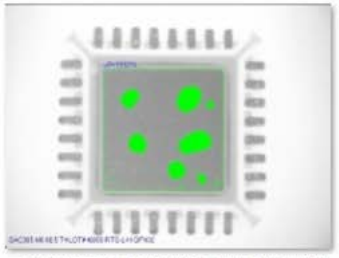
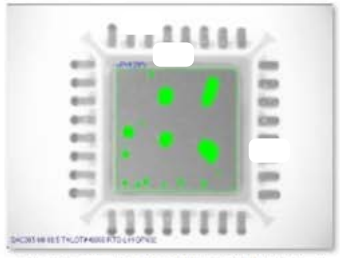
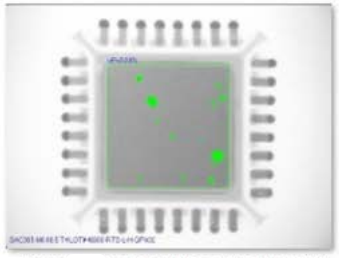
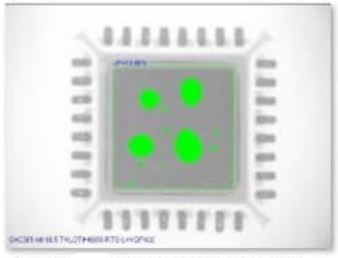
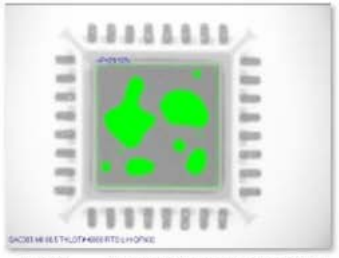
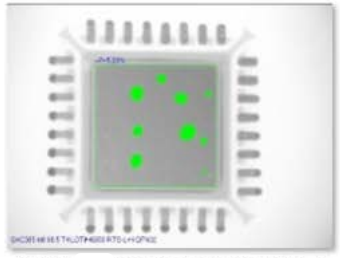
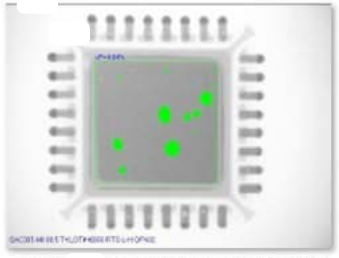




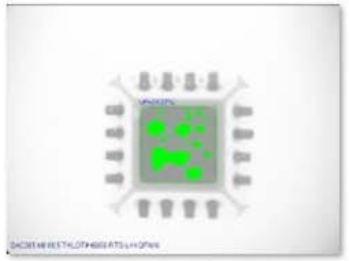
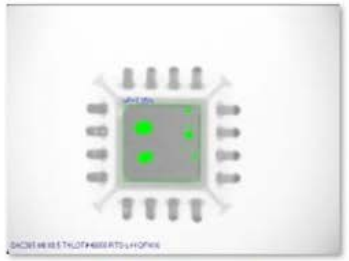
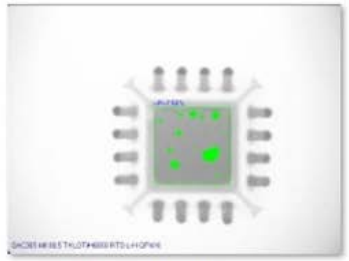
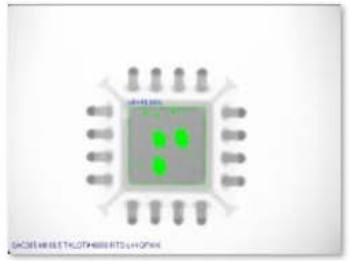
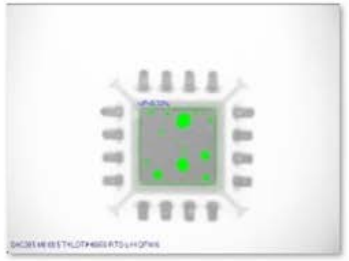
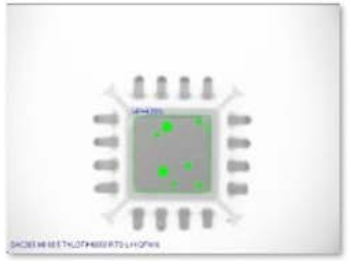
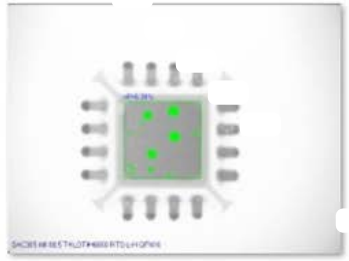
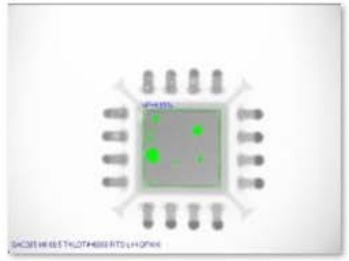
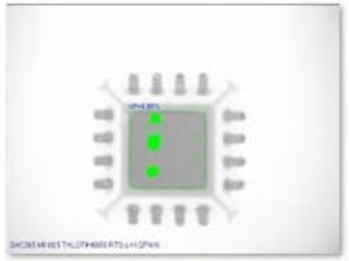
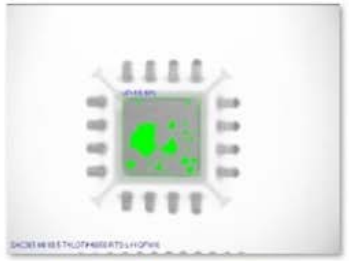
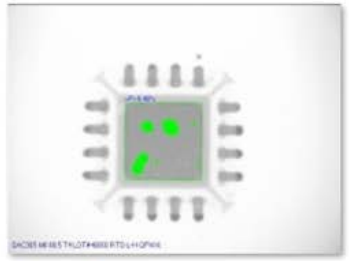
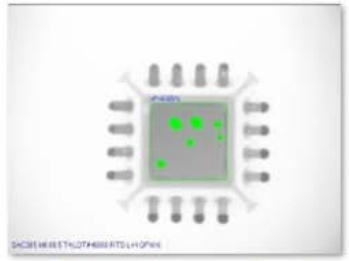
QFN48 Average Voiding

1:1	10 mil	20 mil	30 mil
8.99%	7.82%	3.99%	3.46%
			
SAC305 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN48-1 STD_IO 7.68%	SAC30[illegible]8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN48-2 IO_10MIL 7.83%	SAC30[illegible]8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN48-3 IO_20MIL 1.05%	SAC305 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN48-4 IO_30MIL 1.46%
			
SAC30 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN48-1 STD_IO 8.43%	[illegible]C30[illegible]8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN48-2 IO_10MIL 6.86%	SAC30[illegible]8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN48-3 IO_20MIL 2.25%	SAC305 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN48-4 IO_30MIL 1.50%
			
SAC30 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN48-1 STD_IO 6.17%	SAC30[illegible]8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN48-2 IO_10MIL 10.43%	SAC305 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN48-3 IO_20MIL 4.66%	SAC30[illegible]8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN48-4 IO_30MIL 1.84%

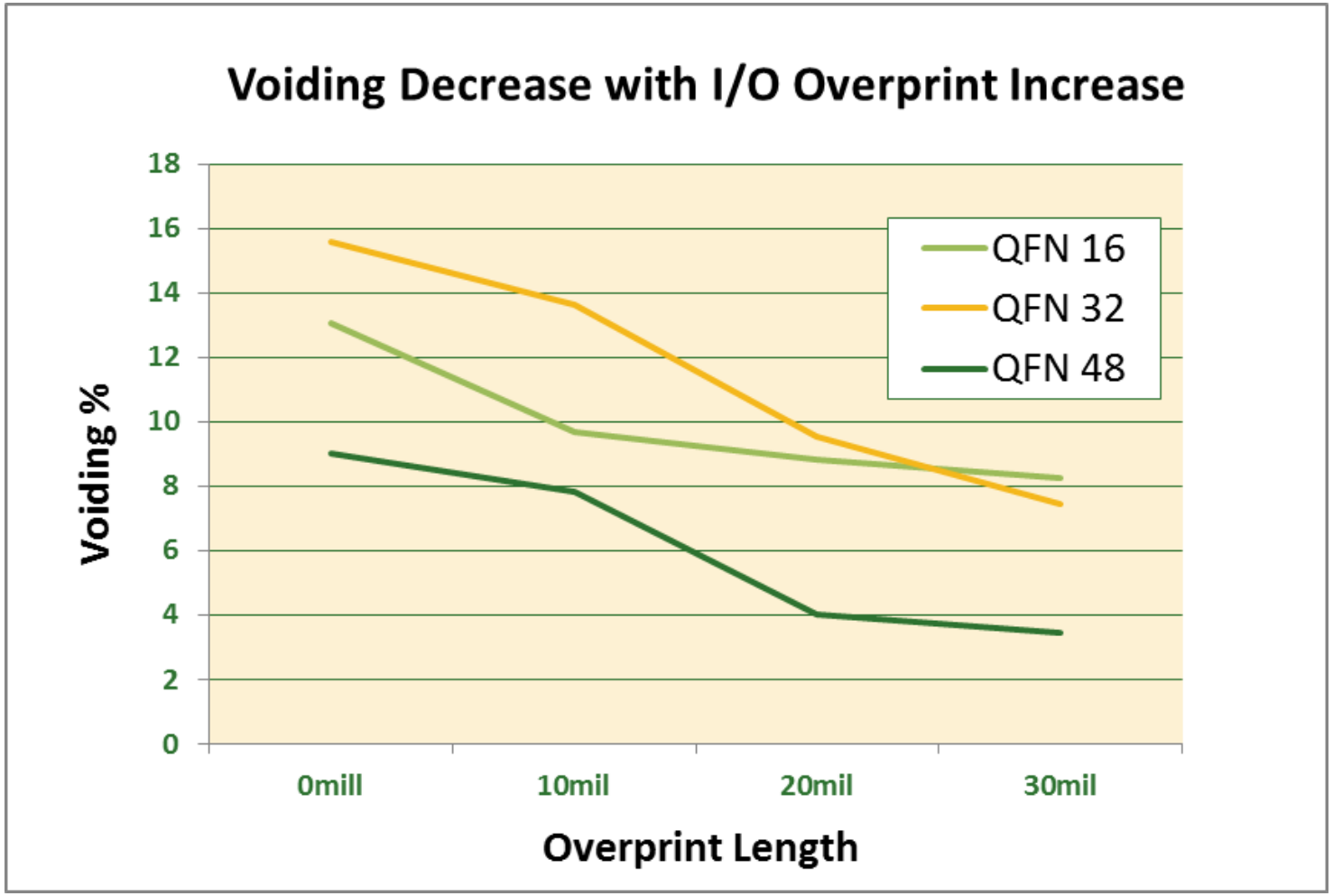
QFN32 Average Voiding

15.58%	13.63%	9.52%	7.45%
			
SAC305 3.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN32-1 STD_IO 21.80%	SAC30! 38.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN32-2 IO_10MIL 18.61%	SAC30! 38.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN32-3 IO_20MIL 11.38%	SAC30! 38.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN32-4 IO_30MIL 6.77%
			
SAC305 3.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN32-1 STD_IO 17.32%	SAC30! 38.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN32-2 IO_10MIL 13.52%	SAC305 3.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN32-3 IO_20MIL 9.29%	SAC30! 38.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN32-4 IO_30MIL 2.24%
			
SAC305 3.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN32-1 STD_IO 13.49%	SAC30! 38.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN32-2 IO_10MIL 29.12%	SAC305 3.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN32-3 IO_20MIL 5.23%	SAC30! 38.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN32-4 IO_30MIL 4.94%
1:1	10 mil	20 mil	30 mil

QFN16 Average Voiding

1:1	10 mil	20 mil	30 mil
13.04%	9.66%	8.83%	8.25%
			
SAC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN16-1 STD_IO 24.27%	SAC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN16-2 IO_10MIL 7.35%	SAC305 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN16-3 IO_20MIL 7.58%	SAC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#7 QFN16-4 IO_30MIL 10.90%
			
SAC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN16-1 STD_IO 9.33%	SAC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN16-2 IO_10MIL 4.70%	SAC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN16-3 IO_20MIL 6.39%	AC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#8 QFN16-4 IO_30MIL 4.95%
			
SAC305 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN16-1 STD_IO 6.86%	SAC305 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN16-2 IO_10MIL 18.44%	SAC30 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN16-3 IO_20MIL 9.48%	SAC30! 8.5 T4 QFN I-O EXP-II RTS-L-H PCB#9 QFN16-4 IO_30MIL 6.56%

Results and Discussion



Results and Discussion

- The hypothesis stated that higher volumes of solder paste on the I/O pads help "lift" the component above the center pad's solder paste to enable better outgassing before the center pad paste reaches liquidus temperature.
- It is impossible to measure the small height differential of the liquidus deposits during the reflow process. They are calculated theoretically using the following assumptions to simplify:
  - The volume of the solder (metal) is 50% of the volume of the solder paste overprint.
  - The overprint coalesces fully onto the pad.
  - The height is determined by dividing the calculated volume by the I/O pad area.

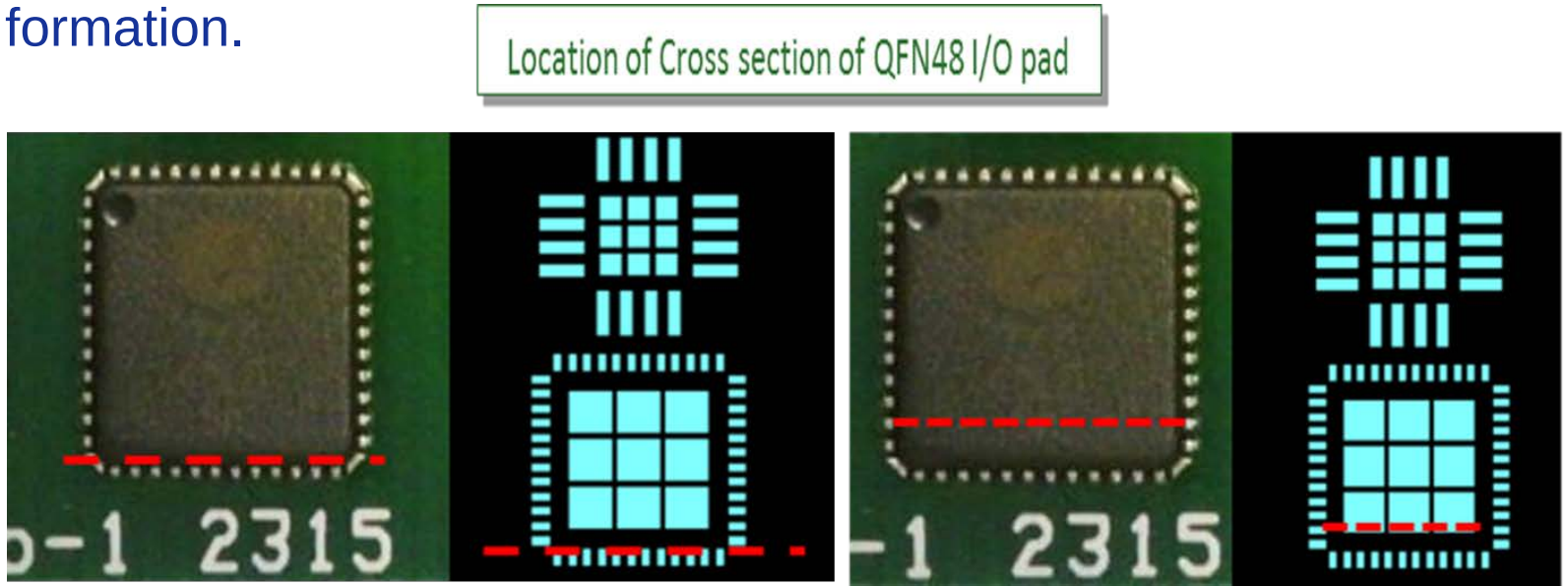
Component Size	Extra Standoff from I/O Overprint (mils)			
	0mill	10mil	20mil	30mil
MLF 16	0	0.93	1.85	2.78
MLF 32 & 48	0	0.73	1.45	2.18

Results and Discussion

- The three packages tested all showed decreased voiding as overprint increased.
- The two larger devices exhibited similar trends with respect to decreased voiding, but the smaller package did not exhibit as much void reduction.
- Three possible reasons for the different behavior in the smallest package:
  - The smaller package outline and lower thermal mass result in a shorter outgassing time between the I/O pads reaching liquidus and the center pad reaching liquidus.
  - The I/O pads are smaller on the 16-pin device than the 32 and 48 pin devices. Therefore, less overprint is needed to lift the package to the height necessary to achieve the improved outgassing.
  - A mathematical relationship may exist between the ratio of areas of the I/O pads and center pad, the I/O prints and the center pad print, or the perimeters of the I/O and center pads, based on buoyancy forces prior to wetting or surface tension during wetting.

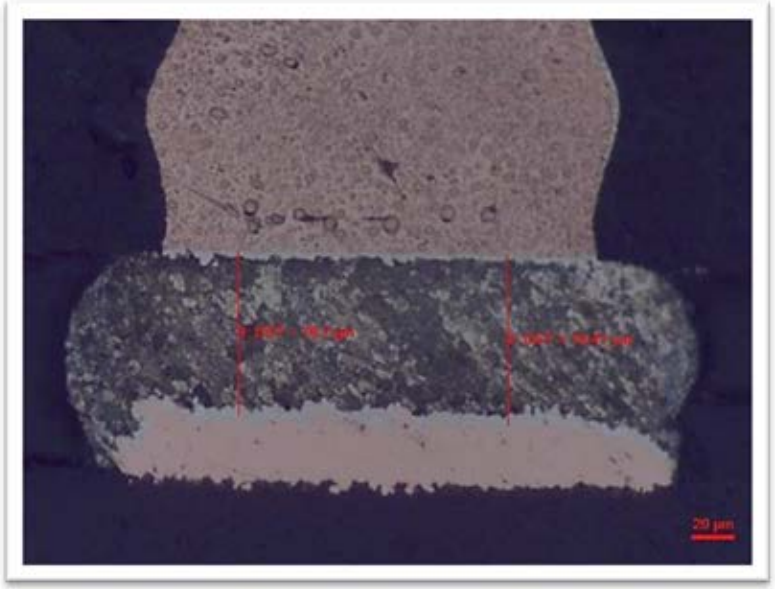
Results and Discussion

- Solder Joint Formation
  - Samples were cross-sectioned in two section views to examine the solder joint formation on both the I/O pads and the center pad. The first section view is through a row of leads to measure multiple I/O joint heights.
  - The second was through the leads and center pad to measure both perimeter and center solder joint heights and evaluate solder fillet formation.

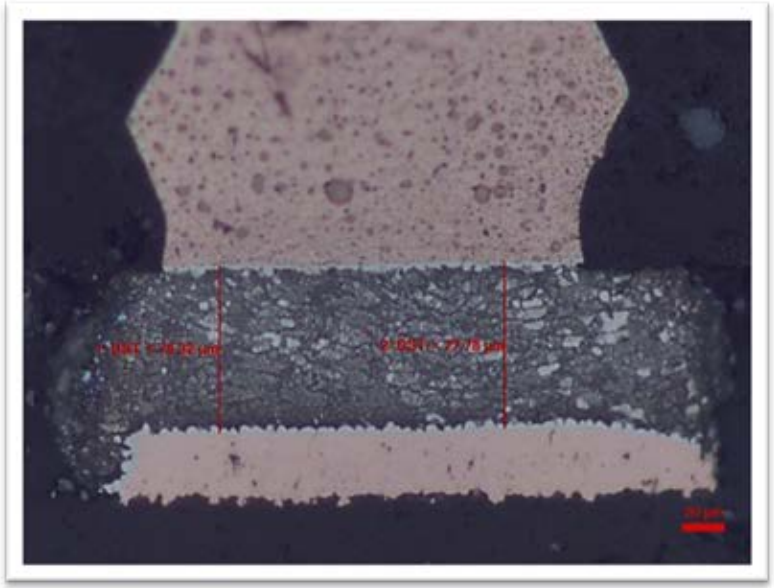


Component Height

QFN 48



No Overprint
78.05µm

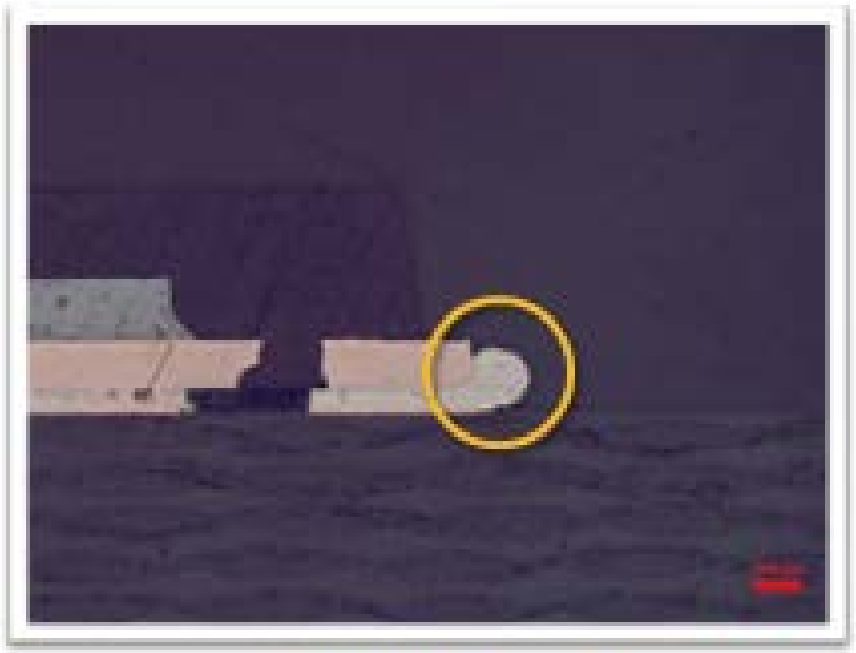


30mil Overprint
78.06µm

Solder joint heights (thickness) on I/O pad are nearly identical despite a 2.5% increase in paste volume.

Solder Joint Formation
QFN16

No Overprint
Typical Solder Fillet



30mil Overprint
Potential Excessive

Conclusions

- Voids were reduced to levels below 10% on all components with the QFN48 having the most dramatic. The largest void measured with +30 mils overprint (5.28%) is approximately the same size as the smallest void measured (5.22%) with the standard 1:1 print.
- Each package size responded differently. The smallest package did not appear to benefit from longer overprints as much as the larger packages did.
- The temporary standoff generated by the I/O overprints raise the component approximately 1-1.5 mil promoting outgassing before wetting and collapse.
- The impact of reflow profile on the void reduction effect is unclear as only one profile was tested. The profile used is considered the most challenging for void reduction and represents a common worst case scenario.

Future Work

- This study was a screening test establishing the efficacy of the I/O aperture technique.
- Further testing will assess the impact of other variables on the effect of the I/O overprint technique, including reflow profile, PCB surface finish and component type.
- Field implementation is underway to determine if the lab results are reproducible on the assembly line, and the extent to which this new I/O design can limit voiding in a production environment.