

# Status and Outlooks of Flip Chip Technology

John H. Lau

ASM Pacific Technology, Hong Kong

john.lau@asmpt.com

## Abstract

Status of flip chip technology such as wafer bumping, package substrate, flip chip assembly, and underfill will be reviewed in this study. Emphasis is placed on the latest developments of these areas in the past few years. Their future trends will also be recommended. Finally, the competition on flip chip technology will be briefly mentioned.

## Introduction

The flip chip technology was introduced in the early 1960s for solid logic technology, which became the logical foundation of the computer line [1]. Figure 1(a) shows the first flip chip with three terminal transistors, which are Ni/Au plated Cu balls embedded in a Sn-Pb solder bump on the three I/O pads of transistor. A Cr-Cu-Au adhesion/seed layer is deposited between the Al-Si contact pads on the Si chip and the solder bump. Figure 1(b) shows the first flip chip assembly (three chips) on a ceramic substrate.

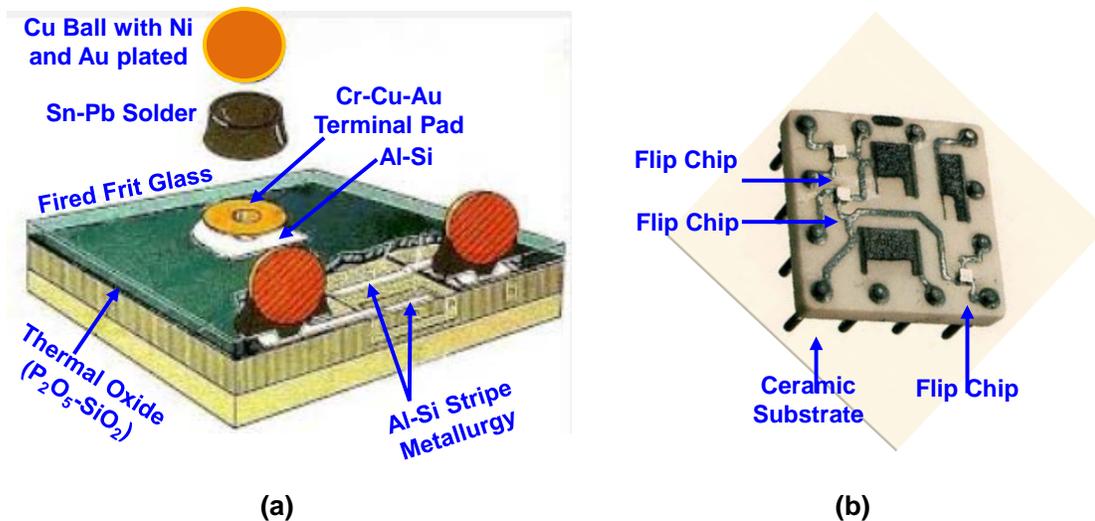


Figure 1 - (a) First flip chip component with 3 terminal transistors. (b) First flip chip assembly (3 chips) on a ceramic substrate

As the I/Os increase, the Cu ball is replaced by solder bump. The controlled-collapse chip connection (C4) technology [2] utilizes high-lead solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and all solder joints are made simultaneously by reflowing the solder.

Today, the applications of flip chip technology have been extended to [3, 4, 5] chip-to-chip, face-to-face, and face-to-back. Figure 2(a) shows a specific package [6]. It can be seen that the package is actually defined by two levels of nesting die. The three daughter dies are flip-chip attached to the larger mother die which is then attached to the largest grandma die. The grandma die is then flip-chip attached to the package substrate. The bumps between the daughter dies and the mother die are microbumps (Cu-pillar with solder cap). C4 bumps are used between the mother die and grandma die, and between the grandma die and package substrate. Figure 2(b) shows 3D IC integration technology for the DDR4 (double data rate type 4) DRAM (dynamic random access memory) of the 128GB RDIMM (dual inline memory module). It can be seen that the DRAMs are bonded (stacked) with microbumps and NCF (non-conductive film).

Flip chip technologies have been used extensively for the processors of mainframe computers, servers, personal computers, notebooks, smartphones, tablets, games, etc., the application specific integrated circuits (ASICs) of networking, telecommunications, etc., and the memories of data storage devices, etc. Most of the flip chip assemblies are mass reflowed. Recently, because of the requirements of higher functionalities of the chips and shrinking the chips' area, the number of pin-outs of the processors, ASICs, and memories increases and their pitch (or the spacing between the pin-out pads) decreases.

Also, because of the trends of smaller form factors for mobile (e.g., smartphones and tablets) and portable (e.g., notebooks) products, the thickness of the chips and package substrates must be as thin as possible. Higher pin counts, tighter pitches, thinner chips, and thinner package substrates lead to the necessity of the thermocompression bonding (TCB) method for flip-chip assemblies. In this study, besides mass reflow, various TCB techniques are mentioned.

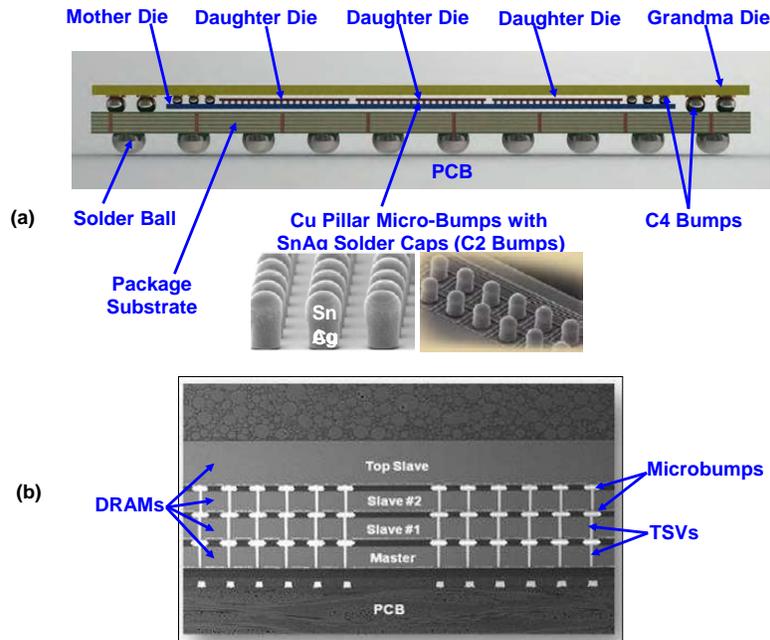


Figure 2 - (a) 3D IC packaging and (b) 3D IC integration

Recent advances in high-density and low-cost package substrates have promoted more flip chip applications. In this study, the organic build-up substrate, through-silicon via (TSV)-interposer, TSV-less interposer, coreless substrate, bump-on-lead (BOL), and embedded-trace-substrate (ETS) will be discussed.

In order to enhance the solder joint reliability of flip chip assemblies, underfill is a must, especially for organic package substrate. In this study, the pre-assembly underfill such as the no-flow underfill (NUF), nonconductive paste (NCP), and nonconductive film (NCF) will be discussed. Also, the post-assembly underfill such as the capillary underfill (CUF) and molded underfill (MUF) will be examined. Since wafer bumping is the mother of flip chip technology, it will be briefly mentioned first.

### Wafer Bumping

There are many ways to perform the wafer bumping (at least 12 are shown in [7]), and the most common method is by electrochemical deposition (ECD) or electroplating [8]. Stencil printing method [9, 10] is also used for wafer bumping but it will not be presented herein.

**C4 Bumps.** Usually the pad size is equal to  $100\mu\text{m}$  and the target bump height is equal to  $100\mu\text{m}$ . After redefining the passivation opening (usually it is not required), either Ti or TiW ( $0.1\text{--}0.2\mu\text{m}$ ) are sputtered over the entire surface of the wafer first, followed by  $0.3\text{--}0.8\mu\text{m}$  of Cu. Ti-Cu and TiW-Cu are called under bump metallurgy (UBM). In order to obtain  $100\mu\text{m}$  bump height, a  $40\mu\text{m}$  layer of resist is then overlaid on the Ti-Cu or TiW-Cu and a solder bump mask is used to define (ultraviolet exposure) the bump pattern as shown in steps #1–4 in Figure 3. The opening in the resist is  $7\text{--}10\mu\text{m}$  wider than the pad opening in the passivation layer. A  $5\mu\text{m}$  layer of Cu is then plated over the UBM, followed by electroplating the solder. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve the target ( $100\mu\text{m}$ ), the solder is plated over the resist coating by about  $15\mu\text{m}$  to form a mushroom shape. The resist is then stripped off and the Ti-Cu or TiW-Cu is removed with a hydrogen peroxide or plasma etching. The wafer is then reflowed with flux, which creates smooth truncated spherical solder C4 bumps, due to surface tension as shown in steps #5–8 on the upper right-hand side of Figure 3 [7, 8].

**C2 (Cu-Pillar with Solder Cap) Bumps.** Because of higher pin-count and tighter pitch (smaller spacing between pads), there is a possibility of shorting the adjacent solder C4 bumps. Wire interconnects [11] and Cu-pillar with solder cap [12, 13] can be a solution. The fabrication process is basically the same as that of the C4 bumps except electroplating the Cu instead of solder as shown in step #5 on the lower right-hand side of Figure 3. It is followed by electroplating the solder cap and then

reflowing the solder with flux. Because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the self-alignment of the Cu pillar with the solder cap bump and therefore, it is sometimes called a C2 (chip connection) bump. Besides being able to handle finer pitch, C2 bumps also provide better thermal and electrical performances than C4 bumps. This is because the thermal conductivity (W/m K) and electrical resistivity ( $\mu\Omega\text{m}$ ) of Cu (400 and 0.0172) are superior than those (55–60 and 0.12–0.14) of solder.

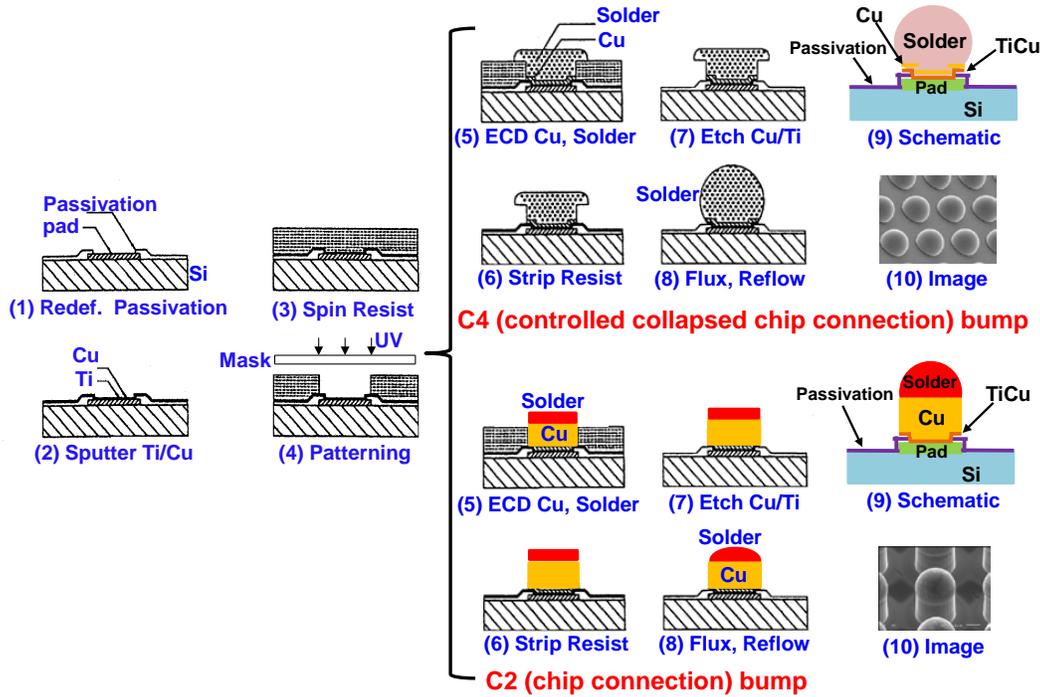
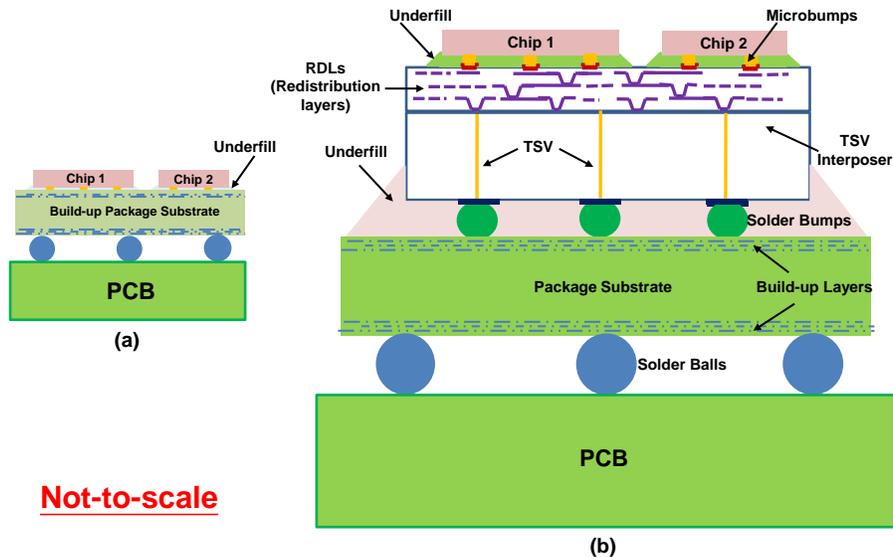


Figure 3 - Wafer bumping by ECD or electroplating method for C4 and C2 bumps

### Flip Chip Package Substrate

In the past few years, tremendous efforts have been devoted to enhance/advance the capabilities of the conventional low-cost build-up organic package substrates by increasing the number of build-up layers, fabricating thin-film layers on top of the build-up layer, shrinking the dimensions of the metal line width and spacing, reducing the pad size and pitch, eliminating the core, making the BOL, and laminating the ETS. For silicon substrates, first come with the TSV-interposer and the future trend is for TSV-less interposer. Ceramic substrate will not be discussed herein.



**Not-to-scale**

Figure 4 - (a) Build-up package substrate for flip chips. (b) Build-up substrate with TSV-interposer for flip chips  
Surface Laminar Circuit (SLC) Technology.

Almost 25 years ago, the SLC technology was invented [14, 15], which formed the basis of today's very popular low-cost organic package substrates, Figure 4(a), with build-up layers vertically connected through microvias [16] to support flip

chips. There are two parts of the SLC technology: one is the core substrate and the other is the SLC for the signal wiring. The core substrate is made by the ordinary glass epoxy panel. However, the SLC layers are sequentially built up with the dielectric layers made of photo sensitive epoxy and the conductor plane of copper plating (semi-additive technique). In general, a package substrate with twelve layers (e.g., two core-layers and ten build-up layers (5-2-5)) and 10µm-line width and spacing is more than adequate to support most of the chips.

**TSV-Interposers.** In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced field programmable gate array (FPGA), even a twelve build-up layers (6-2-6) package substrate is not enough to support the chips and a TSV interposer, Figure 4(b), is needed [17, 18]. For example, the left-hand side of Figure 5 shows the sliced FPBG chip on wafer on substrate (CoWoS). It can be seen that the TSV interposer has four top RDLs (redistribution layers): three Cu damascene layers and one aluminum layer. The 10,000+ of lateral interconnections between FPGA chips are connected mainly by the RDLs of the interposer.

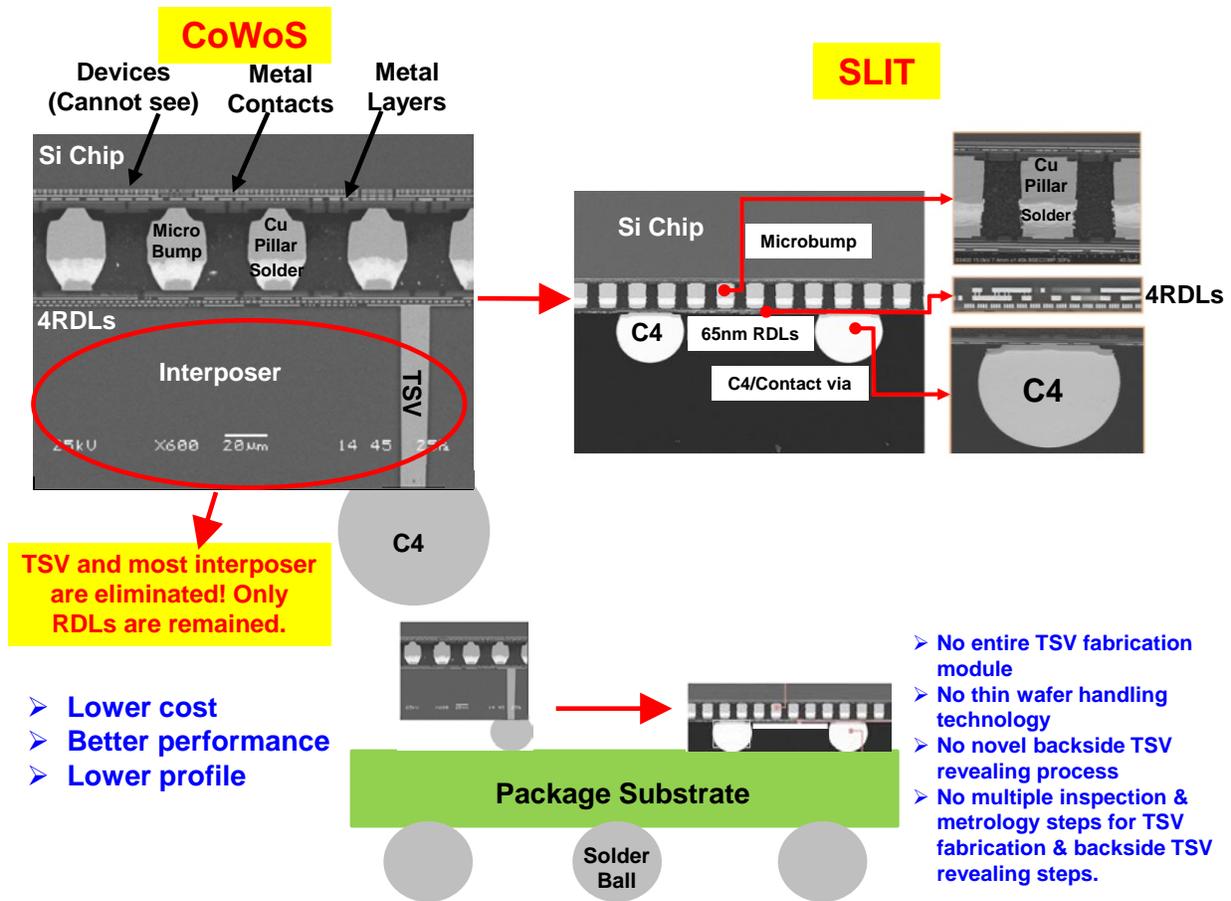


Figure 5 – CoWoS (left) and SLIT (right)

**TSV-Less Interposer: Silicon-Less Interconnect Technology (SLIT).** So far, TSV-interposer is very expensive [3-5]. In order to lower the cost, enhance the electrical performance, and reduce the package profile, in 2014 a TSV-less interposer was proposed for the sliced FPGA chips called SLIT [19]. The right-hand corner of Figure 5 shows the new packaging structure. It can be seen that the TSVs and most of the interposer are eliminated and only those four RDLs are kept to perform, mainly, the lateral communication of the sliced FPGA chips. Depending on the line-width/spacing of RDLs' conductive wiring, the fabrication method of RDLs can be either by using a polymer for the dielectric layer and ECD Cu for the conductive wiring (line-width/spacing ~5µm), or by using plasma enhance chemical vapor deposition to make the SiO<sub>2</sub> dielectric layer and Cu damascene + chemical-mechanical polishing (CMP) to make the conductive wiring (line-width/spacing <5µm). Figure 6 schematically shows the cross section of the SLIT.

**TSV-Less Interposer: Non-TSV Interposer (NTI).** In 2016, a similar paper was published [20] with more characterization results such as warpage data and called it non-TSV interposer (NTI).

**TSV-Less Interposer: Silicon Interposer-Less Integrated Module (SLIM).** In 2015, a very similar technology to SLIT was announced called SLIM [21].

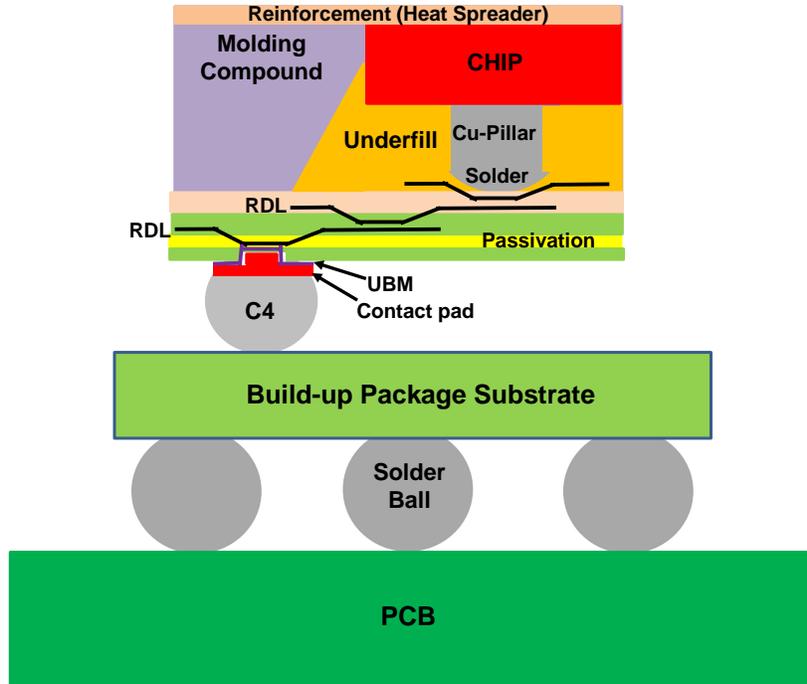


Figure 6 - SLIT

**TSV-Less Interposer: Embedded Multidie Interconnect Bridge (EMIB).** In September 2014, an EMIB [22] was proposed to replace the TSV-interposer. The lateral communication between the chips will be taken care of by the silicon embedded bridge and the power/ground and some signals will go through the vias of the organic package substrate to the PCB as shown in Figure 7 [23]. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB and the other is to make the substrate with EMIB. For making the EMIB, first build the RDLs (including the contact pads) on a Si-wafer by either polymer + ECD or Cu damascene + CMP methods. Then, thin down the wafer to ~60µm. Finally, attach the non-RDL side of the Si-wafer to a die-attach film and then singulate the Si-wafer.

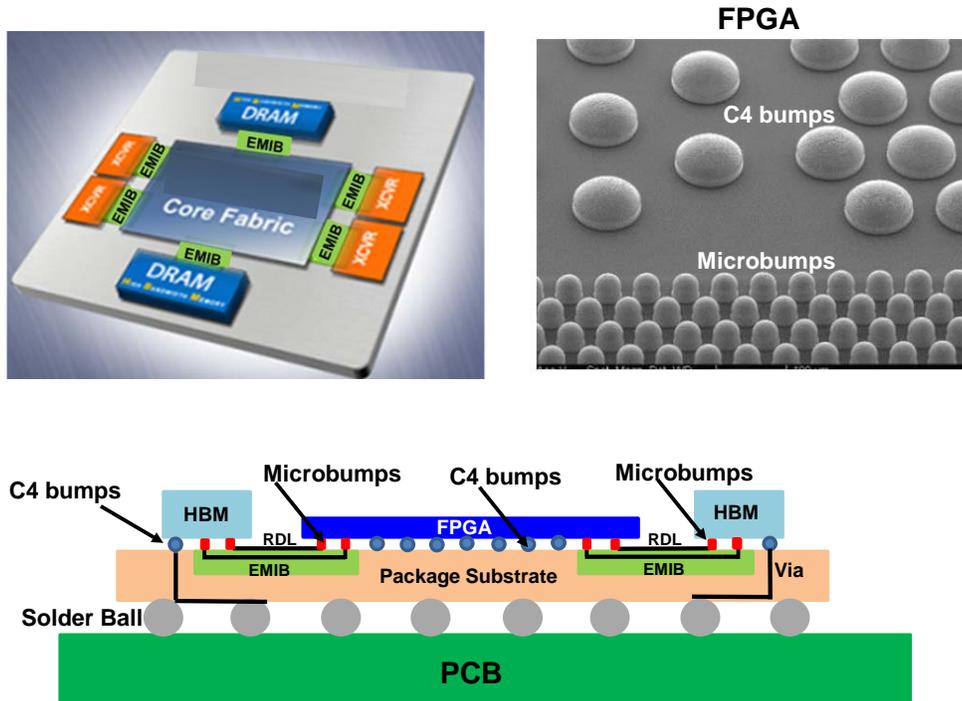
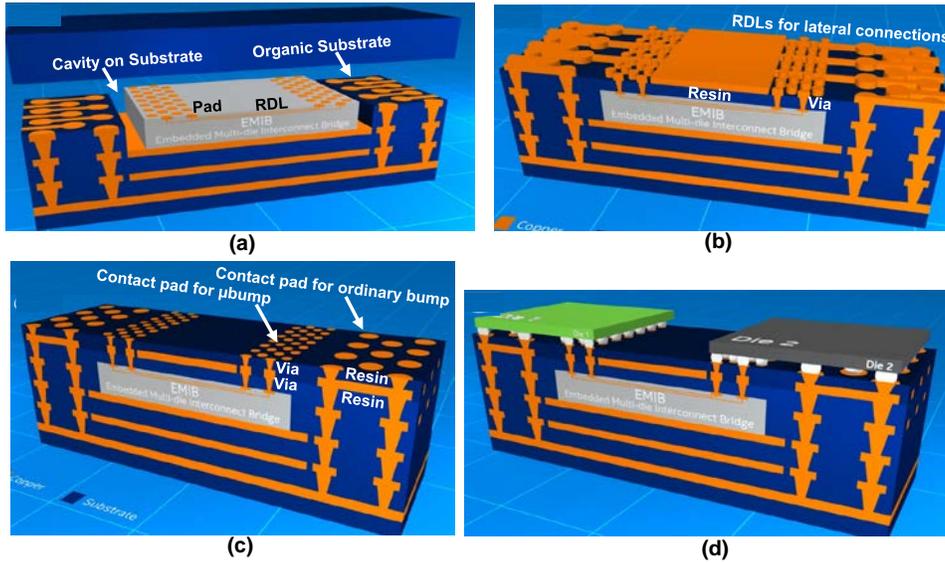


Figure 7 - High bandwidth communications between the FPBA and HBMs by EMIB

For making the substrate with EMIB, first place the simulated EMIB with the die-attached film on top of the Cu foil in the cavity of the substrate, Figure 8(a). It is followed by laminating a dielectric film on the whole organic package substrate. Then, drilling (on the dielectric film) and Cu plating to fill the holes (vias) are done to make connections to the contact pads

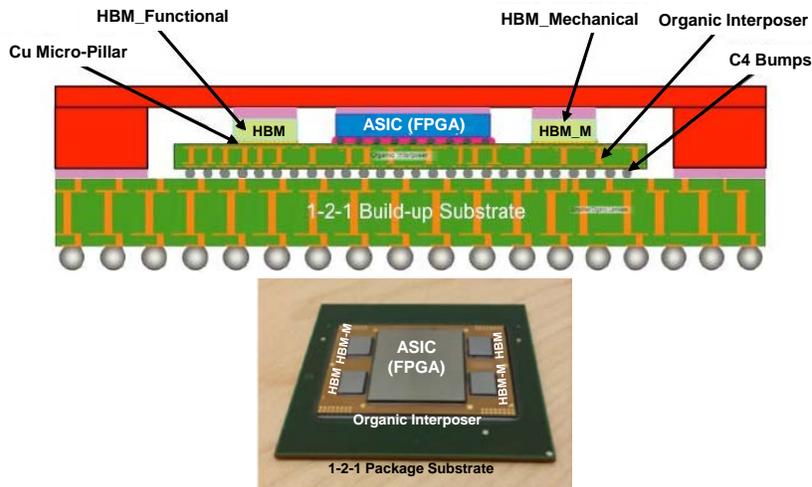


**Figure 8 - Simple process flow of the EMIB technology**

of the EMIB. Continue Cu plating to make lateral connections of the substrate as shown Figure 8(b). Then, it is followed by laminating another dielectric film on the whole substrate and drilling (on the film) and Cu plating to fill the holes and make contact pads, Figure 8(c). (Smaller pads on finer pitch are for microbumps while larger pads on gross pitch are for ordinary C4 bumps.) The organic package substrate with EMIB is ready for bonding of the chips as shown in Figure 8(d).

On November 9, 2015, the industry’s first heterogeneous system-in-package (SiP) devices were announced [24] that integrate stacked HBM (high bandwidth memory) with high-performance FPGAs and SoCs (system-on-chip) as shown in Figure 7. It can be seen that the lateral communications between the chips and the HBMs are taken care of by the EMIB and a TSV interposer is not needed.

**TSV-less Interposer: Organic Interposer.** Figure 9 shows a 3D SiP with a large organic interposer (instead of a TSV interposer) [25]. The organic interposer has a size of 38mm x 30mm x 0.4mm. The linewidth, spacing, and thickness of the front-side and back-side of the organic interposer are the same and are, respectively, 6μm, 6μm, and 10μm. A high-performance application-specific IC (ASIC) die measured at 19.1mm x 24mm x 0.75mm is attached on top of the organic interposer along with four HBM DRAM die stacks. The 3D HBM die stack with a size of 5.5mm x 7.7mm x 0.48mm includes one base buffer die and four DRAM core dice which are interconnected with TSVs and fine-pitch micro-pillars.



**Figure 9 – SiP with organic interposer**

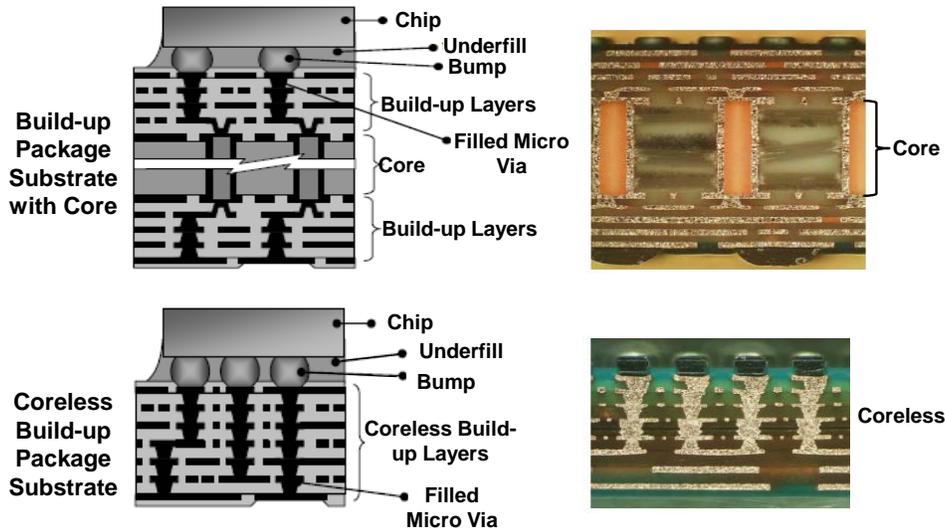


Figure 10 - (Top) flip chip on conventional build-up package substrate. (Bottom) flip chip on coreless substrate

**Coreless Substrate.** Coreless substrate was first proposed in 2006[26]. Figure 10 shows the comparison between the conventional organic package substrate with build-up layers and the organic coreless package substrate. It can be seen that the biggest difference is that there is not a core in the coreless package substrate and all the layers of the coreless package substrate are the build-up layers. The advantages of the coreless package substrate are: (a) because of eliminating the core, the cost of the coreless substrate is lower; (b) by eliminating the core, higher wiring ability can be achieved; (c) better electrical performance because of good high-speed transmission characteristic; and (d) definitely smaller form factor. On the other hand, the disadvantages are: (a) because of eliminating the core, the warpage of the coreless substrate is larger; (b) easier to have laminate chipping; (c) poor solder joint yield because of less substrate rigidity; and (d) new manufacturing infrastructure is necessary. In 2010, the first coreless package substrate was manufactured for the cell processor of a production game console device [27]. Even though coreless substrates have many advantages, they are not popular because of the warpage control issue. One of the key factors affecting the warpage is the coefficient of thermal expansion mismatch of substrate materials. Thus, a proper control of this factor will help reduce the warpage issue of coreless substrates. Another factor affecting the warpage is the package assembly. Thus, a proper package assembly warpage correction control (with vacuum and pressure) will help improve the warpage problem of coreless substrate.

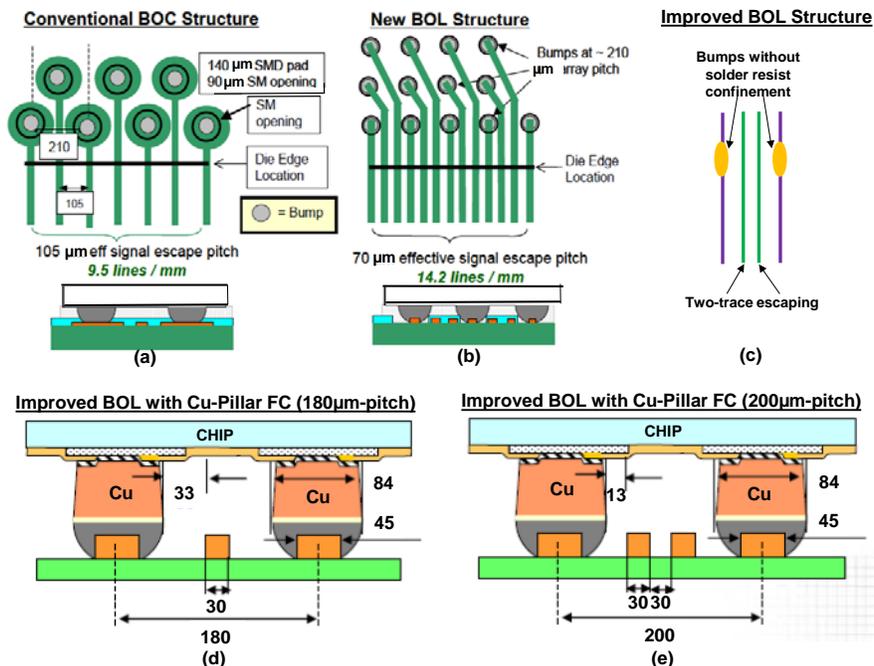
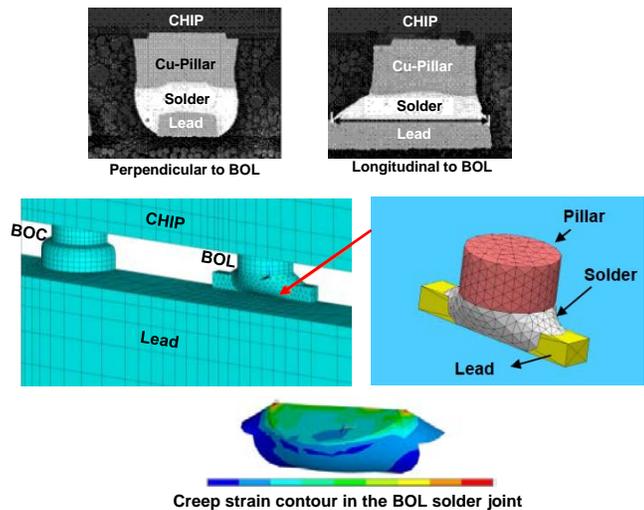


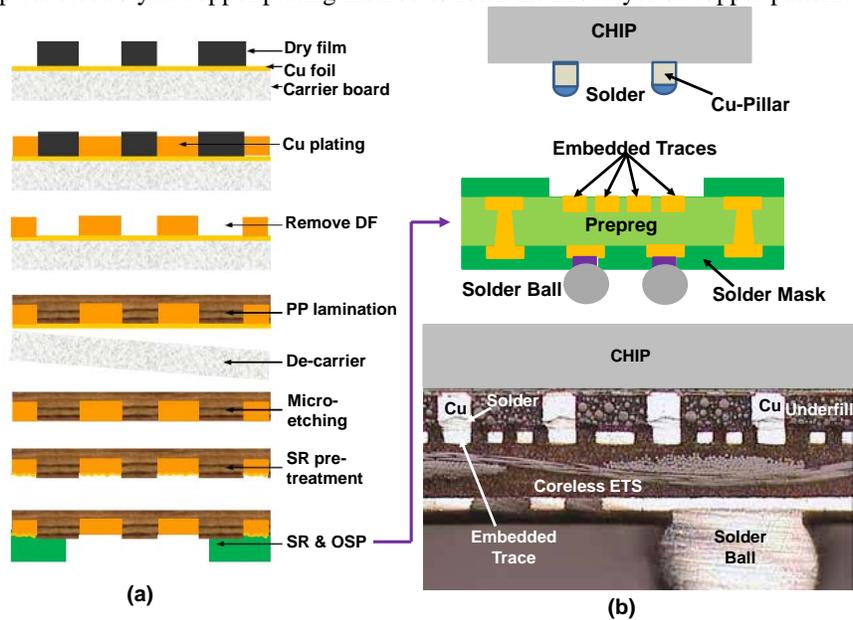
Figure 11 - BOL (a) conventional BOP, (b) new BOL, (c) improved BOL, (d) improved BOL with Cu-pillar flip chip (180μm-pitch), and (e) improved BOL with Cu-pillar flip chip (200μm-pitch)

**BOL.** BOL was patented in 2004 [28] and was used by other companies [29, 30]. A conventional bump-on-capture pad (BOC) or simply bump-on-pad (BOP) flip chip organic substrate layout is shown in Figure 11(a). It can be seen that the flip chip pads are on a 210 $\mu\text{m}$  area array pitch in an solder mask (SR) defined configuration with one signal escape between bump pads resulting in an effective escape pitch of 105 $\mu\text{m}$ . The BOL methodology is shown in Figure 11(b); here, the landing pad on the substrate is merely the trace (lead) itself, or a slightly widened version of the trace which results in freeing up of enough routing space to allow routing an additional trace between bumps thereby resulting in an effective escape pitch of 70 $\mu\text{m}$  without changing the design rules (trace width and space) of the substrate. The improved BOL structure is shown in Figure 11(c). It can be seen that the bump pads are without any solder resist confinement, i.e., open SR [29]. The test vehicles, Cu-column on BOL, used in Ref. [29] are shown in Figures 11(d) and 11(e). It can be seen that one trace between the 180 $\mu\text{m}$  bump pitch and up to two traces with the 200 $\mu\text{m}$  bump pitch can be comfortably routed. Typical cross sections of the perpendicular-to-BOL and longitudinal-to-BOL are shown in the upper portion of Figure 12. A 3D slide finite element model showing the BOL, BOC (or BOP), and solder joint is shown in the middle of Figure 12. The creep strain contours of the BOL solder joint are shown in the lower portion of Figure 12 [31] and are too small to create solder joint reliability problem under most conditions.



**Figure 12 - Images of the perpendicular-to-BOL and longitudinal-to-BOL. Finite element models and creep strain contours in the BOL solder joint**

**ETS.** ETS is one of the coreless substrates with fine linewidth/spacing embedding the top metal trace pattern into prepreg layer [32, 33]. The process flow of ETS is shown in Figure 13(a). It starts from a carrier board with a removable Cu foil. It is followed by using a typical electrolytic copper plating method to form the first layer of copper pattern.

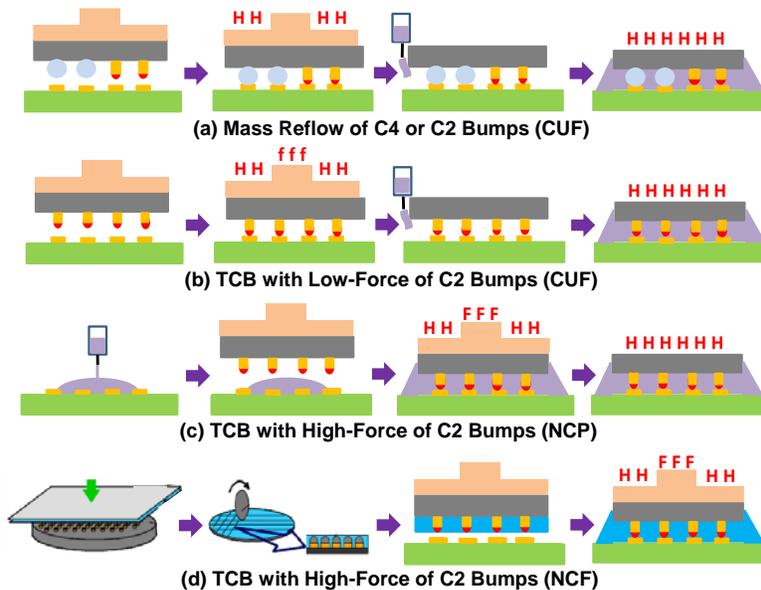


**Figure 13 - (a) Process flow for fabricating the ETS and (b) flip chip with C2 bumps on ETS assembly**

Then, laminate a prepreg on the copper pattern. It is followed by laser via drilling, electroless copper coating, dry film laminating, exposing and developing, second layer copper pattern plating, stripping, and micro etching. Once all the copper pattern layers have been completed, the carrier board will be removed. Since the Cu foil is connected to the first copper pattern, micro etching is necessary before SR coating. After the SR opening process, it is completed by metal finishes treatment, e.g., organic solderability preservatives (OSPs). Figure 13(b) shows a cross section of a Cu-pillar flip chip on ETS assembly [33]. The linewidth/spacing of ETS in use today is  $15\mu\text{m}/15\mu\text{m}$ . However,  $13\mu\text{m}/13\mu\text{m}$  is in production [34].

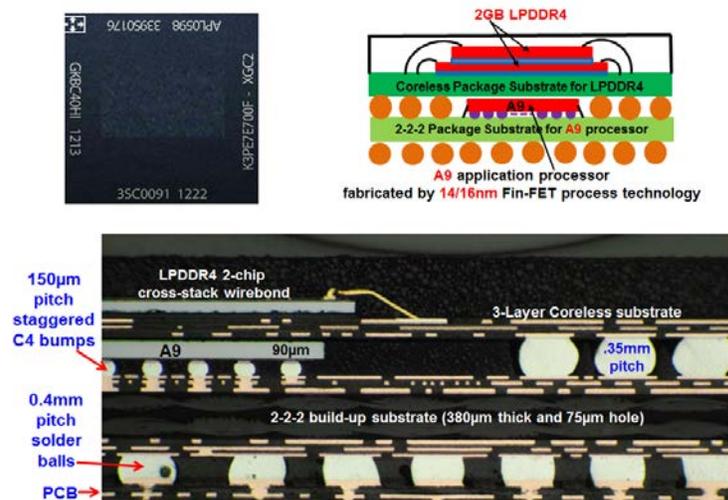
### Flip Chip Assembly

Basically, there are two groups of flip chip assemblies: one is with an intermediate layer between the bonding pads/traces, and the other is not, i.e., nothing! Flip-chip assembly with intermediate layers such as solder for mass reflow and Cu-pillar with solder cap by TCB are called indirect bonding, which is the focus of this paper. Cu-to-Cu diffusion bonding, which does not have anything between the bonding pads/traces on the chip/wafer, is therefore, called direct bonding, which is out of the scope of the present study.



**Figure - 14 Flip chip assembly: (a) mass reflow of chips with C4 or C2 bumps with CUF, (b) TCB with low-force of chips with C2 bumps with CUF, (c) TCB with high-force of chips with C2 bumps with NCP, and (d) TCB with high-force of chips with C2 bumps with NCF**

**C4 Solder Mass Reflow.** Solder mass reflow has been used for flip-chip assembly for almost 50 years. Most of the solder C4 bumps are mass reflowed on either silicon, ceramic, or organic substrates. The assembly process is very simple, Figure 14 (a): (i) use a look-up and look-down camera to identify the location of the bumps on the chip and the pads on the substrate;



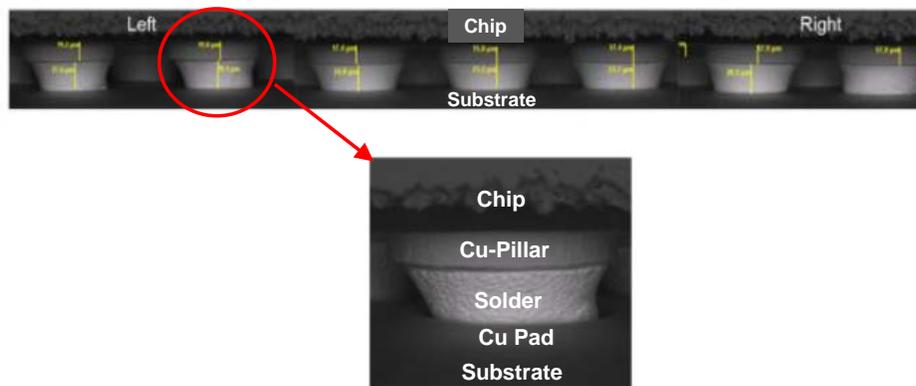
**Figure - 15 PoP in a production smartphone. In the bottom package, the C4 solder bumped (AP) flip chip is mass reflowed on a 2-2-2 package substrate with an underfill, and then BGA to the PCB**

apply flux on either the C4 bumps, or the substrate, or both; and (iii) pick and place the C4 bumped chips on the substrate, then mass reflow with temperature H. Because of the surface tension of the solder bumps during reflow, the process is very robust (self-alignment). Figure 15 shows the cross section of a production smartphone. It can be seen that the application processor (AP) is housed in a PoP format (bottom package) and the solder bumped flip chip is mass reflowed on a 2-2-2 organic package substrate with underfill. In general, the spacing between the bumps on the solder mass reflow of C4 bumped chips can be as small as 50 $\mu$ m.

**C2 Solder Mass Reflow.** In the past few years, solder mass reflow of C2 (Cu-pillar with solder cap) bumped chips on either silicon, ceramic, or organic package substrates has been tried for high pin-count and fine-pitch flip-chip assemblies. The assembly process, Figure 14(a), is exactly the same as that of the C4 bumps, but the self-alignment characteristic is nowhere near the same, and thus, it is seldom being used. In general, the spacing between the pillars on the solder mass reflow of C2 bumped chips can be as small as 25 $\mu$ m.

**C2 TCB.** In the past few years, TCB of chips with an intermediate layer such as C2 (Cu-pillar with solder cap) bumps on silicon, ceramic, or organic package substrates, has been attracting attention for high-density and ultrafine pitch flip chip assemblies. Basically, there are two methods, one is with low-bonding force and the other is with a high-bonding force.

**C2 TCB with Low-Bonding Force.** For the one with low bonding force, the assembly process is simple, Figure 14(b): (i) first, use the look-up and look-down camera to locate the position of the C2 bumps on the chip and their corresponding pads on the substrate; (ii) apply flux on the solder cap or on the substrate or both; and (iii) pick-and-place the chip on the substrate and then apply temperature (H) to melt the solder and a low force (f) to hold the chip at a certain distance from the substrate. The above procedure is done one chip at a time and therefore, the throughput is low in comparison with the C2 solder mass reflow process. Figure 16 shows a typical cross section of a flip chip assembly with TCB with low force on C2 bumps [35]. In general, the spacing between the pillars on the C2 chip by TCB with a low-bonding force can be as small as 8 $\mu$ m.



**Figure 16 - Cross section of a C2 flip chip assembled on an organic package substrate by a TCB with low-force (CUF)**

**C2 TCB with High-Bonding Force.** For TCB with a high-bonding force on the C2 chip, the assembly process must be combined with the NCP or NCF underfill, which will be discussed in the next section.

### Underfill/Reliability

The reliability of flip chip solder joints is enhanced by the application of underfill [7], especially on organic substrate. Most underfills consist of low-expansion fillers such as fused silica (SiO<sub>2</sub>) and a liquid prepolymer such as thermosetting resin (adhesive) that can be cured to a solid composite. In 1987, it has been shown that with underfill, the thermal fatigue life of the flip chip solder joints on ceramic substrate increased [36]. In 1992, it was proposed to use low-cost organic substrate instead of high-cost ceramic substrate for flip chip assemblies [14, 15]. This showed that with underfill, the large thermal expansion mismatch between the silicon chip (2.5x10<sup>-6</sup>/°C) and the organic substrate (15-18x10<sup>-6</sup>/°C) is reduced substantially and the solder joints are reliable for most applications. This opened up the doors for today's very popular solder bumped flip chip on low-cost organic substrate packages used, e.g., in the processors of personal computers, notebooks, smartphones, tablets, etc. Basically, there are two different procedures to apply the underfill, namely pre-assembly underfill and post-assembly underfill.

**Post-assembly Underfill.** For post-assembly underfill, the application of underfill is after the flip chip assembly, i.e., the flip chip is already on the substrate and the solder joints are already mass reflowed (either with C2 or C4 bumps) or low-force TCB with C2 bumps. For post-assembly underfill, there are basically two methods, namely CUF [37] and MUF [38-42]. CUF is the first method that went into volume production. For CUF, the underfill is dispensed by a needle or jet w/o vacuum

assisted on one (or two) sides of the flip chip on substrate assembly. Because of capillary action, this underfill completely fills the space between the chips, solder joints, and substrates. The chip and the substrate are then firmly bonded by curing the underfill. CUF is performed one chip assembly at a time, thus, throughput is an issue.

Molded underfill was first proposed in 2000 [38] and later by others [39], [40], [41], [42], and [43]. For MUF, the modified epoxy mold compound (EMC) is transferred molding the chip and filling the gap between the chip, solder joints, and the substrate of the flip chip assembly. The encapsulant of the chip and the underfill are formed at the same time, which will increase the throughputs. However, the challenges of MUF are: (a) the flow of MUF between the chip and the substrate is usually assisted by vacuum, (b) the size of the silica filler of the EMC must be very small for flowability, (c) the cost of modified EMC for MUF is much higher than that for package molding, (d) package warpage is an issue due to the thermal expansion mismatch between the EMC, chip, and substrate, (e) the molding temperature is limited by the melting point of the solder joints, and (f) the standoff-height and pitch of the solder joints cannot be too small. In order to increase the throughput of CUF and avoid the drawbacks of MUF, a method of post-assembly underfill has been proposed in [44], where a stencil is designed for printing the underfill material for flip chips on organic-panel and Si-wafer assemblies.

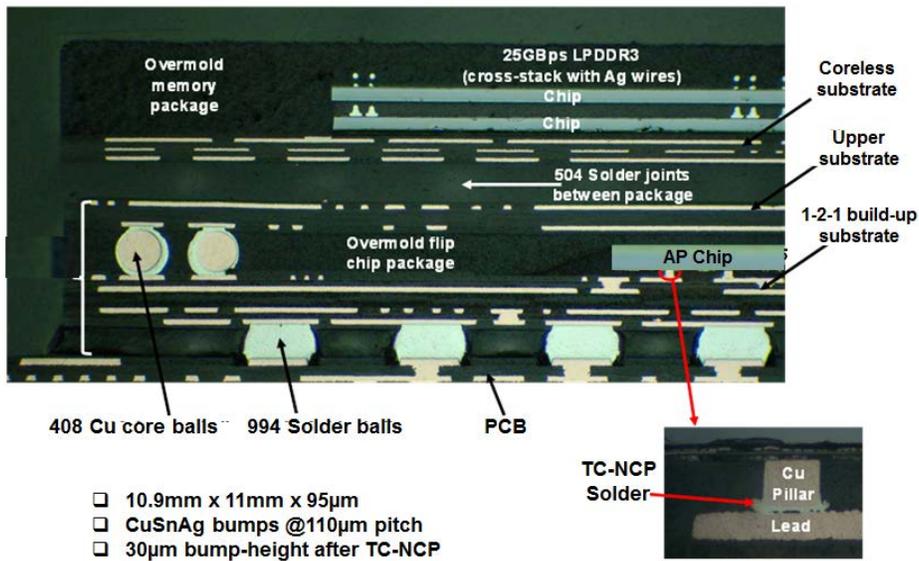


Figure 17 - PoP in a production smartphone. The C2 flip chip is TCB with high-force on a package substrate (TC-NCP)

**Pre-Assembly Underfill.** For pre-assembly underfill, the application of underfill is either on the substrate or wafer and is before the flip-chip assembly. Solder reflow of the C4 bumps with underfill on substrates is called NUF [45]. High-bonding force TCB of the C2 bumps with nonconductive paste (TC-NCP) underfill on the substrate,

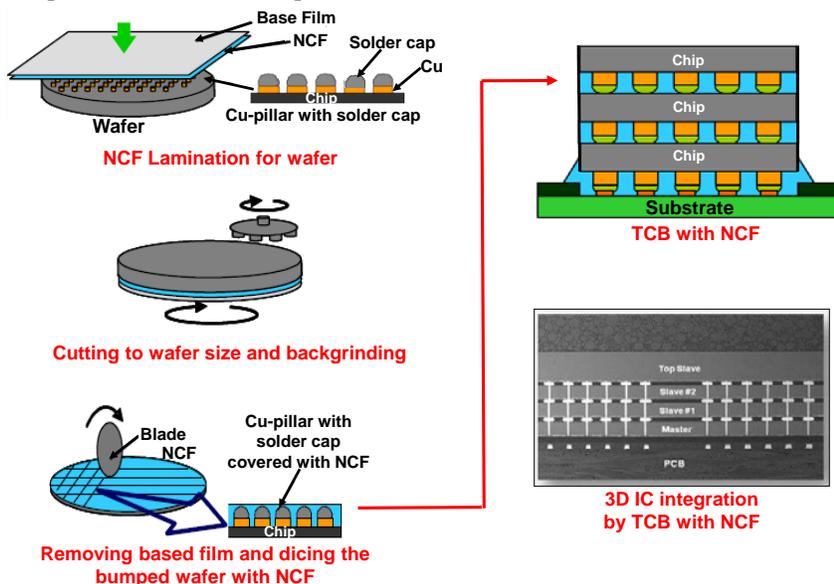


Figure - 18 Lamination of NCF on a C2 bumped wafer, dicing, and TCB of NCF flip chips (one by one)

Figure 14(c), was presented in 2009 [46] and has been used to assemble the application processor for a production smartphone as shown in Figure 17. The NUF and NCP underfills can be spun on, dispensed by a needle, or vacuum assisted.

By learning from the chip-on-glass technology, high-bonding force TCB of C2 bumps with nonconductive film underfill on wafers have been studied, e.g., [47], [48, 49], [50, 51], [52], [53], [54, 55], [56], and [57-59] for 3D IC integration. Figure 18 shows the lamination of NCF on the Cu-pillar with a solder cap bumped wafer. High-bonding force TCB of the C2 chips with NCF (after singulation from the laminated wafer) has been in production for 3D IC integration on the TSV-based DDR4 DRAM, Figure 18. This 3D memory cube is stacked one chip at a time and each chip takes ~ 10s for the underfill film to gel, the solder to melt and solidify. Throughput is a problem!

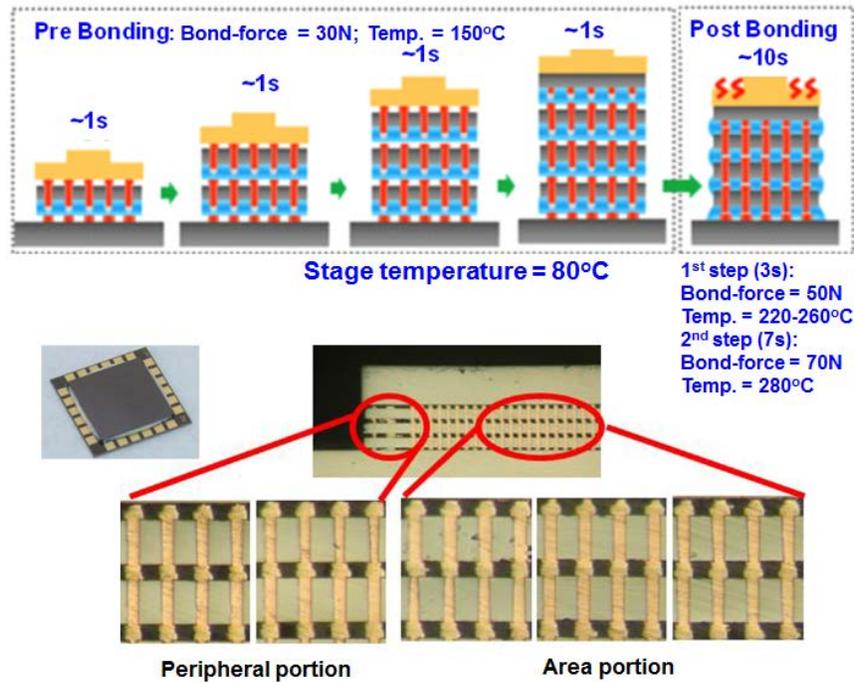


Figure 19 - Collective TCB with high-force with NCF flip chips

In order to resolve this problem, it was proposed [58, 59] to have a collective bonding method which is shown in Figure 19. It can be seen that the C2 chip with NCF is prebond (bond force = 30N, temperature = 150°C, and time <1s) on a stage with temperature = 80°C. For postbond (first step (3s): bond-force = 50N, temperature = 220–260°C, second step (7s): bond-force = 70N, temperature = 280°C) on a stage temperature = 80°C. Thus, instead of using 40s in stacking up four chips by the conventional method, it only takes less than 14s by the collective TCB method. Some images of the cross section of the proposed collective bonding method are shown in Figure 19. Reasonable good joints are achieved with optimized conditions. In general, the spacing between the pillars on the C2 chip with either NCP or NCF by TCB with high bonding force can be as small as 10µm.

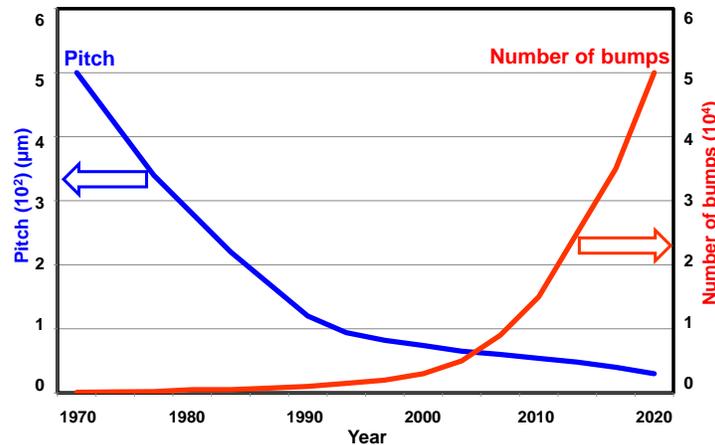


Figure 20 - Trend in flip chip bump and pitch

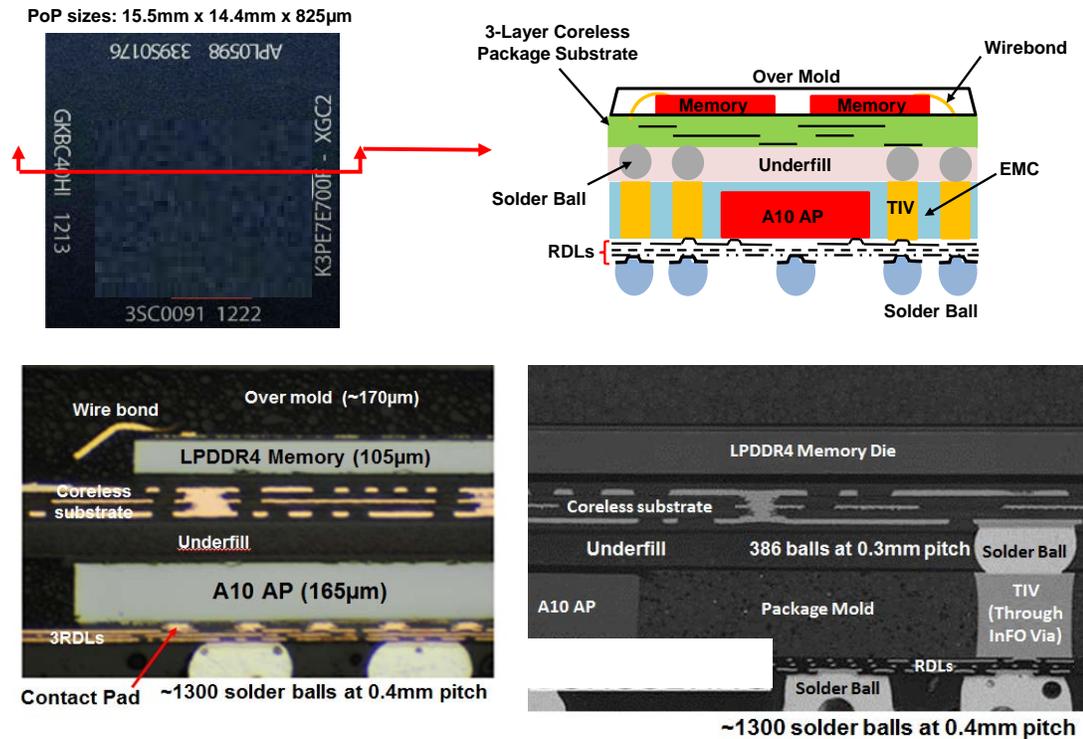
## Summary and Recommendations

Wafer bumping, package substrate, assembly, and underfill for flip-chip technology have been investigated in this study. Some important results and recommendations are as follows:

- Flip chip technology has come a long way. From the three-bump flip chip to 10,000-bump flip chip, and could be 50,000-bump flip chip by the year of 2020. Also, by that time, the flip-chip pitch could be as small as 30 $\mu$ m as shown in Figure 20.
- C2 bumps have better thermal and electrical performance and can go down to finer pitch (smaller spacing between pads) than C4 bumps.
- The self-alignment characteristic (one of the most unique features of flip chip technology) of the C2 bumps is nowhere near the C4 bumps. Thus, mass reflow is usually applied to C4 bumped chips.
- C2 bumped chips are usually assembled by TCB with high-force, while low-force is sometime used.
- The advantages of TCB are for higher pin-count, finer pitch, thinner chips, higher-density, and thinner package substrates, and controlling warpage and die tilt. One of the drawbacks of TCB is throughput (compared with mass reflow).
- A package substrate with ten build-up layer (5-2-5) and 10 $\mu$ m linewidth and spacing is more than adequate to support most of the flip chips. In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced FPGA, even a 12 build-up layer (6-2-6) package substrate is not enough to support the chips and a TSV interposer is needed.
- As of today, TSV-interposer is very expensive. In order to lower the cost, enhance the electrical performance, and reduce the package profile, TSV-less interposers such as the SLIT, SLIM, NTI, EMIB, and organic interposer have been developed. This will be the trend in package substrate for high-density and performance flip chip applications.
- More research and development works should be done on innovative and low-cost ETS and coreless substrates for portable, mobile, wearable, and IoTs applications. More research and development works should be done to effectively use the BOL technique to increase routing density, and thus, lower the cost and reduce the size of organic package substrate.
- For the post-assembly underfill approach, the CUF or MUF is usually applied to flip-chip assemblies with mass reflow and TCB with low-bonding force methods.
- For the pre-assembly underfill approach, the NUF, NCP, or NCF is usually applied before flip-chip assemblies; NUF is with mass reflow and NCP or NCF is with high-force TCB. In general, the NUF and NCP are applied on the substrate and the NCF is laminated onto the C2 bumped wafer and then diced into individual chips.
- The collective TCB with high-force method can be a potential high-throughput process for stacking C2 chips with laminated NCF.
- Flip chip technology is facing stiff competition. Some of its market share will be taken away by the fan-out wafer/panel-level packaging (FOW/PLP or simply FOWL) technology [60, 61, 62]. Figure 21 shows the schematic and SEM (scanning electron microscope) images of the cross section of the PoP which houses the AP and mobile DRAMs of a production smartphone. This PoP is fabricated with the InFO (integrated fan-out) WLP technology [62]. It can be seen from the bottom package that the wafer bumping, fluxing, flip chip assembly, cleaning, underfill dispensing and curing, and build-up package substrate (of the AP shown in Figure 15) have been eliminated and are replaced by the EMC and RDLs (for the AP as shown in Figure 21). This results into a lower cost, higher performance, and lower profile package. This is very significant, since the smartphone company and the component company developing these packages are the “sheep leaders”. Once they use it, then many others will follow. Also, this means that FOWL is not just only for packaging baseband, RF (radio frequency) switch/transceiver, PMIC (power management integrated circuit), audio codec, MCU (micro control unit), RF radar, connectivity ICs, etc., it can also be used for packaging high-performance and large (>120mm<sup>2</sup>) SoC such as APs.
- With the popularity of SiP, fan-out (which can handle multiple dies) will be used more because the flip-chip WLCSP (wafer-level chip scale package) can only handle single die.

## References

- [1] Davis, E., Harding, W., Schwartz, R., and Corning, J., "Solid Logic Technology: Versatile, High Performance Microelectronics", *IBM Journal of Research and Development*, 1964, pp. 102-114.
- [2] Totta, P., and Sopher, R., "SLT Device Metallurgy and Its Monolithic Extension", *IBM Journal of Research and Development*, 1969, pp. 226-238.
- [3] Lau, J. H., *3D IC Integration and Packaging*, McGraw-Hill Book Company, New York, 2016.
- [4] Lau, J. H., *Through-Silicon Vias for 3D Integration*, McGraw-Hill Book Company, New York, 2013.
- [5] Lau, J. H., *Reliability of RoHS-Compliant 2D and 3D IC Interconnects*, McGraw-Hill Book Company, New York, 2011.
- [6] Sutanto, J., "POSSUM Die Design as a Low Cost 3D Packaging Alternative," *3D Packaging*, 2012, pp. 16-18.
- [7] Lau, J. H., 2000, *Low Cost Flip Chip Technologies*, McGraw-Hill Book Company, New York, 2000.
- [8] Lau, J. H., and Pao, Y., *Solder Joint Reliability of BGA, CSP, and Flip Chip Assemblies*, McGraw-Hill Book Company, New York, 1997.



**Figure 21 - PoP in production smartphone. In the bottom package, the AP is embedded in the EMC and its circuitry is fanned out through the RDLs to the PCB [63]**

- [9] Elenius, P., Leal, J., Ney, J., Stepniak, D., and Yeh, S., "Recent Advances in Flip Chip Wafer Bumping Using Solder Paste Technology", *IEEE Proceedings of Electronic and Components Technology Conference*, 1999, pp. 260-265.
- [10] Lau, J. H., and Chang, C., "Taguchi Design of Experiment for Wafer Bumping by Stencil Printing", *IEEE Transactions on Electronics Packaging Manufacturing*, 21(3), 2000, pp. 219-225.
- [11] Love, D., Moresco, L., Chou, W., Horine, D., Wong, C., and Eilin, S., "Wire Interconnect Structures for Connecting an Integrated Circuit to a Substrate", *US Patent no. 5,334,804*, 1994.
- [12] Tung, F., "Pillar Connections for Semiconductor Chips and Method of Manufacture", *US patent no. 6,578,754*, 2003.
- [13] Tung, F., "Pillar Connections for Semiconductor Chips and Method of Manufacture", *US Patent no. 6,681,982*, 2004.
- [14] Tsukada, Y., Tsuchida, S., and Mashimoto, Y., "Surface Lamina Circuit Packaging", *IEEE Proceedings of Electronic and Components Technology Conference*, 1992, pp. 22-27.
- [15] Tsukada, Y., and Tsuchida, S., "Surface Lamina Circuit, A Low Cost High Density Printed Circuit Board", *Proceedings of Surface Mount International Conference*, 1992, pp. 537-542.
- [16] Lau, J. H., and Lee, S. W. R., *Microvias for Low Cost, High Density Interconnects*, McGraw-Hill Book Company, New York, 2001.
- [17] Chaware, R., Nagarajan, K., and Ramalingam, S., "Assembly and Reliability Challenges in 3D Integration of 28nm FPGA Die on a Large High Density 65nm Passive Interposer", *IEEE Proceedings of Electronic and Components Technology Conference*, 2012, pp. 279-283.
- [18] Banijamali, B., Chiu, C., Hsieh, C., Lin, T., Hu, C., Hou, S., Ramalingam, S., Jeng, S., Madden, L., Yu, D., "Reliability Evaluation of a CoWoS-enabled 3D IC Package", *IEEE Proceedings of Electronic and Components Technology Conference*, 2013, pp. 35-40.

- [19] Kwon, W., Ramalingam, S., Wu, X., Madden, L., Huang, C., Chang, H., Chiu, C., Chiu, S., and Chen, S., "Cost Effective and High Performance 28nm FPGA with New Disruptive Silicon-Less Interconnect Technology (SLIT)", *Proceedings of International Symposium on Microelectronics*, 2014, pp. 599-605.
- [20] Liang, F., Chang, H., Tseng, W., Lai, J., Cheng, S., Ma, M., Ramalingam, S., Wu, X., and Gandhi, J., "Development of Non-TSV Interposer (NTI) for High Electrical Performance Package", *IEEE Proceedings of Electronic and Components Technology Conference*, 2016, pp. 31-36.
- [21] Hiner, D., Kelly, M., Huemoeller, R., and Reed, R., "Silicon Interposer-less Integrated Module - SLIM", *11th International Conference and Exhibition on Device Packaging*, 2015.
- [22] Chiu, C., Qian, Z., and Manusharow, M., "Bridge Interconnect with Air Gap in Package Assembly", *US Patent Application No. 8,872,349*, 2014.
- [23] Mahajan, R., R. Sankman, N. Patel, D. Kim, K. Aygun, Z. Qian, Y. Mekonnen, I. Salama, S. Sharan, D. Iyengar, and D. Malliket, "Embedded multi-die interconnect bridge (EMIB) – a high-density, high-bandwidth packaging interconnect," *IEEE Proceedings of Electronic and Components Technology Conference*, 2016, pp. 557-565.
- [24] <http://newsroom.altera.com/press-releases/nr-dram-sip.htm>.
- [25] Li, L., P. Chia, P. Ton, M. Nagar, S. Patil, J. Xue, J. DeLaCruz, M. Voicu, J. Hellings, B. Isaacson, M. Coor, and R. Havens, "3D SiP with organic interposer of ASIC and memory integration," *IEEE Proceedings of Electronic and Components Technology Conference*, 2016, pp. 1445-1450.
- [26] Koide, M., Fukuzono, K., Yoshimura, H., Sato, T., Abe, K., and Fujisaki, H., "High-Performance Flip-Chip BGA Technology Based on Thin-Core and Coreless Package Substrate," *IEEE Proceedings of Electronic and Components Technology Conference*, San Diego, CA, May 30–June 2, 2006, pp. 1869–1873.
- [27] Nishitani, Y., "Coreless Packaging Technology for High-Performance Application," IEEE/ECT/CMPT Seminar on Advanced Coreless Package Substrate and Material Technologies, at *IEEE Electronic and Components Technology Conference*, May 29–June 1, 2012.
- [28] Pendse, R., "Bump-On-Lead Flip Chip Interconnection," U.S. Patent No. 7,368,817, filed Nov. 10, 2004 and issued May 6, 2008.
- [29] Movva, S., Bezuk, S., Bchir, O., Shah, M., Joshi, M., Pendse, R., Ouyang, E., Kim, Y., Park, S., Lee, H., Kim, S., Bae, H., Na, G., and Lee, K., "CuBOL (Cu-Column on BOL) Technology: A Low Cost Flip Chip Solution Scalable to High I/O Density, Fine Bump Pitch and Advanced Si-Nodes," *IEEE Electronic and Components Technology Conference*, May 31–June 3, 2011, pp. 601–607.
- [30] Kuo, F., Lee, J., Chien, F., Lee, R., Mao, C., and Lau, J. H., "Electromigration Performance of Cu Pillar Bump for Flip Chip Packaging With Bump on Trace by Using Thermal Compression Bonding," *IEEE Electronic and Components Technology Conference*, May 27–30, 2014, pp. 56–61.
- [31] Li, M., Tian, D., Cheung, Y., Yang, L., and Lau, J. H., "A High Throughput and Reliable Thermal Compression Bonding Process for Advanced Interconnections," *IEEE Electronic and Components Technology Conference*, May 26–29, 2015, pp. 603–608.
- [32] Chen, C., Lin, M., Liao, G., Ding, Y., and Cheng, W., "Balanced Embedded Trace Substrate Design for Warpage Control," *IEEE Electronic and Components Technology Conference*, May 26–29, 2015, pp. 193–199.
- [33] Lu, M., "Challenges and Opportunities in Advanced IC Packaging," *Chip Scale Rev.*, 18(2), 2014, pp. 5–8.
- [34] Lee, K., Cha, S., and Shim, P., "Form Factor and Cost Driven Advanced Package Substrates for Mobile and IoT Applications," *China Semiconductor Technology International Conference*, Shanghai, China, Mar. 13–14, 2016.
- [35] Eitan, A., and Jing, K., "Thermo-Compression Bonding for Fine-Pitch Copper-Pillar Flip Chip Interconnect—Tool Features as Enablers of Unique Technology," *IEEE Electronic and Components Technology Conference*, May 26–29, 2015, pp. 460–464.
- [36] Nakano, F., Soga, T., and Amagi, S., "Resin-Insertion Effect on Thermal Cycle Resistivity of Flip-Chip Mounted LSI Devices," *ISHM International Symposium on Microelectronics*, Minneapolis, MN, Sep. 28–30, 1987, pp. 536–541.
- [37] Lau, J. H., Krulevitch, T., Schar, W., Heydinger, M., Erasmus, S., and Gleason, J., "Experimental and Analytical Studies of Encapsulated Flip Chip Solder Bumps on Surface Laminar Circuit Boards," *Circuit World*, 19(3), 1993, pp. 18–24.
- [38] Gilleo, K., Cotterman, B., and Chen, I. A., "Molded Underfill for Flip Chip in Package," *Proceedings of High Density Interconnects*, 2000, pp. 28–31.
- [39] Rector, L. P., Gong, S., Miles, T. R., and Gaffney, K., "Transfer Molding Encapsulation of Flip Chip Array Packages," *Int. J. Microcircuits Electron. Packag.*, 23(4), 2000, pp. 401–406.
- [40] Lai, Y. M., Chee, C. K., Then, E., Ng, C. H., and Low, M. F., "Capillary Underfill and Mold Encapsulation Method and Apparatus," *U.S. Patent No. 7,262,077*, filed Sep. 30, 2003 and issued Aug. 28, 2007.
- [41] Lee, J. Y., Oh, K. S., Hwang, C. H., Lee, C. H., and Amand, R. D. S., "Molded Underfill Development for FlipStack CSP," *IEEE Electronic and Components Technology Conference*, San Diego, CA, May 26-29, 2009, pp. 954–959.
- [42] Joshi, M., Pendse, R., Pandey, V., Lee, T. K., Yoon, I. S., Yun, J. S., Kim, Y. C., and Lee, H. R., "Molded Underfill (MUF) Technology for Flip Chip Packages in Mobile Applications," *IEEE Electronic and Components Technology Conference*, Las Vegas, NV, June 1–4, 2010, pp. 1250–1257.

- [43] Ferrandon, C., Jouve, A., Joblot, S., Lamy, Y., Schreiner, A., Montmeat, P., Pellat, M., Argoud, M., Fournel, F., Simon, G., and Cheramy, S., "Innovative Wafer-Level Encapsulation and Underfill Material for Silicon Interposer Application," *IEEE Electronic and Components Technology Conference*, Las Vegas, NV, May 28–31, 2013, pp. 761–767.
- [44] Lau, J. H., Zhang, Q., Li, M., Yeung, K., Cheung, Y., Fan, N., Wong, Y., Zahn, M., and Koh, M., "Stencil Printing of Underfill for Flip Chips on Organic-Panel and Si-Wafer Substrates," *IEEE Transactions on CPMT*, 5(7), 2015, pp. 1027–1035.
- [45] Wong, C. P., Baldwin, D., Vincent, M. B., Fennell, B., Wang, L. J., and Shi, S. H., "Characterization of a No-Flow Underfill Encapsulant During the Solder Reflow Process," *IEEE Electronic Components and Technology Conference*, Seattle, WA, May 25–28, 1998, pp. 1253–1259.
- [46] Lee, M., Yoo, M., Cho, J., Lee, S., Kim, J., Lee, C., Kang, D., Zwenger, C., and Lanzone, R., "Study of Interconnection Process for Fine Pitch Flip Chip," *IEEE Electronic Components and Technology Conference*, Seattle, WA, May 25–28, 2009, pp. 720–723.
- [47] Okayama, Y., Nakasato, M., Saitou, K., Yanase, Y., Kobayashi, H., Yamamoto, T., Usui, R., and Inoue, Y., "Fine Pitch Connection and Thermal Stress Analysis of a Novel Wafer Level Packaging Technology Using Laminating Process," *IEEE Electronic Components and Technology Conference*, Las Vegas, NV, June 1–4, 2010, pp. 287–292.
- [48] Honda, K., Enomoto, T., Nagai, A., and Takano, N., "NCF for Wafer Lamination Process in Higher Density Electronic Packages," *IEEE Electronic Components and Technology Conference*, Las Vegas, NV, June 1–4, 2010, pp. 1853–1860.
- [49] Honda, K., Nagai, A., Satou, M., Hagiwara, S., Tuchida, S., and Abe, H., "NCF for Pre-Applied Process in Higher Density Electronic Package Including 3D-Package," *IEEE Electronic Components and Technology Conference*, San Diego, CA, May 29–June 1, 2012, pp. 385–392.
- [50] Fukushima, T., Ohara, Y., Bea, J., Murugesan, M., Lee, K.-W., Tanaka, T., and Koyanagi, M., "Non-Conductive Film and Compression Molding Technology for Self-Assembly-Based 3D Integration," *IEEE Electronic Components and Technology Conference*, San Diego, CA, May 29–June 1, 2012, pp. 385–392.
- [51] Ito, Y., Murugesan, M., Kino, H., Fukushima, T., Lee, K., Choki, K., Tanaka, T., and Koyanagi, M., "Development of Highly-Reliable Microbump Bonding Technology Using Self-Assembly of NCF-Covered KGDs and Multi-Layer 3D Stacking Challenges," *IEEE Electronic Components and Technology Conference*, San Diego, CA, May 26–29, 2015, pp. 336–341.
- [52] Choubey, A., Anzures, E., Fleming, D., Dhoble, A., Herong, L., Barr, R., Calvert, J., and Oh, J., "Non-Conductive Film (NCF) Underfill for Flip Chip Assembly and High Reliability," *International Wafer Level Packaging Conference (IWLPC)*, San Jose, CA, Nov. 11–13, 2014.
- [53] Lee, D., Kim, K., Kim, K., Kim, H., Kim, J., Park, Y., Kim, J., Kim, D., Park, H., Shin, J., Cho, J., Kwon, K., Kim, M., Lee, J., Park, K., Chung, B., and Hong, S., "A 1.2V 8Gb 8-Channel 128GB/s High-Bandwidth Memory (HBM) Stacked DRAM With Effective Microbump I/O Test Methods Using 29nm Process and TSV," *IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 9–13, 2014, pp. 433–435.
- [54] Shin, J., Kim, Y., Lee, H., Kang, U., Seo, S., and Paik, K., "Effects of Thermo-Compression Bonding Parameters on Joint Formation of Micro-Bumps in Non-Conductive Film (NCF)," *IEEE Electronic and Components Technology Conference*, San Diego, CA, May 26–29, 2015, pp. 910–915.
- [55] Lee, H., Choi, Y., Shin, J., and Paik, K., "Wafer Level Packages (WLPs) Using B-Stage Non-Conductive Films (NCFs) for Highly Reliable 3D-TSV Micro-Bump Interconnection," *IEEE Electronic and Components Technology Conference*, San Diego, CA, May 26–29, 2015, pp. 331–335.
- [56] Hiner, D., Kim, D., Ahn, S., Kim, K., Kim, H., Lee, M., Kang, D., Kelly, M., Huemoeller, R., Radojcic, R., and Gu, S., "Multi-Die Chip on Wafer Thermo-Compression Bonding Using Non-Conductive Film," *IEEE Electronic Components and Technology Conference*, San Diego, CA, May 26–29, 2015, pp. 17–21.
- [57] Nonaka, T., Kobayashi, Y., Asahi, N., Niizeki, S., and Fujimaru, K., "High Throughput Thermal Compression NCF Bonding," *IEEE Electronic and Components Technology Conference*, Orlando, FL, May 27–30, 2014, pp. 913–918.
- [58] Matsumura, K., Tomikawa, M., Sakabe, Y., and Shiba, Y., "New Non Conductive Film for High Productivity Process," *IEEE CPMT Symposium Japan (ICSJ)*, Kyoto, Japan, Nov. 9–11, 2015, pp. 19–20.
- [59] Asahi, N., Miyamoto, Y., Nimura, M., Mizutani, Y., and Arai, Y., "High Productivity Thermal Compression Bonding for 3D-IC," *IEEE International 3D Systems Integration Conference*, Sendai, Japan, Aug. 31–Sep. 2, 2015, pp. TS7.3.1–TS7.3.5.
- [60] Lau, J. H., N. Fan, and M. Li, "Design, Material, Process, and Equipment of Embedded Fan-Out Wafer/Panel-Level Packaging", *Chip Scale Review*, Vol. 20, May/June 2016, pp. 38-44.
- [61] Lau, J. H., "Patent Issues of Fan-Out Wafer/Panel-Level Packaging", *Chip Scale Review*, Vol. 19, November/December 2015, pp. 42-46.
- [62] Tseng, C., C. Liu, C. Wu, and D. Yu, "InFO (Wafer Level Integrated Fan-Out) Technology," *IEEE Electronic Components and Technology Conference*, May 2016, pp. 1-6.
- [63] Binghamton University/Prismark and SystemPlus Consulting.

# Status and Outlooks of Flip Chip Technology

**John H Lau**  
**ASM**

**[John.Lau@asmpt.com](mailto:John.Lau@asmpt.com)**

# PURPOSES

To present the **status** of flip chip technology such as:

- Wafer bumping
- Package substrates
- Flip chip assembly
- Underfill

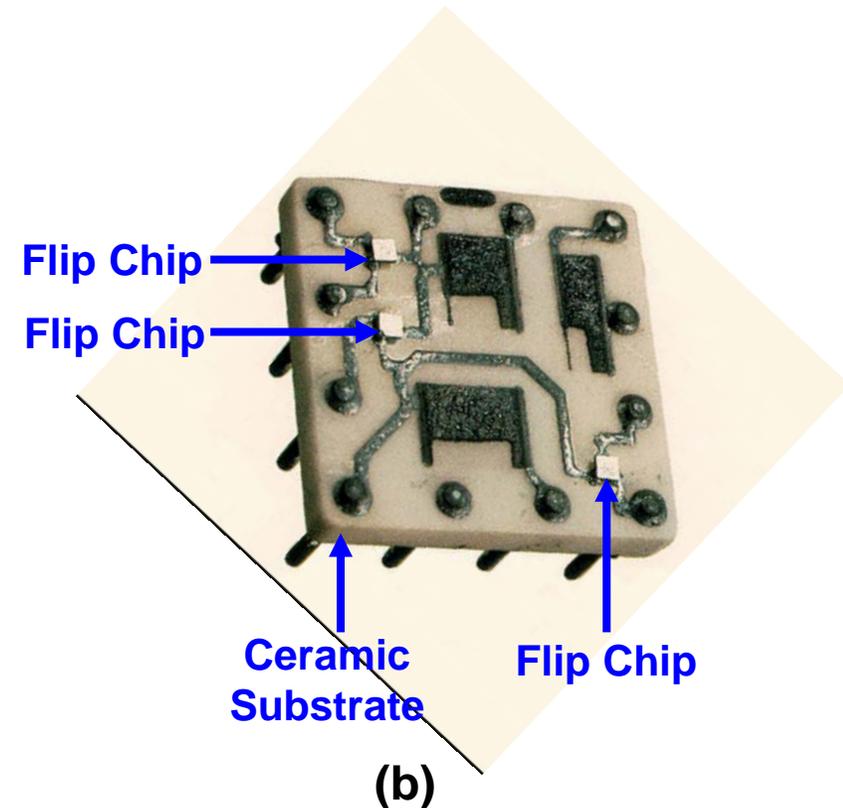
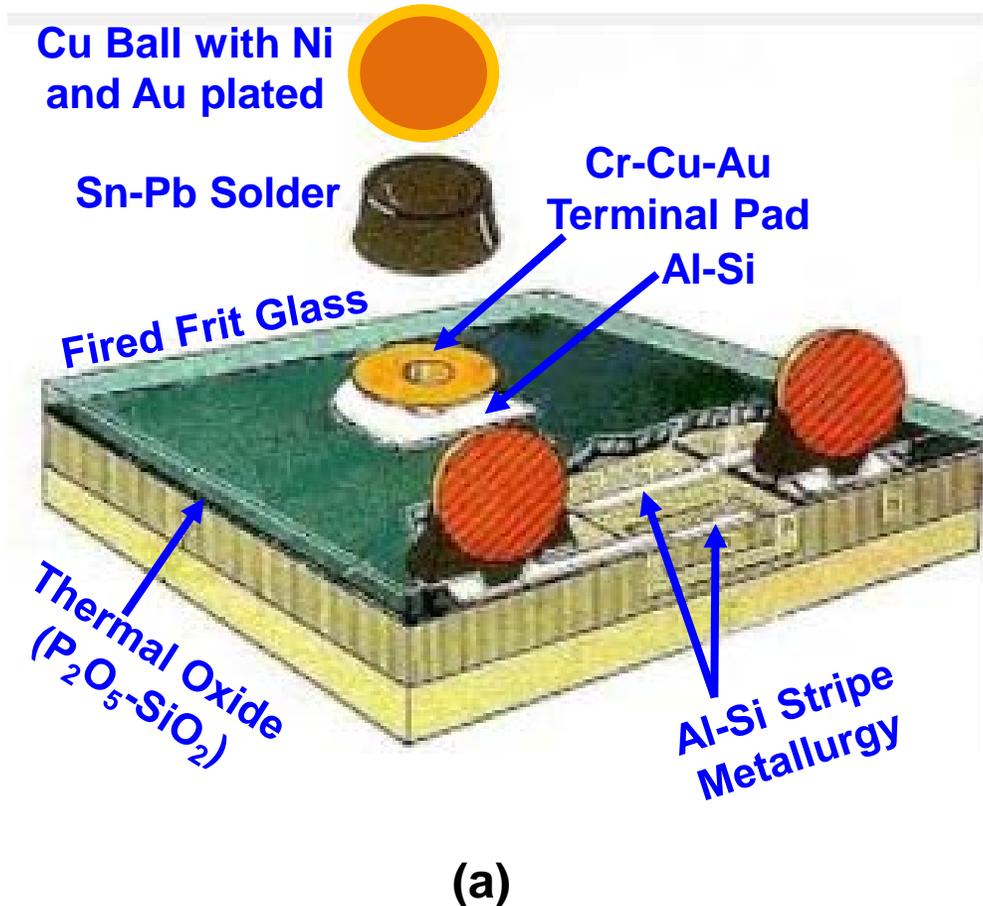
Their future **trends** will also be recommended.

Finally, the **competition** on flip chip technology will be briefly mentioned.

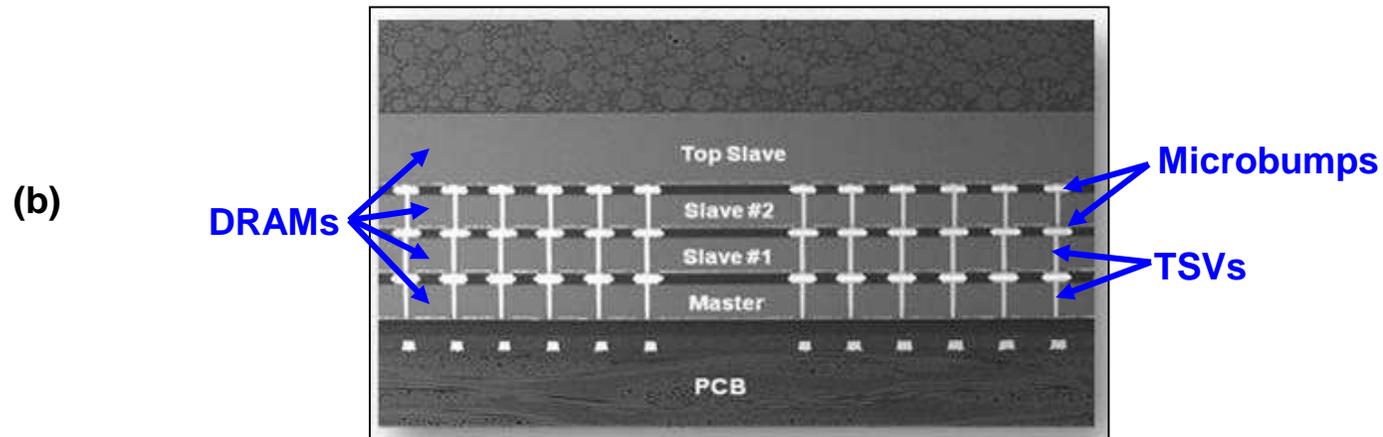
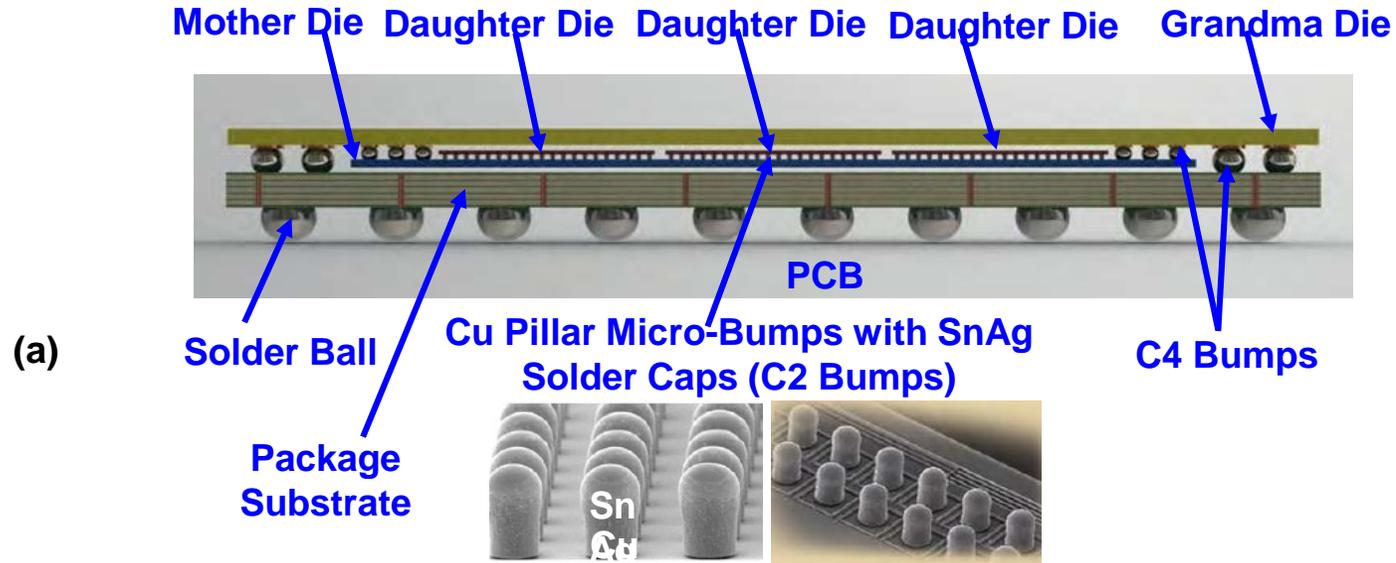
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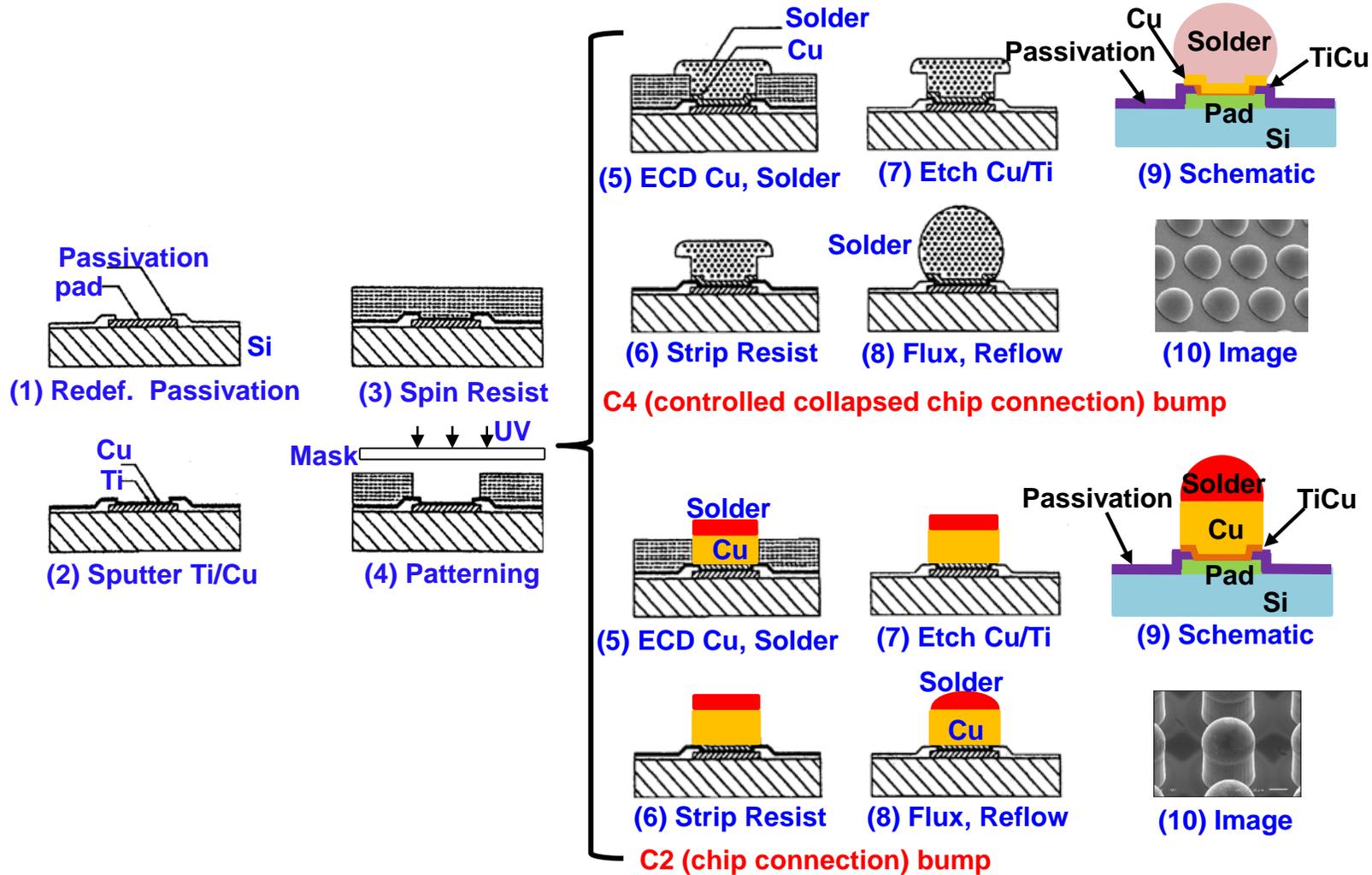
**(a) IBM's First Flip Chip Component with 3 Terminal Transistors**  
**(b) IBM's First Flip Chip Assembly on a Ceramic Substrate**



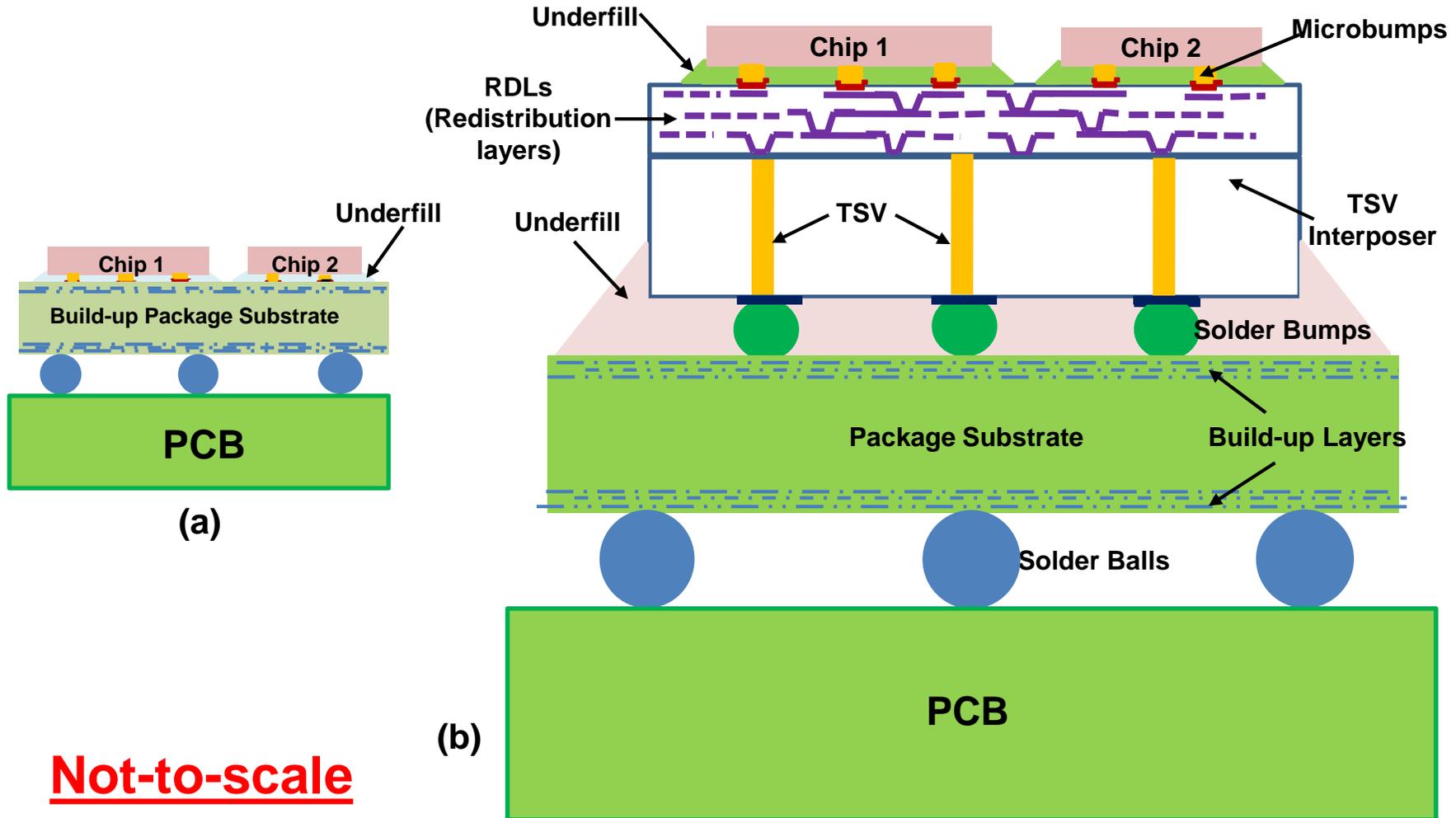
**(a) 3D IC Packaging and (b) 3D IC Integration**



**Wafer Bumping by ECD or Electroplating Method for C4 and C2 Bumps**

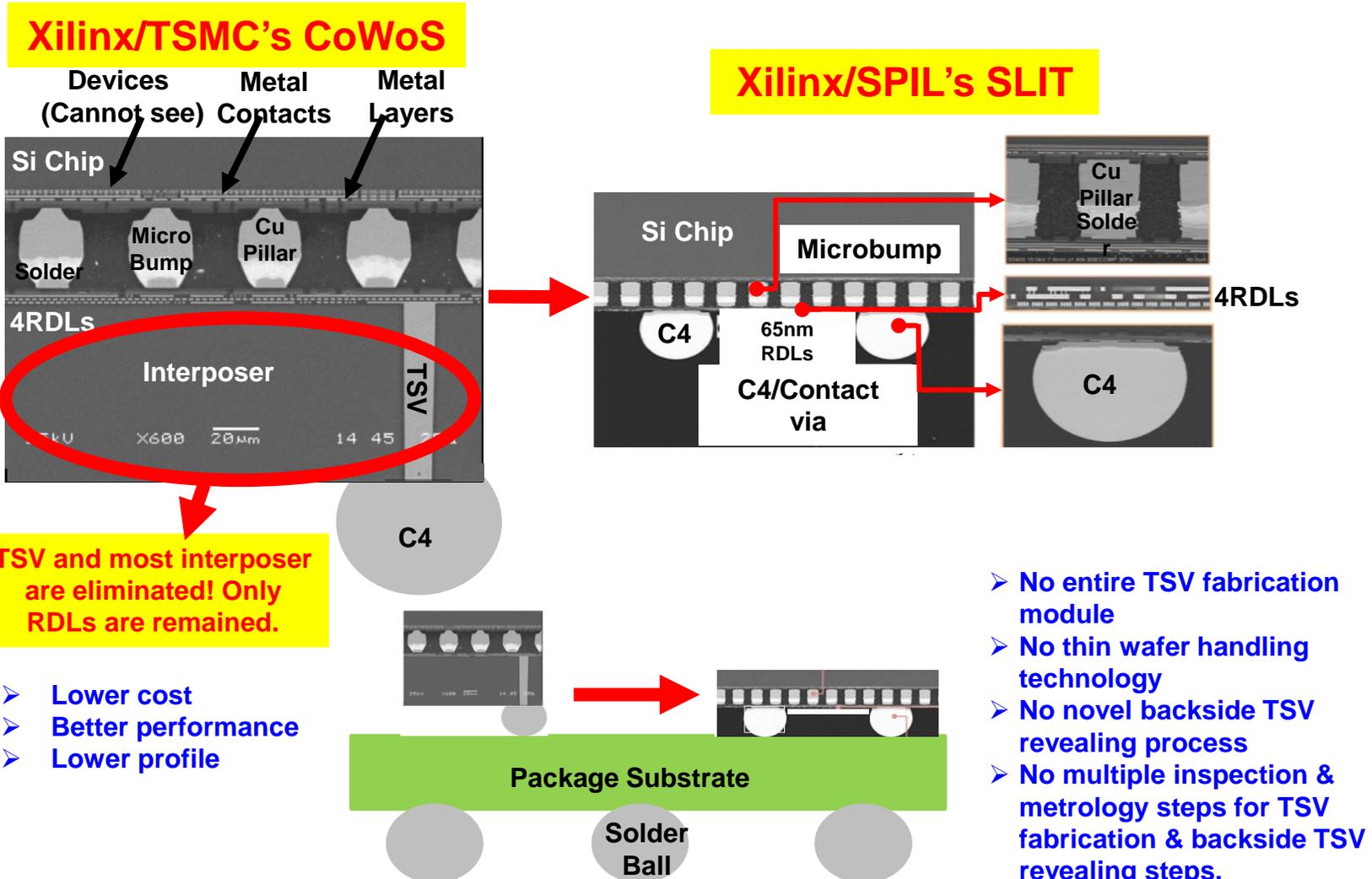


**(a) Build-up Package Substrate for Flip Chips**  
**(b) Build-up Substrate with TSV-interposer for Flip Chips**



**Not-to-scale**

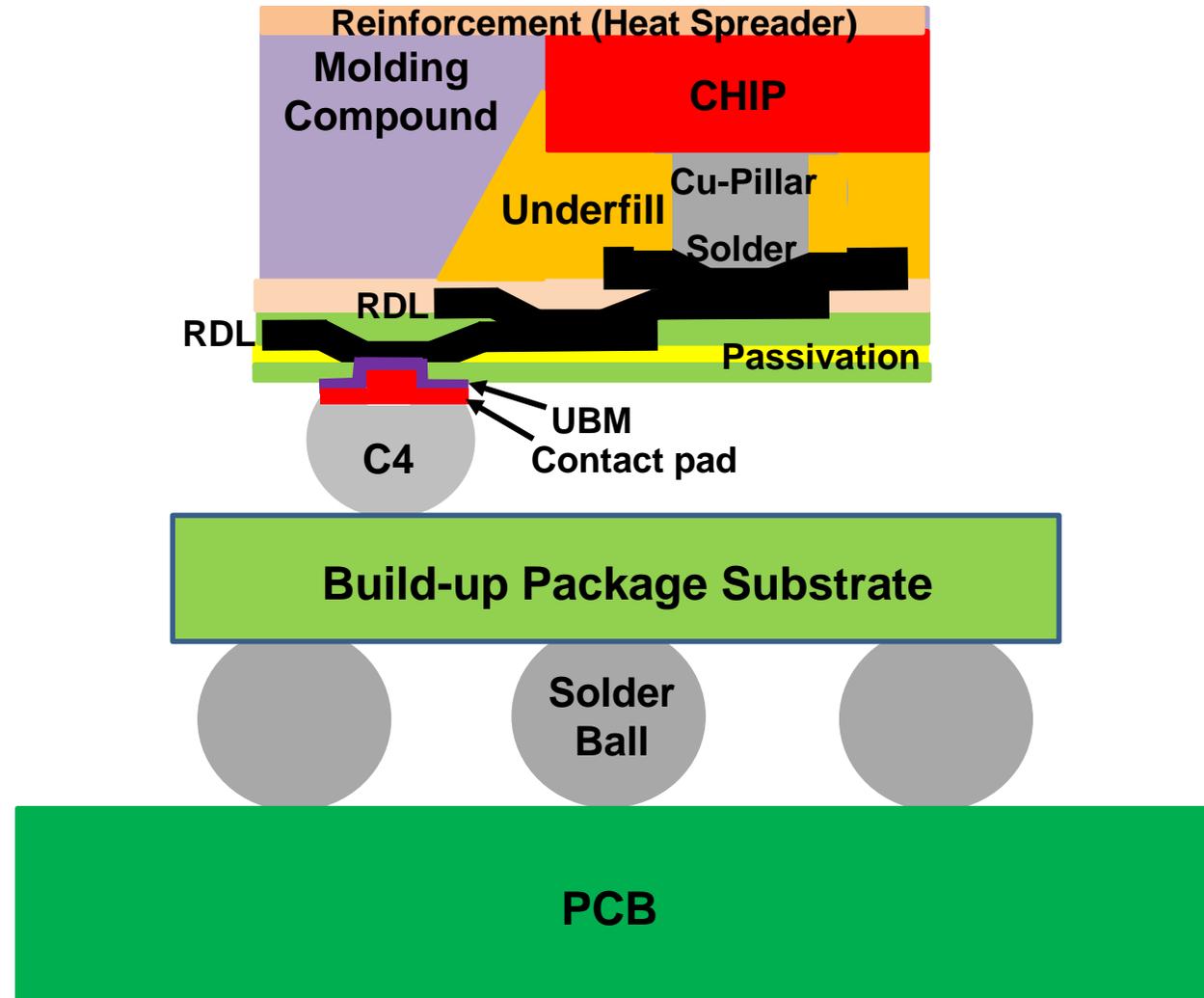
**Xilinx/TSMC's CoWoS (left) and Xilinx/SPIL's SLIT (right)**



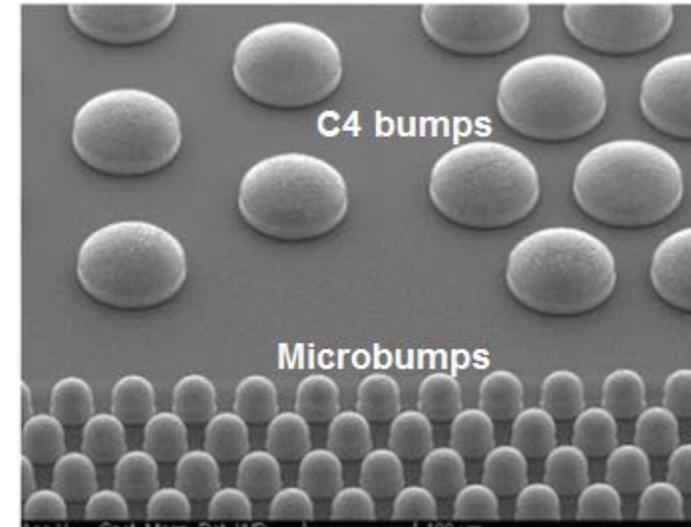
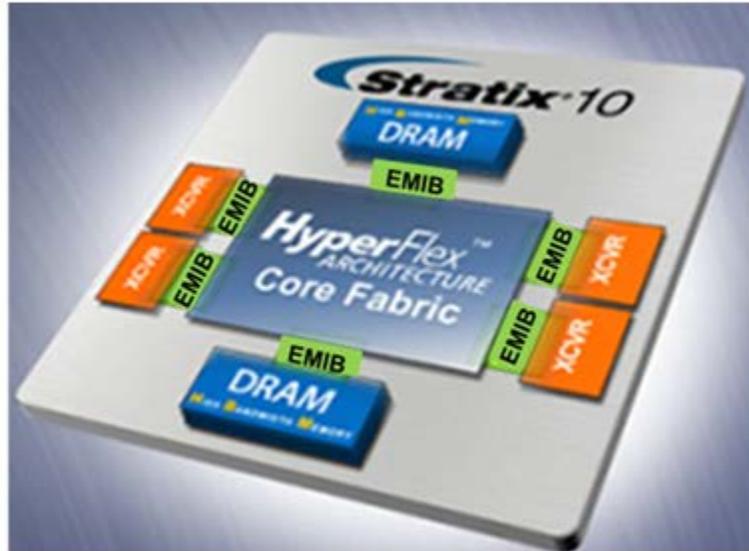
- Lower cost
- Better performance
- Lower profile

- No entire TSV fabrication module
- No thin wafer handling technology
- No novel backside TSV revealing process
- No multiple inspection & metrology steps for TSV fabrication & backside TSV revealing steps.

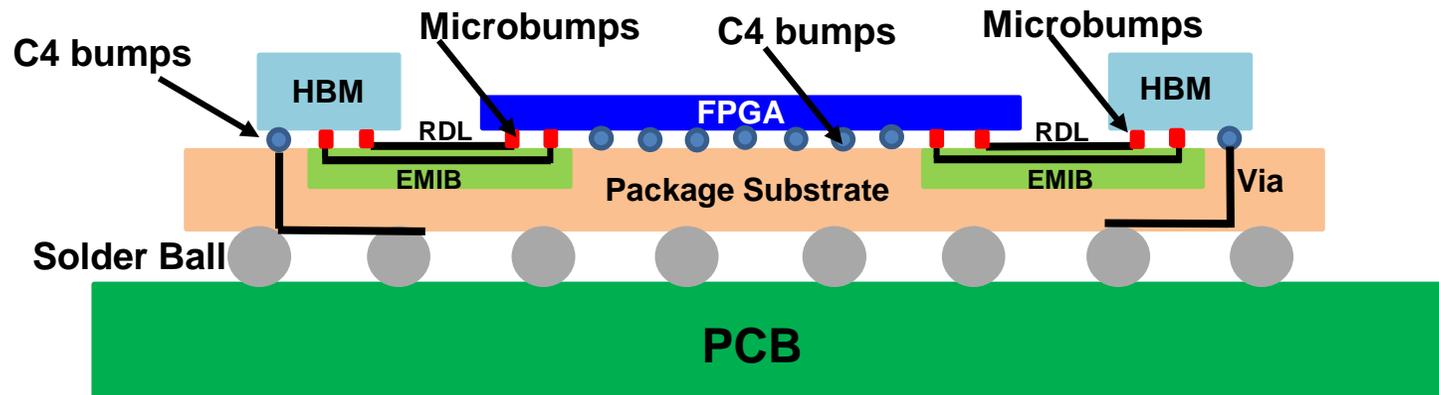
**Xilinx/SPIL's SLIT (Silicon-Less Interconnect Technology)**



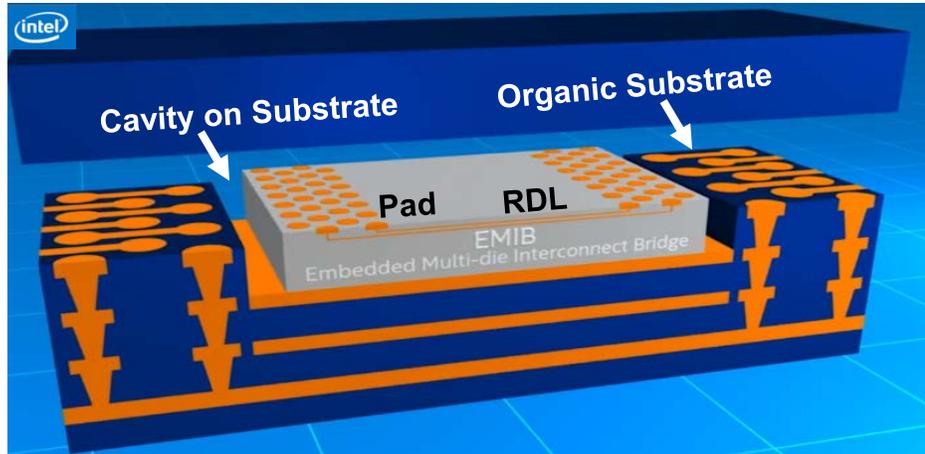
## Intel/Altera's High Bandwidth Communications between the FPBA and HBMs by EMIB



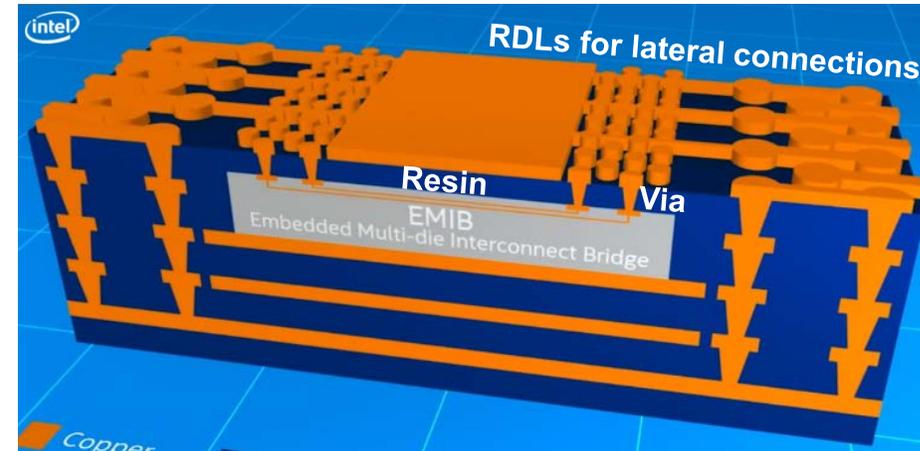
FPGA



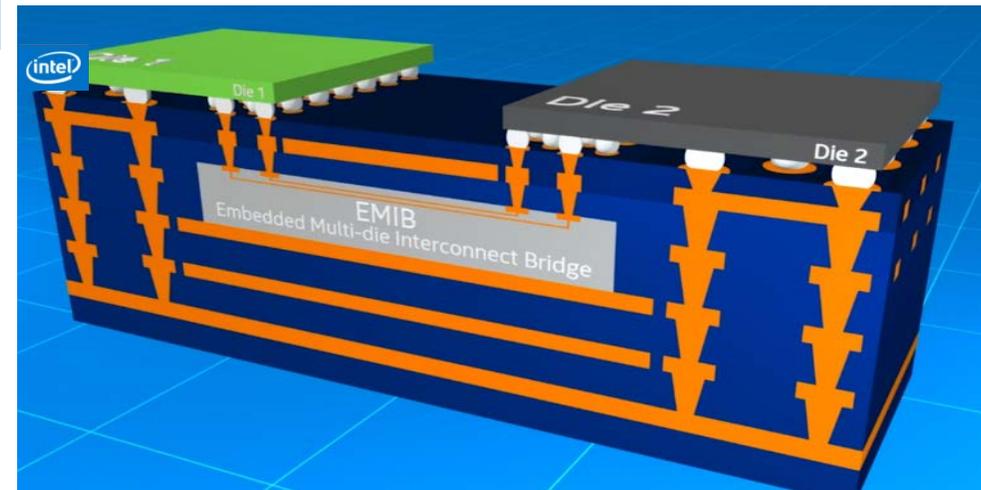
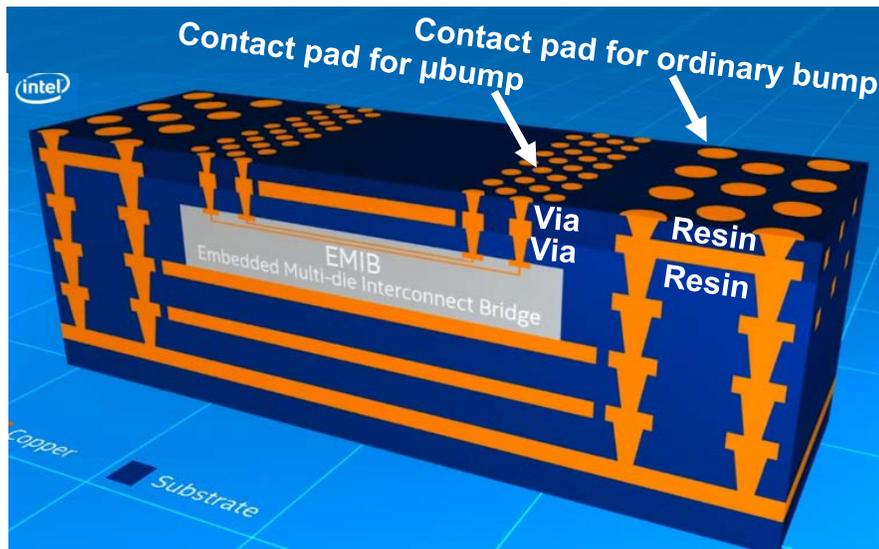
## Simple Process Flow of the Intel EMIB Technology



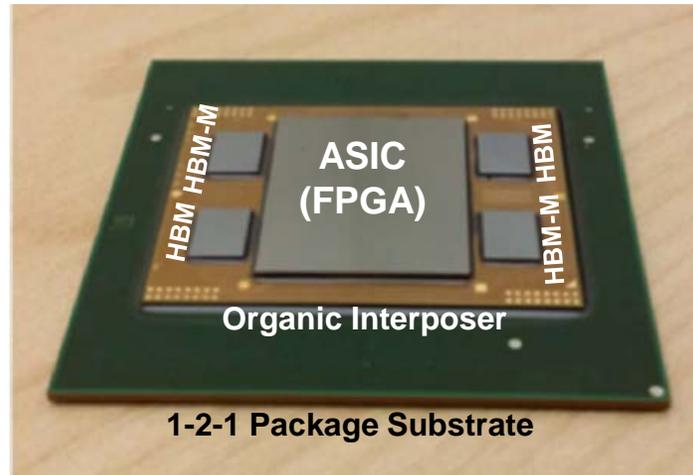
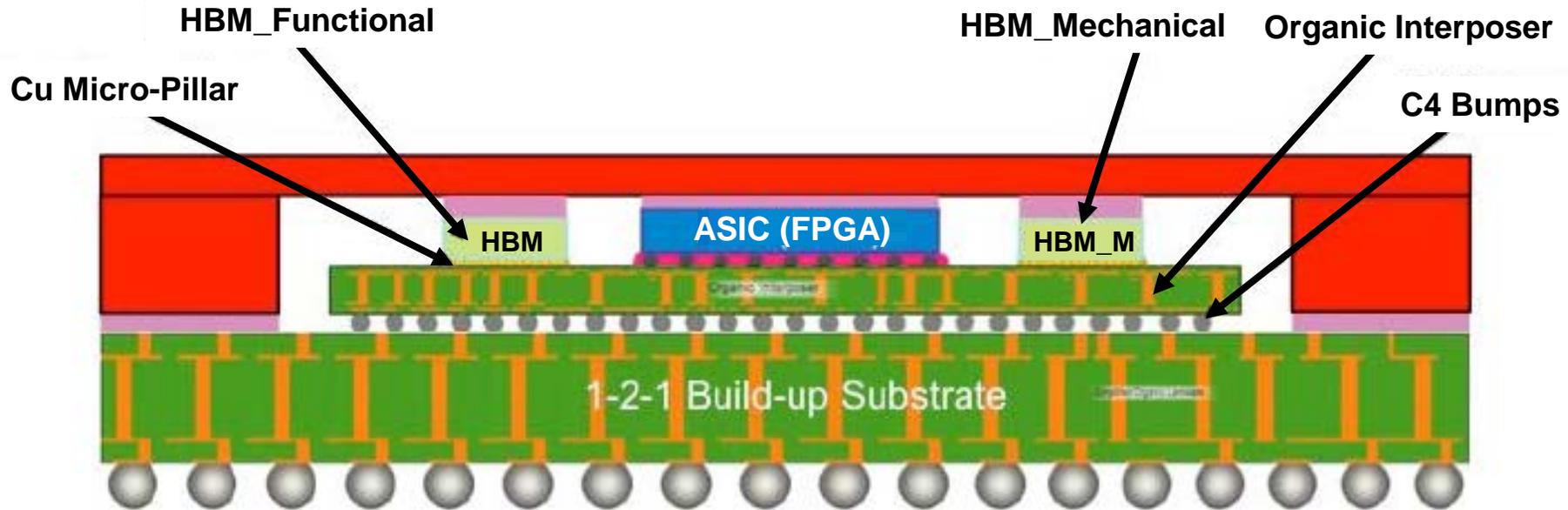
(a)



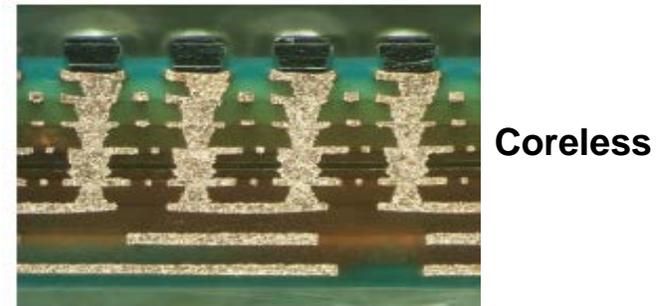
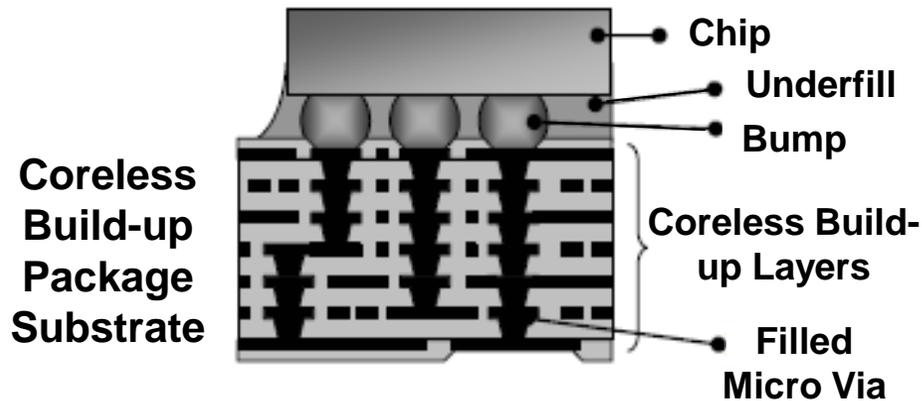
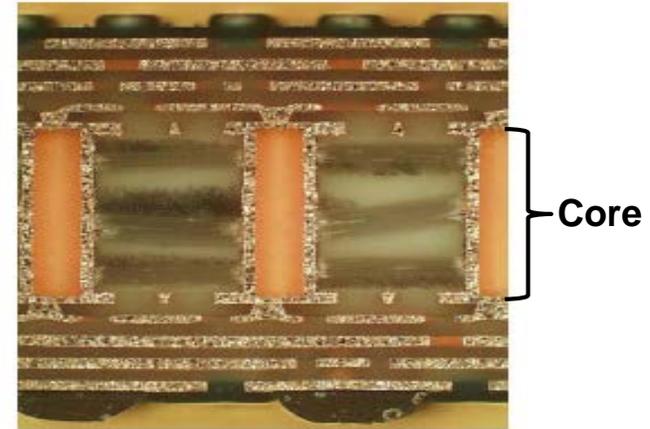
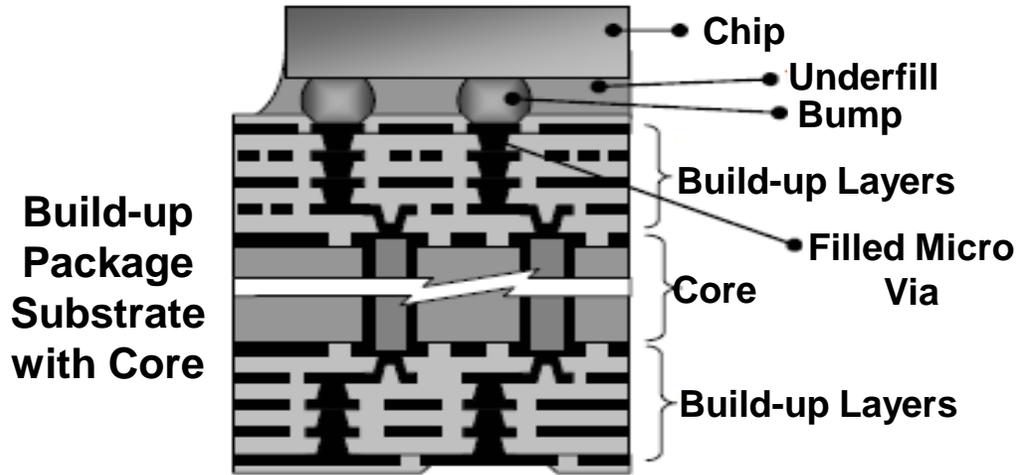
(b)



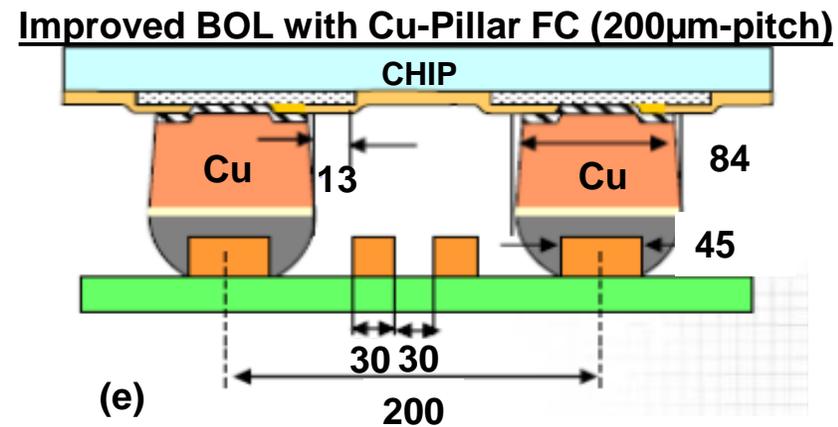
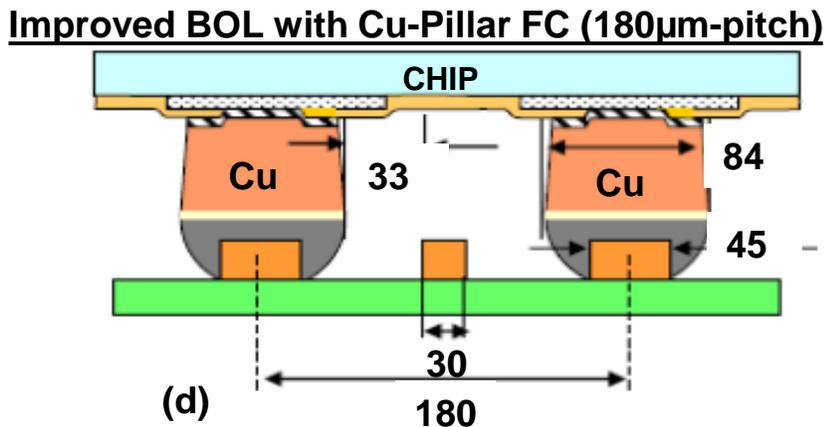
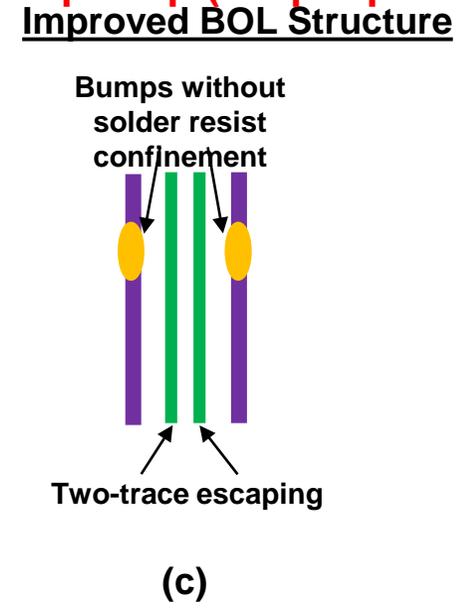
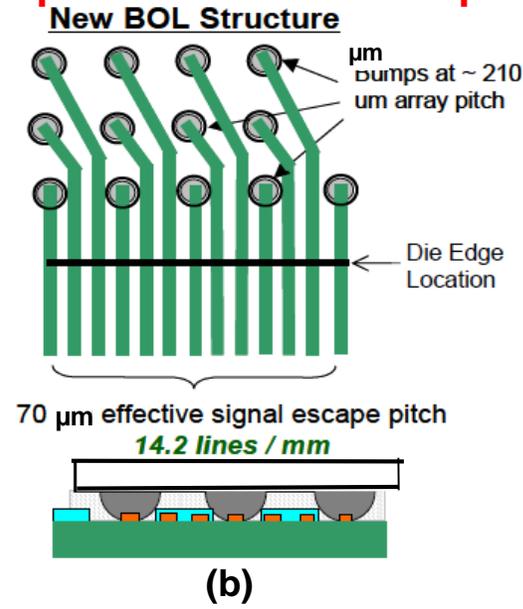
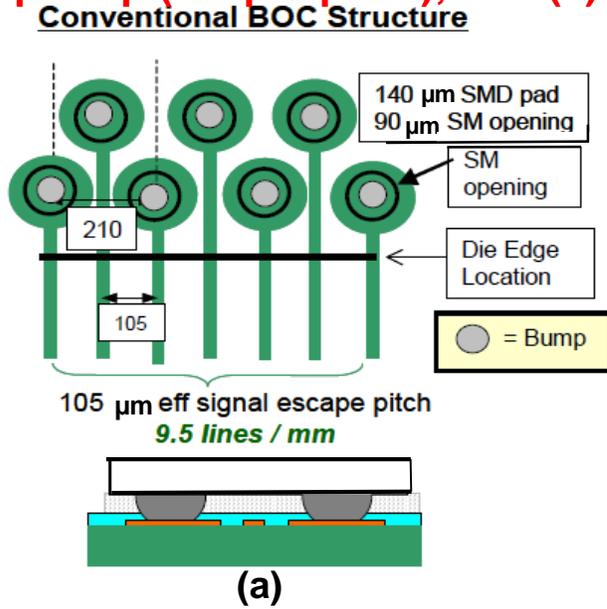
## Cisco/eSilicon's SiP with Organic Interposer



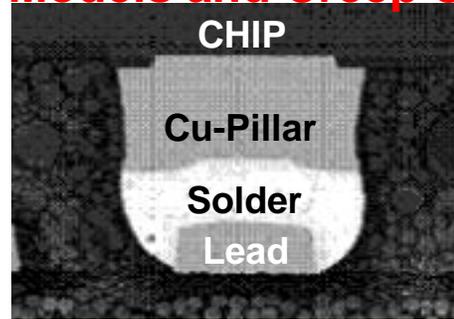
**(Top) Flip Chip on Conventional Build-up Package Substrate.  
(Bottom) Flip Chip on Coreless Substrate**



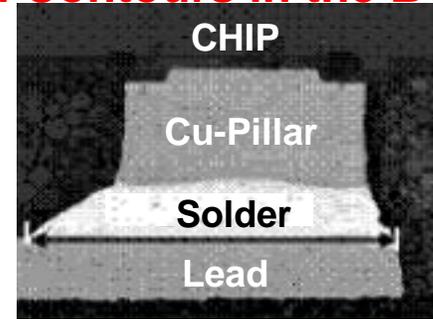
**BOL (a) Conventional BOP, (b) New BOL, (c) Improved BOL, (d) Improved BOL with Cu-pillar Flip Chip (180 $\mu$ m-pitch), and (e) Improved BOL with Cu-pillar Flip Chip (200 $\mu$ m-pitch)**



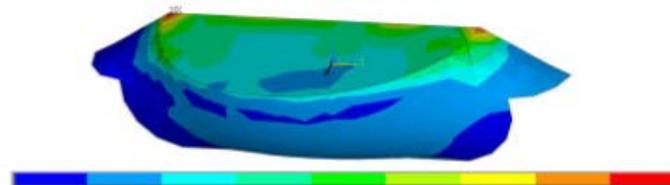
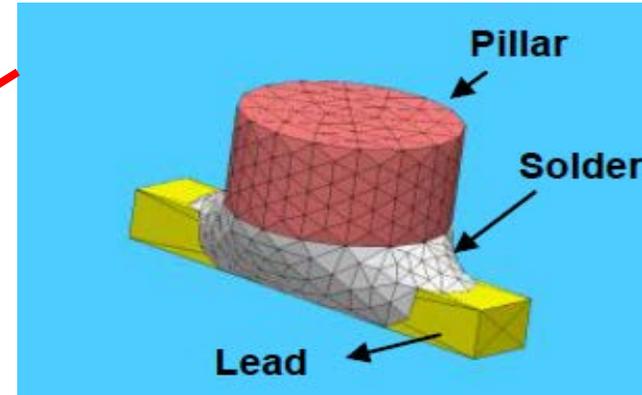
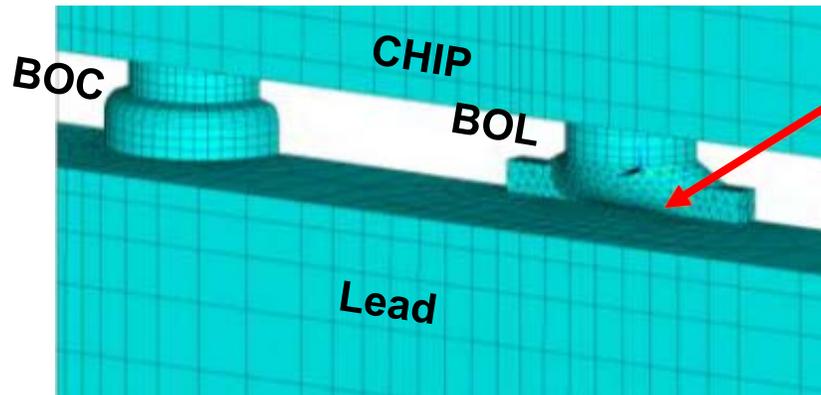
**Images of the Perpendicular-to-BOL and Longitudinal-to-BOL.  
Finite Element Models and Creep Strain Contours in the BOL Solder Joint**



Perpendicular to BOL

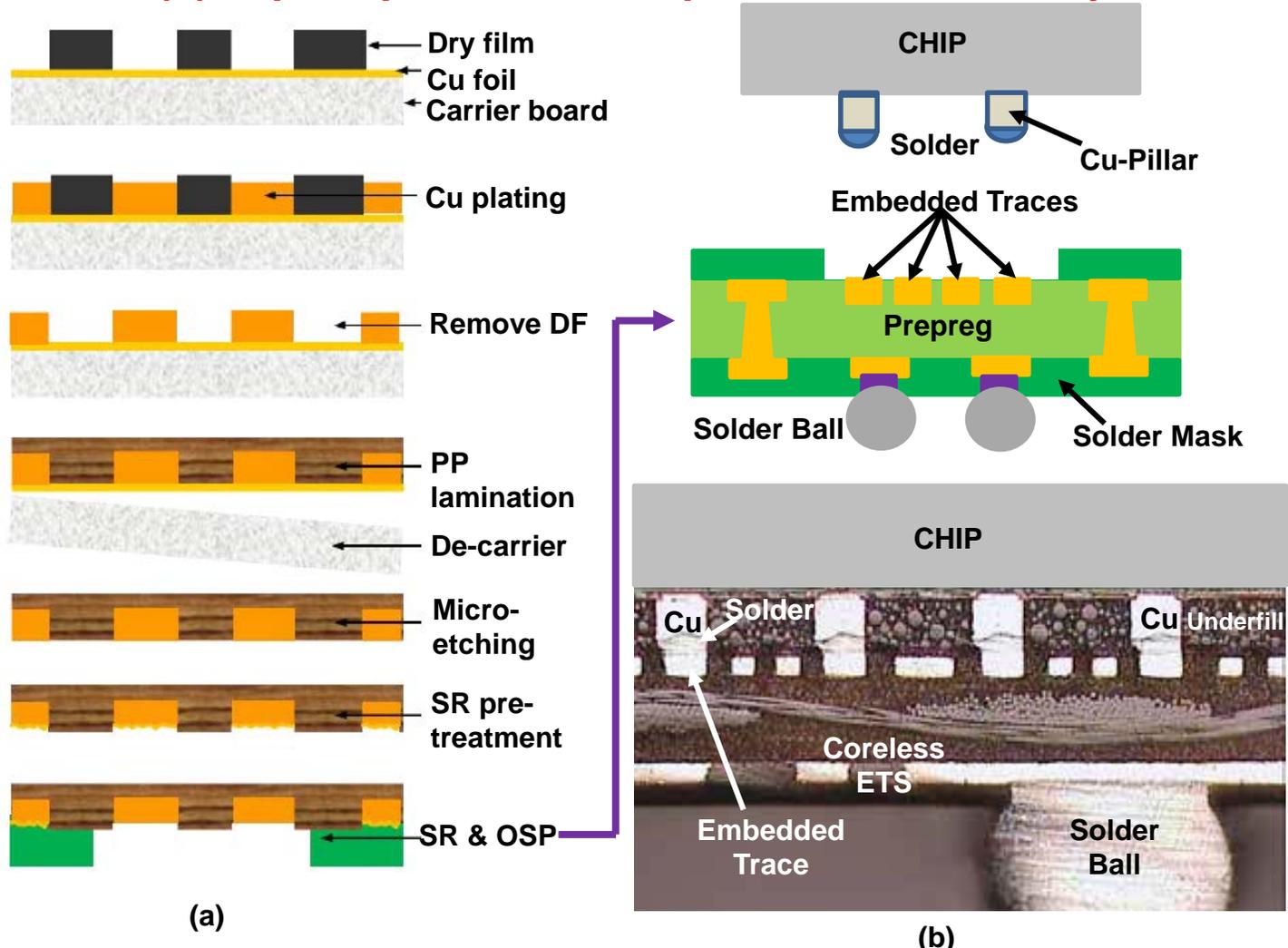


Longitudinal to BOL

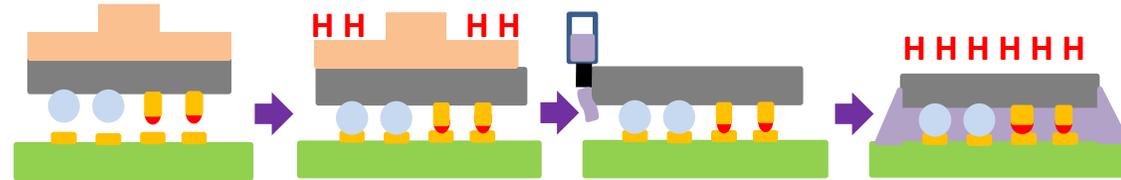


Creep strain contour in the BOL solder joint

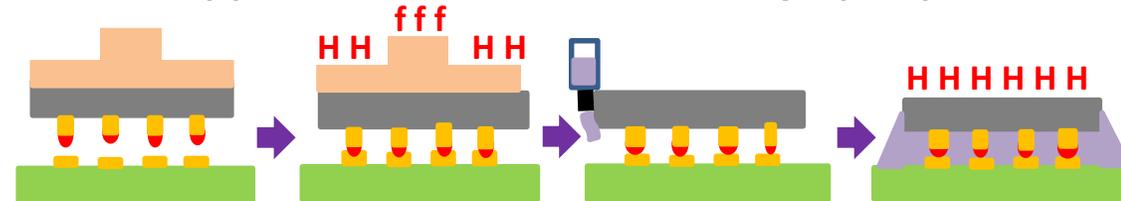
**(a) Process Flow for Fabricating the ETS and  
(b) Flip Chip with C2 Bumps on ETS Assembly**



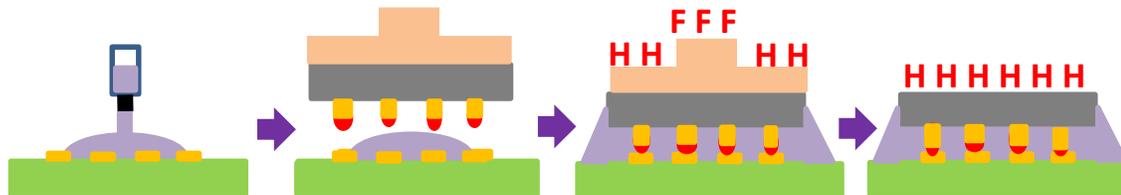
**Flip Chip Assembly: (a) Mass Reflow of Chips with C4 or C2 Bumps with CUF, (b) TCB with Low-Force of Chips with C2 Bumps with CUF, (c) TCB with High-Force of Chips with C2 Bumps with NCP, and (d) TCB with High-Force of Chips with C2 Bumps with NCF**



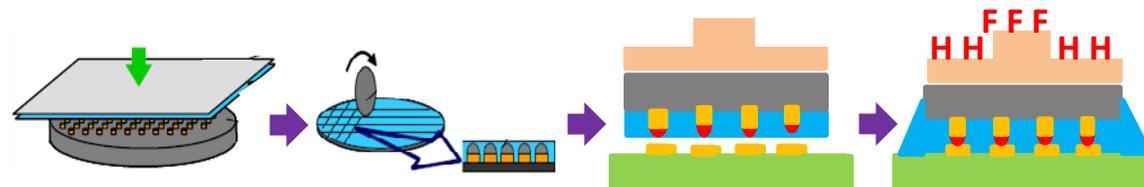
**(a) Mass Reflow of C4 or C2 Bumps (CUF)**



**(b) TCB with Low-Force of C2 Bumps (CUF)**

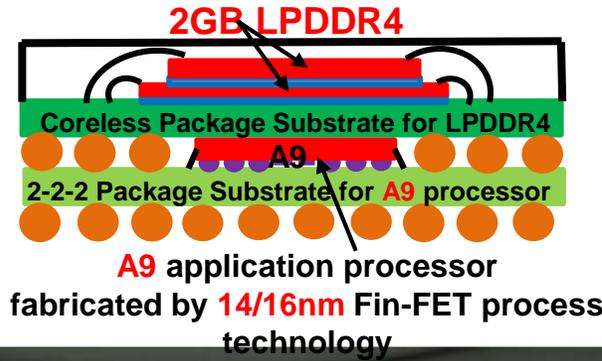


**(c) TCB with High-Force of C2 Bumps (NCP)**



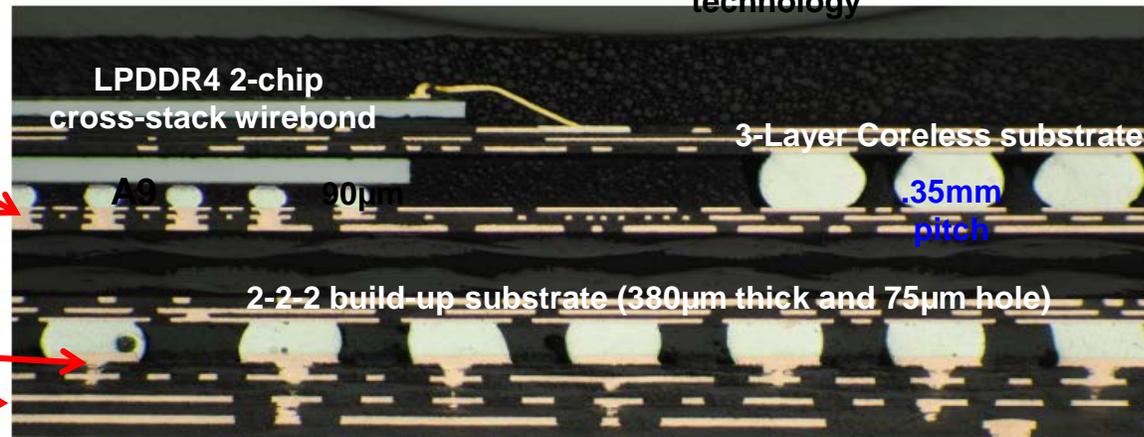
**(d) TCB with High-Force of C2 Bumps (NCF)**

**PoP in Apple's iPhone 6/6+. In the Bottom Package, the C4 Solder Bumped (A9 AP) Flip Chip is Mass Reflowed on a 2-2-2 Package Substrate with an Underfill, and then BGA to the PCB**

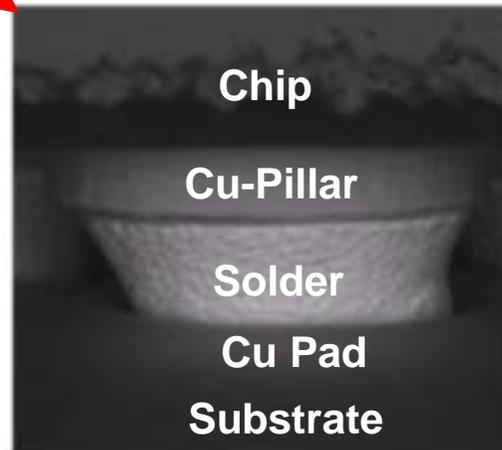
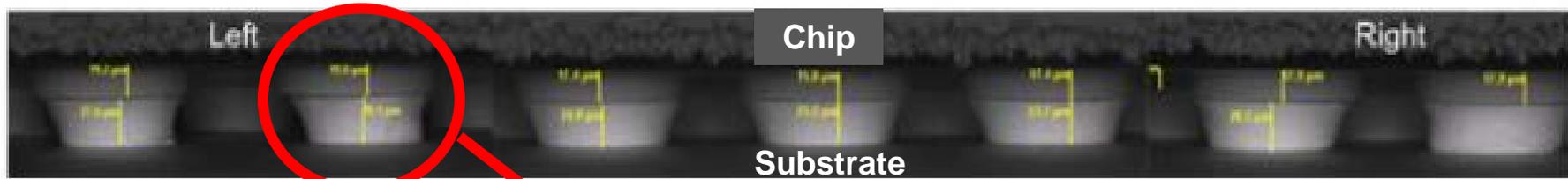


150µm pitch  
staggered  
C4 bumps

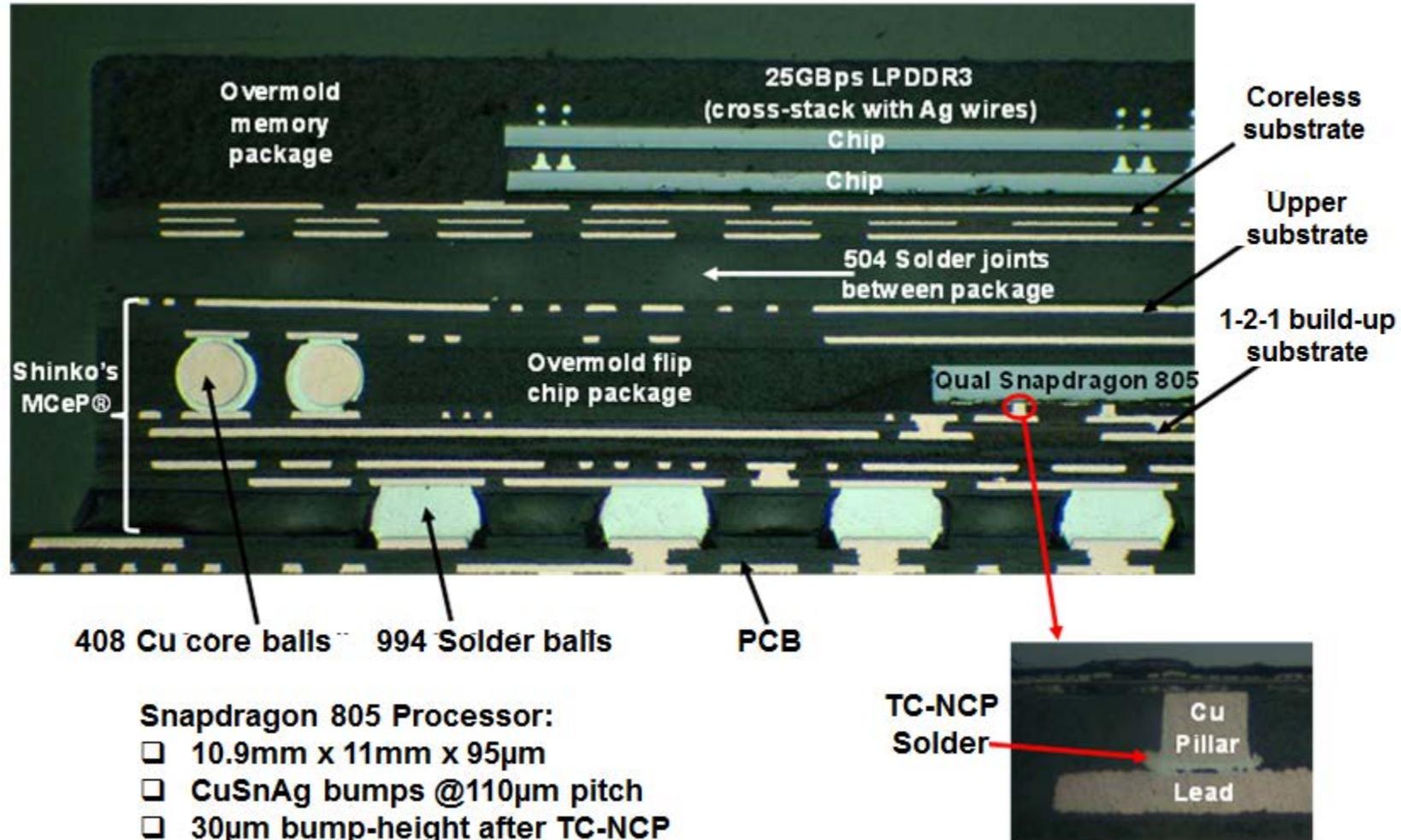
0.4mm pitch  
solder balls  
PCB



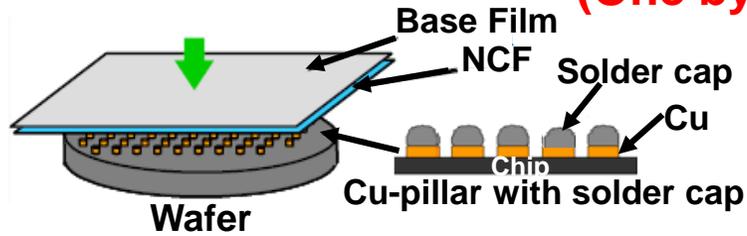
**Cross Section of a C2 Flip Chip Assembled on an  
Organic Package Substrate by a TCB with Low-Force (CUF)**



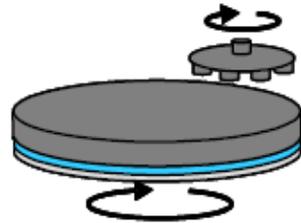
**PoP in Samsung's Smartphone. The C2 Flip Chip is TCB with High-Force on a Package Substrate (TC-NCP)**



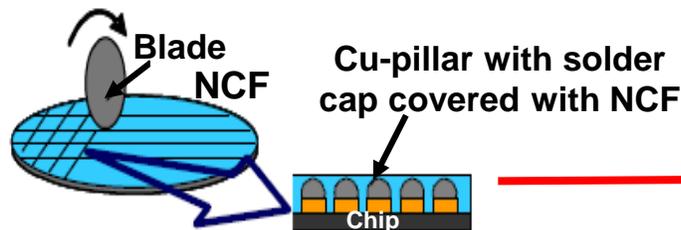
**Lamination of NCF on a C2 Bumped Wafer, Dicing, and TCB of NCF Flip Chips  
(One by One)**



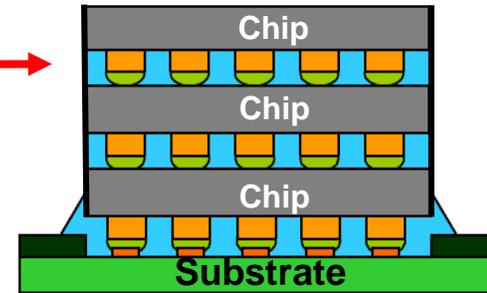
**NCF Lamination for wafer**



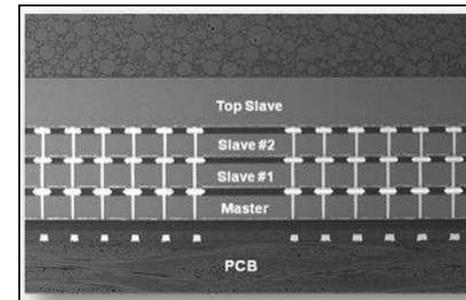
**Cutting to wafer size and backgrinding**



**Removing based film and dicing  
the bumped wafer with NCF**

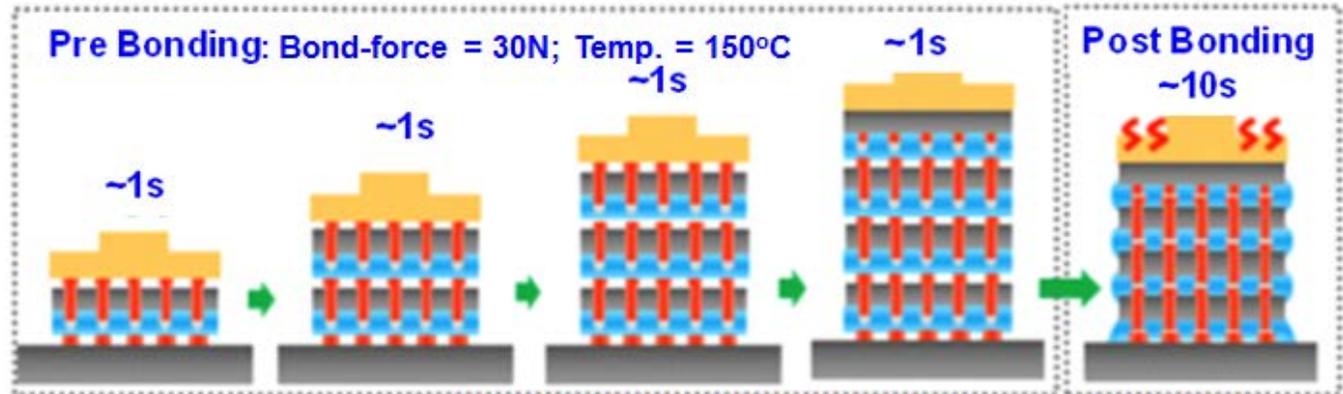


**TCB with NCF**



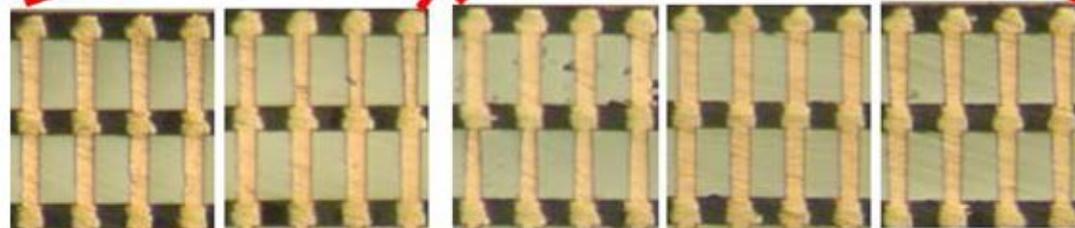
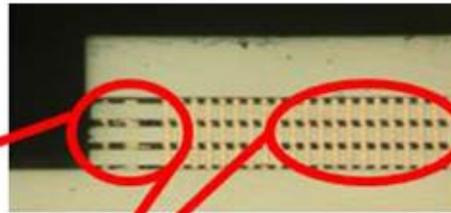
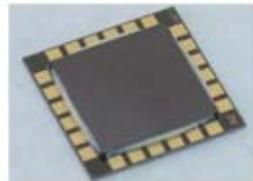
**Samsung's 3D IC integration  
by TCB with NCF**

**Toray's Collective TCB with High-Force with NCF Flip Chips**



Stage temperature = 80°C

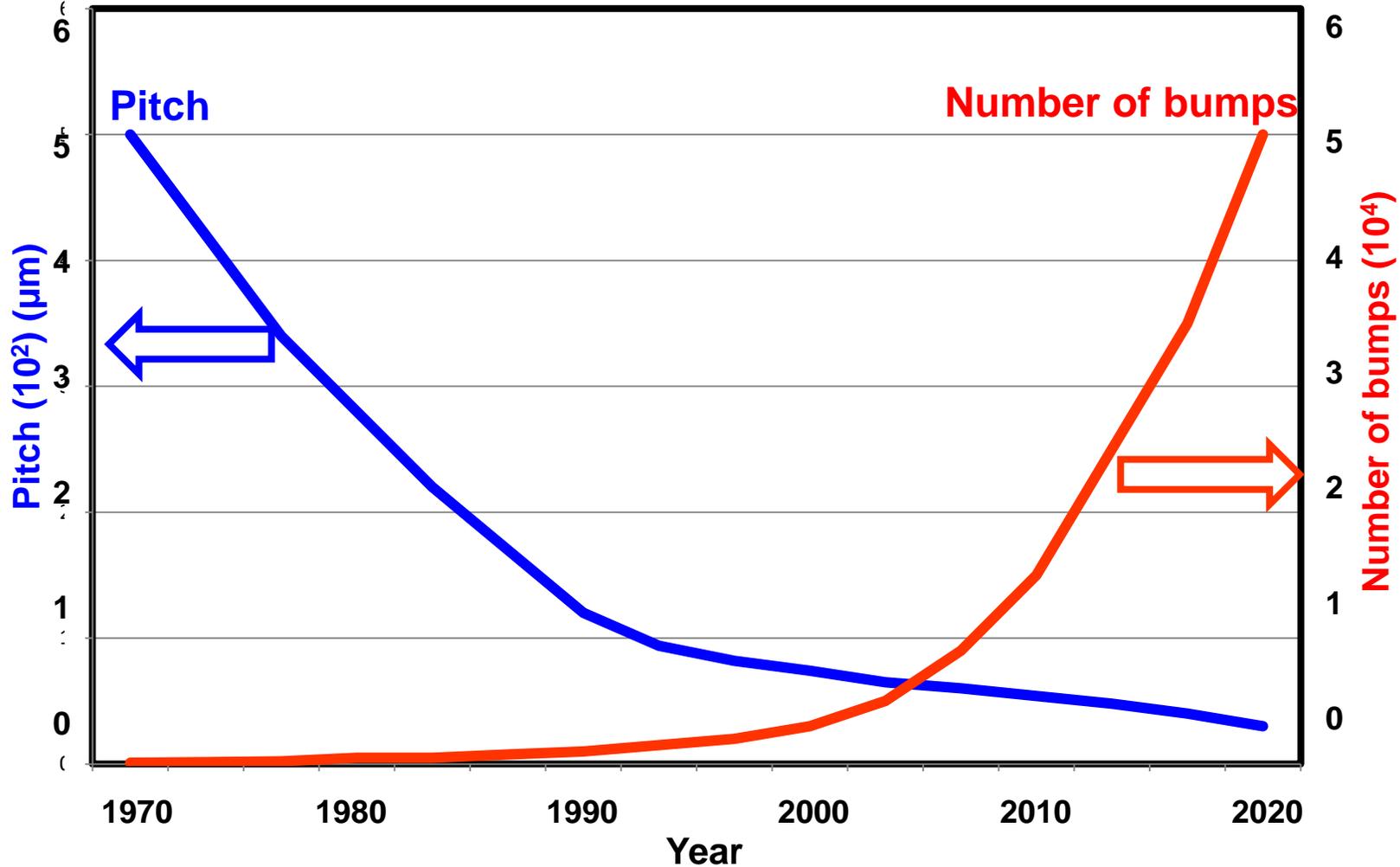
1<sup>st</sup> step (3s):  
Bond-force = 50N  
Temp. = 220-260°C  
2<sup>nd</sup> step (7s):  
Bond-force = 70N  
Temp. = 280°C



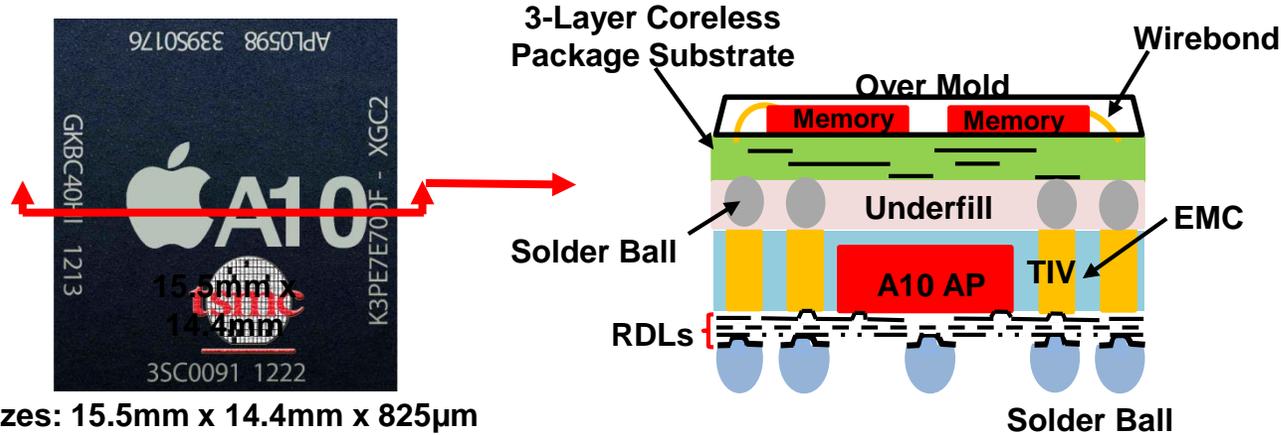
Peripheral portion

Area portion

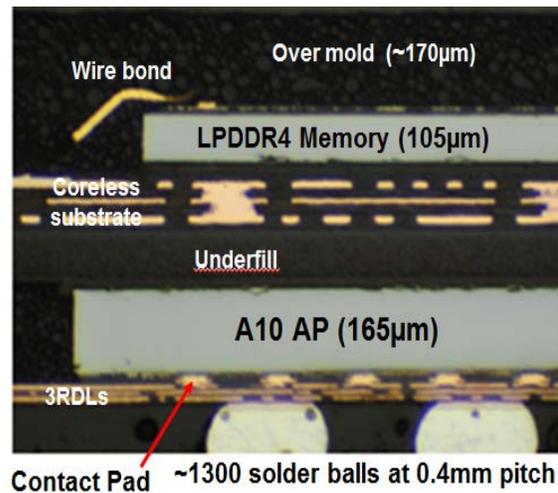
**Trend in Flip Chip Bump and Pitch**



**PoP in Apple's iPhone 7/7+. In the Bottom Package, the A10 AP is Embedded in the EMC and its Circuitry is Fanned Out through the RDLs to the PCB**

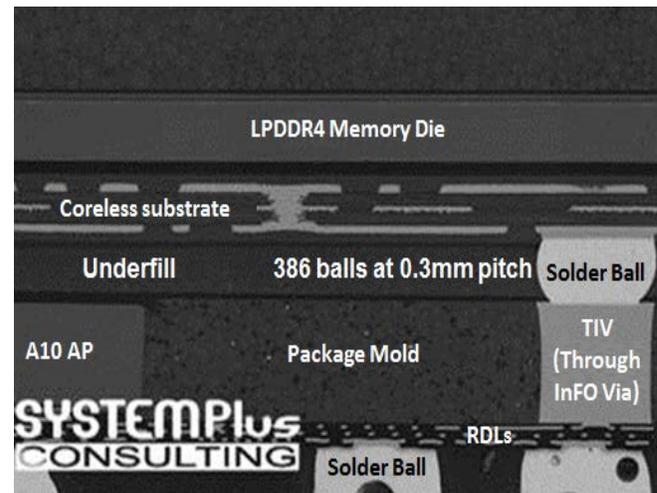


PoP sizes: 15.5mm x 14.4mm x 825µm



~1300 solder balls at 0.4mm pitch

Binghamton University/Prismark



~1300 solder balls at 0.4mm pitch

SYSTEMPLUS CONSULTING

## SUMMARY

- Flip chip technology came from a long way. From the three-bump flip chip to 10,000-bump flip chip, and could be 50,000-bump flip chip by the year of 2020. Also, by that time, the flip-chip pitch could be as small as 30µm.
- C2 bumps have better thermal and electrical performance and can go down to finer pitch (smaller spacing between pads) than C4 bumps.
- The self-alignment characteristic (one of the most unique features of flip chip technology) of the C2 bumps is nowhere near the C4 bumps. Thus, mass reflow is usually applied to C4 bumped chips.
- C2 bumped chips are usually assembled by TCB with high-force, while low-force is sometime used.
- The advantages of TCB are for higher pin-count, finer pitch, thinner chips, higher-density, and thinner package substrates, and controlling warpage and die tilt. One of the drawbacks of TCB is throughput (compared with mass reflow).
- A package substrate with ten build-up layer (5-2-5) and 10µm linewidth and spacing is more than adequate to support most of the flip chips. In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements.
- such as the sliced FPGA, even a 12 build-up layer (6-2-6) package substrate is not enough to support the chips and a TSV interposer is needed.
- As of today, TSV-interposer is very expensive. In order to lower the cost, enhance the electrical performance, and reduce the package profile, TSV-less interposers such as the Xilinx/SPIL's SLIT, Amkor's SLIM, SPIL/Xilinx's NTI, Intel's EMIB, and Cisco/eSilicon's organic interposer have been developed. This will be the trend in package substrate for high-density and performance flip chip applications.
- More research and development works should be done on innovative and low-cost ETS and coreless substrates for portable, mobile, wearable, and IoTs applications. More research and development works should be done to effectively use the BOL technique to increase routing density, and thus, lower the cost and reduce the size of organic package substrate.

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**Thank you!**

**Questions?**

**Thank you very much for your  
attention!**

