Using Condensation Testing with Surface Insulation Resistance Measurements for QFN Reliability Assessment

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Quad Flat Non-lead (QFN) packages are finding increased uses in high reliability applications due to their smaller footprints, improved thermal and electrical performance [1] and as such there is increased focus on their reliability performance in harsh environments [2 to 5]. In order to investigate issues with condensation and surface insulation resistance (SIR), a range of test vehicles were assembled incorporating QFN components alongside other components, using two advanced production lines in Sweden. These boards were produced with multiple no-clean solder pastes using convection and vapour phase soldering. The aim of the project was to take surface insulation test boards based on the IPC B52 test pattern and assess the impact of conventional SIR testing of QFNs alongside a newly developed condensation test.

This condensation test has been driven by an increased requirement to understand the performance of electronic assemblies in humid environments. Whenever there are high levels of ambient humidity, if parts of the assembly drop below the dew point, there is the opportunity for the formation of condensed water on the surface of components and substrate. This can significantly reduce the insulation resistance of the substrate surface, resulting in malfunctioning electronics.

Reproducing repeatable levels of condensation during testing can be challenging. Most humidity chambers are designed to achieve stable, well controlled humidity and temperature conditions, but none of these offer condensing options. Therefore the user has to improvise. Existing common approaches include ramping at a fast enough rate to cause condensation, or running chambers very close to 100% relative humidity. A drawback of these approaches is that chambers of different designs will perform differently, and will be sensitive to small drops in cooling performance.

At the company, a new approach has been developed where the test board is mounted on a platen whose temperature can be independently controlled without changing the ambient condition in the humidity chamber. Thus, the temperature of the test board can be lowered below ambient to any desired point and hence, produce different levels of condensation. It is therefore straightforward to cycle between condensing and non-condensing conditions on the test board in a constant ambient environment. The technique has been demonstrated to be repeatable and controllable, with the user able to select a temperature differential that matches their worst in-use conditions, or to understand the performance of their system under a range of condensing conditions.

Modification of the test board in this project, allowed the group to test the impact of residues under the QFN/LGA packages with the introduction of SIR test patterns under four packages per board. There has been much debate on the reliability of the cleanliness under these packages and the possibility of surface corrosion. This work investigates the current uncertainty.

This paper outlines the processes and parameters used for manufacture which featured surface mount reflow and through-hole selective soldering with no-clean fluxes. The results from the same boards with different paste products have been compared with testing under traditional exposure to elevated temperature and relatively humidity plus the controlled introduction of moisture to the test board.

Introduction

The electronics industry has a long history of utilizing smaller component packages to increase packing density, to reduce the form factor of products or to improve functionality within the same outlines. QFN/BTC packages are finding an increasing number of applications including space and other high reliability applications. Their smaller dimensions coupled with relatively large heat sinks result in good heat dissipation. Smaller size and leadless interconnects also leads to low parasitics and improved electrical performance. However, the reduced pitch of these devices has led to concerns about their performance in humid environments, where under bias, the short path lengths between terminals to form electrical shorts through electrochemical corrosion may lead to surface insulation resistance (SIR) reductions.

The SIR technique has been widely used to assess the effect of contaminants on the reliability of assemblies. When compared with other methods, SIR measurements have the advantage that they can be used to detect the localised contamination and can measure the effect of contaminants, both ionic and non-ionic, on the reliability of the printed circuit assembly. Reliability is a key issue impacting on today's electronics, and the SIR technique has been widely used to assess the effect of contaminants on the reliability of assemblies. The technique periodically measures the insulation resistance between two conductors under an applied bias in a humid environment. If contamination is present, this affects the insulation resistance of the patterns, and this change is usually measured over a seven-day period. If all other variables are equal, closer spacing of

the conductors will lead to lower SIR values and potentially earlier failures. Hence the concerns associated with the finer pitches of QFNs.

SIR testing is undertaken in non-condensing environments at elevated levels of temperature and humidity (45 to 85ºC, 65 to 93%RH) which creates an absorbed water layer on the surface of the assembly. It is in this layer that the corrosion cell forms. In condensing environments, the thickness of the water layer is significantly increased, increasing the mobility of the contaminants. The results for powered electronics assemblies are short-circuits or even permanent corrosion.

There are existing methods for generating condensing conditions within humidity chambers, utilising differing approaches which have been summarised previously by the authors [6]. These include rapid ramping of the temperature and humidity conditions, introducing moisture by a secondary moisture source or using a multi-chamber approach where the working area climatic environment is rapidly changed by injecting an alternative environment from a reservoir chamber. While these methods can demonstrate condensation, the control and ease by which they generate condensation remains challenging. Almost all of these approaches generate condensation in humidity chambers, and this leads to a challenge, since the chamber systems are developed to minimise condensation. In these cases, chambers are run very close to 100%RH, inducing condensation. However, the uniformity of this condensation within the chamber is unknown. Hence, reproducibility of the given approaches will be variable between different chambers from different manufacturers. None of these approaches control the sample temperature condition, and hence the uniformity of the condensed water layer is unknown and the stability of the condensed water film with time may not be controllable, as the chamber control system attempts to compensate for the variance in the nominal conditions set for the chamber.

The approach developed at the company overcomes many of these difficulties by controlling the temperature of the circuit assembly under test. By lowering the temperature below the dew point in a high humidity environment, the level of condensation of the assembly can be reproducibly controlled.

Experimental setup

The test vehicle was an IPC B52 SIR test-board modified to accommodate four QFN/LGA packages. The QFN terminations were 0.5mm pitch with 0.15mm tracks between each of the mounting pads (0.76mm x 0.2mm). There was no solder mask around the mounting pads. The available interconnection on the test board only allowed two separate channels to be monitored so two QFN parts were linked together in each pattern. The test vehicle and a close-up of the QFN patterns are shown in Figure 1. Each test vehicle incorporated a range of common components including one quad flat pack (QFP)160 in addition to the QFN packages.

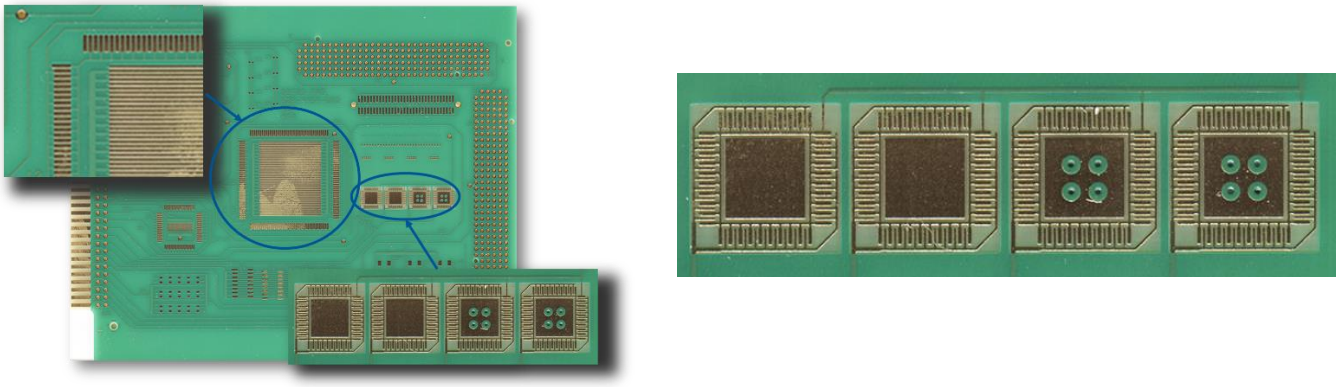

Figure 1: Modified B52 test vehicle (Left). Close-up of the SIR test pattern (right) added to the IPC-B52 board.

The test vehicles were produced on a production line operating over three days at a Swedish exhibition. Three different no-clean solder pastes from different manufacturers were jetted onto test vehicles with a nickel gold finish using a production jet paste dispenser. Surface mount (SM) components were auto-placed using production placement equipment and soldering was conducted by a production vapour phase soldering batch system using a fluid with a boiling temperature of 240ºC the peak temperature of reflow soldering for the lead-free pastes. The through-hole connectors were manually inserted prior to selective soldering using production equipment. Post assembly the test vehicles were X-ray inspected to ensure no shorting on the SIR patterns and also automatically optically inspected before packaging for dispatch to the company's test facilities. The completed assembly with an annotated diagram showing SIR patterns is shown in Figure 2.

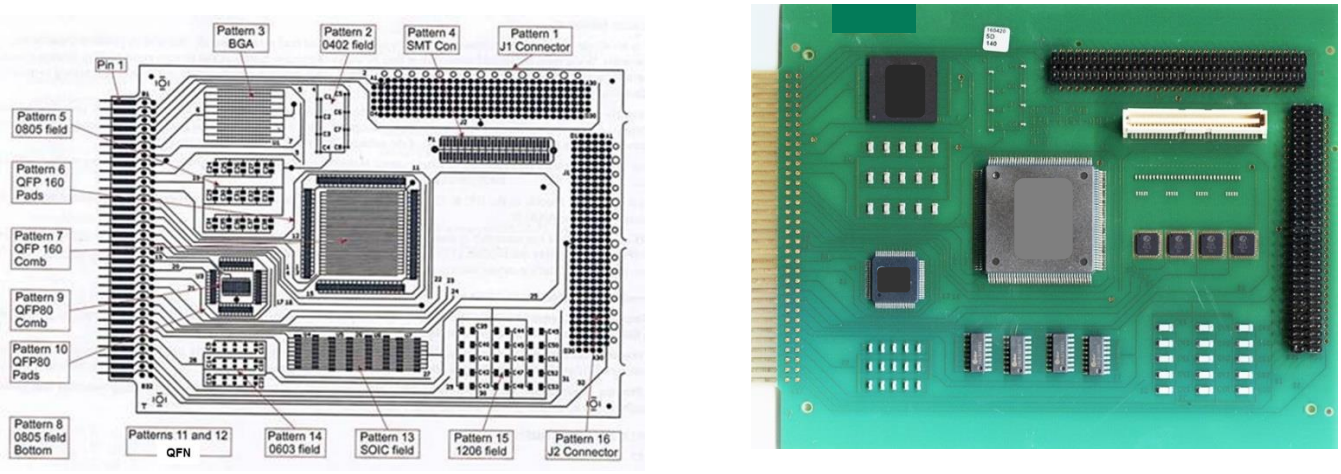

Figure 2 : Completed assembly with annotated diagram showing SIR patterns

SIR measurements were performed under constant temperature and humidity conditions of 40°C/93%RH. The first measurement for all test boards was taken under ambient conditions, then the temperature and humidity slowly increased to 40°C/40%RH over 20 minutes, and then to 40°C/93%RH over 20 minutes to avoid condensation where it was maintained for the remainder of the test. A bias voltage of 50 V DC was applied during the whole test period of 168 hours. The SIR was measured every 20 minutes. There was a 10^6 Ω resistor on each test channel to protect dendrite formation.The equipment used for the SIR measurements was a production SIR tester. At least three repeats were carried out for each solder paste. The test vehicles and SIR test mounts are shown in Figure 3.

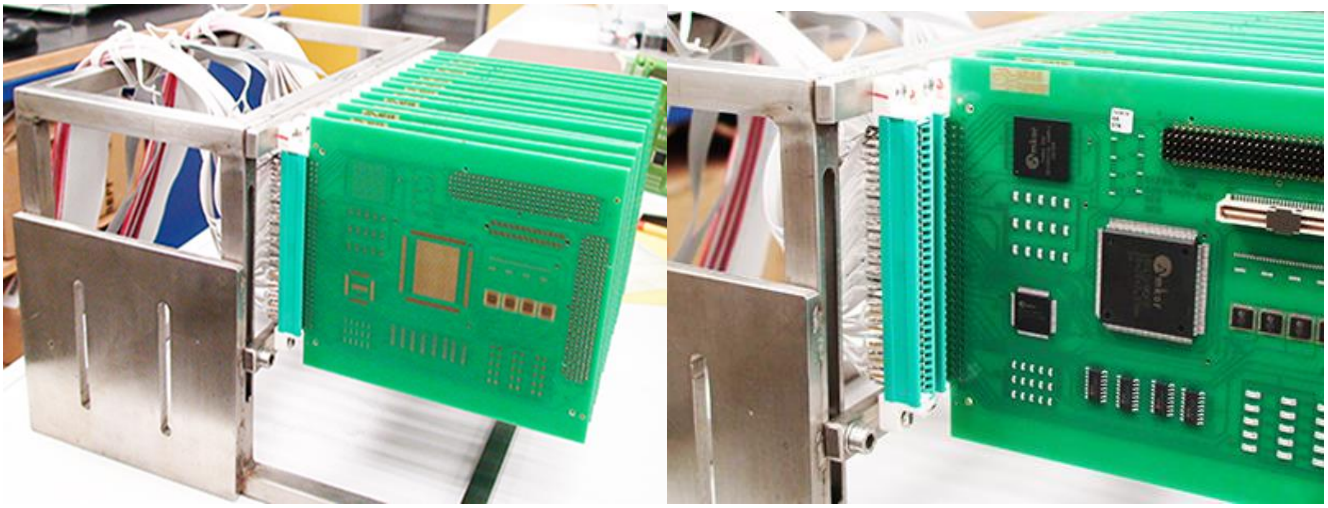

Figure 3: Sample boards mounted ready for conventional SIR testing in a temperature and humidity test chamber

Condensation testing was undertaken by mounting the test vehicles on a platen whose temperature can be independently controlled within a high humidity environment. By lowering the platen temperature below the chamber ambient, condensation will occur on the platen and the test board. The circuit board under test has a flat unimpeded under side so that it made good thermal contact with the platen. In Figure 4 PCBs are shown mounted on the platen. To allow good thermal contact with the platen, these PCBs were assembled without the through-hole connectors.

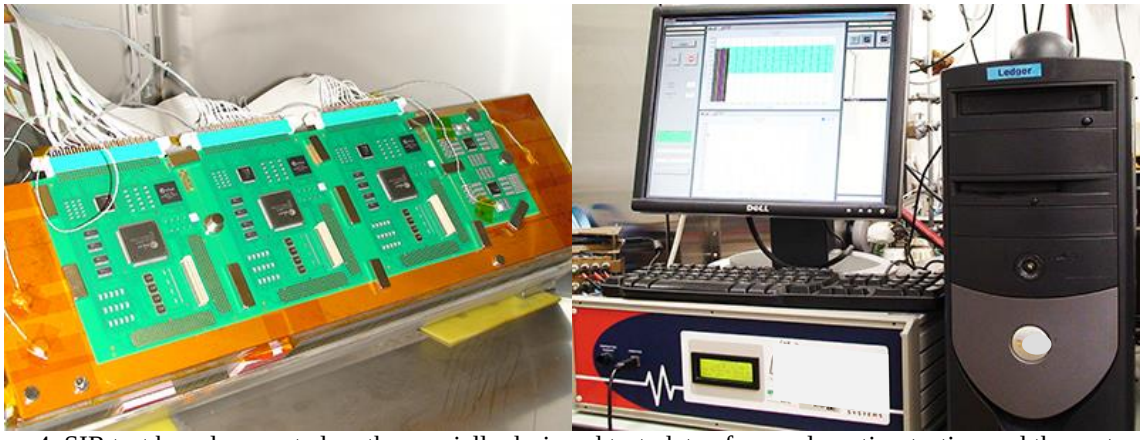

Figure 4: SIR test boards mounted on the specially designed test platen for condensation testing and the system for continuous monitoring of the test boards

The mounting technique is simple, the boards are held in position on the platen surface which is at 45º by magnets. The PCBs under test can be connected using edge connectors, since these are off the platen. In Figure 5, an example of the ability of the platen to control test board temperatures is shown.

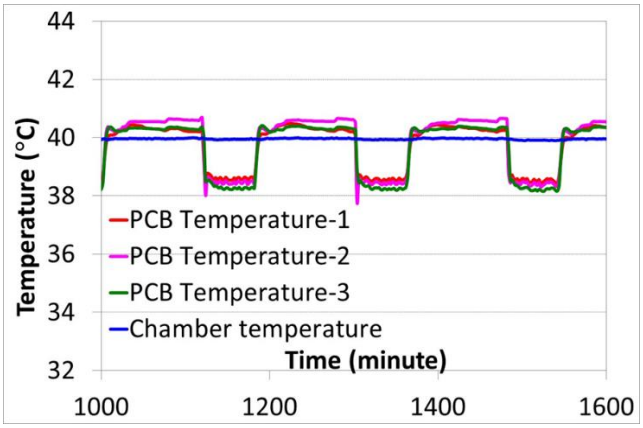

Figure 5: PCB temperature profile during platen thermal cycling

The temperature profiles shown in Figure 5 include the chamber temperature, and it can be clearly seen that this does not change as the platen and PCBs cycle up and down by 2ºC, with a nominal chamber temperature of 40ºC. This is an important advantage of this approach in that there is no attempt to use transitioning in the humidity chamber condition to create temporary condensing conditions. Furthermore, it can be seen that the transition is rapid in the cooling and heating phase of the cycle, and additionally the low temperature part of the cycle can be sustained indefinitely, or as long as set in the programme cycle.

In this work, the effect of using the condensing condition on the modified B52 test vehicle was explored using chamber conditions of 40ºC/85%RH with a 10V bias voltage. The dew point for 40ºC/85%RH is 36.8°C and the platen temperatures were cycled down to 36.6ºC (-0.2 ºC), 36.5ºC (-0.3 ºC) and 36.3ºC (-0.5 ºC) with a 2 hour cycle time.

Surface Insulation Resistance Results

The SIR results for an unassembled PCB is shown in Figure 6. The SIR does not fall below $10^{10}\Omega$ showing that any failures in assembled test vehicles were not attributable to the substrates.

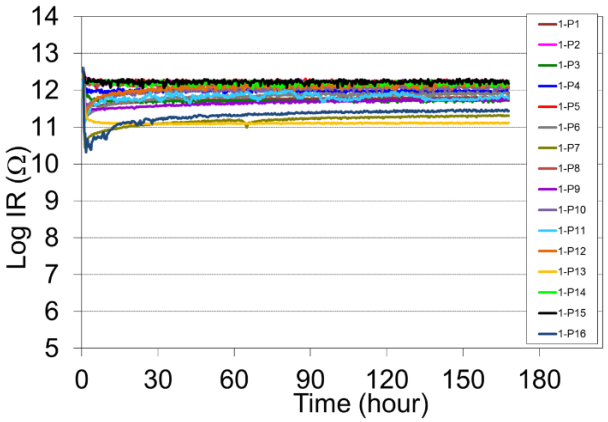

Figure 6: Bare PCB showing no failures attributable to the substrates of the test vehicles

Examples of the SIR results for the three different solder pastes can be seen in Figures 7 to 9. In all cases the SIR of patterns 1 and 16 for the two connectors were low but constant at approximately $10^8\Omega$. This was attributed to a surface finish applied to the connectors during manufacturing. For paste A, all components remained above $10^9\Omega$ and can be considered a pass. For paste B, the resistance of pattern 11 reduced to $10^6\Omega$ in the latter part of the test. This pattern is associated with the QFN components but this was the only pattern of eight repeats to fail. A similar result was noted for paste C with pattern 13, also a QFN pattern, dropping to $10^7\Omega$. This occurred on only one of six repeats. Additionally with this solder paste, the SIR for pattern 6 for the QFP160 also reduced during the test to approximately $10^6\Omega$. This occurred on only one of three repeats.

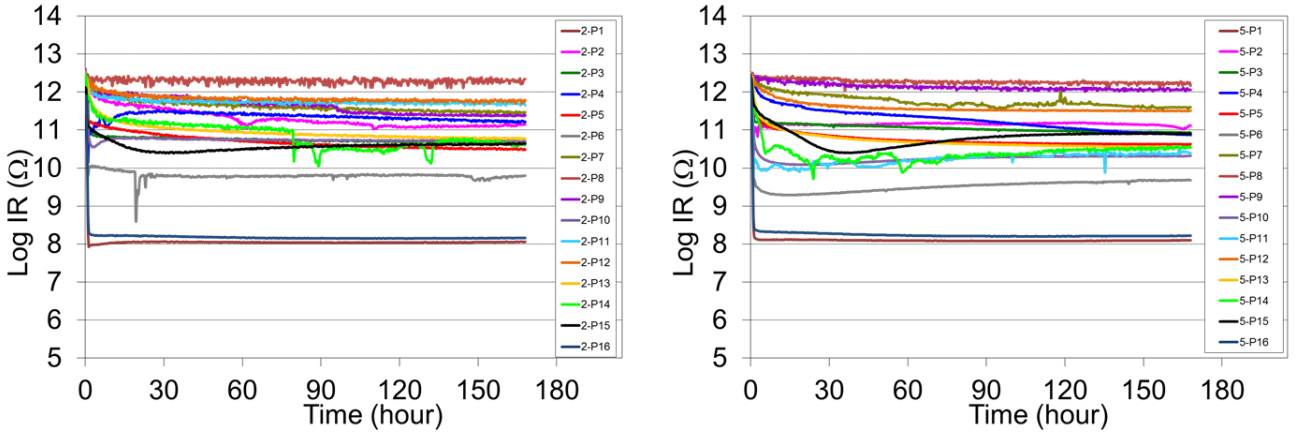

Figure 7: Example SIR measurements for paste A

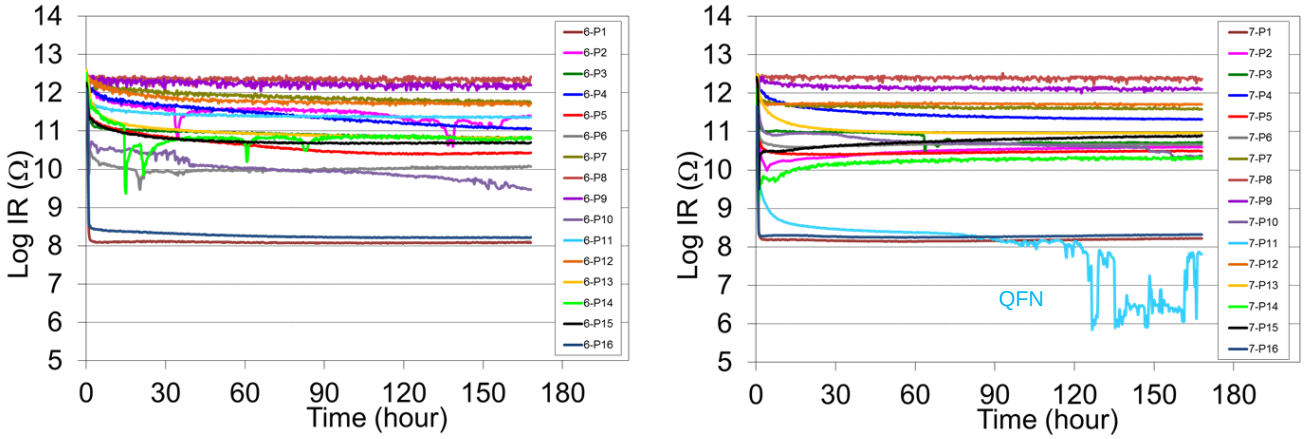

Figure 8: Example SIR measurements for paste B

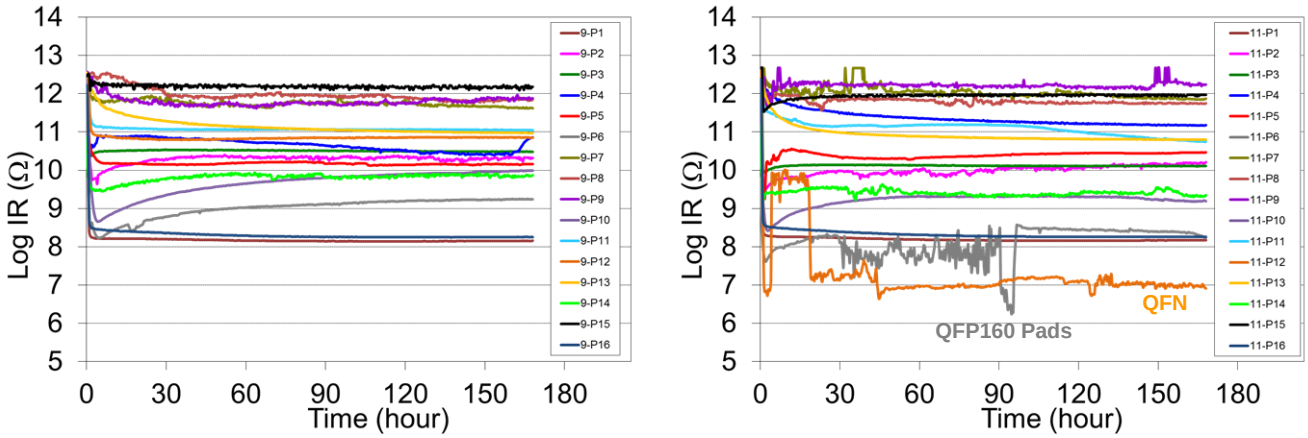

Figure 9: Example SIR measurements for paste C

Surface Insulation Resistance Discussion

Paste A showed no drop in SIR during the testing. Both pastes B and C showed some limited failures for QFN patterns. The SIR measurement test patterns for these components was very demanding, due to the small spacing on the pattern. In the QFN test pattern, one side of the pattern was formed by a track, uncovered by resist, placed between the QFN pads. This resulted in a gap between the ground and signal patterns of 75 µm. The spacing between conductors on the only other pattern to fail (QFP160 pads) was considerably greater at 250 µm. The field strength is inversely proportional to the gap, hence where the gap is smaller, it is likely to yield more failures for the same contamination levels.

Condensation Testing Results

The condensation results for the three solder pastes and all the components on the test vehicle are shown in Figure 10. For clarity the data for the QFP160 pads and QFN test patterns has been shown separately in Figures 11 to 13.

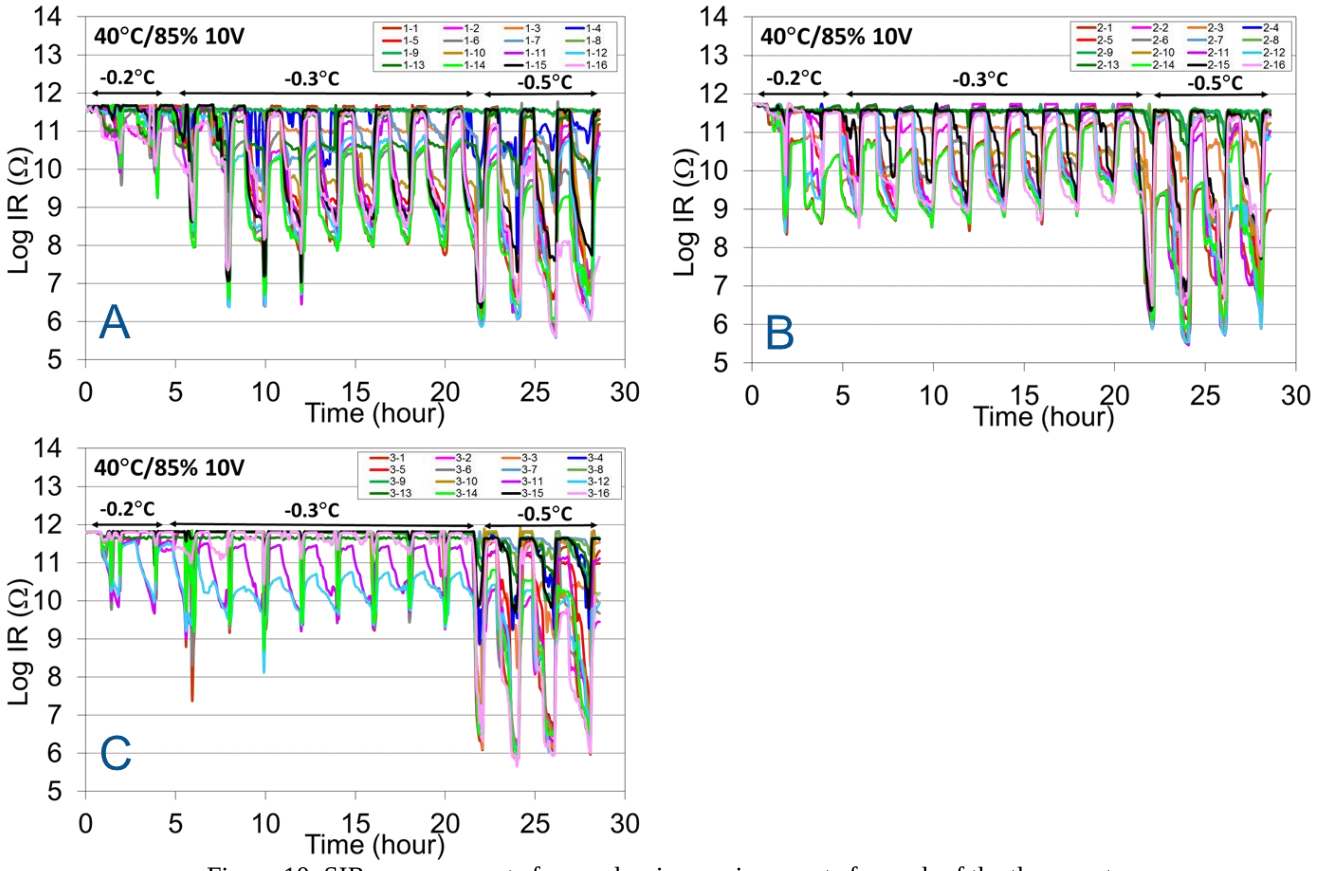

Figure 10: SIR measurements for condensing environments for each of the three pastes

For the QFP and QFN components differing responses from the three solder pastes were observed. For paste A, the SIR did not recover to its initial value when the platen temperature returned to ambient at the end of each condensation cycle and the SIR at this point in the cycle, could be seen to reduce in subsequent cycles. This effect begins to occur during cycles at -0.2 ºC platen temperature for the QFN patterns and at -0.3 ºC for the QFP pads pattern. For paste B, this only occurred for the QFN patterns at -0.5 ºC. With paste C, the responses were similar to that for Paste B but the degradation for the QFN patterns occurred earlier, starting during the cycling with the platen temperature at -0.3 ºC below the dew point.

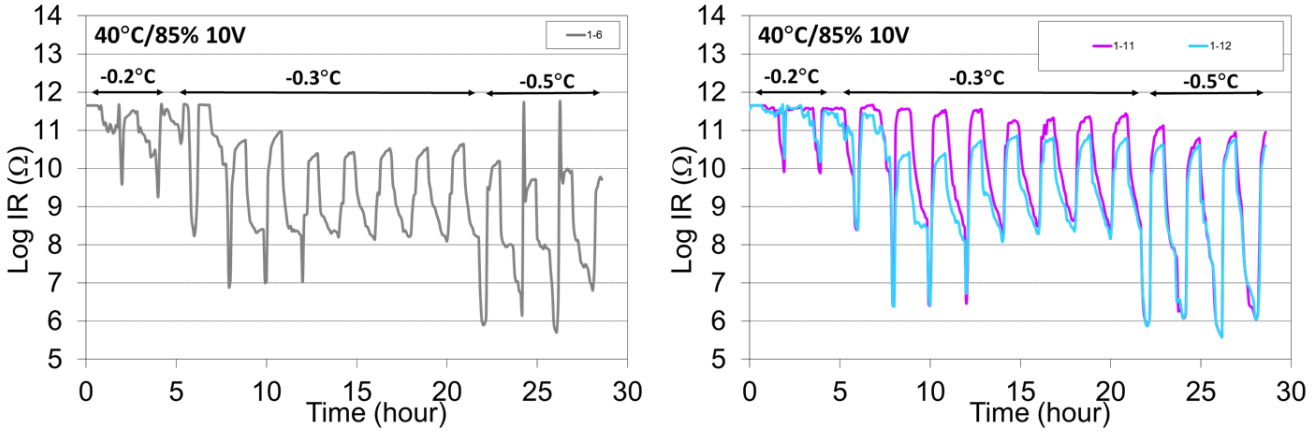

Figure 11: SIR measurements for condensing environments for paste A with QFP160 (left) and QFN40 (right)

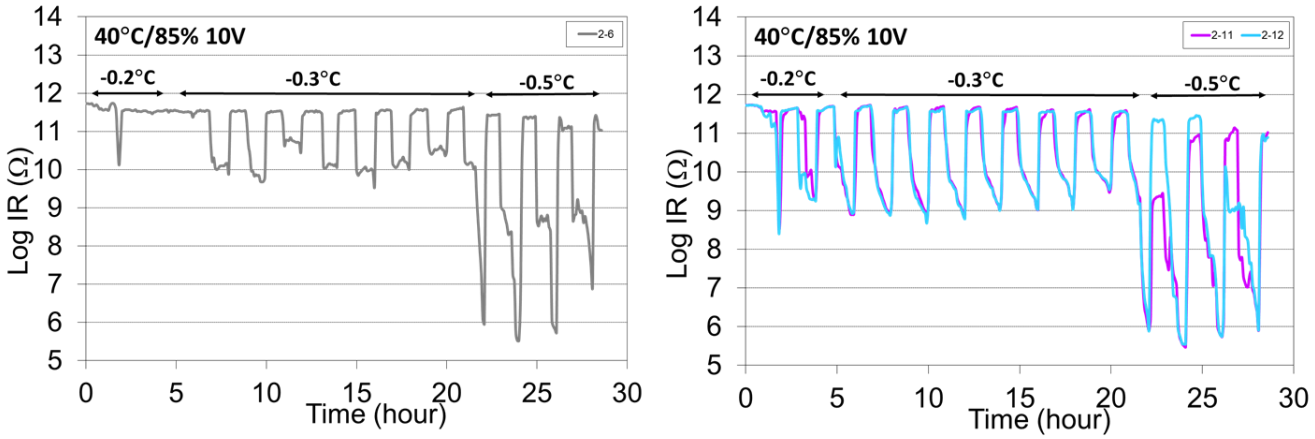

Figure 12: SIR measurements for condensing environments for paste B with QFP160 (left) and QFN40 (right)

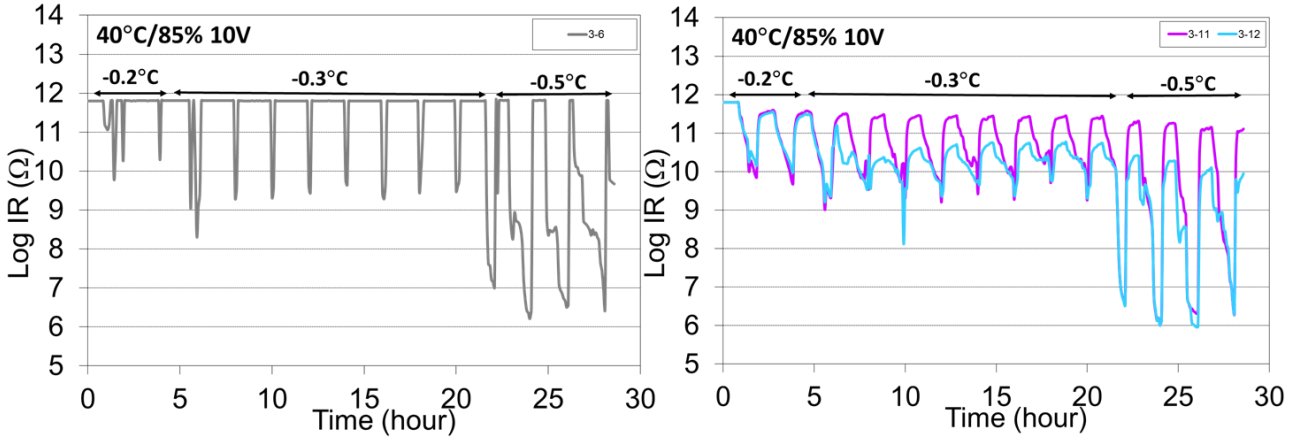

Figure 13: SIR measurements for condensing environments for paste C with QFP160 (left) and QFN40 (right)

Condensation Testing Discussion

It is well known that water films resulting from condensation can lead to anodic corrosion on powered circuitry. The condensation testing here has shown differences in responses for the different solder pastes tested. The failure to return to the initial SIR value in some patterns is an indication that damage is occurring during the condensation cycle which is not recoverable within the cycle time as the platen returns to ambient. This occurred in both the QFP160 pad and QFN patterns for Paste A and only in the QFN patterns for pastes B and C. Degradation in the QFN test pattern for paste C occurred earlier than for paste B. Whilst this data set is limited, there are indications that the responses from the solder pastes are different in condensing and non-condensing environments. During SIR measurement in the non-condensing environment, paste A offered a better performance than the other pastes, whilst this paste did not perform the best in the condensing environment. In the condensing environment, the responses from the components were also different with more degradation occurring with the QFN test patterns than for the QFP160 pad patterns. As noted previously, the SIR measurement test patterns for these components were very challenging, due to their small spacing. This smaller gap is likely to yield more failures for the same level of condensation.

The results here represent a limited data set but highlight the differences in responses for solder pastes in condensing and non-condensing environments. The condensing technique described here that has recently been developed and offers a wide range of flexibility in the test conditions. In the current setup, controlled levels of condensation can be achieved above 30ºC over a range of humidities. This work is part on an on-going programme at the company to develop this condensation method. Future work will include using this technique to evaluate a wide range of test vehicles, manufacturing techniques and protective coatings.

Conclusions

This paper has presented a comparison between the performances of test vehicles assembled using three different no-clean solder pastes. The performance has been evaluated using SIR measurements in both non-condensing and condensing environments. The solder pastes have been shown to perform differently in the differing conditions. The key result is that the paste which performed best in the non-condensing environment was not the best performer in condensing conditions.

Under both conditions, the finer pitch components (QFP160 and QFN40) showed poorer performance than coarser pitch components. The SIR measurement test pattern for the QFN patterns used here was very challenging, due to the small spacing on the pattern. In the QFN test pattern, one side of the pattern was formed by a track, uncovered by resist, placed between the QFN pads. This resulted in a gap between the ground and signal patterns of 75 μm. The spacing between conductors on the only other pattern to fail (QFP160 pads) was considerably greater at 250 μm. The field strength generated by the smaller gap is likely to lead to more failures for similar contamination and condensation levels. Further work should be undertaken in QFN test pattern design to determine their relative performance compared to other components.

These results demonstrate the need for condensation testing to determine the performance of differing manufacturing options for electronics designed to be subjected to condensing environments. The technique developed has been shown to achieve specific condensing conditions but the desired test parameters to best evaluate process and design variables still need to be developed, and this will be the scope of further work.

References

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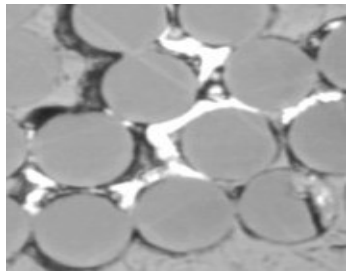
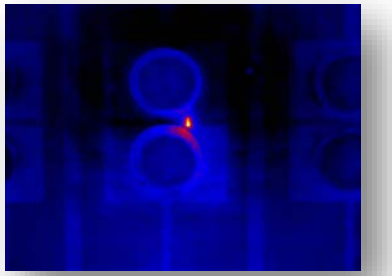
Introduction

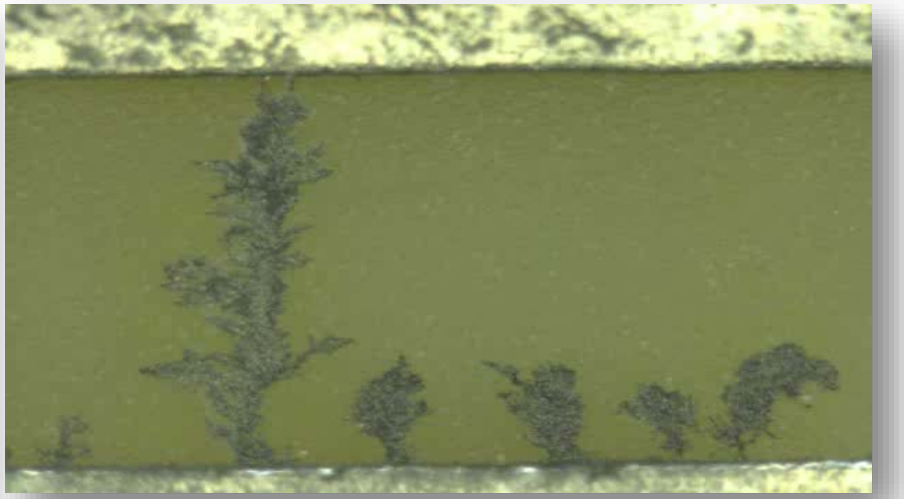
- Failure by electrochemical migration is an increasing issue as electronic feature sizes diminish, voltage and environmental stress increase
- Sensitivity to various factors need to be assessed and test methods are in various stages of development including Surface Insulation Resistance Testing and Condensation Testing
- For biased circuits the most important metal corrosion induced failures are dendrites and CAF formation.

Dendrite short two conductors

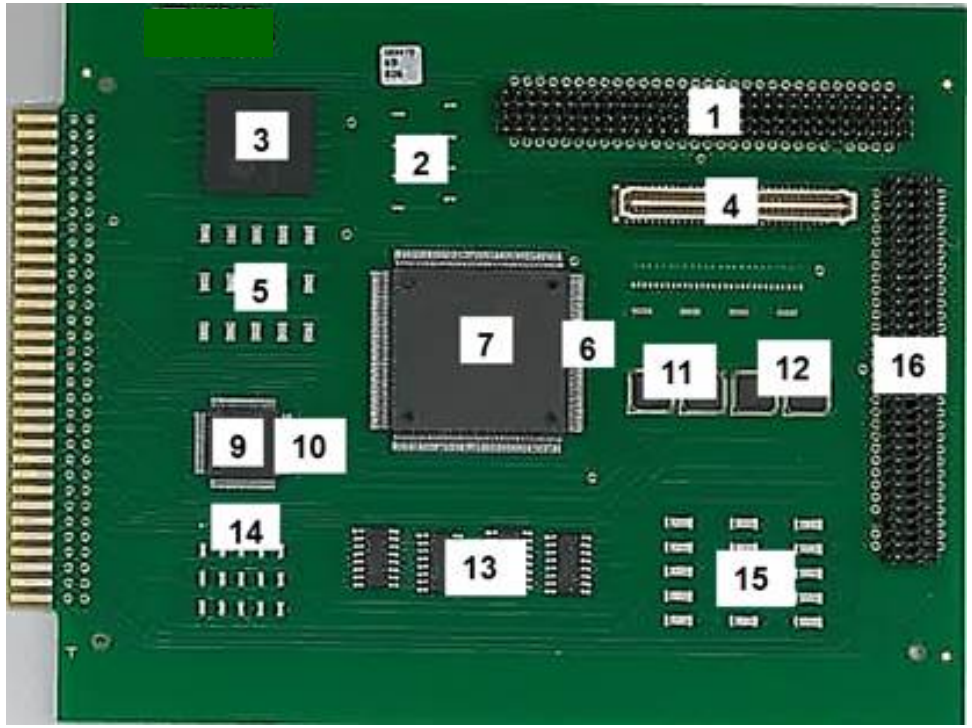


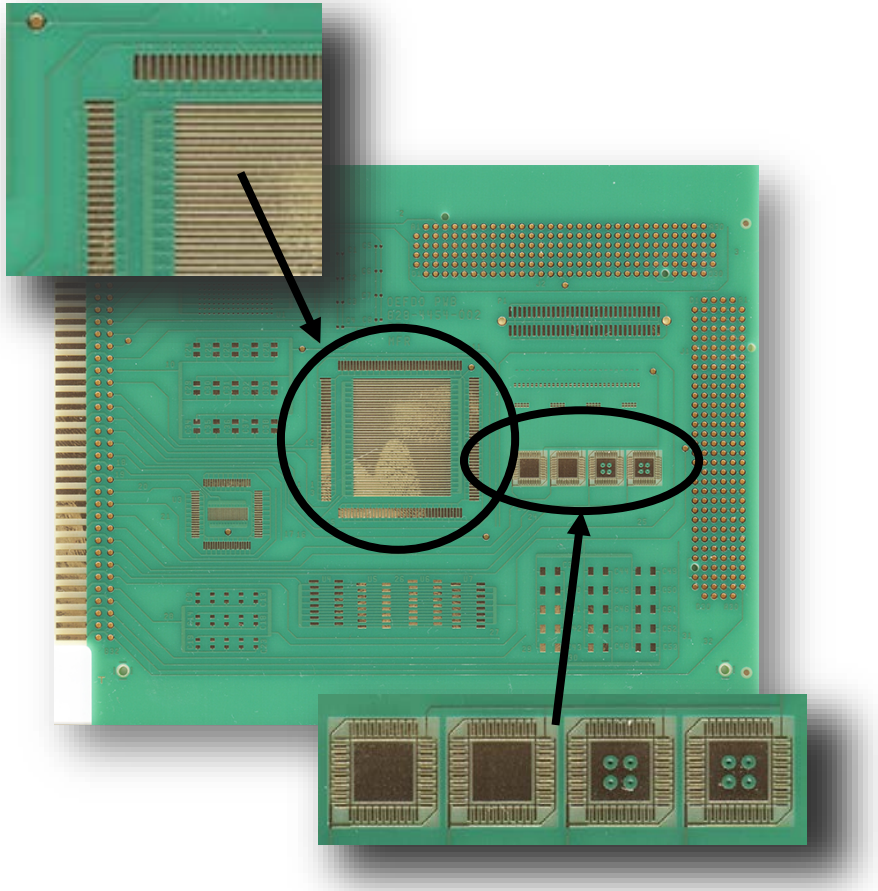


Surface electrochemistry phenomena



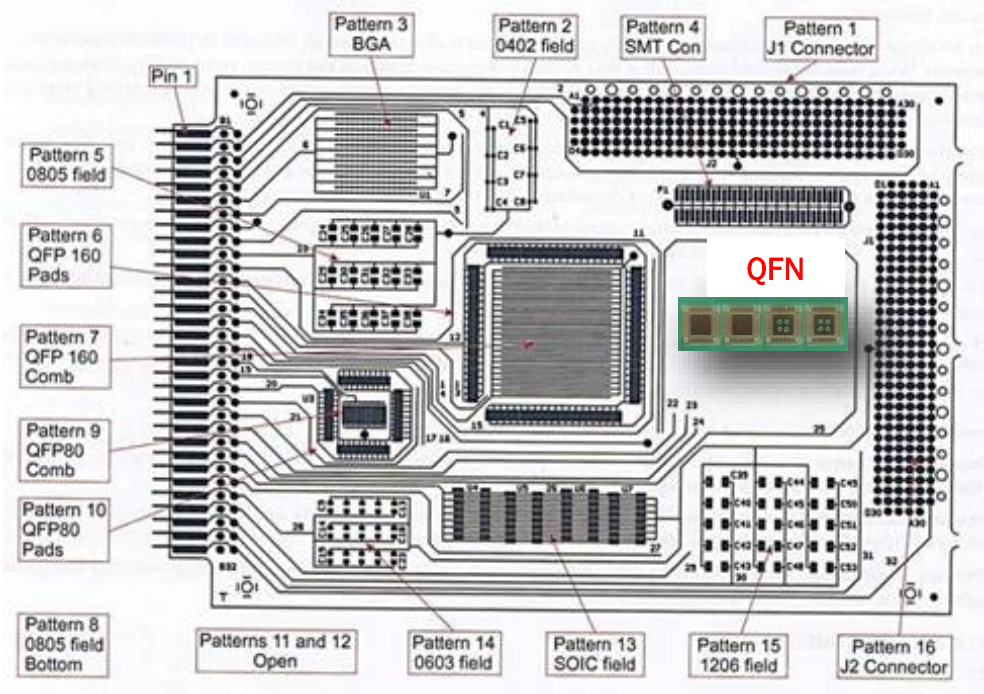
SIR Test Board with QFN Test Pattern





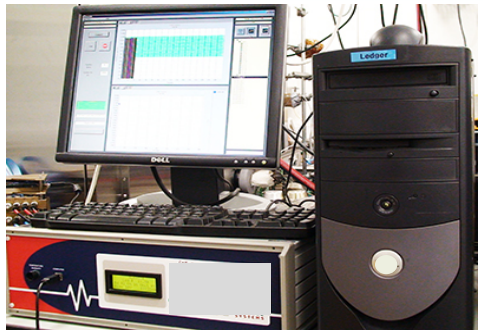
Modified IPC B52 with QFN

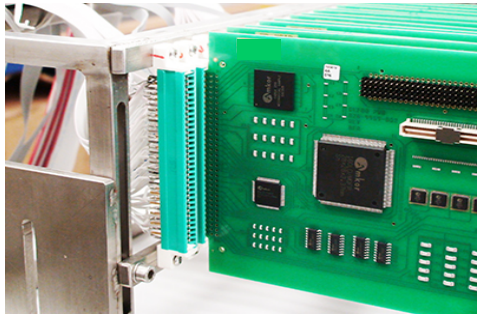
- Three different no-clean solder pastes from different manufacturers
- Jetted onto test vehicles with a nickel gold finish
- Surface mount (SM) components were auto-placed using production placement equipment and soldering was conducted by a production vapour phase soldering batch system using a fluid with a boiling temperature of 240°C (the peak temperature of reflow soldering for the lead-free pastes).
- The through-hole connectors were manually inserted prior to selective soldering using production equipment.



Surface Insulation Resistance Testing

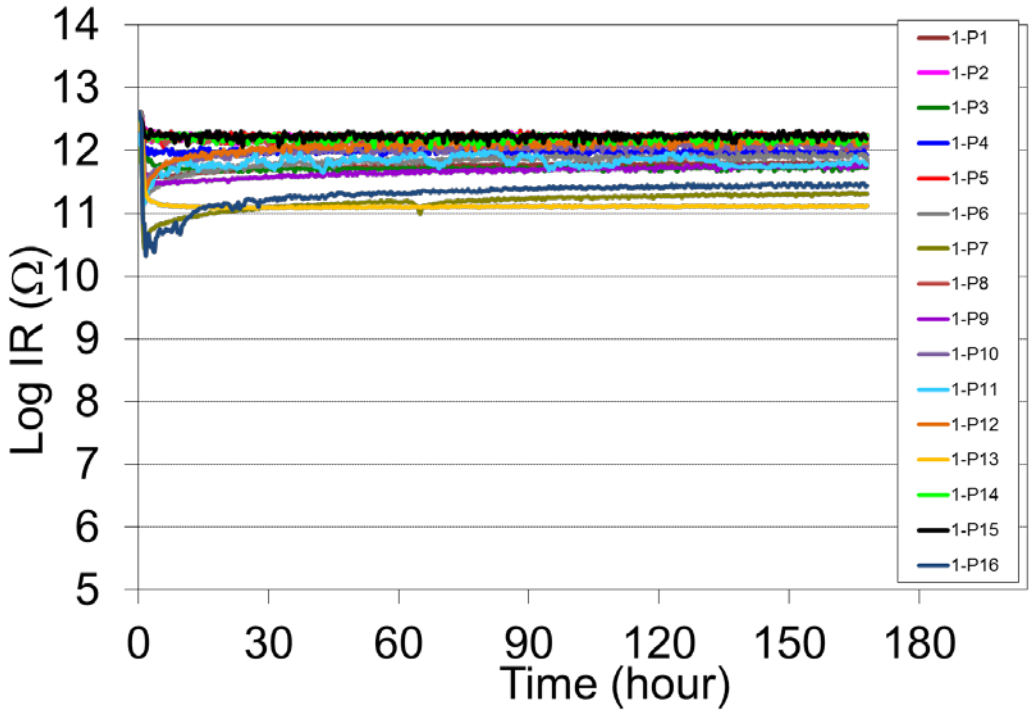
- Bareboard and assemblies tested at 40°C/93%RH and 50V for 168 hours
- SIR measurements were performed under constant temperature and humidity conditions of 40°C/93%RH.
- The first measurement for all test boards was taken under ambient conditions, then the temperature and humidity slowly increased to 40°C/40%RH over 20 minutes, and then to 40°C/93%RH over 20 minutes to avoid condensation where it was maintained for the remainder of the test.
- A bias voltage of 50 V DC was applied during the whole test period of 168 hours.
- The SIR was measured every 20 minutes.
- There was a 10^6 Ω resistor on each test channel to protect dendrite formation. The equipment used for the SIR measurements was a production SIR tester.



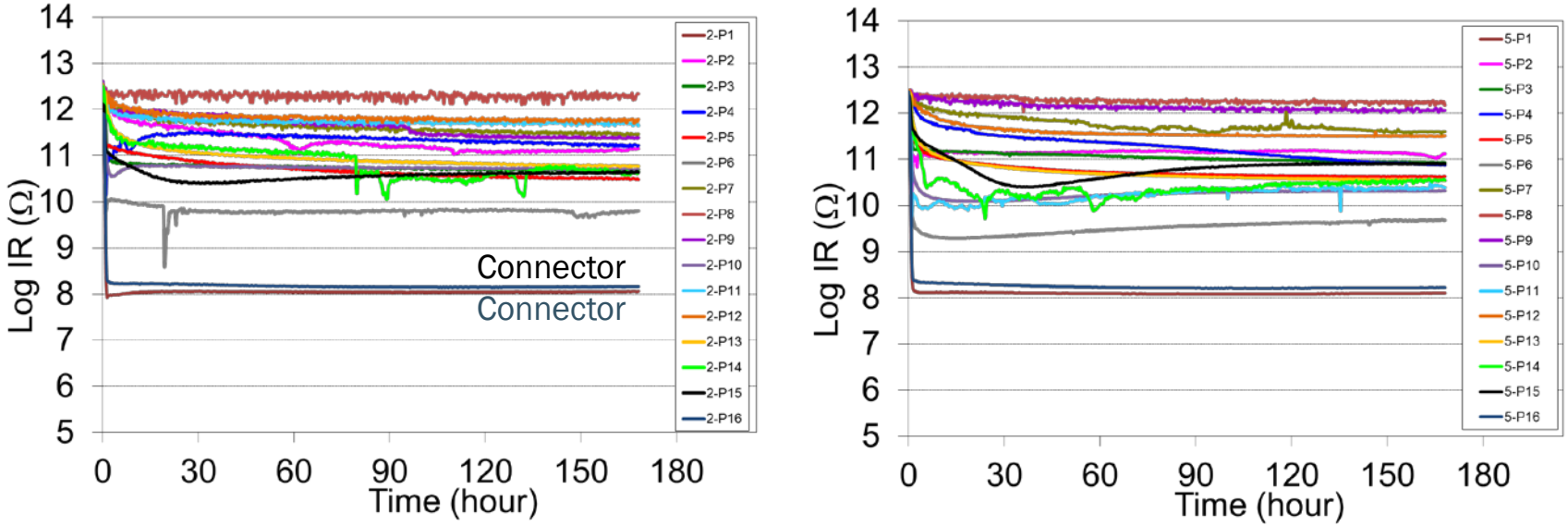


Bare PCB - 40°C/93%RH 50V

- The SIR does not fall below 10^{10} Ω showing that any failures in assembled test vehicles were not attributable to the substrates.

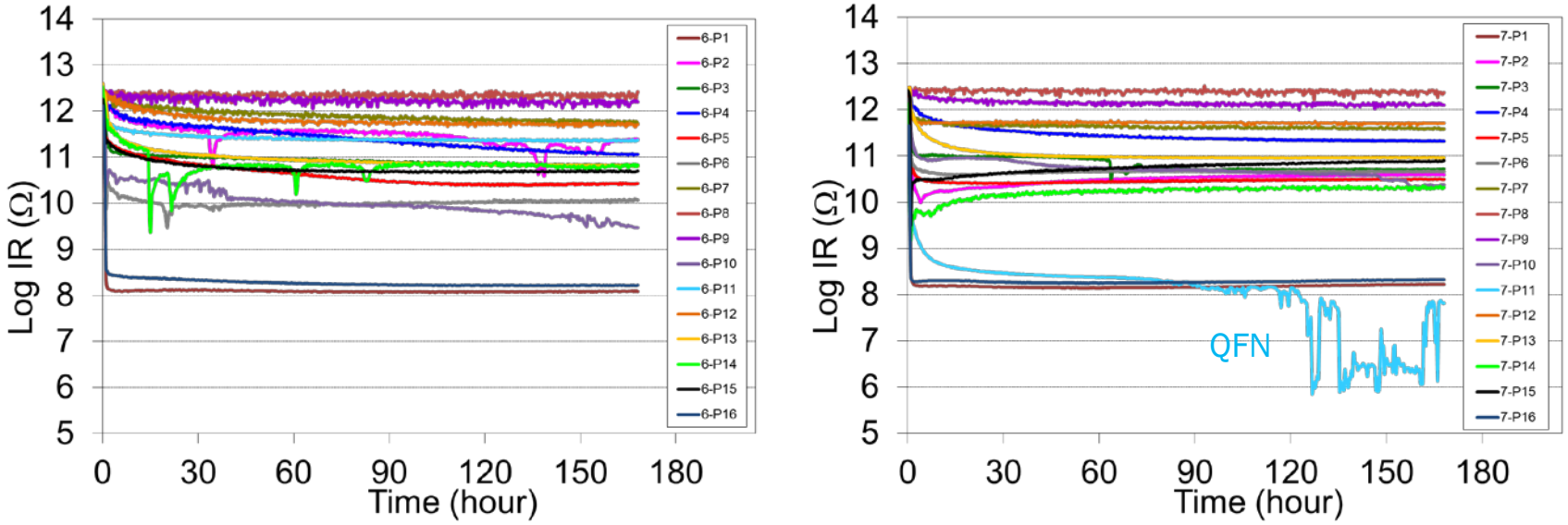


Paste A - 40°C/93%RH 50V



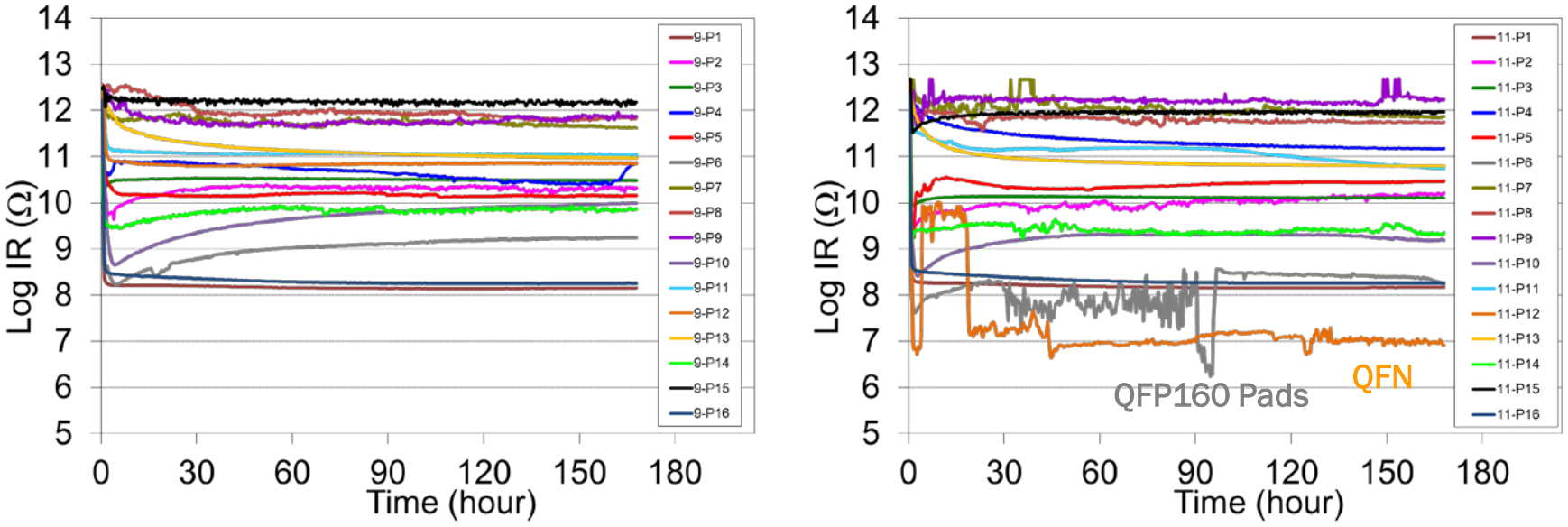
- In all cases the SIR of patterns 1 and 16 for the two connectors were low but constant at approximately 10^8 Ω. This was attributed to a surface finish applied to the connectors during manufacturing.
- For paste A, all components remained above 10^9 Ω and can be considered a pass.

Paste B - 40°C/93%RH 50V



- For paste B, the resistance of pattern 11 reduced to $10^6\ \Omega$ in the latter part of the test. This pattern is associated with the QFN components but this was the only pattern of eight repeats to fail.

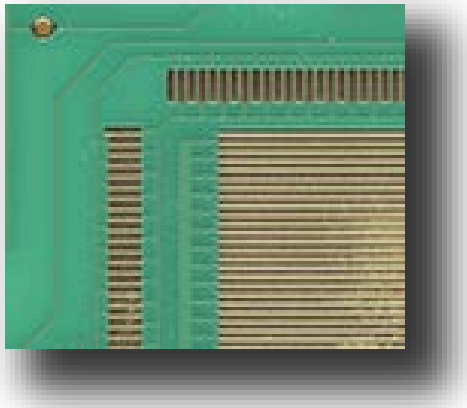
Paste C - 40°C/93%RH 50V

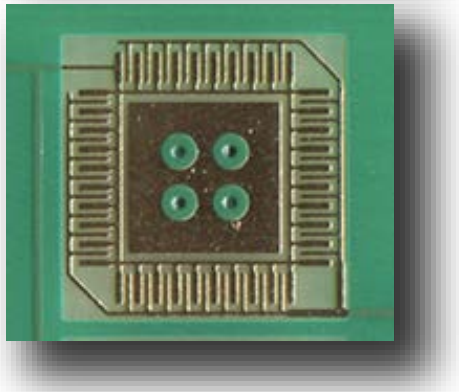


- A similar result was noted for paste C with pattern 13, also a QFN pattern, dropping to 10^7 Ω. This occurred on only one of six repeats. Additionally with this solder paste, the SIR for pattern 6 for the QFP160 also reduced during the test to approximately 10^6 Ω. This occurred on only one of three repeats.

QFP 160 & QFN

- Paste A showed no drop in SIR during the testing. Both pastes B and C showed some limited failures for QFN patterns. The SIR measurement test patterns for these components was very demanding, due to the small spacing on the pattern.
- In the QFN test pattern, one side of the pattern was formed by a track, uncovered by resist, placed between the QFN pads. This resulted in a gap between the ground and signal patterns of 75 μm.
- The spacing between conductors on the only other pattern to fail (QFP160 pads) was considerably greater at 250 μm. The field strength is inversely proportional to the gap, hence where the gap is smaller, it is likely to yield more failures for the same contamination levels.



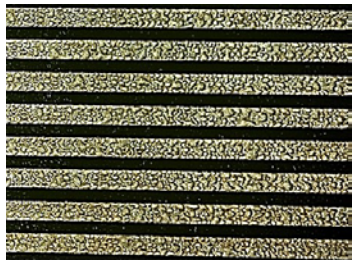


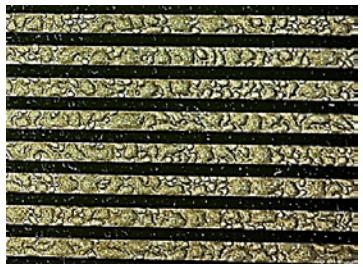
Condensation Testing

- Achieving high reliability in service is the key issue in today's high-density electronics circuit. Contaminants and bias with moisture facilitate electrochemical corrosion processes that result in a loss of continuity or short circuit.
- Electrochemical failure is very sensitive with moisture. When move from ~100 nm (85°C/85%RH) to visible liquid water layer (condensation), the metal corrosion on circuit board can be significantly accelerated. Failures can be happen in a few minutes. Condensation is very dangerous for circuit boards.
- Condensation only happened where there is rapid temperature and humidity change either for objects or for surrounding environment.

Condensation on circuit boards in real world

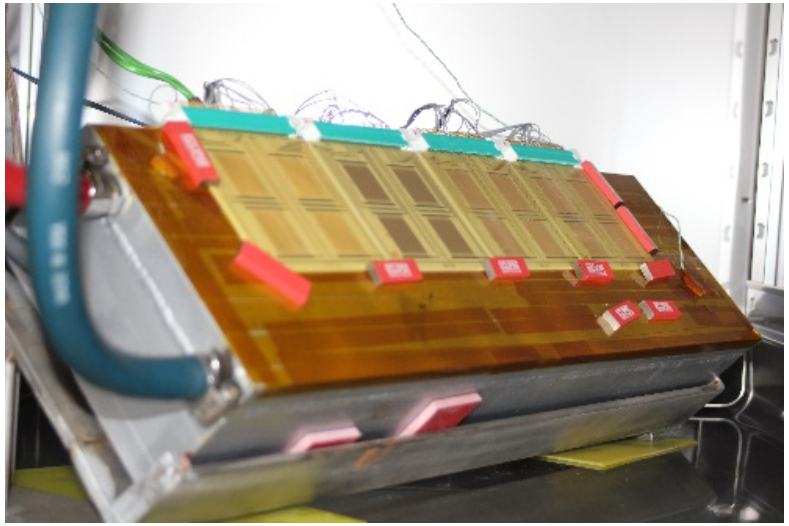
- When there is rapid temperature change for circuit board or ambient condition. Low temperature on board (below dew point) will cause condensation, eg aircraft descending from high altitude. These conditions can last for minutes, maybe half an hour.
- If the board sits in this environment long enough, board temperature will reach ambient temperature slowly, then condensation will evaporate and disappear.
- If temperature difference between board and ambient can be maintained, condensation will build up continually.
- Condensation is not an equilibrium and stable state, it is difficult to control and repeat.

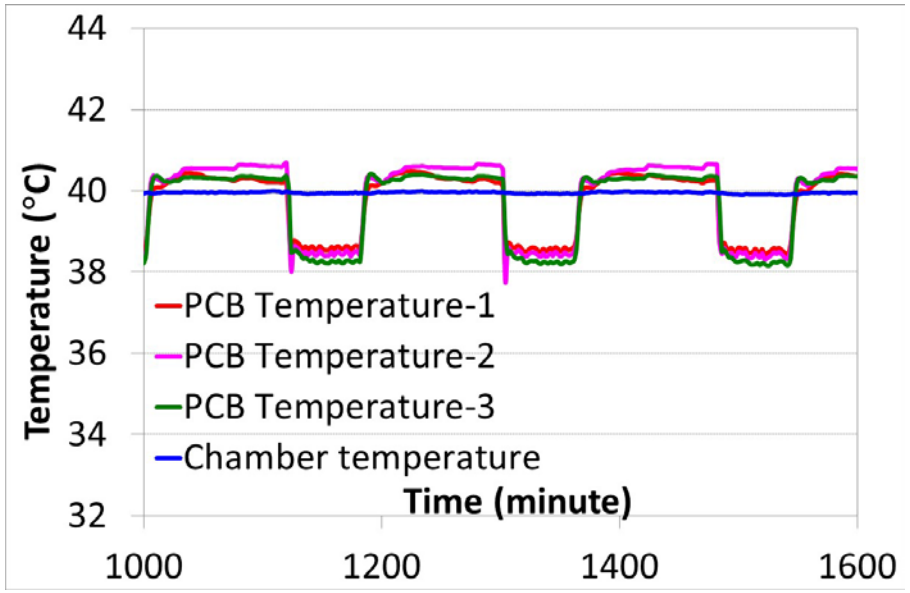




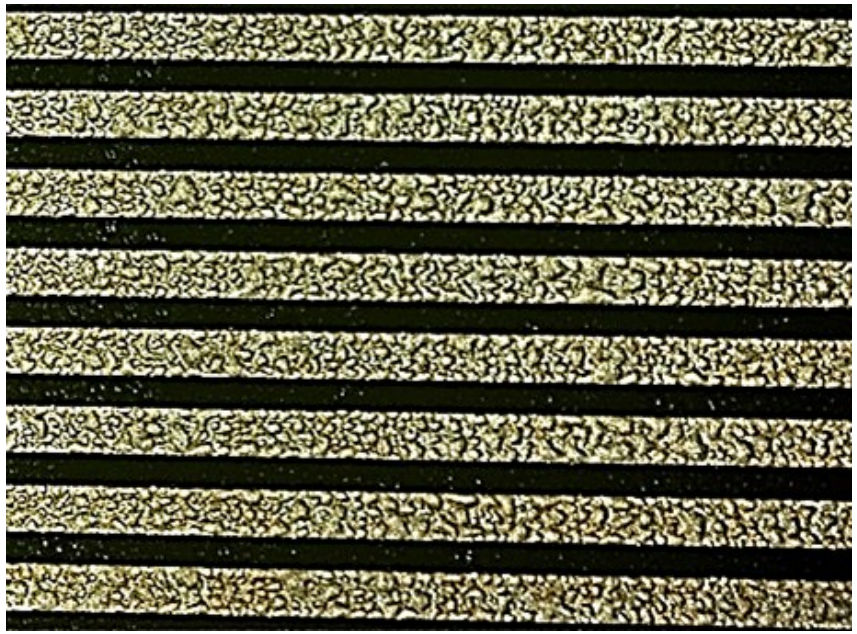
How it works: The condensation system

- The test boards are mounted on a platen.
- The platen temperature is independently controlled, and can be lowered to required temperature to control condensation level.

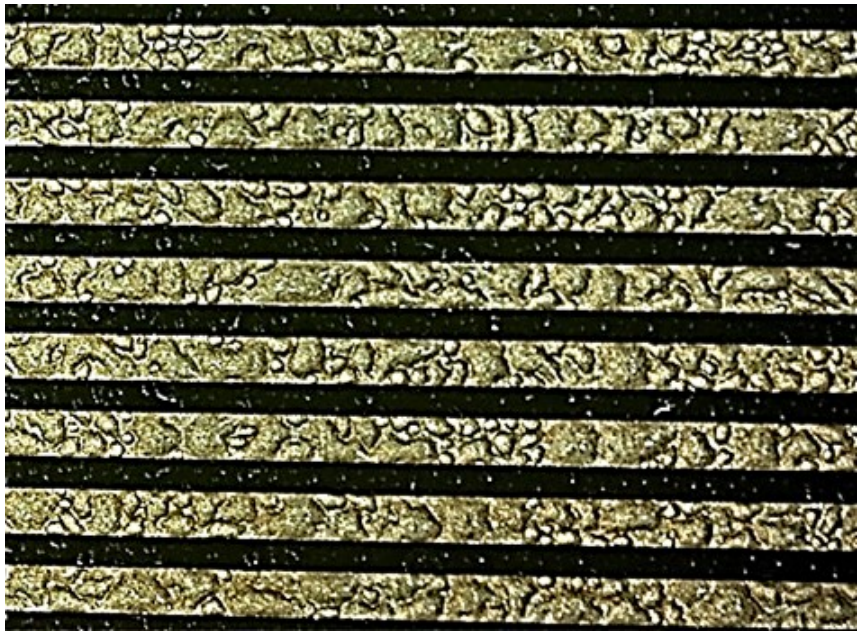




Condensation builds up in 60 minutes

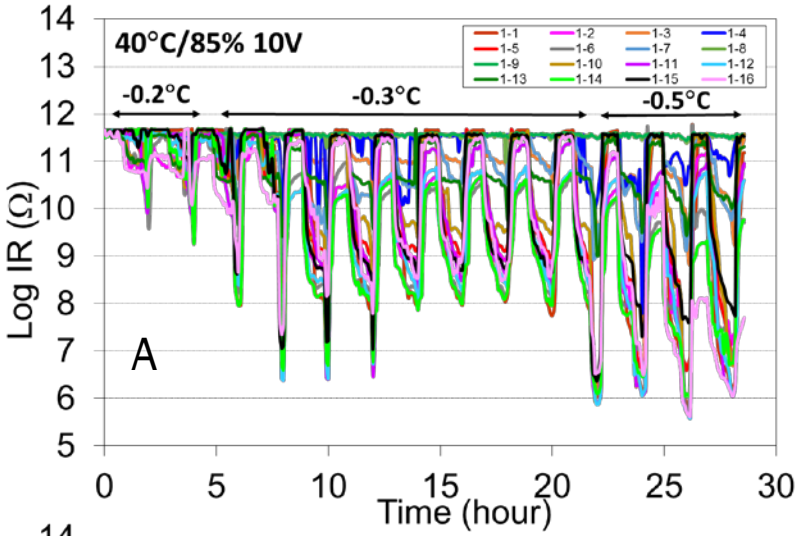


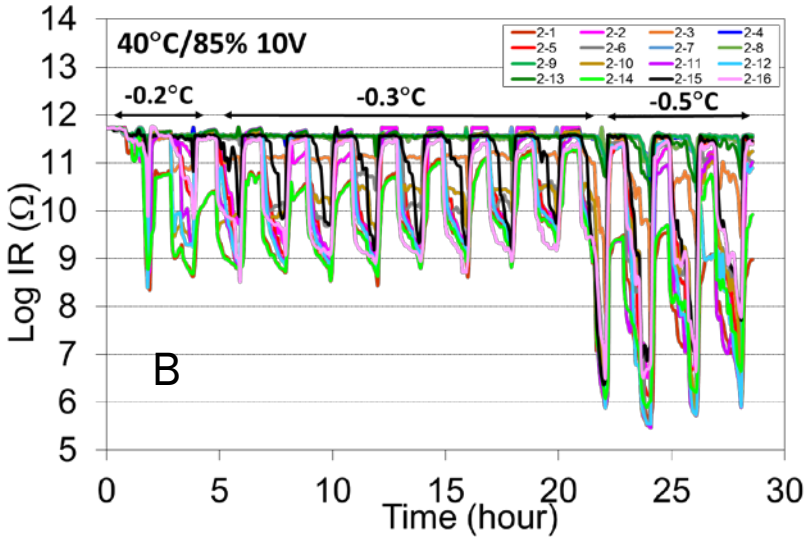
At 30 minute

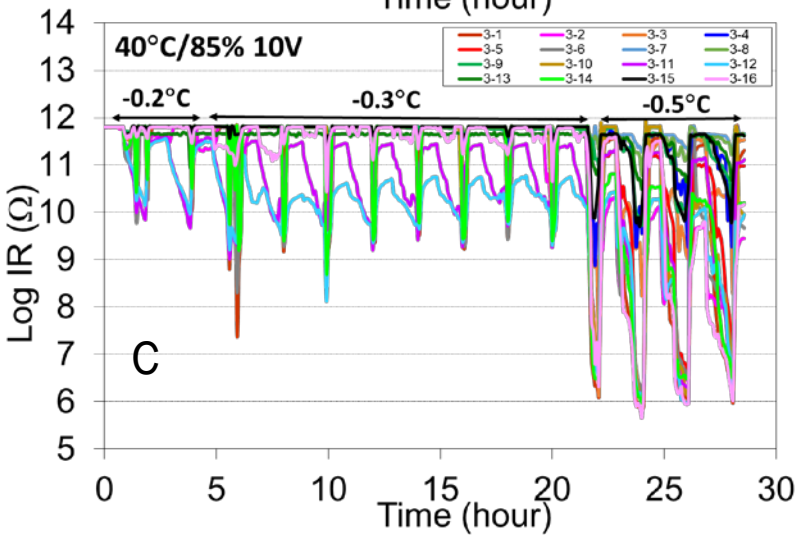


At 60 minute

Condensation Testing – 3 pastes

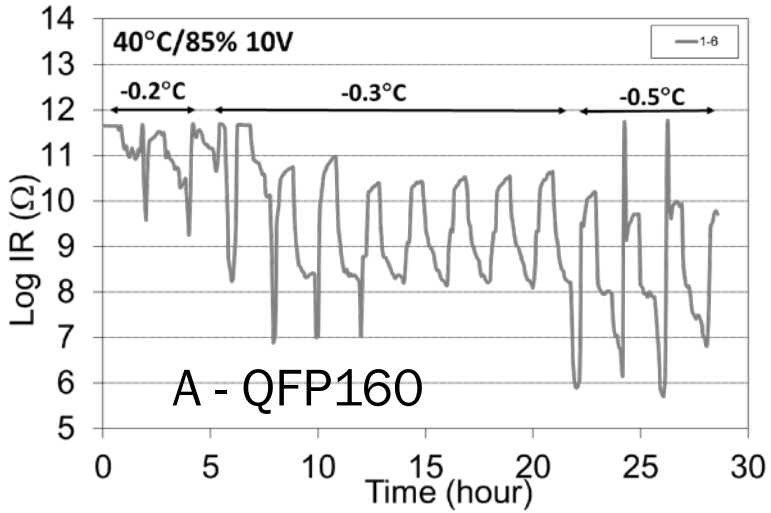


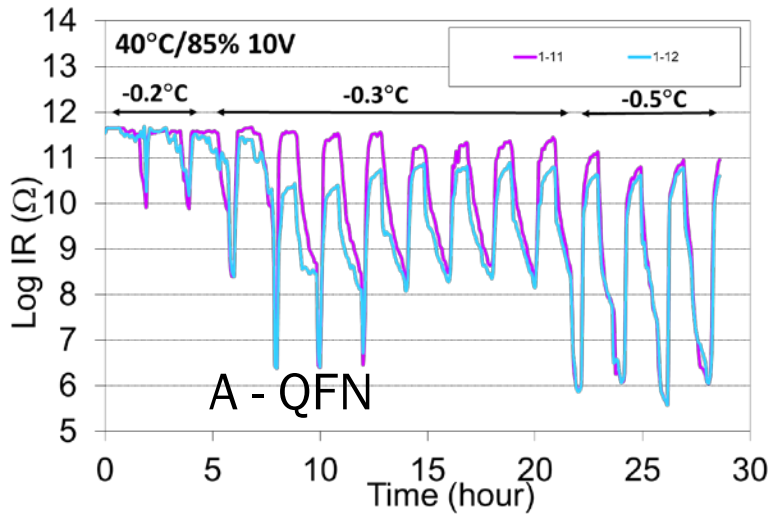




- Constant environment – 40°C, 85%RH with a 10V bias using same monitoring equipment as SIR testing
- Platten temperature set at -0.2, -0.3 & -0.5°C below dew point
- Platten cycled between these set points and above dew point every two hours (one hour dwells)

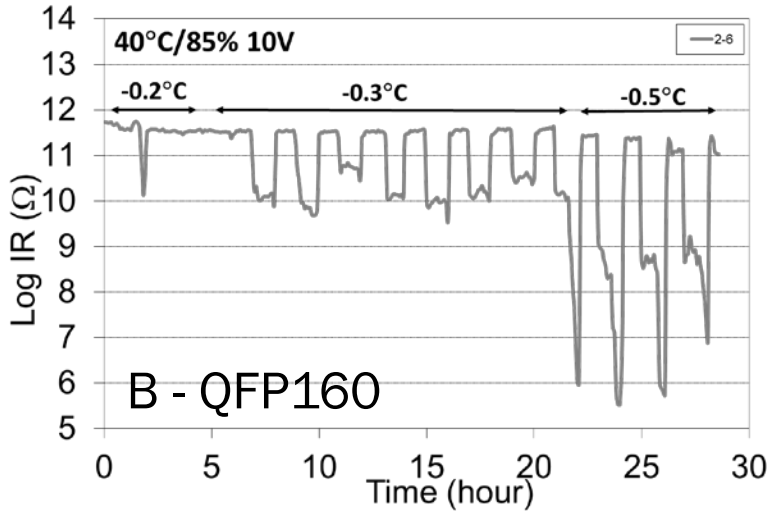
Condensation Testing – Paste A - QFP160 & QFN

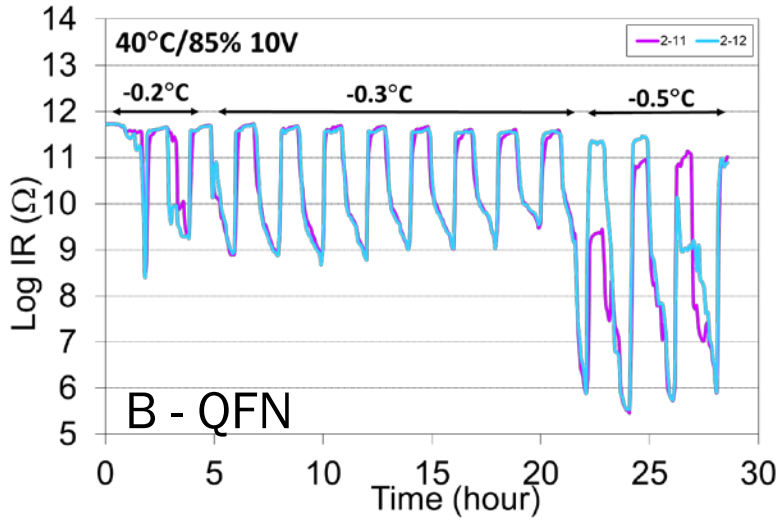




- For paste A, the SIR did not recover to its initial value when the platen temperature returned to ambient at the end of each condensation cycle and the SIR at this point in the cycle, could be seen to reduce in subsequent cycles.
- This effect begins to occur during cycles at -0.2 °C platen temperature for the QFN patterns and at -0.3 °C for the QFP pads pattern.

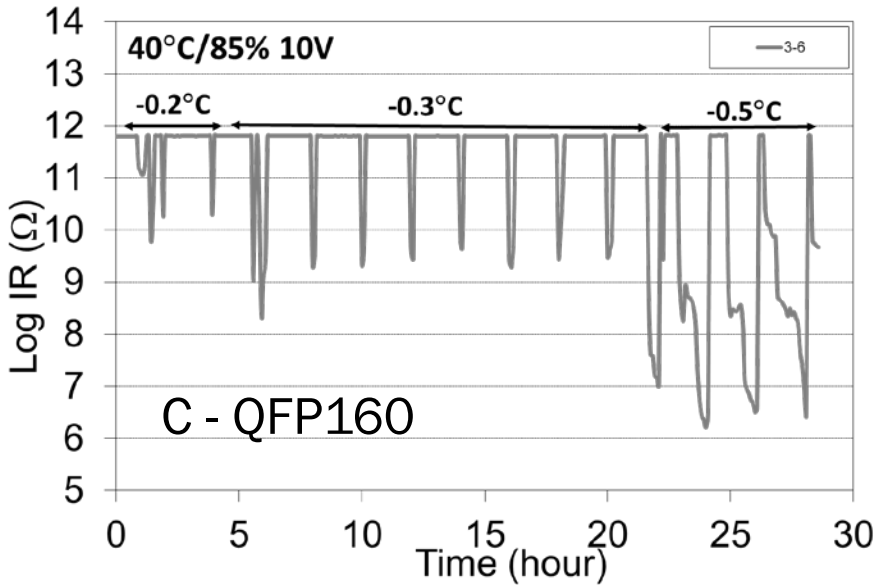
Condensation Testing – Paste B - QFP160 & QFN

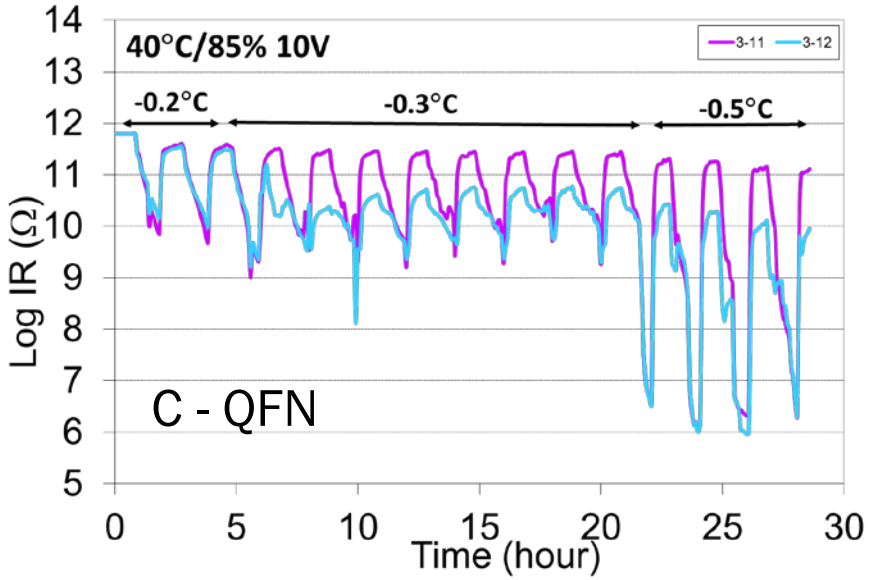




- For paste B, the SIR recovered to its initial value when the platen temperature returned to ambient at the end of each condensation cycle except for the QFN patterns at -0.5 ºC.
- The SIR could be seen to reduce during later cycles.

Condensation Testing – QFP160 & QFN





- With paste C, the responses were similar to that for Paste B but the degradation for the QFN patterns occurred earlier, starting during the cycling with the platen temperature at -0.3 °C below the dew point.

Condensation testing

- The condensation testing here has shown differences in responses for the different solder pastes tested.
- The failure to return to the initial SIR value in some patterns is an indication that damage is occurring during the condensation cycle which is not recoverable within the cycle time as the platen returns to ambient.
- This occurred in both the QFP160 pad and QFN patterns for Paste A and only in the QFN patterns for pastes B and C. Degradation in the QFN test pattern for paste C occurred earlier than for paste B. Whilst this data set is limited, there are indications that the responses from the solder pastes are different in condensing and non-condensing environments.
- During SIR measurement in the non-condensing environment, paste A offered a better performance than the other pastes, whilst this paste did not perform the best in the condensing environment. In the condensing environment, the responses from the components were also different with more degradation occurring with the QFN than for the QFP160.

Conclusions

- The performance has been evaluated using SIR measurements in both non-condensing and condensing environments. Solder pastes have been shown to perform differently in the differing conditions. The key result is that the paste which performed best in the non-condensing environment was not the best performer in condensing conditions.
- Under both conditions, the finer pitch components (QFP160 and QFN40) showed poorer performance than coarser pitch components.
- The SIR measurement test pattern for the QFN patterns used here was very challenging, due to the small spacing on the pattern. The field strength generated by the smaller gap is likely to lead to more failures for similar contamination and condensation levels. Further work should be undertaken in QFN test pattern design to determine their relative performance compared to other components.
- These results demonstrate the requirement for condensation testing to determine the performance of differing manufacturing options for electronics designed to be subjected to condensing environments. The technique developed has been shown to achieve specific condensing conditions but the desired test parameters to best evaluate process and design variables still need to be developed, and this will be the scope of further work.