Assembly Reliability of TSOP/DFN PoP Stack Package

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Abstract
Numerous 3D stack packaging technologies have been implemented by industry for use in microelectronics memory applications. This paper presents a reliability evaluation of a particular package-on-package (PoP) that offers a reduction in overall PCB board area requirements while allowing for increases in functionality. It utilizes standard, readily available device packaging methods in which high-density packaging is achieved by: (1) using standard "packaged" memory devices, (2) using standard 3-dimensional (3-D) interconnect assembly. The stacking approach provides a high level of functional integration in well-established and already functionally tested packages. The stack packages are built from TSOP packages with 48 leads, stacked either 2-high or 4-high, and integrated into a single dual-flat-no-lead (DFN) package.

To determine thermal cycle reliability, daisy-chain packages were soldered either using lead-free or tin-lead solder with added additional daisy-chain patterns on the PCB to enable resistance monitoring of the stack at thermal cycling intervals. The 3-D stacks were bonded to the board for improving resistance to mechanical loading such as drop and vibration. A number of 2-high and 4-high 3-D stack assemblies were subjected to thermal cycling in the range of -55°C to +125°C. The daisy-chain resistances were measured at RT and at 50 cycle intervals during thermal cycling. Test results to 500 thermal cycles are presented as well as images gathered from X-ray and optical microscopy to illustrate damage progression and to establish failure mechanisms. Furthermore, comparison was also made between 2D X-ray and X-ray tomography with optical microscopy to determine effectiveness of these non-destructive evaluation techniques. The paper concludes with a summary and recommendations for the next step of investigation.

Key words: PoP, package-on-package, solder joint reliability, thermal cycle, X-ray

1.0 STACK PACKAGING TECHNOLOGIES

1.1 Introduction

The demand for high-frequency operation, high-input/output (I/O) density, and low parasitics, as well as the need for package-level integration with small form factors and extreme miniaturization, have led to numerous 2.5D and 3D packaging technologies [1-4]. The vertically integrated 3D packages combine conventional flip-chip and wire-bond interconnection, build-up, and laminate substrates, and bring about package-level integration of disparate die and device functions through die or package stacking.

From the existing 3D packaging technology options, wire-bonding is well developed for use in low-density connections of less than 200 I/Os per chip. This technology has limitations in meeting the increasing frequency requirements and increasing demands for higher interconnection due to the limitation of peripheral wire-bonding. In order to overcome such wiring connectivity issues, multiple flip-chip die with passive redistribution interposed have been introduced by industry for high-end applications. Ultimately the 3D chip stacking technology using through-silicon vias (TSVs) is being pursued by industry since it offers the possibility of solving serious interconnection problems, while offering integrated functions for higher performance.

For high-density packaging, the migration to conventional interconnection 3D, more than "Moore", has become mainstream. Even though initially conventional 3D packaging included leaded stack configuration, the trend is moving towards area array interconnections. The conventional 3D packaging (see Fig. 1) consists of stacking of packaged devices, known as package-on-package (PoP), and stacking of die within a package, known as package-in-package (PiP) or system-in-package (SiP).

Numerous variations of PoP and PiP technologies are in use today including staking of packages by using through mold via interconnection technology.

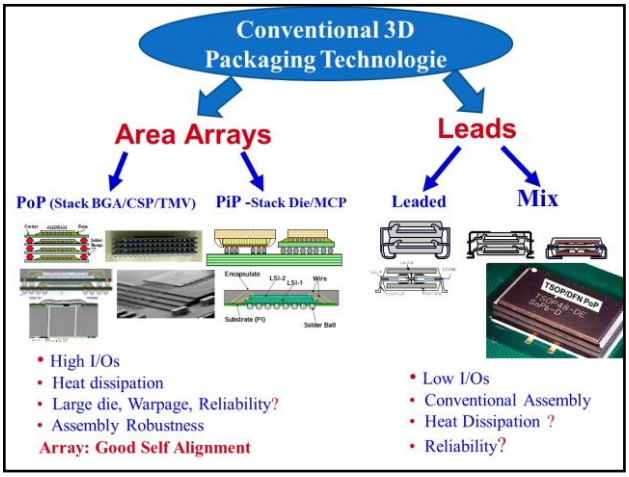

Fig. 1. Conventional 3D packaging technologies including the image of TSOP/DFN PoP 3D stack (bottom right) used for assembly reliability evaluation.

1.2 Package-on-Package (PoP)

PoP is a packaging technology placing one package on top of another to integrate different functionalities while still remaining compact in size. This packaging technology offers procurement flexibility, lower cost of ownership, better total system costs, and faster time to market. Normally, designers use the top package for memory application and the bottom package for application-specific integrated circuits (ASICs), baseband, or processor applications. By using this packaging technology, the issue of known-good-die (KGD) for a-memory die can be mitigated since the die can be burned-in for the bottom package first before the stacking of the PoP.

PoP also answers issues with wafer thinning, die attach, wire bond, and thermal dissipation. Three categories of the stack technologies are: (1) PoP with center mold and flip chip, (2) PoP with partial cavity structure, and (3) through-mold via (TMV).

1.3 Package-in-Package (PiP)

Handsets and other mobile handheld products are defining a new application for packaging technology that goes beyond the realm of traditional packaging. The optimum solution often lies in a judicious combination or hybridization of these seemingly dissimilar technologies and approaches. One such package is often called PiP. A PiP with a wire-bonded stack die is well established. Vertical chip stacking can be performed as chip-to-chip, chip-to-wafer, or wafer-to-wafer processes. Stacked die products inside a package result in the thinnest package with the highest board-level reliability and lowest assembly cost. Most of the time, stacked die are multiple memory chips and rarely mixed device types, such as stacked memory with added logic devices. Special low-profile wire bonding has been developed and is a critical process for this technology.

Stacked die concepts utilizing silicon spacers or epoxy filled with spherical spacers have been used. In the silicon-spacer concept, a thin piece of silicon is used to separate the active dies in the stack. In the glue-spacer concept, this is accomplished with a spherical-filled die-attach. Adding silicon into the package increases the bending resistance. Associated with this is the increased risk and/or propensity for cracks during assembly and/or reliability and qualification testing, either in the package body (molding compound) or in the die itself.

1.4 Conventional Reliability Methods

Figure 2 schematically illustrates the key elements of electronic packaging assemblies under thermal stresses: global and local both stack layering and solder joint to lead, or no-lead mismatches. Reliability under thermal stress for package (3D stack as a unit), PCB, and assembly depends on the reliability of constituent elements, e.g., the PCB and its global/local interfaces (attachments). Three elements play key roles in defining reliability for a system, global, local, and interconnections. The characteristics of these three elements — package (e.g., die, substrate, solder joint, underfill, and 3D stack layers, and adhesive underfill), PCB (e.g., polymer, copper (Cu), plated through hole, via, and microvia), solder joints (e.g., tin-lead solder joints, lead-free solder joints, balls in BGA as solder and solder attachments, solder column with solder attachments, and plated-through-hole via)— together with the use conditions, the design life, and the acceptance failure probability for the electronic assembly, determine the subsystem reliability.

In other words, reliability is the ability of a system (here microelectronics) to function as expected under the expected operating conditions for an expected time period without exceeding the expected failure levels. However, reliability is susceptible to early failure by infant mortality due to workmanship defects, lack of sound manufacturing, and use of a design without reliability consideration. Design for manufacturability (DfM), design for assembly (DfA), design for testability (DfT), and so on, are prerequisites to assure the reliability of the product. Only design for reliability (DfR) can assure that a manufactured product with an acceptable quality will also be reliable in the product application.

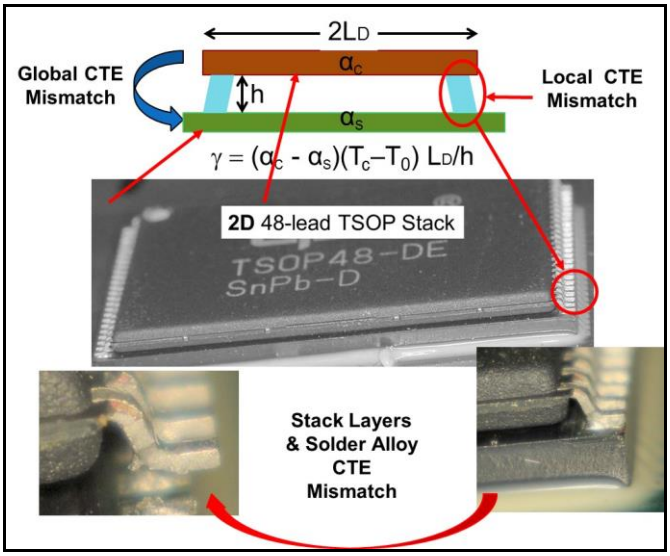

Fig. 2. Key elements of reliability failure mechanisms under thermo-mechanical loading condition. Under thermal stress, three key elements that define reliability are due to global, local, and solder alloy microstructural coefficient of thermal expansion (CTE) mismatches.

This paper documents a reliability evaluation of a particular implementation of package-on-package (PoP) high-density electronic packaging technology. The PoP is just one of the several new high density packaging technologies that offer significant reductions in overall required PCB board area while allowing for significant and often unique increases in device performance and functionality. The particular PoP technology tested for this report was provided by a supplier [5] that utilizes standard, readily available device packaging methods in which high-density packaging is achieved through a combination of several technologies:

- Standard packaged memory devices
- 3-dimensional (3D) interconnect assembly

2.0 APPROACHES

2.1 Test veicle build

The PoP packaging technology consists of 48-lead TSOPs solder stacked (both 2-high and 4-high) and integrated into single dual-flat no-lead (DFN) packages (see Fig. 3)

1) Conventional dummy packages were used in a daisy chain configuration for interconnect testing
2). Lead-free solder was used in the stacking assembly process and 63Sn37Pb solder was used to mount the bottom TSOP package to the test board.

An underfill material was applied after mounting to the board. This particular underfill exhibits high Tg and high-fracture toughness and is engineered to withstand the 260°C peak reflow temperature associated with lead-free soldering. All material selections and assembly were performed by the industry partner.

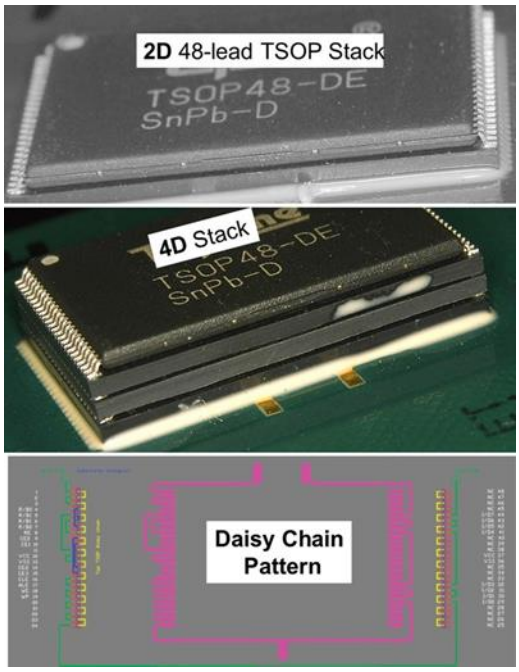

Fig. 3. Representative image of the 2-high (top) and 4-high (middle) TSOP/DFN unique stack packaging technology evaluated for assembly reliability using package daisy chain with complementary PCB pattern (bottom).

2.2 Thermal Cycle Condition

Thermal shock (TS) cycle testing was conducted in accordance with MIL-STD-883, Method 1010, Test Condition B. The TS ranges is within the IPC9701 standard specification, TC4, except for the ramp/cooling rates that exceeded the 20°C per minute defined for thermal cycle condition. This TS cycle range should provide a rapid characterization of this technology since the reliability of this technology was unknown even though it appears to be a robust PoP technology. See Figure 4 for typical profile. Series resistance was monitored at intervals to 500 cycles and recorded.

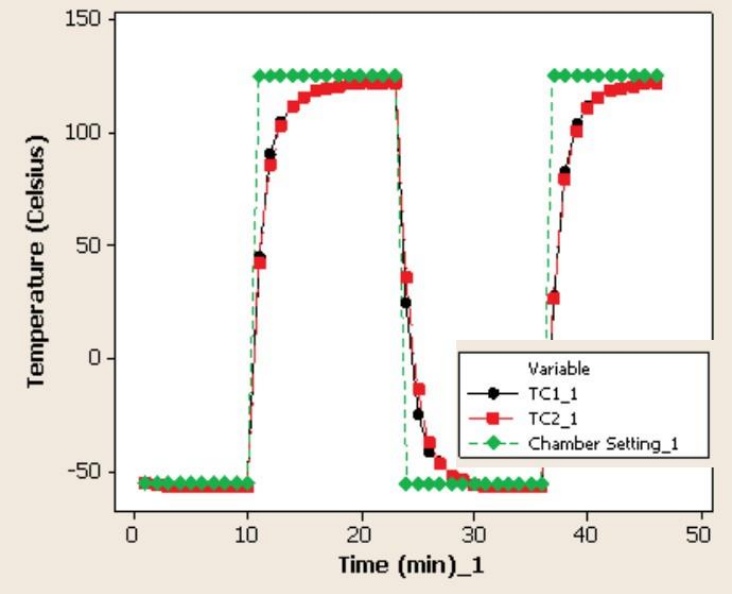

Fig. 4. A representative thermal cycle profile (–55°C to +125°C) used for solder joint reliability evaluation of 2- and 4-high stack TSOP/DFN assemblies. Note temperature lags for the board compared to chamber setting.

2.3 Thermal Cycle Results

The daisy chain series resistance is shown in Table 1 for the 2-high stack assemblies and in Table 2 for the 4-high stack assemblies. The yellow color marks a resistance increase by 20% per IPC 9701 standard and higher up to complete opens with more than 1000 Ohms. Complete failure is shown with red color.

Table 1. Daisy-chain resistance variation of ten 2-high stack assemblies with thermal cycles checked at room temperature at 50 cycle intervals, Yellow show 20% increase in resistance whereas red shows complete opens (>1000 Ohms).

SN	R0 cyc	50	100	150	200	250	300	350	400	450	500
1	1.6	1.6	1.6	6.0	1.6	1.6	1.6	1.6	1.6	1.6	1.6
2	1.5	1.5	1.5	1.5	1.5	1.6	1.6	1.7	1.9	2.1	0.0
3	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
4	1.5	1.5	1.5	1.5	1.6	1.7	2.5	3.6	9.5	7.7	11.5
5	1.5	1.5	1.5	1.5	1.5	1.6	1.6	1.6	1.7	1.7	1.8
6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.7
7	1.5	1.5	1.5	1.5	1.5	1.6	1.8	0.0	0.0	0.0	0.0
8	1.6	1.6	1.6	1.6	1.7	1.8	1.9	2.0	2.1	2.1	2.2
9	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
10	1.5	1.6	1.5	1.6	1.6	1.6	1.6	1.6	1.7	1.9	2.6
Visual inspection: **SN1,** Failed TSOP solder failure											
		SN7, Whole row on one side failed									
	Failure, 20% increase in resistance										
	Failure, Complete open >1000 Ohms										

The change in electrical resistance with the increasing number of temperature cycles is an indication of an imminent interconnection failure. An electrical resistance of greater than or equal to 1000 ohms (Ω) is considered an electrical open— a clear failure and shown by red color. The 2-high stack package exhibited stability (less than 20% changes in resistance at RT) within 250 cycles of testing, whereas the 4-high stack package became unstable within the first 50 thermal cycles. The number of cycles to failure were lower for the 4-high stack package assemblies.

Plots of cumulative percentage failures versus the number of thermal cycles show that the 4-high stack has an increased failure rate over the 2-high stack by a factor of 1.43, which is the ratio of the two slopes using a linear fit.

Table 2. Daisy-chain resistance variation of ten 4-high stack assemblies with thermal cycles checked at room temperature at 50 cycle intervals. Yellow show a 20% increase in resistance whereas red shows complete opens (>1000 Ohms)..

SN	R0 cyc	50	100	150	200	250	300	350	400	450	500
11	1.9	2.2	2.0	2.4	3.3	0.0	0.0	0.0	0.0	0.0	0.0
12	1.9	2.1	2.1	2.2	2.4	2.5	3.1	10.2	9.7	6.5	6.9
13	2.0	2.4	3.1	3.6	4.2	5.9	6.2	7.7	11.1	12.8	18.9
14	2.0	2.0	2.0	2.1	2.2	2.2	2.8	2.7	3.2	12.4	0.0
15	1.8	2.1	2.1	2.2	2.5	2.7	2.9	0.0	0.0	0.0	0.0
16	1.9	2.1	2.2	2.5	4.2	8.3	6.0	5.6	11.8	11.5	14.7
17	1.9	2.3	2.4	2.9	3.1	3.5	4.2	4.4	5.5	11.7	0.0
18	1.8	2.4	2.5	3.2	4.3	4.7	5.3	5.6	6.4	6.9	8.1
19	1.9	2.1	2.1	2.3	2.8	13.0	12.2	7.1	21.1	0.0	0.0
20	1.9	2.2	2.3	2.5	2.6	2.8	3.1	3.4	3.9	4.1	4.4

Visual inspection: **SN11,** Middle TSOP solderjoint failure
SN13, possibly lower package failure
SN19, Top package OK, possibly lower package failure

Failure, 20% increase in resistance

Failure, Complete open >1000 Ohms

The 3D assemblies, both 2-high and 4-high, were subject to visual inspection and X-ray characterization. The bottom package solder joint was mostly covered with adhesive and therefore it was difficult to inspect for joint failures. The rest of the joints with either TSOP lead or no-lead solder interconnections were exposed and therefore could be clearly inspected for their damage level or failure.

2.4 Visual inspection and X-ray

Visual inspection of peripheral TSOP leads and DFN (no-leads) were performed after 500 thermal cycles (–55°C and +125°C) to determine potential failure sites. The solder joints of the bottom TSOP leads were mostly covered by adhesive; therefore, it was not possible to determine the damage condition of solder joints. For the 2-high stack package, this means that only 50% of solder conditions could be visually characterized. Even with this limitation, a correlation between visual inspection and failure was apparent. SN01 showed individual solder joint failures, whereas, the SN04 showed complete failure of a row of solder joints. Figure 5 shows representative photomicrographs of a number of 2-high stack test vehicles. For the 4-high stack similar to the 2-high stack, the bottom TSOP could not be visually inspected for solder joint conditions. However, the test vehicles show more pronounced failures, as also shown by optical photomicrographs in Fig. 6. When, in some cases clear failures were not apparent and should have failed based on daisy-chain opens, the failure contributed to the bottom package solder joints which were covered with adhesive and were difficult to inspect.

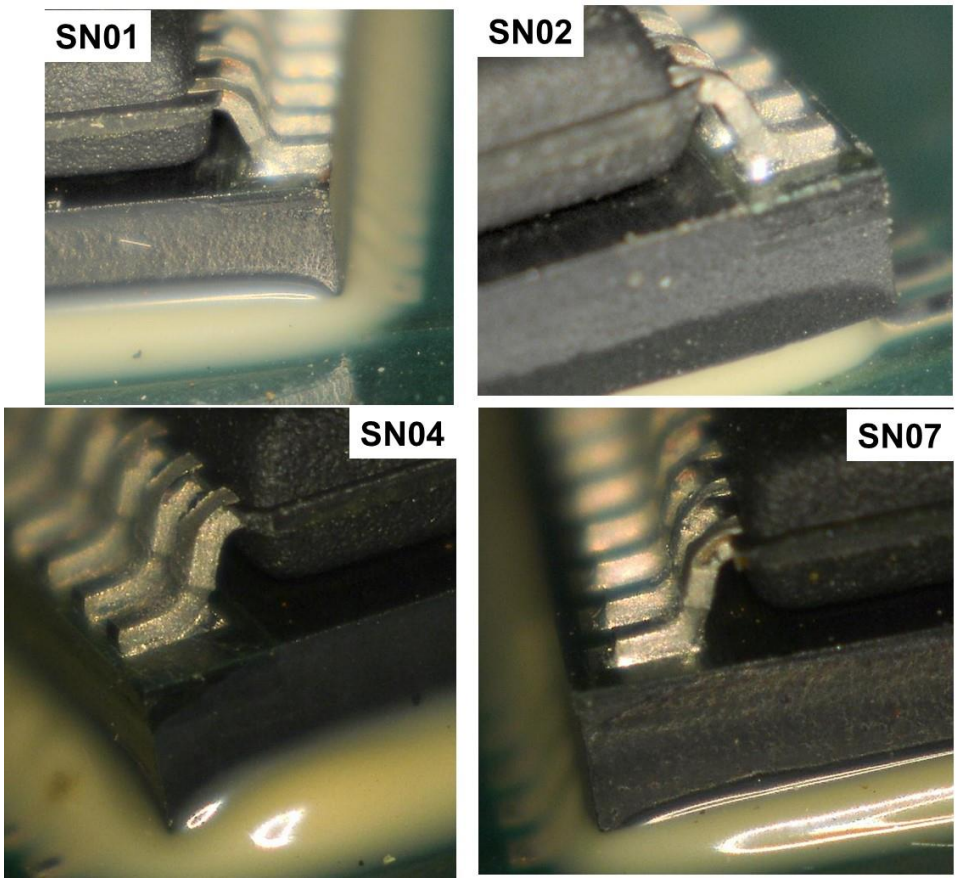

Fig. 5. Representative image of the 2-high (top) TSOP/DFN stack solder joint assemblies after 500 thermal cycles (–55°C to +125°C) showing signs of solder damage and failures.

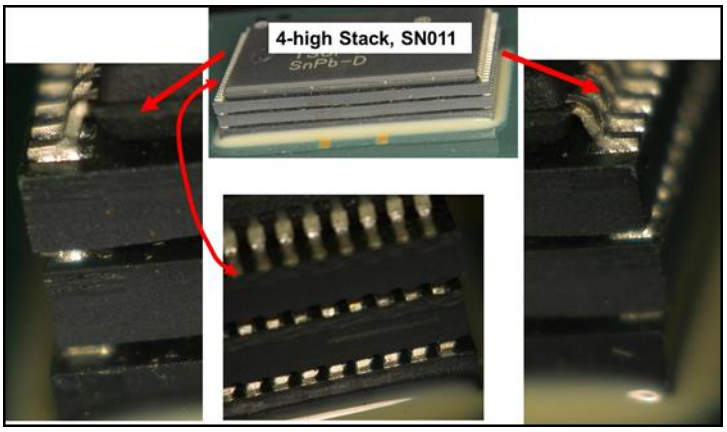

Fig. 6. Representative images of the 4-high (top) TSOP/DFN stack solder joint assemblies after 500 thermal cycles (–55°C to +125°C) showing signs of solder damage and failure.

X-ray evaluation was needed, especially for the bottom package. Both 2D and 3D X-ray were performed to determine the integrity of the bottom package, as well as if the pronounced separation that was detected by visual inspection could also be determined by the X-ray inspection. Figure 7 shows two X-ray photomicrograph images for the 2-high stack, clearly revealing the TSOP leads for the top and the bottom packages. The leads for bottom could not be visually inspected. Figure 8 shows the 3D X-ray images for a 4-high stack configuration. Even though X-ray clearly characterize the shift in the leads due to solder failures, it could not reveal the no-lead solder joint separation observable by visual inspection.

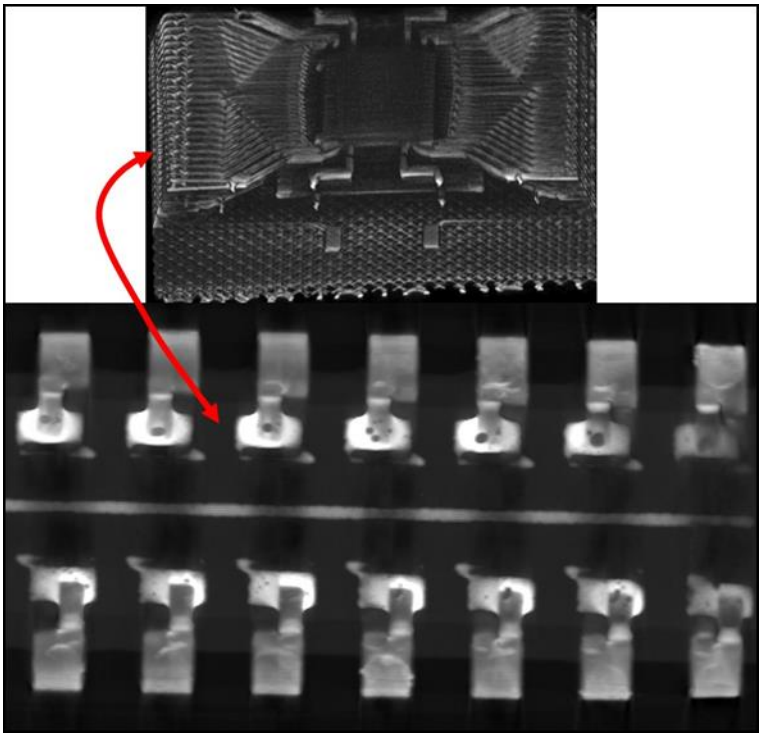

Fig. 7. Representative 2D/3D X-ray images of the 2-high TSOP/DFN showing the overall stack configuration (top) and specific image for the front showing the TSOP leads even for those covered with adhesive bonding material.

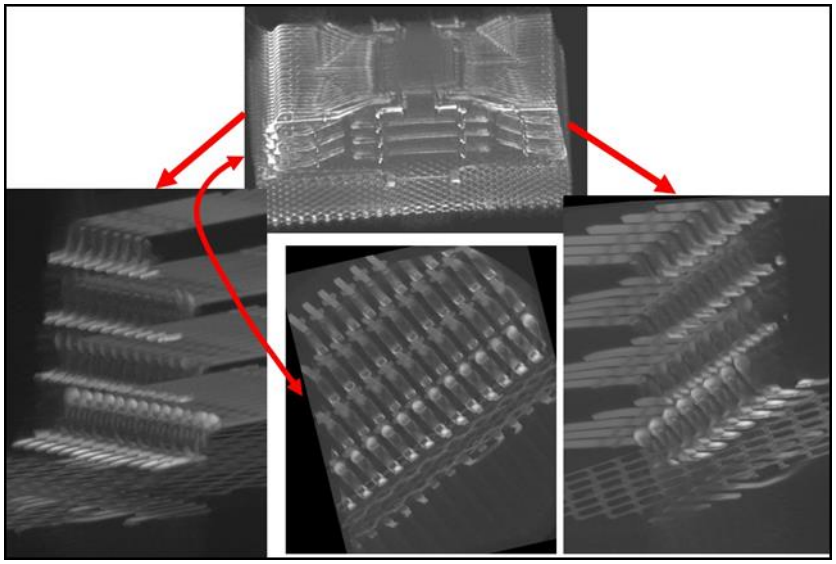

Fig. 8. Representative 2D/3D X-ray images of the 4-high TSOP/DFN showing the overall stack configuration (top) and specific image for the front showing the TSOP leads and DFN solder connections.

3.0 NEXT STEPS: FLEXIBLE TSOP 3D STACK

Subsequently, another TSOP 3D stack technology was evaluated for assembly reliability. This 3D package uses memory TSOP, but adds flexible L-shape leads after stacking for assembly onto the PCB to meet high-reliability application requirements. Figure 9 schematically shows [6] the basic flow for the stacking process. It also includes an image of the assembled 3D stack package ready for thermal cycling, the next phase of this program.

The packaging build process starts with TSOP or bare die using five key steps:

- Stacking and molding with low-outgassing epoxy
- Cutting with a dicing machine
- Plating with Ni/Au
- Patterning etching
- Final electrical test

Contrary to those of the 3D stack TSOP, this approach does not use any solder for stacking, but instead uses Ni/Au as an outer layer for electrical routing. This removes solder, the single largest reliability and quality concern of stacking. However, the outer coating layer adds some restriction on corner staking/bonding due to the risk of peeling. Conductive foreign object debris (FOD) could cause shortening of the coated circuitry and also because of the layup configuration, the part is moisture sensitive and induces restrictions on the reflow parameters. All of these restrictions require careful process development and implementation. After a stack of TSOP molding, a sawing process cuts into the stack allowing for the final cube to be even slightly smaller than the original monolithic TSOP package. Even though the stack mainly uses TSOP for high-density memory application, it can use other packages including SOT, flat pack, and larger pin count PQFP. This approach is particularly useful when the bare die solution is difficult and expensive to implement.

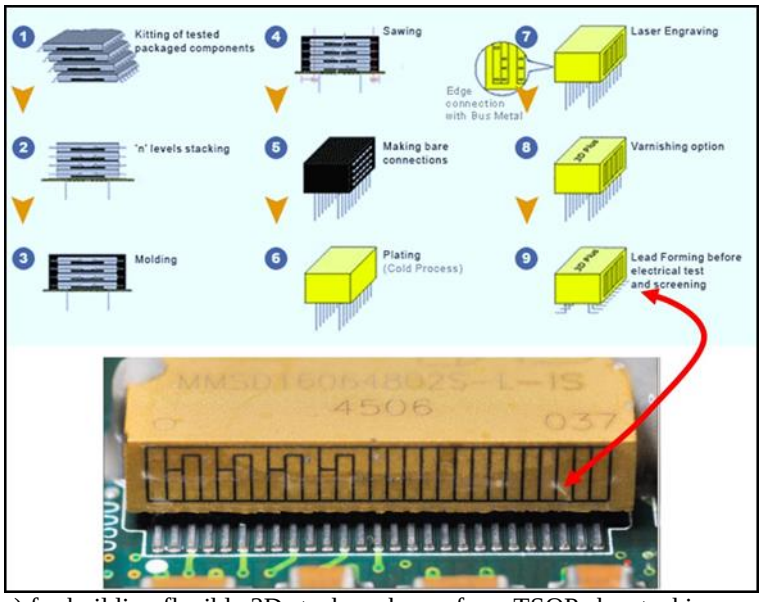

Fig. 9. Process flow (top) for building flexible 3D stack packages from TSOPs by stacking, sawing, Ni/Au coating for interconnection, and also using flexible L-shape lead for solder assembly. Bottom shows the final package assembled onto the board for solder joint reliability evaluation.

4.0 SUMMARY/ CONCLUSIONS

This paper presented thermal cycle reliability evaluations of 2-high and 4-high 3D stacks built with a mix of TSOP and DFN daisy-chain package assembly. Although this particular PoP packaging technology offers advantages in 3D high-density packaging with readily available (TSOP to DFN) technology, it was found that this packaging technology does not meet minimum reliability expectations when evaluated under standard temperature cycling methods typically used in electronics packaging qualification tests for high-reliability and even most commercial applications. Characterization was performed by daisy-chain resistance evaluation followed by visual and 2D/3D X-ray inspections. Visual inspection clearly showed various levels of failures after 500 thermal cycles (–55°C to +125°C). X-rays showed lead shifts and leads covered by adhesive that is not possible to visually inspect, though separation was observed by visual inspection.

A more robust 3D stack memory package is being offered by another manufacturer. Even though this technology uses a stack of tested TSOP memory, it uses more flexible L shaped leads extruded under the part for a more robust assembly reliability. A configuration of this package style is being evaluated with and without edge adhesive bonding. Reliability test data for this style of 3D stack packages is being gathered and would be the subject of a future paper.

5.0 ACKNOWLEDGMENTS

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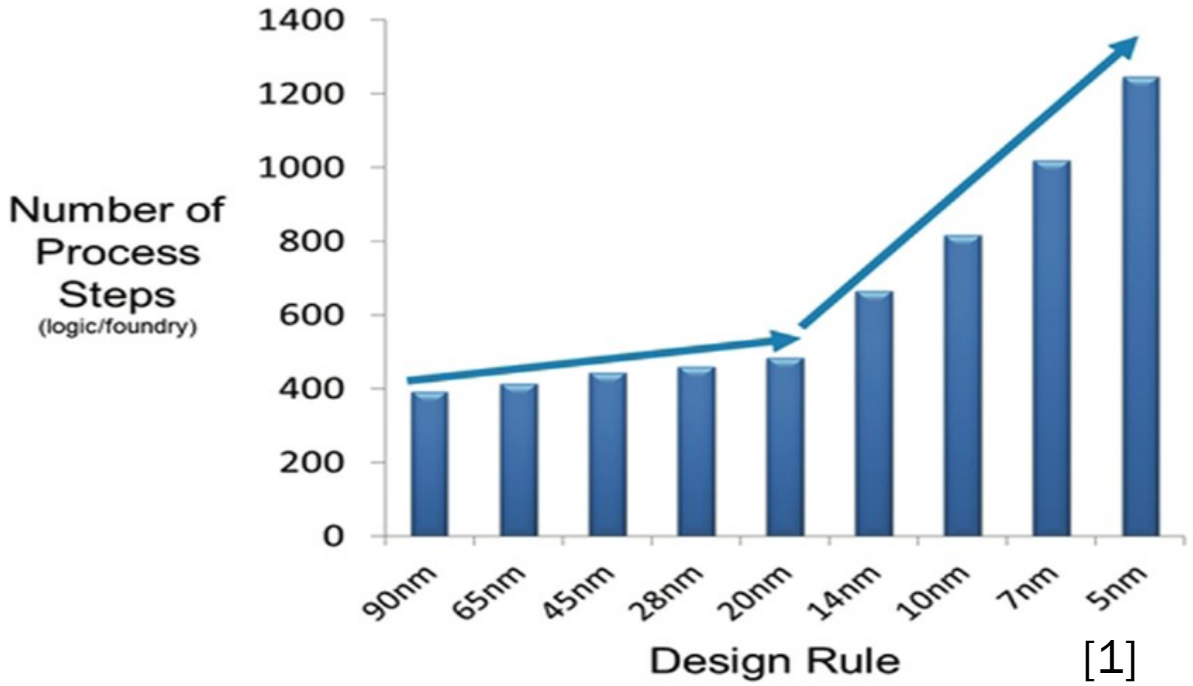
Agenda/ Outline

- Packaging Trends
  - *iNEMI /3D stack*
- Reliability
  - *System/ IPC 9701 Specification*
- Assembly Reliability Tests
  - *2- and 4-high (2D/4D) TSOP/DFN (dual-flat-no Lead) assemblies*
  - *TC Daisy-chain Test Results*
- Characterization
  - *Optical/ 2D/3D X-rays*
  - *Comparison*
- Summary

IC Device vs Packaging Growth

COTS IC Packaging , 3-5X

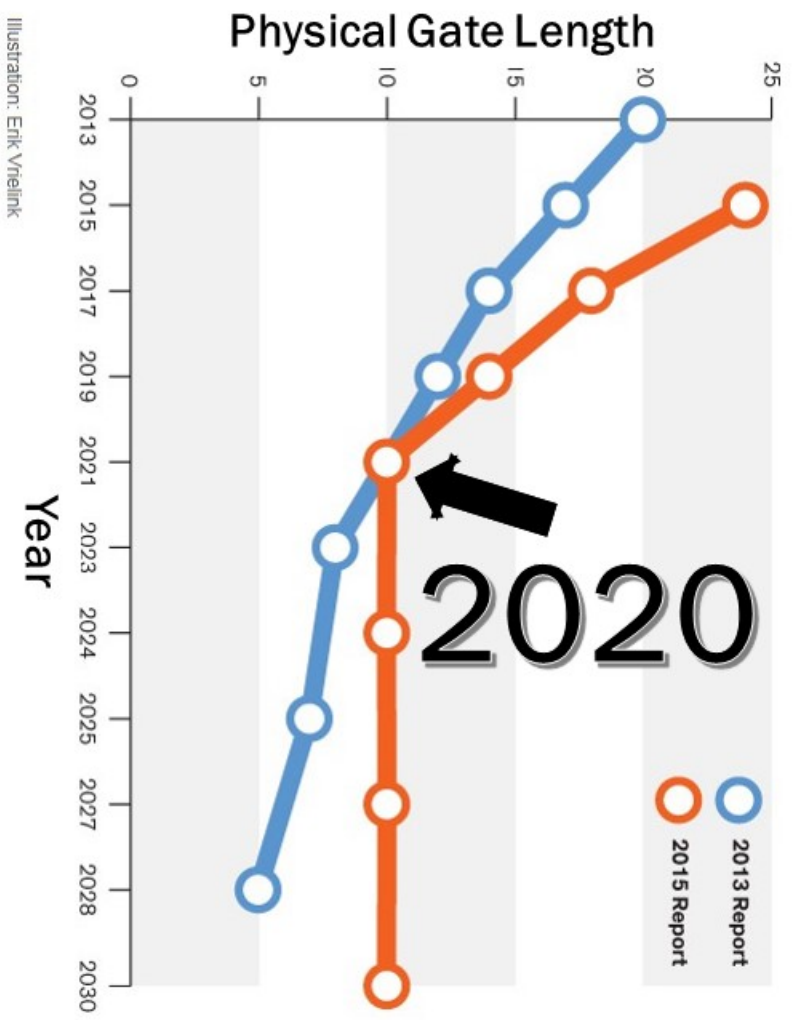


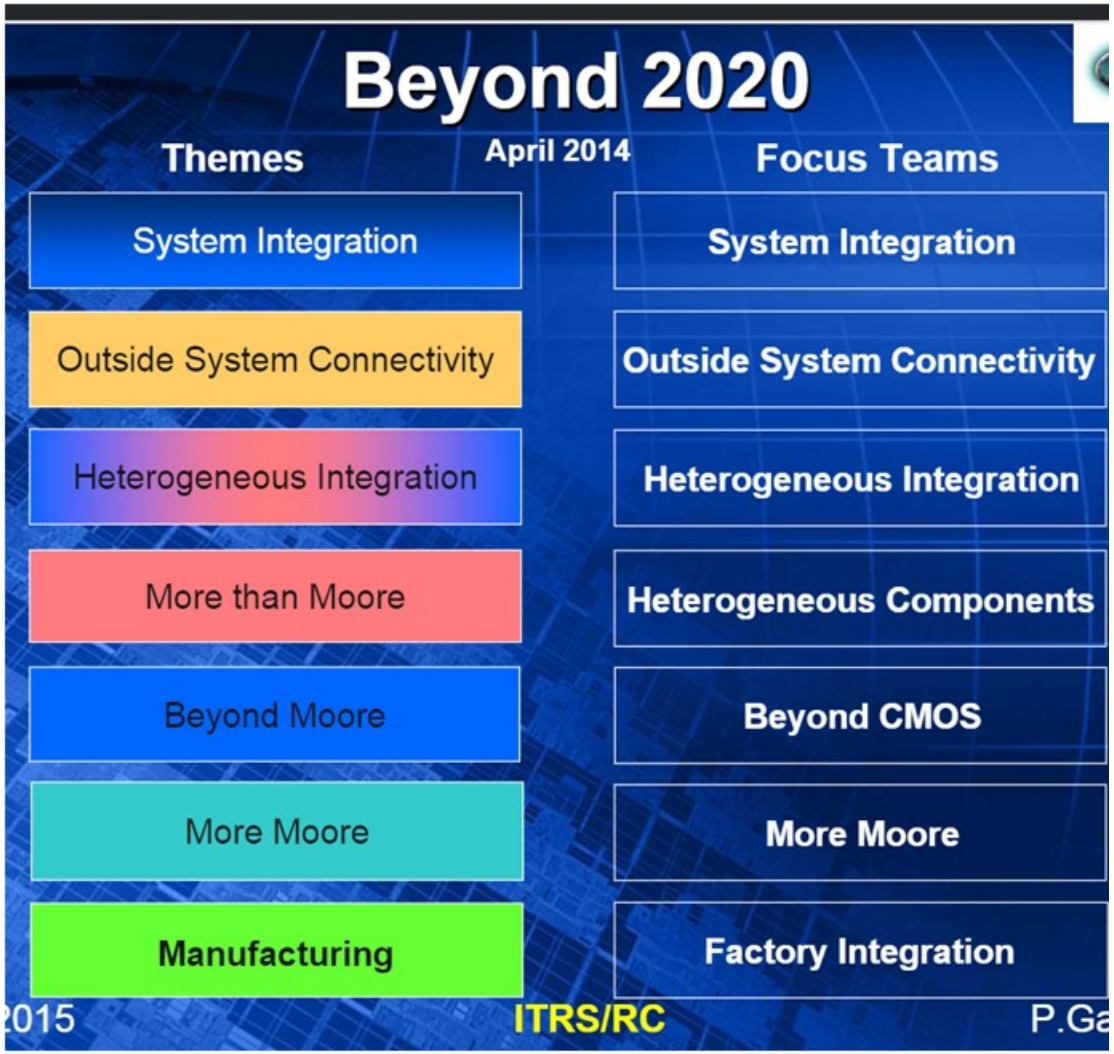
[1]

Moore's Law: 50 Years ICs, ~ 1000X

15µm to 15nm

ITRS Beyond 2020





iNEMI 2017

- ITRS to IRDS (device & system)
- Re-stores Defense/Aerospace
- Data centers as utilities & clouds as “rent vs. buy”
- The “IoT”, sensors ubiquitous- cyber-attacks?
- Remote patient care, proactive/preventive

iNEMI 2017 (Cont.)

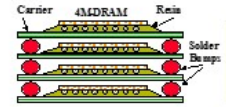
- **Complex products: SiP (2.5D & 3D)**

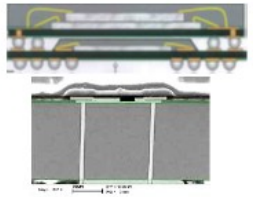
- Embedded passive/active & SoP/SiP, functionality
- Portables shift to “wearables”
- Auto safety systems to proliferate
- Assembly to lower cost/temp Pb-free

Conventional 3D Packaging Technologies

Area Arrays

PoP (Stack BGA/CSP/TMV)

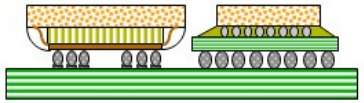


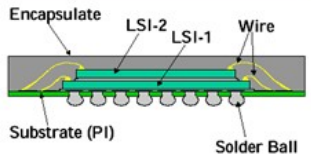


- High I/Os
- Heat dissipation
- Large die, Warpage, Reliability?
- Assembly Robustness

Array: Good Self Alignment

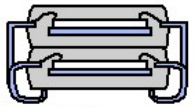
PiP -Stack Die/MCP

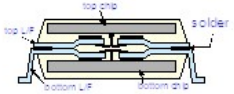




Leads

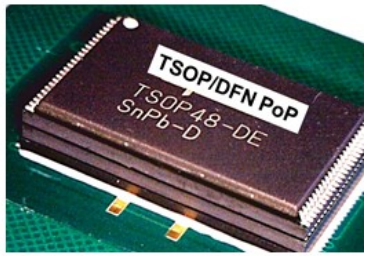
Leaded



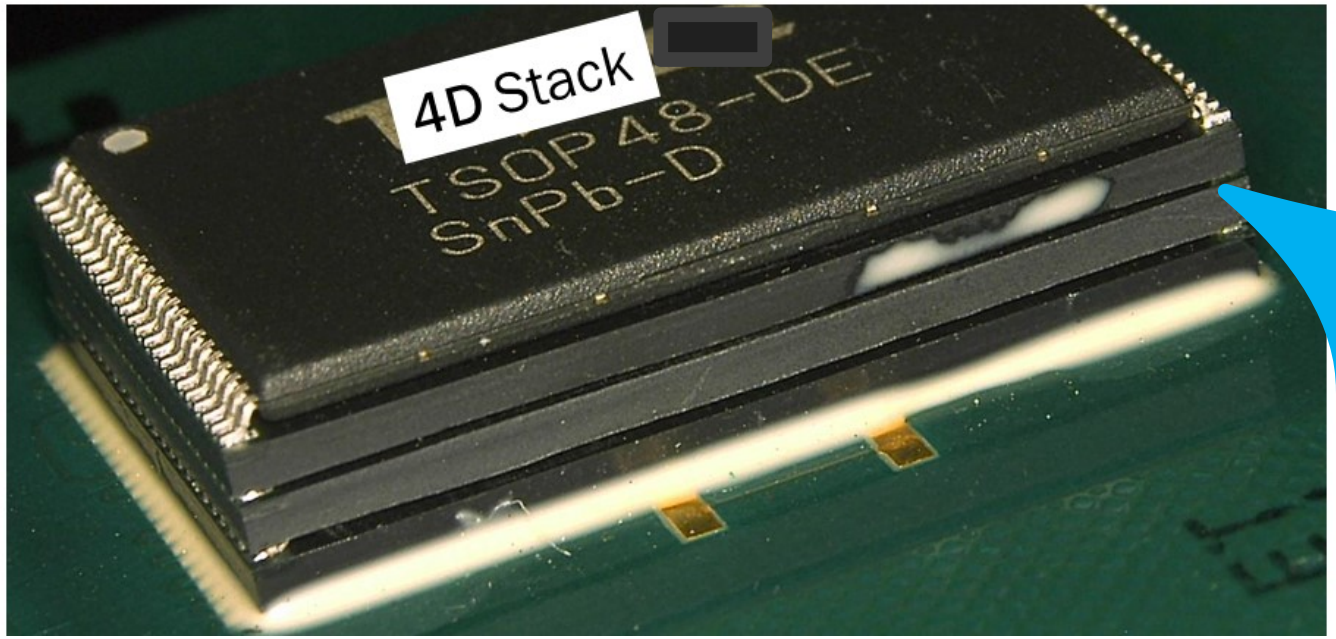


- Low I/Os
- Conventional Assembly
- Heat Dissipation ?
- Reliability?

Mix



2D uses 2 TSOPs bottom TSOP is bonded



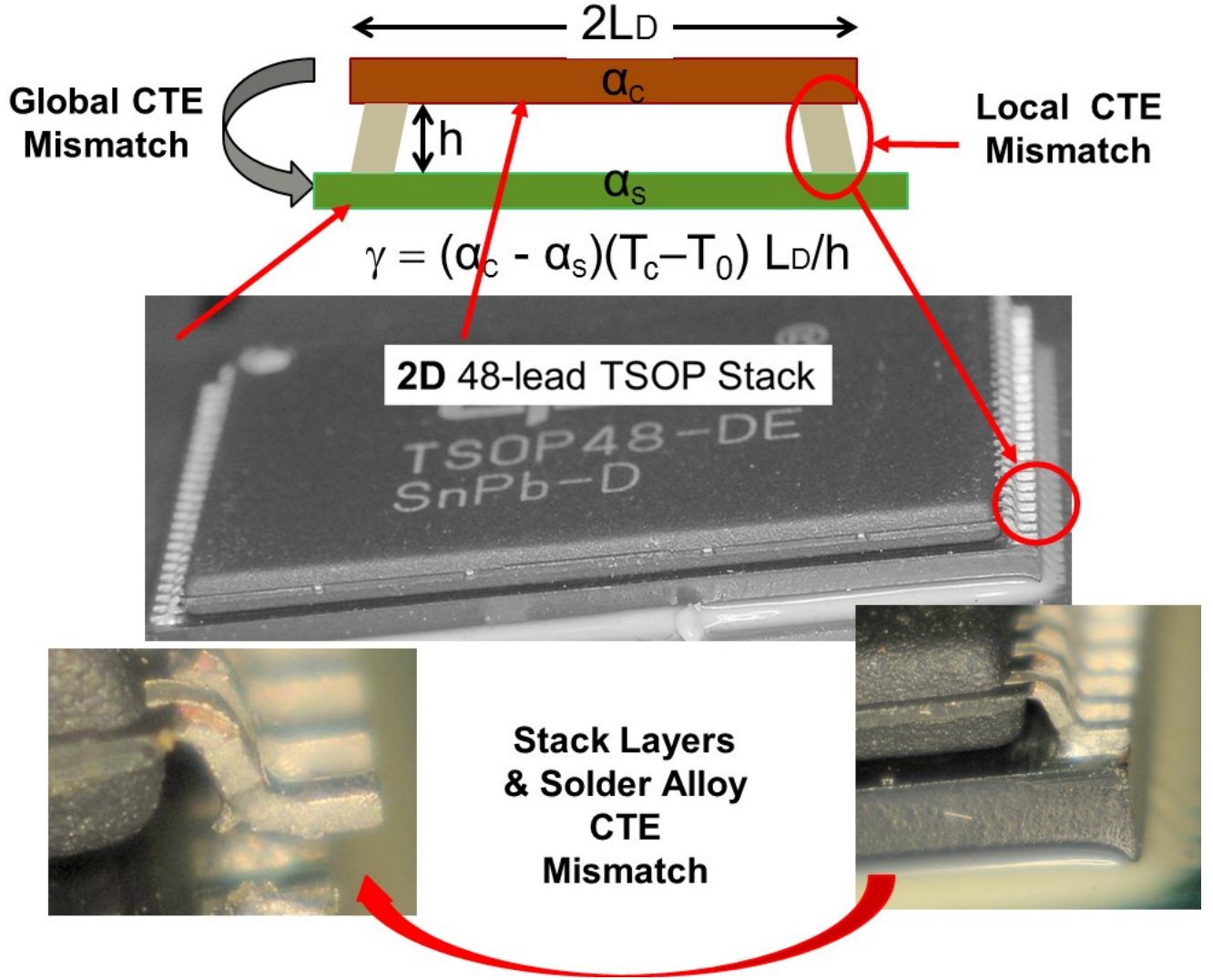
4D uses 2 TSOPs Top/Bottom & 2 DFNs

Reliability

"Reliability is the ability to function as expected under the expected operating conditions for an expected time period without exceeding expected failure levels"

Reliability: Thermal Global/Local

- **Global CTE mismatches typically are the largest. The 3 parameters define the thermal expansion mismatch are greatest**
  - ✓ **The CTE-mismatch (Δα)**
  - ✓ **The temperature swing (ΔT)**
  - ✓ **Package diagonal length (2 *l* or 2 L_D) can be large**

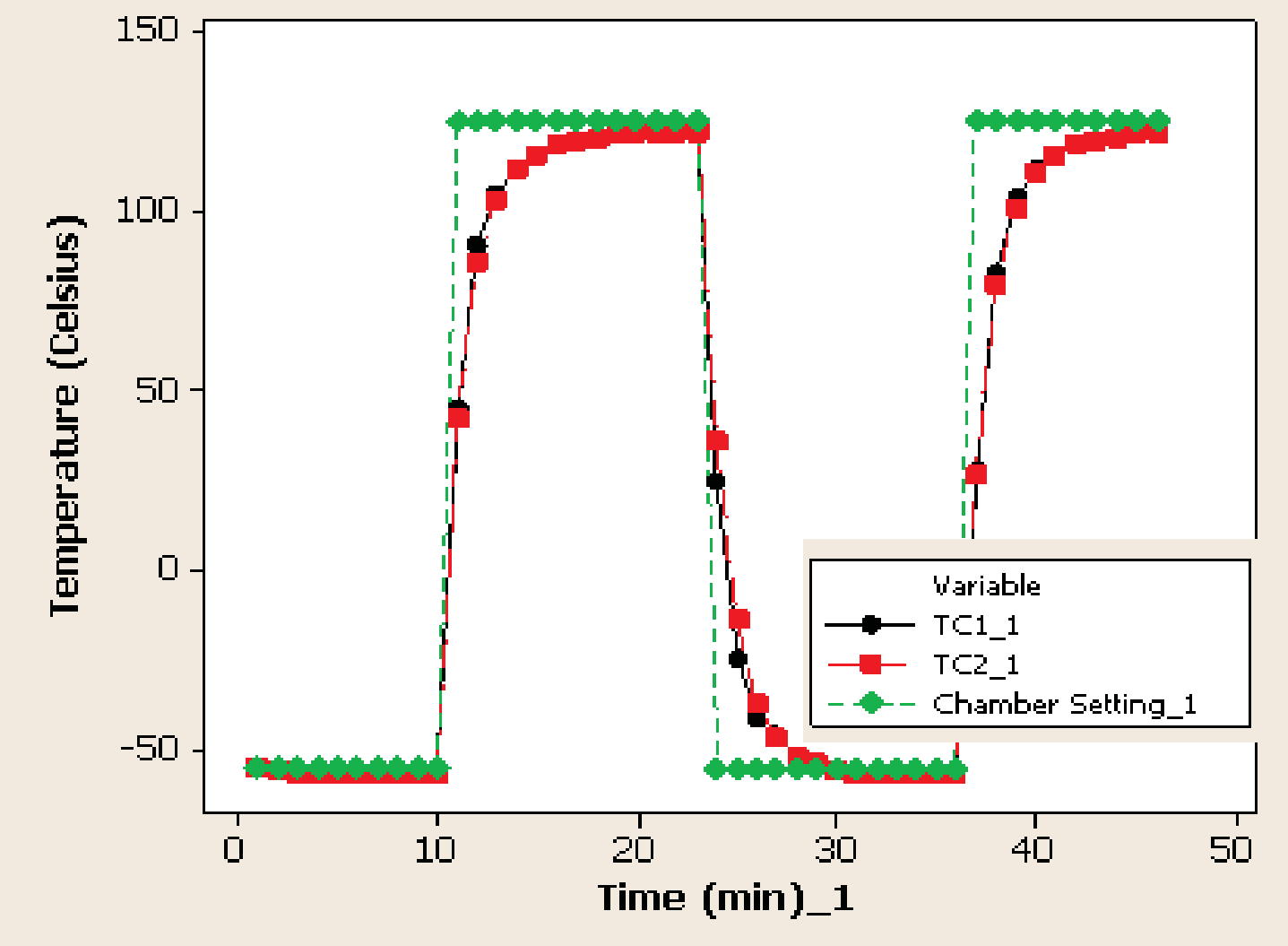


IPC 9701- Thermal Cycles

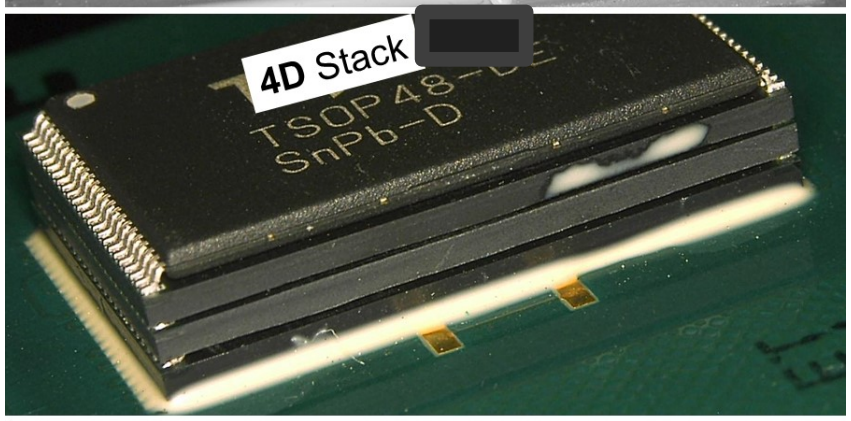
Table 1 Temperature cycling requirements specified in Table 4.1 of IPC 9701

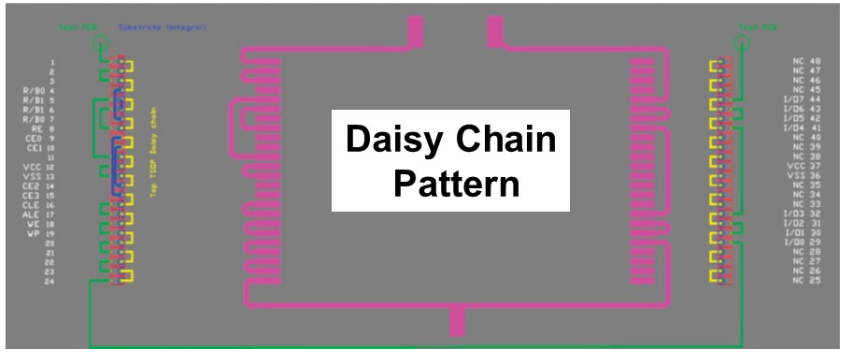
Test Condition	Mandated Condition
Temperature Cycle (TC) Condition: ***TC1***	***0°C ↔ +100°C (Preferred Reference)***
TC2	–25°C ↔ +100°C
TC3	–40°C ↔ +125°C
TC4	–55°C ↔ +125°C
TC 5	-55 °C<-> 100°C
Test Duration	Whichever condition occurs FIRST: 50% ***(preferred 63.2%)*** cumulative failure (Preferred Reference Test Duration) or
Number of Thermal Cycle (NTC) Requirement: NTC-A	200 cycles
NTC-B	500 cycles
NTC-C	1,000 cycles (Preferred for TC2, TC3,and TC4)
NTC-D	3,000 cycles
NTC-E	***6,000 cycles (Preferred Reference TC1***)
Low Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+0/–10°C (+0/–5°C) [+0/–18°F (+0/–9°F)]
High Temperature Dwell	10 minutes
Temp. tolerance (preferred)	+10/–0°C (+5/–0°C) [+18/–0°F(+9/–0°F)]

TSC (-55/125°C)


150
100
50
0
-50
Temperature (Celsius)
0
10
20
30
40
50
Time (min)_1
Variable
TC1_1
TC2_1
Chamber Setting_1

Daisy Chain for Monitoring





2D TC Results

SN	R0 cyc	50	100	150	200	250	300	350	400	450	500
1	1.6	1.6	1.6	6.0	1.6	1.6	1.6	1.6	1.6	1.6	1.6
2	1.5	1.5	1.5	1.5	1.5	1.6	1.6	1.7	1.9	2.1	0.0
3	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
4	1.5	1.5	1.5	1.5	1.6	1.7	2.5	3.6	9.5	7.7	11.5
5	1.5	1.5	1.5	1.5	1.5	1.6	1.6	1.6	1.7	1.7	1.8
6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.7
7	1.5	1.5	1.5	1.5	1.5	1.6	1.8	0.0	0.0	0.0	0.0
8	1.6	1.6	1.6	1.6	1.7	1.8	1.9	2.0	2.1	2.1	2.2
9	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
10	1.5	1.6	1.5	1.6	1.6	1.6	1.6	1.6	1.7	1.9	2.6

Visual inspection: **SN1,** Failed TSOP solder failure

SN7, Whole row on one side failed

Failure, 20% increase in resistance

Failure, Complete open >1000 Ohms

4D TC Results

SN	R0 cyc	50	100	150	200	250	300	350	400	450	500
11	1.9	2.2	2.0	2.4	3.3	0.0	0.0	0.0	0.0	0.0	0.0
12	1.9	2.1	2.1	2.2	2.4	2.5	3.1	10.2	9.7	6.5	6.9
13	2.0	2.4	3.1	3.6	4.2	5.9	6.2	7.7	11.1	12.8	18.9
14	2.0	2.0	2.0	2.1	2.2	2.2	2.8	2.7	3.2	12.4	0.0
15	1.8	2.1	2.1	2.2	2.5	2.7	2.9	0.0	0.0	0.0	0.0
16	1.9	2.1	2.2	2.5	4.2	8.3	6.0	5.6	11.8	11.5	14.7
17	1.9	2.3	2.4	2.9	3.1	3.5	4.2	4.4	5.5	11.7	0.0
18	1.8	2.4	2.5	3.2	4.3	4.7	5.3	5.6	6.4	6.9	8.1
19	1.9	2.1	2.1	2.3	2.8	13.0	12.2	7.1	21.1	0.0	0.0
20	1.9	2.2	2.3	2.5	2.6	2.8	3.1	3.4	3.9	4.1	4.4

Visual inspection: **SN11,** Middle TSOP solderjoint failure

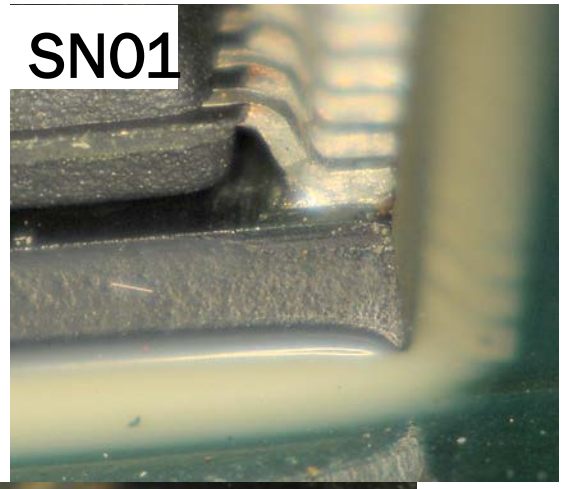
SN13, possibly lower package failure

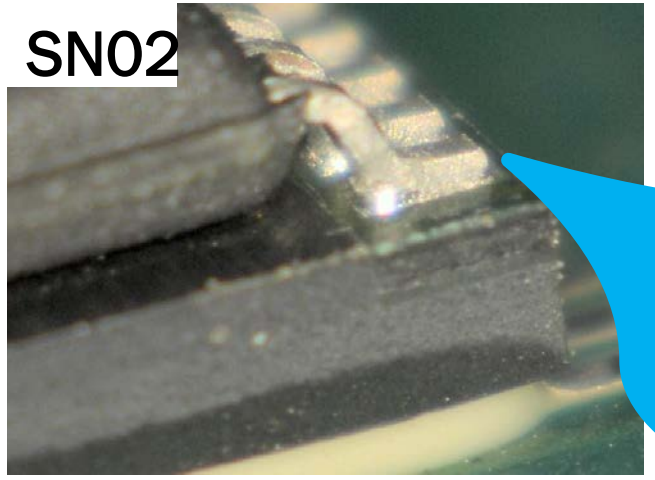
SN19, Top package OK, possibly lower package failure

Failure, 20% increase in resistance

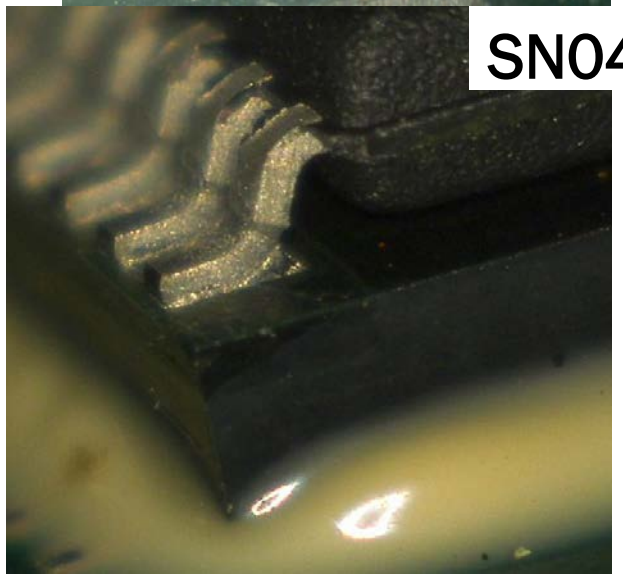
Failure, Complete open >1000 Ohms

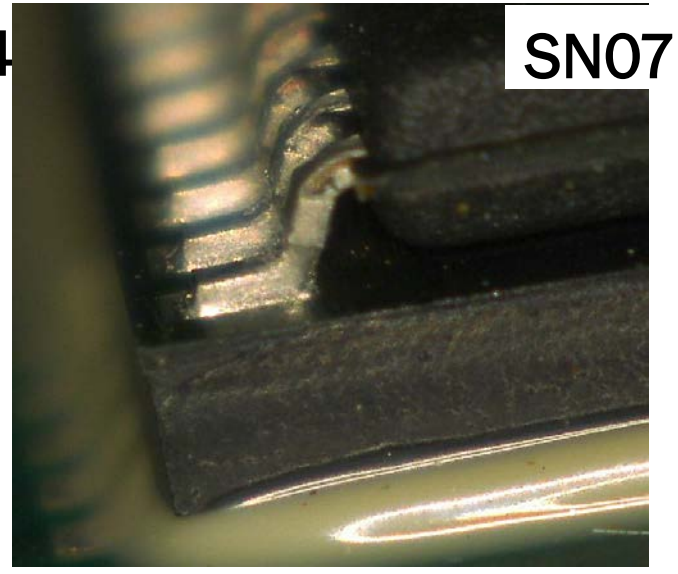
Optical Images for 2D TC Results



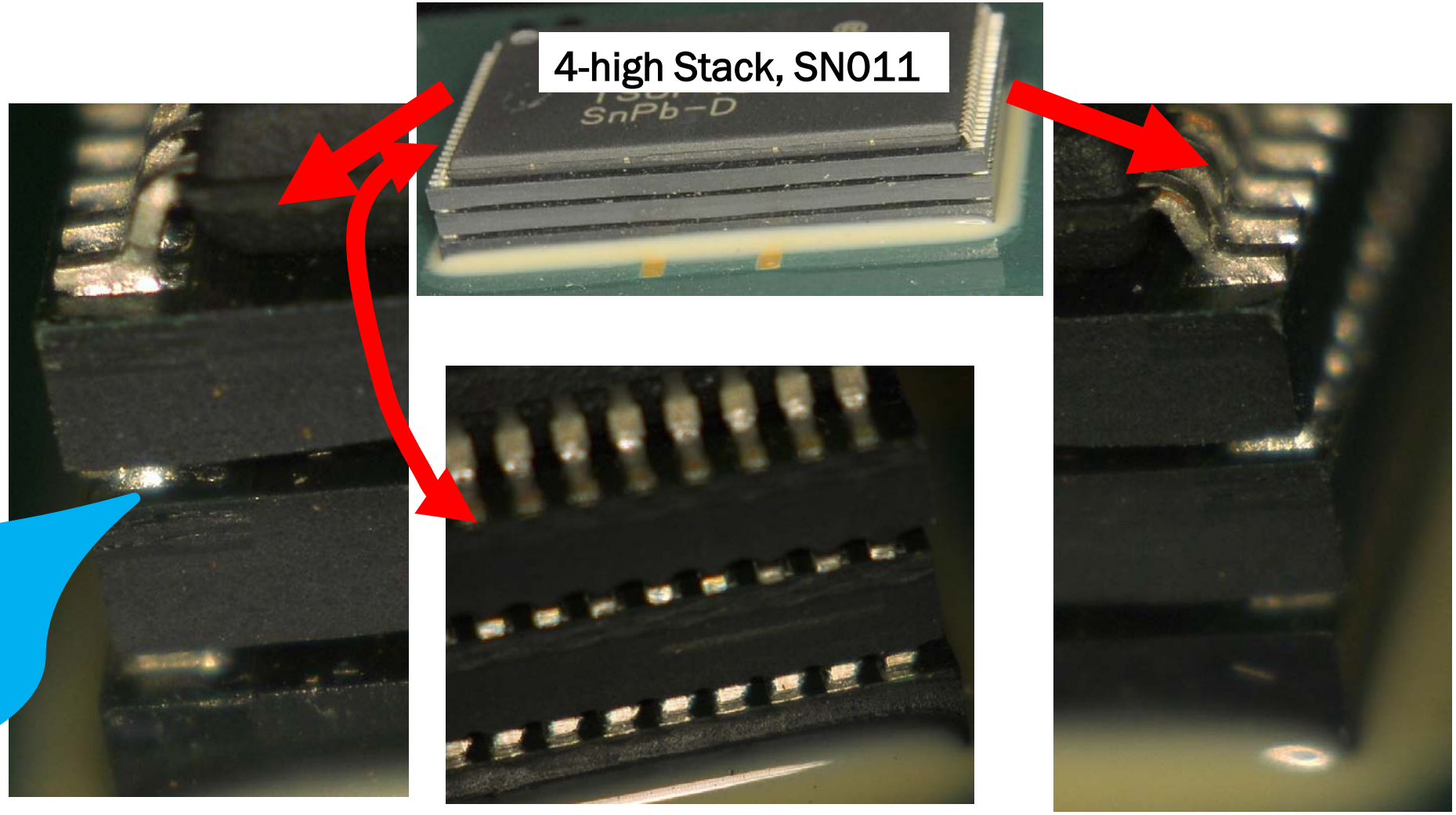


Shift in lead and solder failure was common for TSOP



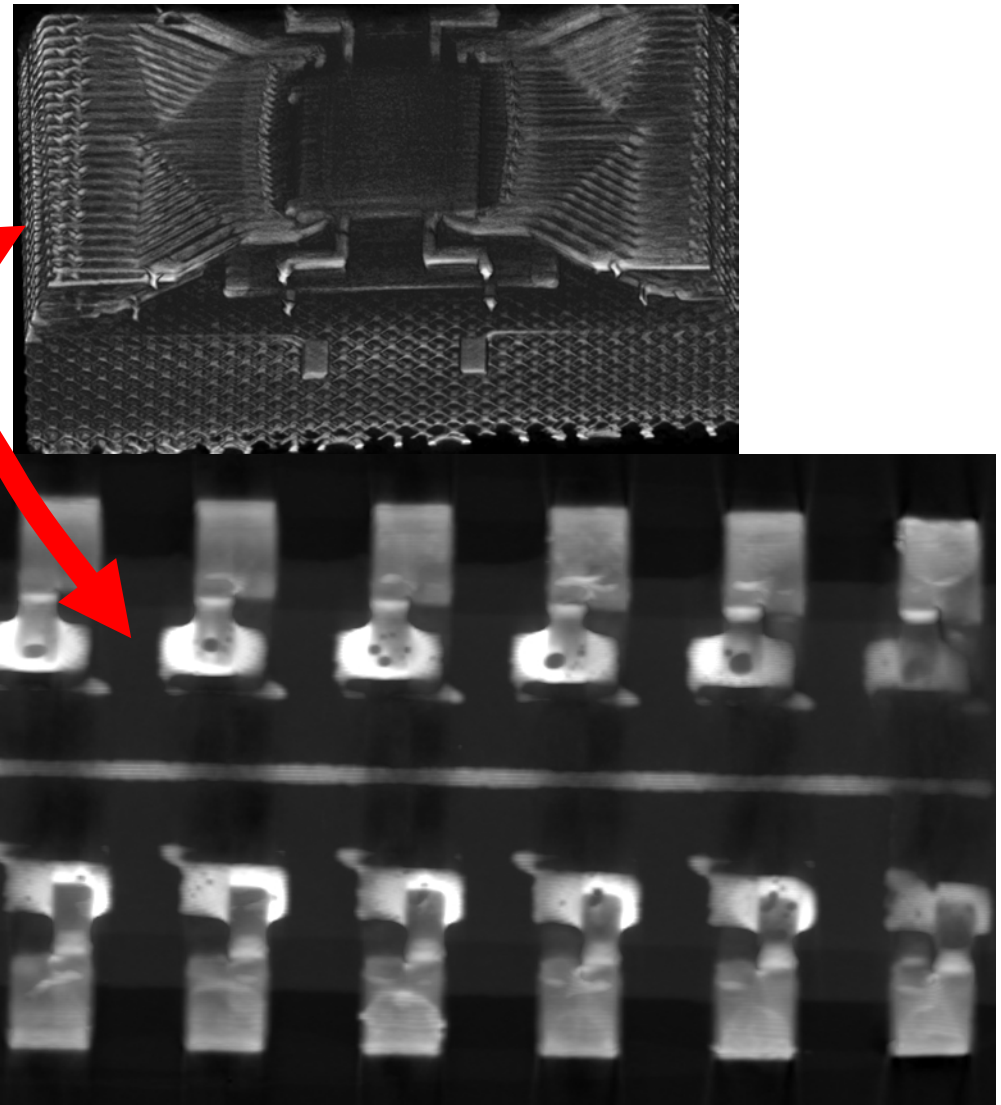


Optical Images for 4D TC Results



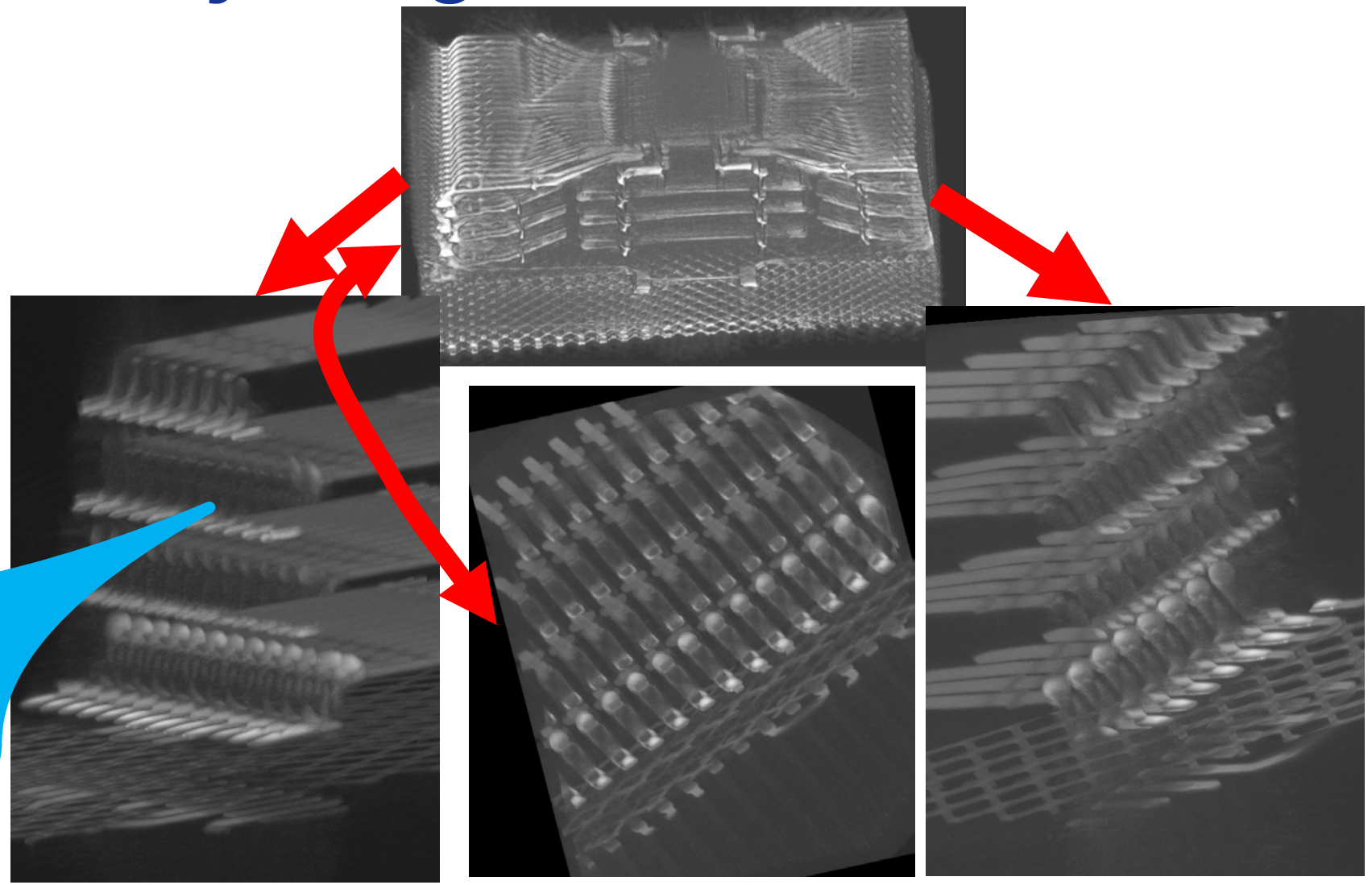
Failure of DFN solders was common for 4D

3D X-ray Images for 2D Stack



X-ray detects TSOP Configuration, but not failure

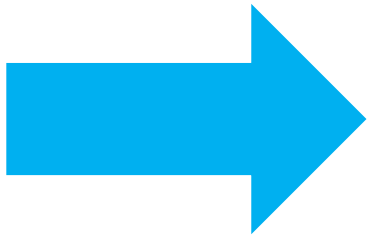
3D X-ray Images for 4D Stack



3D X-ray shows internal lay up of TSOP/DFN, but not solder failures of DFN

Summary

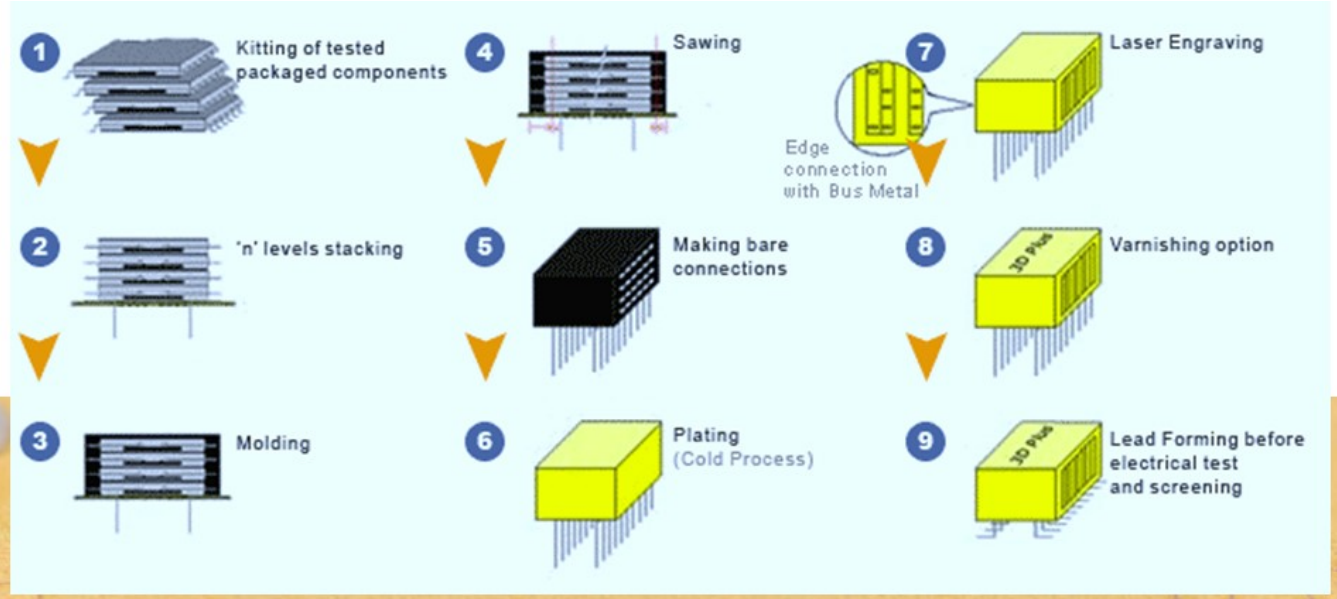
- 3D TSOP/DFN
  - *2-high 3D stack*
  - *4-high 3D stack*
  - *TC (-55C/125°C)*
- Reliability
  - *2-high Failure>250 cycles*
  - *4-high Failure >300 cycles*
- Verified failures by Visual/X-ray

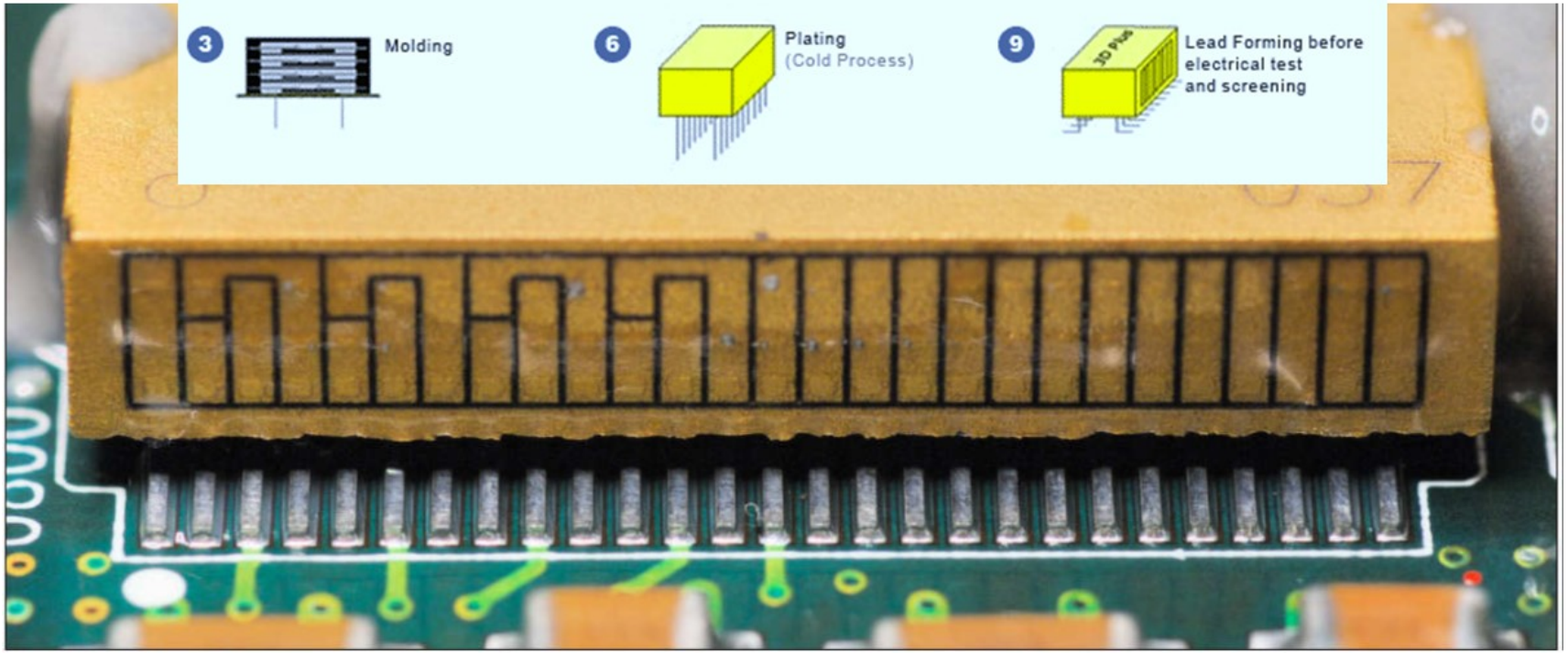


2-high and 4-high TSOP/DFN 3D stack DID NOT meet minimum high-reliability requirement

Other 3D TSOP and BGAs have considered for high- reliability applications

3D TSOP for Hi-Rel





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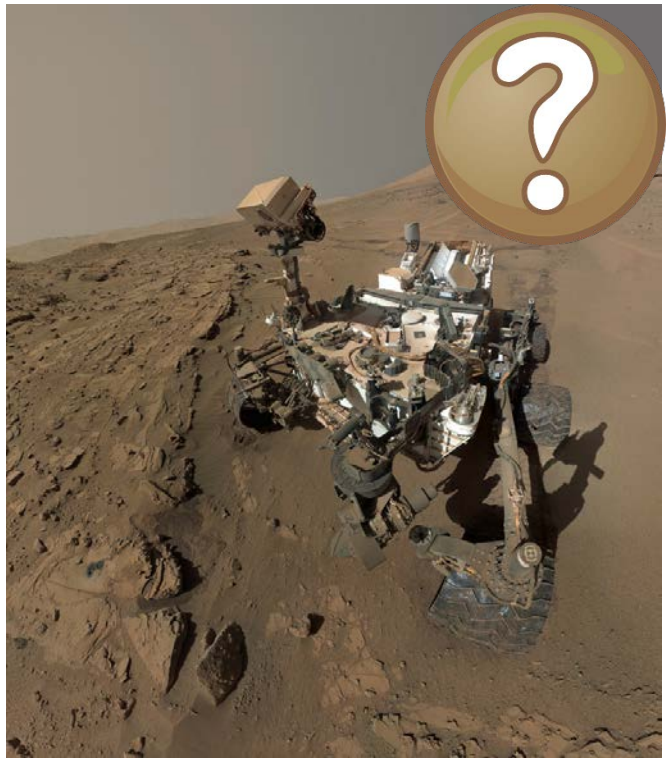
Thank You!



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1. IC Knowledge Strategic Cost Model