Connecting to Embedded Components Using TLPS (Transient Liquid Phase Sintering) Pastes in Via Layers

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Abstract
The electronics industry trend continues to be to continually increase capability and performance within an existing or smaller footprint. Shoehorning all of the required components onto the exterior surface of the PCB has become an increasingly difficult puzzle. The use of stacked microvias instead of plated through holes and stacked ICs in various configurations has freed up some real estate. The use of ever smaller passive devices also saves space, but reintroduces old issues such as tombstoning. The ideal solution would be to provide 'surface' real estate within the architecture of the circuit board – like moving items from a desk to a bookshelf – by embedding components into the board. Leveraging the established buried TLPS (Transient Liquid Phase Sintering) paste microvia technology for z-axis interconnection, "via layers" with TLPS paste inserted into lamination adhesive at the desired interconnect points to the component terminals could be used to connect to embedded components. Ideally, components could be buried at any layer to maximize topside real estate and minimize wiring lengths. The concept of using TLPS-filled via layers to make both connections to buried components and any other z-axis interconnections required on any layer will be explored.

The combination of the sintering paste interconnect and an interposer element is the key to enabling this architecture. This manufacturing strategy presents a number of advantages. The board may be broken down into logical substructures such as high density, core or RF portions. Each of the sub-PCBs can be fabricated according to best manufacturing practices for that portion of the circuit board rather than trying to fabricate a single complicated board. Yield losses from sequential process steps and multiple laminations may be reduced. The component placement can facilitate point-of-source architecture for high electrical performance. The process flow and laboratory demonstrations of this technique will be presented in this paper.

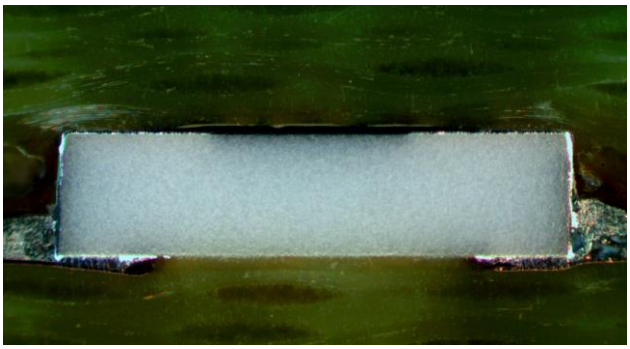


Figure 1: 0805 capacitor embedded and interconnected with TLPS paste

Introduction

A. Embedded Passive Components in PCBs

Embedding passive components within the inner layers of a printed circuit board (PCB) provides a variety of benefits – both in density and in performance.

In a typical PCB, passive components account for 80-95% of the total components and cover over 40% of the surface[1].[1] For example, a typical breakdown of components for a PCB would compose 5% ASIC, 4% connectors, 40% capacitors, 33% resistors and 18% miscellaneous parts[2].[2] Embedding a portion of the resistors and capacitors offers the opportunity to free up substantial topside real estate for added features, or to enable device shrinkage.

Embedding passive components also can improve the routing efficiency between the passive devices and the active devices that they serve. By placing these components in closer proximity, both signal speed and integrity are improved. The parasitic losses endemic to surface mount routing can be substantially reduced.

The most established method for embedding resistors and capacitors is the inclusion of a patternable foil or dielectric layer. These layers are laminated into the core structure of the PCB, processed through wet chemistry to create the desired

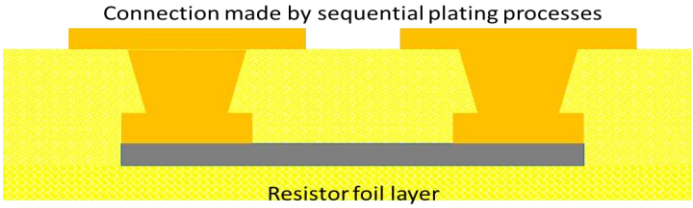


Figure 2: Concept of an embedded foil resistor

components and then interconnected as additional layers are added to the PCB through sequential processes. In the case of resistors formed by such a method, precise resistor values are dialed in using laser trimming the chemically etched feature prior to the next lamination step. Figure 2 shows the concept of a resistor formed from an embedded foil layer. Although this method has been used successfully for many years to produce reliable embedded components, the variety of values that can be achieved, particularly for capacitors, is quite limited and the embedded passives are limited to a single plane within the structure.

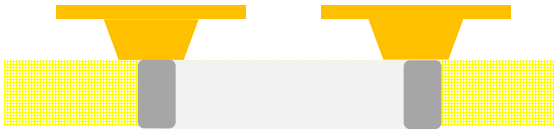


Figure 3: Discrete embedded capacitor concept

The size of discrete passive devices has shrunk dramatically in recent years. This shrinkage makes it feasible to embed discrete passive devices without substantially increasing the thickness of the PCB. This affords the opportunity to have a broad spectrum of precise resistor and capacitor values without the extra wet chemistry and laser trimming steps. The use of discrete devices also enables freedom of placement. Figure 3 depicts the concept of an embedded discrete device interconnected by plated copper vias. The primary detriment of embedding and interconnecting these discrete devices by conventional means is the sequential nature of the process and the potential number of lamination cycles to which the devices will have to be subjected.

B. Background: Transient Liquid Phase Sintering

Sintering is a process in which adjacent surfaces of metal powder particles are bonded by heating. Liquid phase sintering is a special form of sintering during which solid powder particles co-exist with a liquid phase. Densification and homogenization of the mixture occur as the metals diffuse into one another and form new alloy and/or intermetallic species.

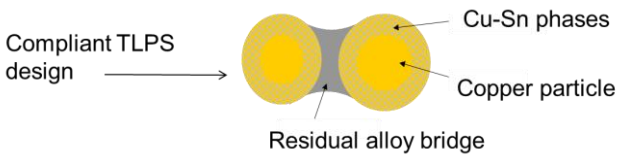


Figure 4: Conceptual view of a sintered TLPS interconnect

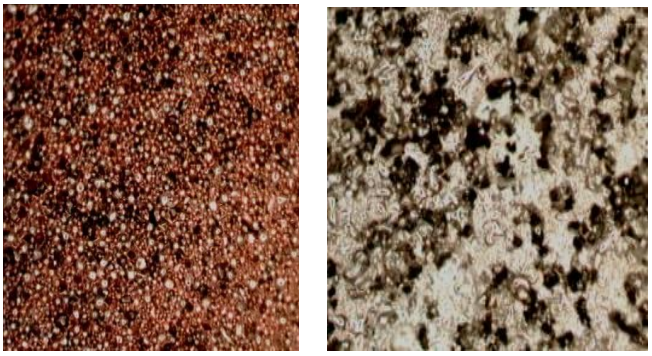


Figure 5: TLPS paste before and after sintering

In transient liquid phase sintering (TLPS) of powders, the liquid phase only exists for a short period of time as a result of the homogenization of the metals to form a mixture of solid alloy and/or intermetallic species. The liquid phase has a very high solubility in the surrounding solid phase, thus diffusing rapidly into the solid, and eventually solidifying. Diffusional homogenization creates the final composition without the need to heat the mixture above its equilibrium melting point. After cooling, subsequent temperature excursions, even beyond the original (LMP) alloy melt temperature, do not reproduce the original melt signature of the mixture. This is the "signature" of a typical low temperature transient liquid phase sintered metal mixture. This signature can be seen in Figure 6 where the paste is initially sintered at 190°C and then subsequently cycled to 280°C multiple times to simulate multiple reflow cycles. As can be seen in the DSC scan, the original endothermic alloy melt is largely gone after the initial cycle and there is some continued interdiffusion in the first simulated reflow cycle, but the microstructure composition is very stable through the remaining reflow cycles.

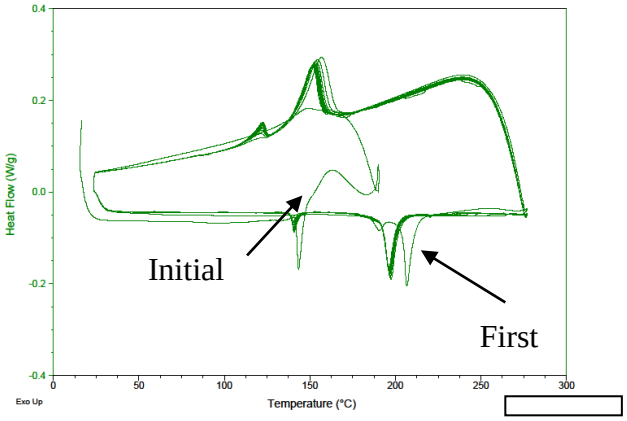


Figure 6: DSC signature of a TLPS reaction

TLPS technology is used to produce conductive compositions that include metal powder(s), solder alloy powder(s), and a permanent flux-polymer system. TLPS compositions are used to form interconnects by creating a patterned deposition of the TLPS composition, and then sintering the metallic components in the composition by heating to relatively low temperature. During heating, the flux-polymer fluxes the metal powders, allowing TLPS to occur. After heating, the flux-polymer chemically binds the resultant metal oxides, rendering them harmless. For this reason, these compositions provide good electrical and thermal conductivity with little opportunity for conductivity deterioration due to oxidation, corrosion or thermal expansion and contraction.

The microstructure of processed TLPS compositions looks like a network of particles of metal, each bearing one or more "shells" of the newly formed alloy/intermetallic compositions, which are in turn interconnected by the non-reactive portion of the original solder alloy. Open areas of the metallic network structure are generally filled with the cured flux-polymer with the interconnected metal forming 60-85 volume percent of the sintered paste depending on the specific formulation. Reaction between the metal and the reactive element(s) of the solder alloy may result in either partial or complete incorporation of the metal particles into the newly formed alloy and/or intermetallic species. The number and nature of the new alloy and/or intermetallic species that form is dependent on the selection of metallic constituents in the TLPS composition, their relative proportions, the particle size distribution and the process temperature. The composition of the residual components of the original solder alloy is likewise dependent on these factors.

Transient liquid phase sintering (TLPS) pastes have been successfully used for almost two decades in printed circuit board (PCB) interconnects -- printed jumper wire and z-axis layer-to-layer connections – that are subjected to subsequent solder reflow. In these applications, TLPS pastes are sintered during common PCB fabrication processes such as lamination, and will not remelt in subsequent assembly operations. Billions of interconnects have been made with TLPS pastes in these PCB applications. Often, the PCBs fabricated with TLPS interconnects are for complex and reliability-critical applications such as supercomputing and aerospace. A single PCB may contain as many as a million interconnects – all of which must function reliably.

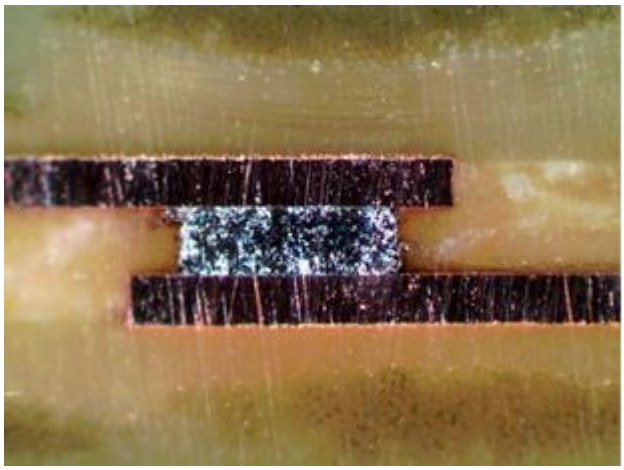


Figure 7: Detailed view of the sintered paste interconnect between copper pads on two cores

C. TLPS Interconnects in PCBs

Sintering paste z-axis interconnections are often used in core-to-core joining applications such as those depicted in Figures 8 and 9. As can be seen in the illustration in Figure 8, the PCB is broken into sections that are fabricated as independent PCB structures with plated through hole (PTH) z-axis interconnections for each section. The individual sections, or 'cores,' are then joined by interleaving prepreg interposers with openings filled with TLPS paste. The TLPS paste forms the electrical interconnections and the prepreg mechanically joins the cores during a standard lamination cycle. The cores may be simple double-sided PCB constructions, or may be complicated boards comprising multiple circuit layers as shown in Figure 9. The TLPS paste interconnects within the interposers, shown in more detail in Figure 7, have high electrical performance and are very reliable because the sintering reaction produces metallic bonding to both the copper pads and through the bulk of the via.

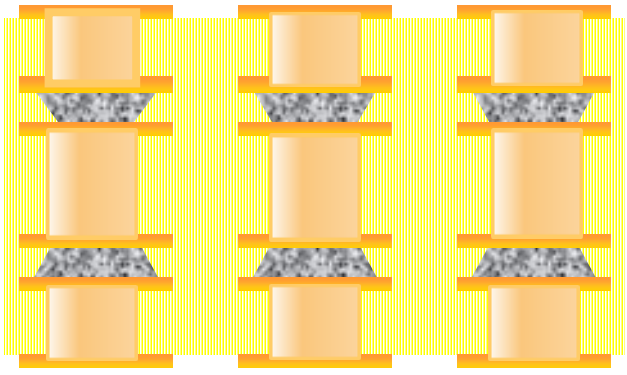


Figure 8: Illustration of core-to-core joining with sintering paste

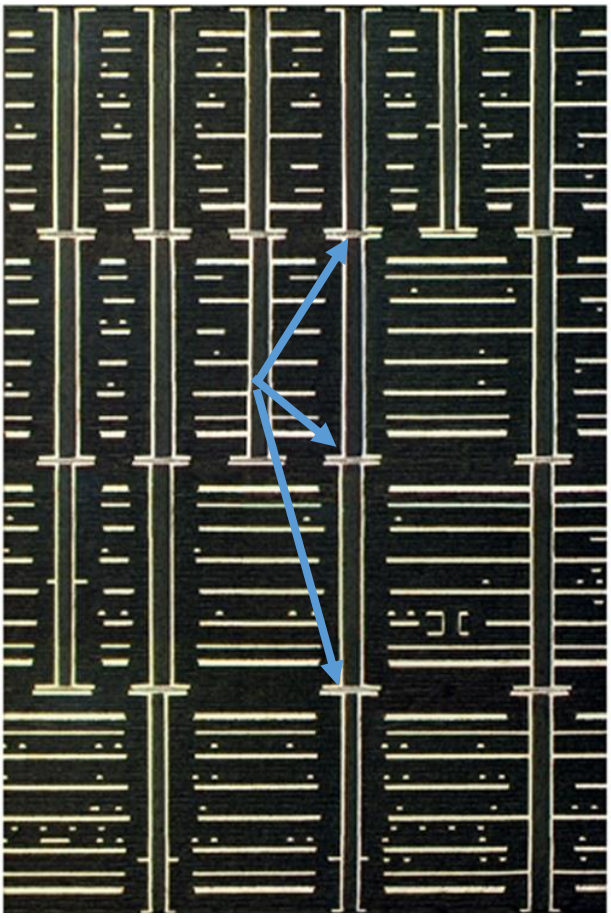


Figure 9: A high-layer-count PCB broken into four cores and joined with sintering paste interposers [3]

Conceivably, these same type of prepreg ‘interposers’ with TLPS vias could be used to simultaneously interconnect between layers of circuitry as well as between discrete component terminals and circuit pads.

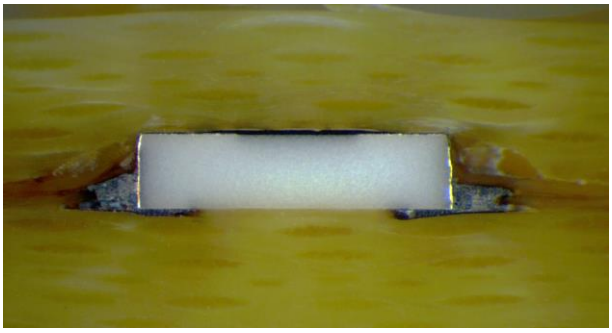


Figure 10: The prototype test vehicle

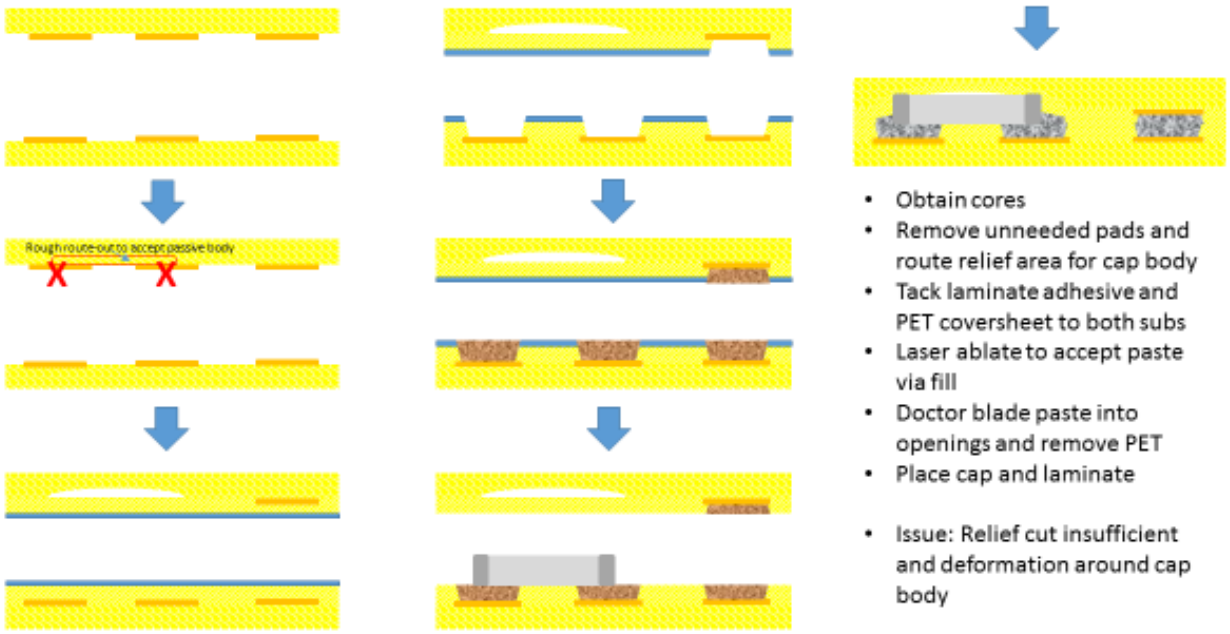


Figure 11: The test vehicle design concept

II. Experimental Design

As detailed in the introduction, embedded passive components have long been a desired PCB feature. Embedding the passives frees outside layer real estate and enables better point-of-need placement of these components. Embedding discrete passives at any layer provides better design flexibility and far superior performance to embedded passive layer technologies. The concept of this experiment was to leverage the established reliability record of core-to-core joining in complex PCBs with TLPS paste z-axis interconnects. As this is already perfomed as a parallel fabrication process, burying discrete passive components in these joining layers is a reasonable extension of proven technology.

To test the concept, a standard daisy chain test board used for evaluating the compatibility of TLPS interconnects with various lamination adhesives was repurposed as an embedded capacitor test vehicle. The daisy chain test vehicle can be seen in Figure 12.

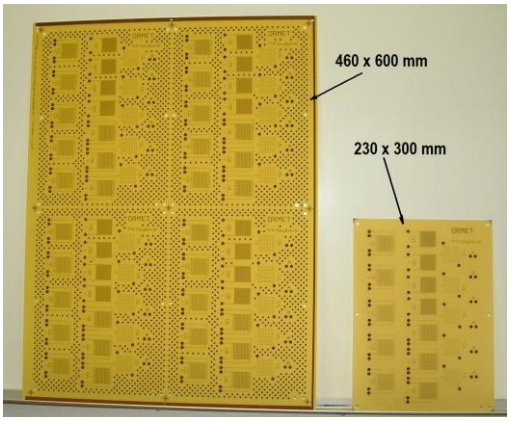


Figure 12: The daisy chain test vehicle

To repurpose the daisy chain test board as an embedded capacitor test vehicle, the footprint of some discrete capacitors were compared with the daisy chain pad layouts. The pad layout of three chains matched the footprint of 0805 chip capacitors, so these chains and components were selected for use. The 0805 capacitor is a large component to embed, with a body thickness of 500µm. The corresponding pattern had 700µm pad diameters on a 2mm pitch.

The intention was to preserve some of the daisy chain in order to evaluate how the TLPS vias fared in connecting the layers as well as connecting the capacitors to the pads. The modified chain can be seen in Figure 13.

In order to prepare the test vehicle to accept the capacitors, pads above the capacitors were selectively removed and a dremel tool was used to create rough relief cavities in the laminate. In Figure 13, the blue pattern on the left should be pictured closing over the orange pattern like a book in order to complete the chain. The yellow ovals represent the pads that were removed and the rough cavities formed to accept the thick capacitor body.

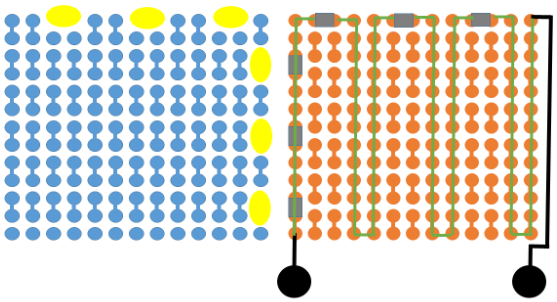


Figure 13: Modified daisy chain for the test vehicle

Prepreg and PET coverfilms were tack laminated onto the joining surfaces and the via holes necessary to connect the capacitors to the pads and to complete the modified daisy chain which were laser ablated through the coversheet and prepreg layers.
After laser ablation, TLPS paste was filled into the via holes and the PET coversheet was removed. The 0805 capacitors were placed and the sub-assemblies were put into a 90°C oven to evaporate the solvent in the TLPS paste prior to lamination.
The layers were aligned in a lamination book and laminated together at 190°C, per the recommended profile for the prepreg adhesive.

III. EXPERIMENTAL RESULTS

After the completed substrate was removed from the lamination press, an attempt was made to test for electrical continuity. Because the capacitors were embedded in series in the daisy chain, it was not possible to check continuity using a DC power supply, but an AC power supply should have provided a result.

Unfortunately, the rough cavities prepared to accept the capacitor bodies were not quite large enough and cross section analysis revealed that at least one capacitor in each of the three daisy chains was cracked, which prevented electrical test.

Figure 14: Overview cross section of the test vehicle

The daisy chains were cross-sectioned and the connections were analyzed. Figure 14 shows an overview of two capacitors and the intervening via connections. It is clear from the bulging of the laminate above and below the capacitors that the cavities were not sufficiently large to accept the capacitor bodies.

In the close up of Figure 15, the glass fibers of the prepreg show the displacement as the prepreg climbed over the top of the body and left a cavity into which the TLPS paste flowed.

Figure 15: Close up of one joint with the capacitor terminal and one via

A close-up look at the connection between the capacitor termination and the copper pad at 200x magnification shows a very high quality TLPS interconnect as can be seen in Figure 16.

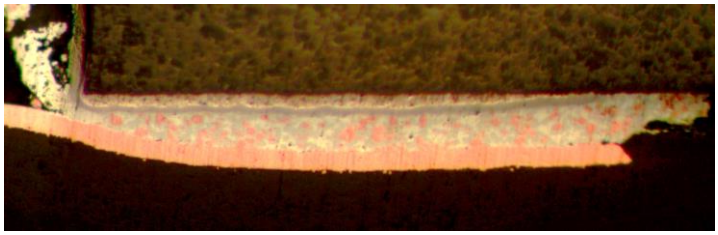


Figure 16: Close up of the interconnection between a capacitor terminal and a copper pad

A similar close-up of one of the double-via interconnects in Figure 17 shows a similarly good connection, with the two vias merged into one. The laser ablated via holes were nominally 250µm in diameter (top side) with the characteristic flower pot shape. As can be seen in the cross-section, this shape has been maintained. During lamination, the adhesive in the prepreg is displaced to encapsulate the circuit traces and the layer is compressed to roughly the thickness of the glass weave reinforcement. This compression is reflected in the spread of the vias to their final diameter of approximately 650µm. As can also be seen in this cross section, the final total thickness of the two face-to-face joining layers is about 175µm. It is not difficult to understand why the 500µm cap body thickness did not find sufficient relief space in the shallow relief cavities provided.

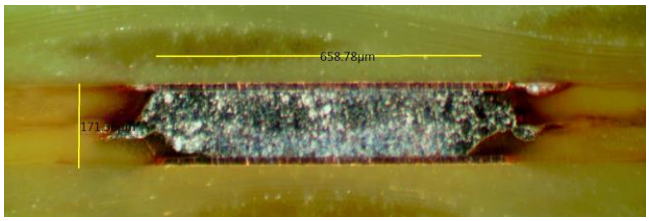


Figure 17: Close up of a double via used to connect the two sides in the daisy chain pattern

IV. DISCUSSION

In this initial feasibility study, the ability to embed discrete passive devices in interconnect layers containing TLPS paste vias was demonstrated. Although insufficient machining of the relief cavities prevented electrical test, cross sections reveal good quality interconnects to the passive devices and between the substrate layers which can be formed simultaneously.

Embedding discrete passive devices in this fashion eliminates the wet chemistry of embedded layer passives as well as that necessary for interconnection to the passive terminals.

Further, because the interconnect/embed layers are fabricated in parallel with the PCB sub-cores, components can be embedded on multiple layers in a single lamination. This also serves to protect the embedded devices from the rigors of multiple lamination cycles which can potentially improve yield. The ability to embed on multiple layers also provides an opportunity for improved overall signal routing versus a single embed layer.

V. CONCLUSIONS

In the first feasibility study, a daisy chain test vehicle typically used to test TLPS paste-filled interposers was repurposed to investigate the concept of simultaneously embedding passive components while also making layer-to-layer interconnections. In this initial construction, two layers of adhesive were used in order to interconnect two circuit layers to complete the daisy chain while also embedding discrete capacitors that were interconnected to one layer of circuitry, but electrically isolated from the other. The capacitors were connected in series with the daisy chain.

Although relief cavities were routed into the laminate to receive the capacitor bodies, the final joint thickness, at 150µm, was far less than the capacitor thickness of 500µm, resulting in cracking of the ceramic capacitor bodies which precluded electrical test. Cross-section analysis demonstrated a robust TLPS paste interconnection between the capacitor terminals and the copper pads, as well as in the stacked via-to-via interconnect between circuit layers.

VI. .FUTURE WORK

The promising interconect results of the initial feasibility study were, unfortunately, stymied by the insufficient routing of the relief cavities in the laminate for the capacitor bodies. The tenting of the overlying prepreg layer at the capacitor bodies as they were pressed into the cavities was an issue as well. Although better routing into the laminate would likely provide substantial resolution to these issues, an alternative build scheme was devised and can be seen in Figure 18.

In this new scheme, a blank laminate of approximately the same thickness as the body of the components is obtained and routed to produce receiving cavities for the discrete passives. As before, prepreg adhesive layers and protective PET film layers are tacked to the joining surfaces, but in this case they are tacked to the interconnect side for the passive devices and to the side of the routed blank that faces the opposing circuit layer. Before the tack step for the routed blank, the components may be placed into the cavities such that, it is theorized, they form a tack bond to the prepreg adhesive that will keep them in place during subsequent handling – perhaps with the assist of a carrier plate on the opposite side.

As before, after tacking, the necessary via holes are laser ablated to create the desired interconnect features. Once ablated, the via holes are filled with TLPS paste, the protective PET films are removed, the solvent is evaporated from the paste and the the layers are booked for lamination.

Aside from the benefit of protecting the components from excessive lamination pressure by providing adequate cavity space, this method would also preserve circuit routing real estate on the circuit layer facing the body of the embedded passive devices.

In the next round of experiments, this method of construction will be explored.

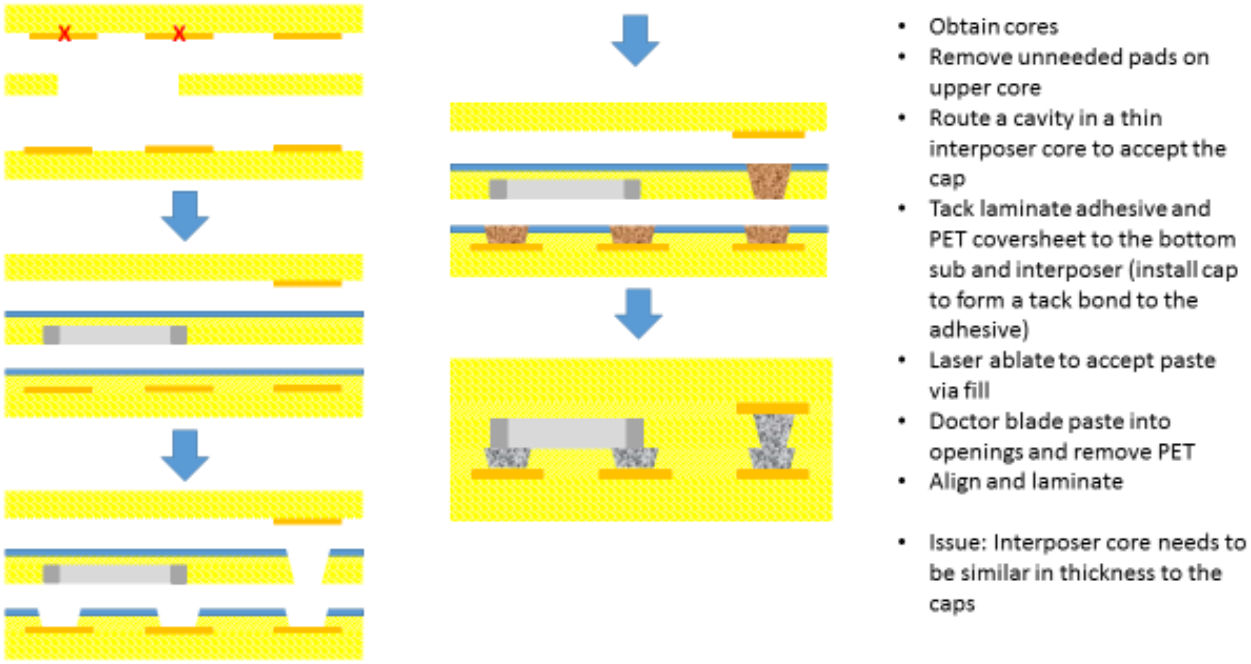


Figure 18: Revised test vehicle for embedding components in a PCB with TLPS paste joining layers

References

1. http://www.circuitsassembly.com/ca/magazine/24540-component-processing-1501.html
2. L. Marcanti and J. Dougherty, “Embedded Passives: Promising Improved Performance,” Circuits Assembly, July 2001
3. Endicott Interconnect

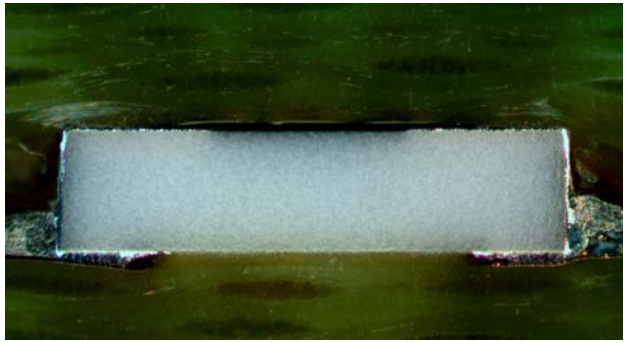
Connecting to Embedded Components Using TLPS Pastes in Via Layers

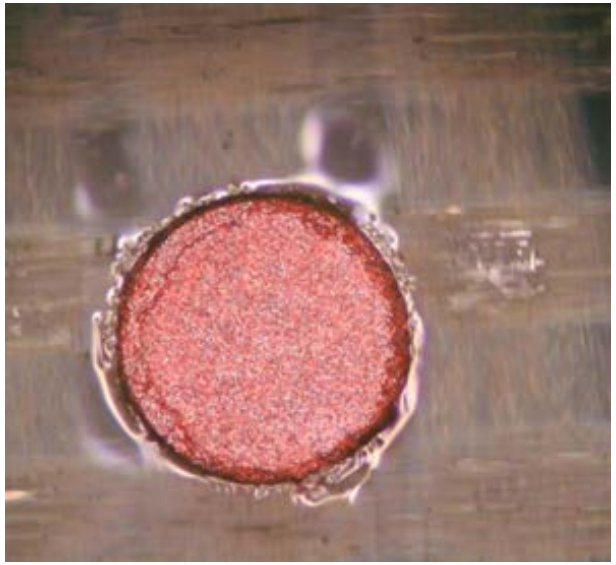
Catherine Shearer

EMD Performance Materials

Introduction

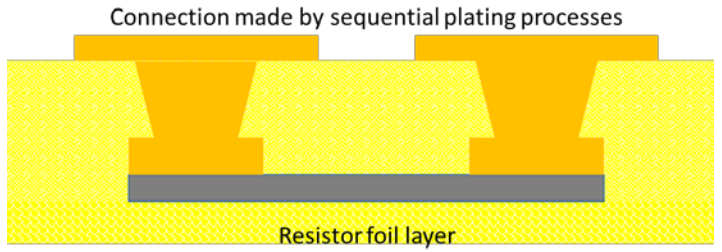
- Embedded passives have long been of interest
  - Freeing top-side real estate
  - Reducing parasitics
- The traditional methods for embedding passives has limitations
  - Embedded layer approaches can have multiple process steps
  - Layer approaches also have limitations in the values that can be achieved
  - It is difficult to embed discrete passives on multiple layers with conventional technology
- Filled TLPS paste vias have been successfully used to interconnect circuit layers in a parallel process
- The parallel-build approach with TLPS vias may provide a path to embedding discrete passives in multiple layers within a PCB
- A test vehicle was developed and an initial feasibility study was performed
- The results and future actions will be reviewed

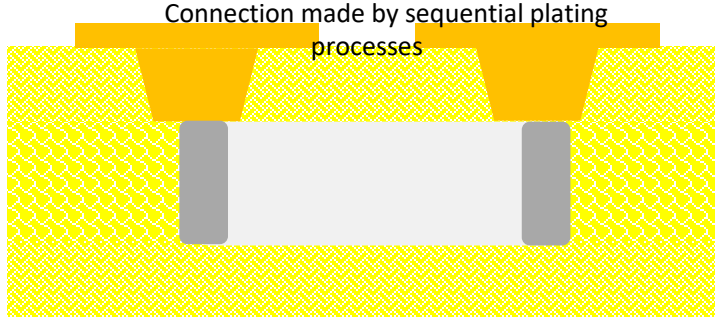




Traditional methods for embedded passives

- Traditionally, embedded passives are incorporated into circuit boards by layer-type methods or by embedding discretes that are interconnected by plated-microvias
- In the layer method:
  - Embedded resistor foils are selectively etched and laser trimmed to achieve the desired values
  - For capacitance, there is a continuous layer embedded with limited ranges available
- In the embedded discrete method:
  - Each layer of embedded discretes requires a layer of plated microvia interconnect
    - Increases the thickness of the PCB
    - Increases the number of lamination cycles required

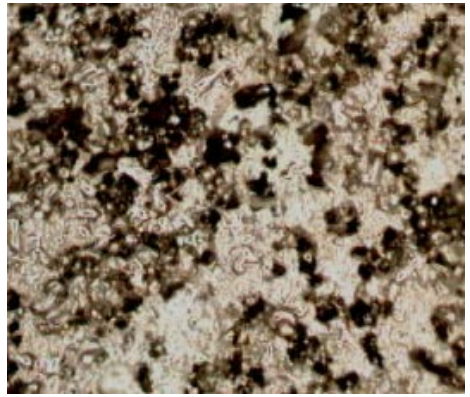




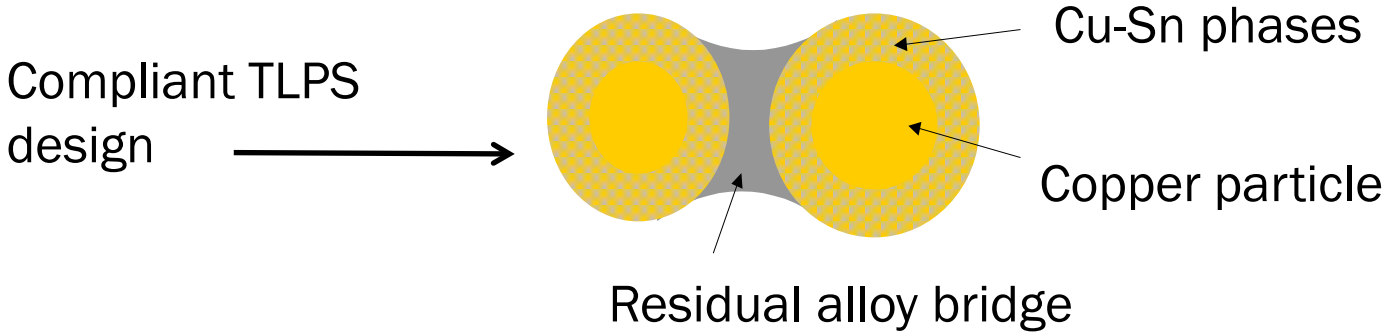
Technology definition: Transient Liquid Phase Sintering (TLPS)

- Copper and tin-alloy particles in a flux mixture
- During a SAC-type reflow the tin-alloy melts and reacts with copper particles and solderable surfaces
  - *Inert environment required (N2, press, vacuum, reducing)*
  - *Pressure not required*
- Continuous metal joint after thermal process
  - *No remelt*
  - *Wide variety of rheologies available*
  - *Electrical, thermal and mechanical properties similar to solders*

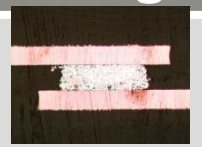
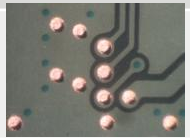
Before reflow



After reflow

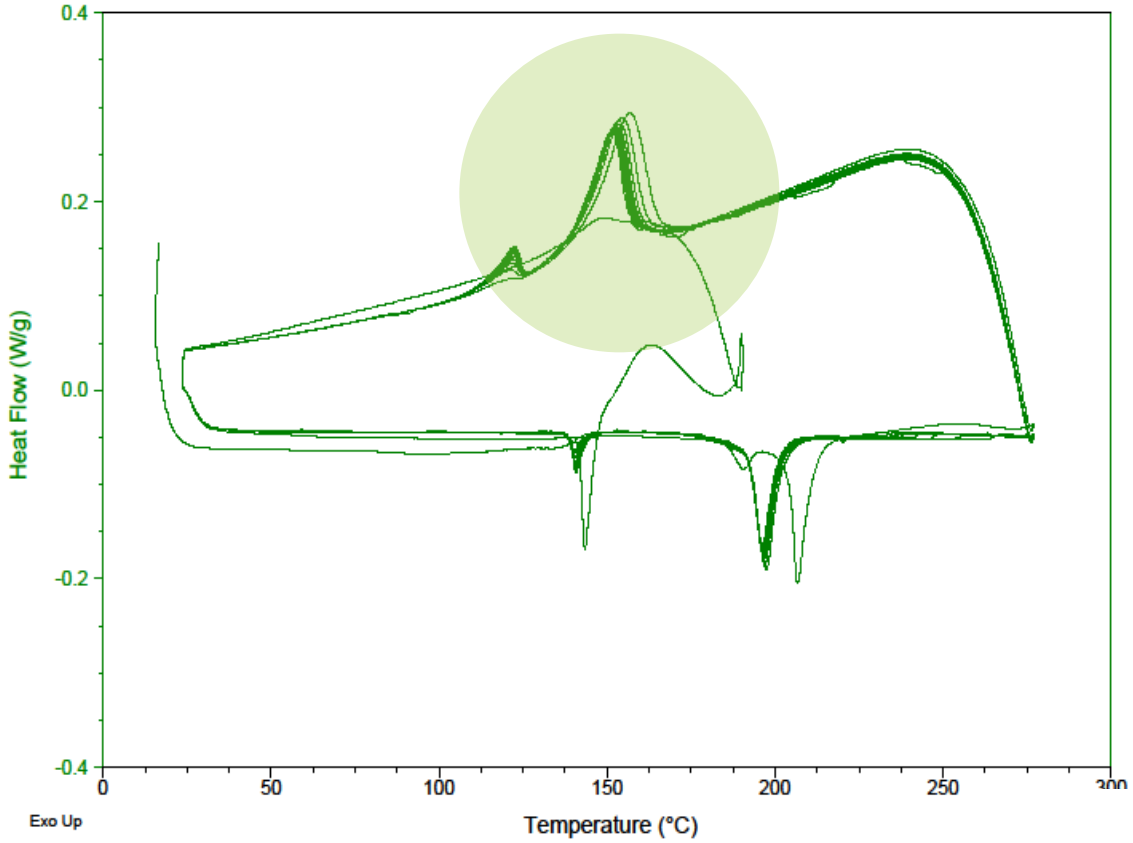


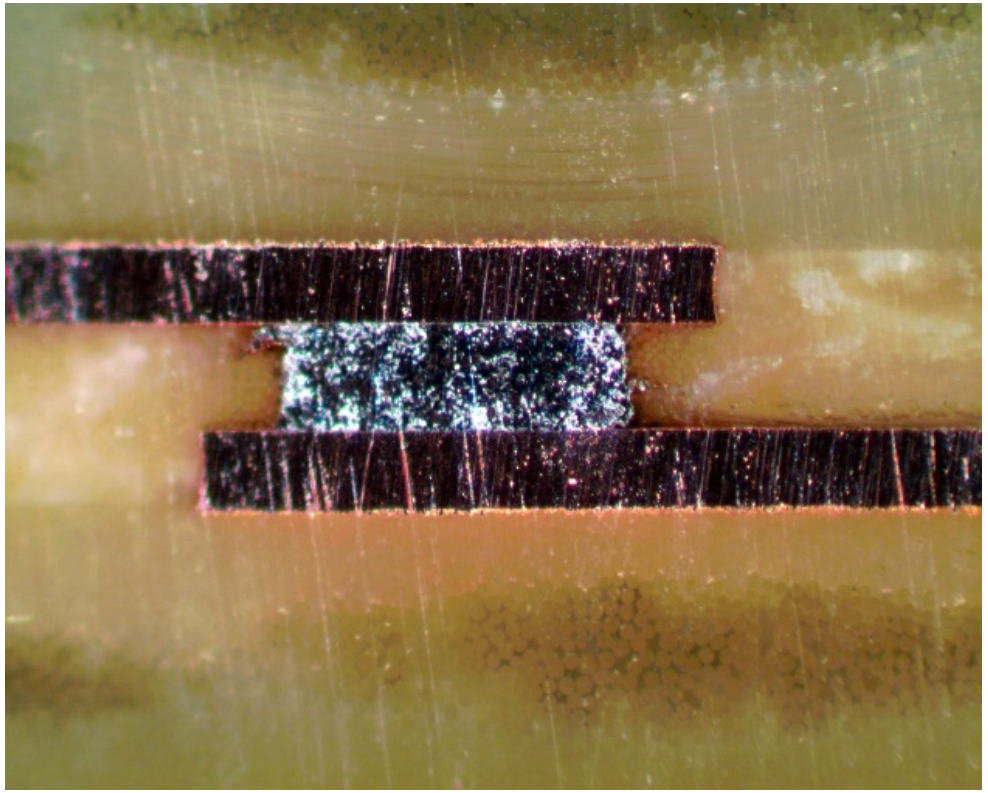
TLPS pastes in a variety of applications

Application	Image
Microvia fill	
Stenciled Interconnect	
Through hole fill	
X-Y Traces	
Component Attach	
Die attach paste	

TLPS pastes have been used for 20+ years in high reliability, high performance PCB applications

TLPS paste joints are highly reliable

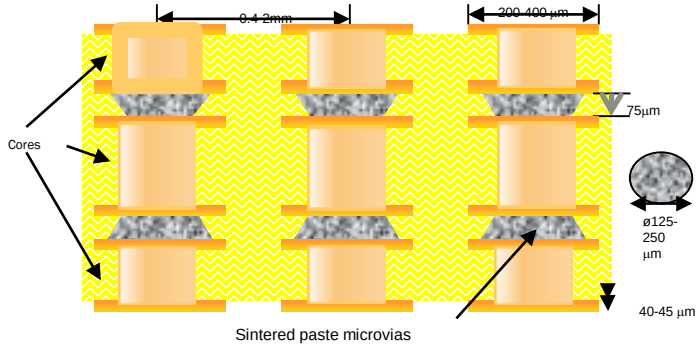


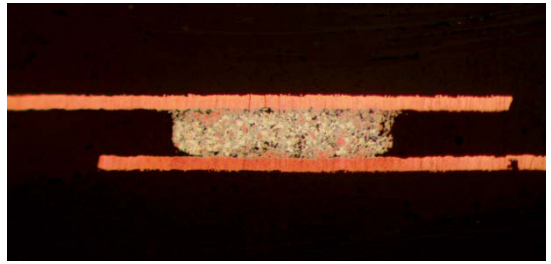


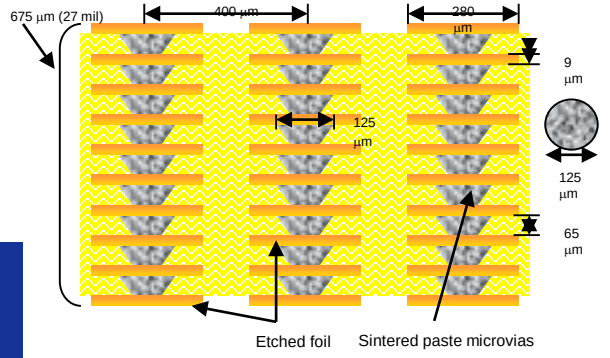
A ductile phase is built into the joint to manage the high CTE in the z-axis

When are TLPS vias typically used in PCB interconnect?

- Electronic devices require that high layer count PCBs are compelling company targets
  - High end computing
  - ATE (test cards)
  - Military applications
- High interconnect density drives high-aspect-ratio PTHs
  - Complex drilling and plating processes,
  - Low yield by conventional processing
- Using TLPS paste breaks up high-aspect-ratio through holes
  - Manufacture subassembly 'cores'
  - Interconnect using paste via layers
  - Proven reliability and good yield
  - Simplified process = lower cost
- TLPS paste vias are a well established solution for the high end PCB market





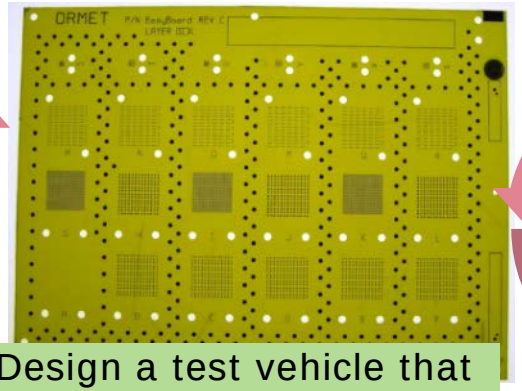


Better performance, shorter cycle time and higher yield than conventional technology for complex substrates

How was the TLPS technology for Z-axis interconnection developed?

Design formulation to satisfy initial key target characteristics

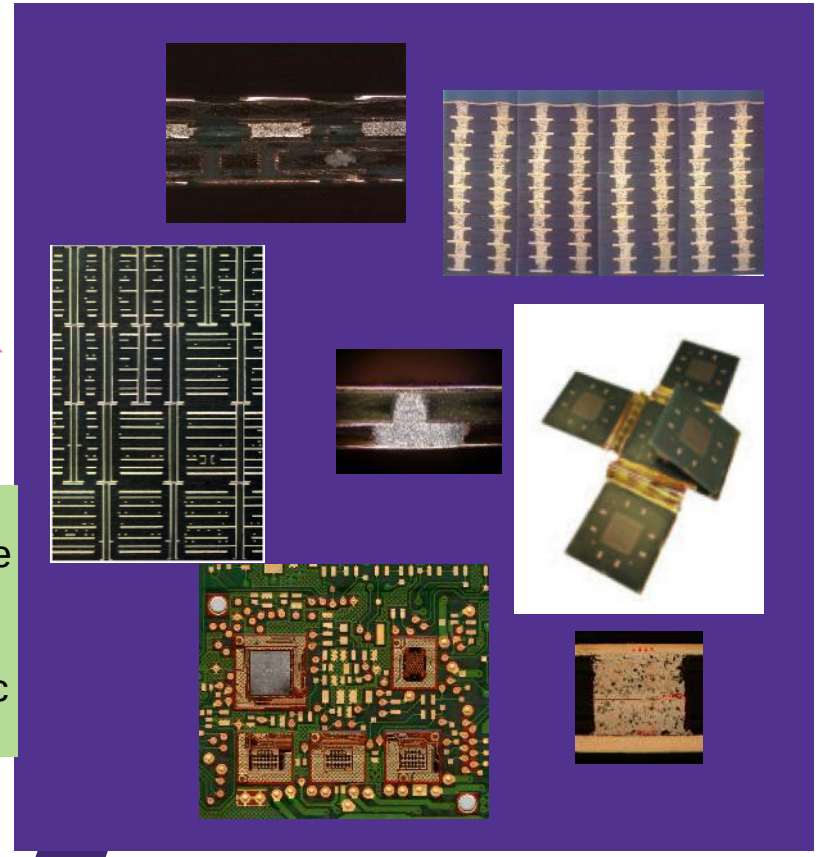
Iterate to clarify and meet key characteristics



Design a test vehicle that captures the key features of the application.

Do not drive development through disconnected materials properties

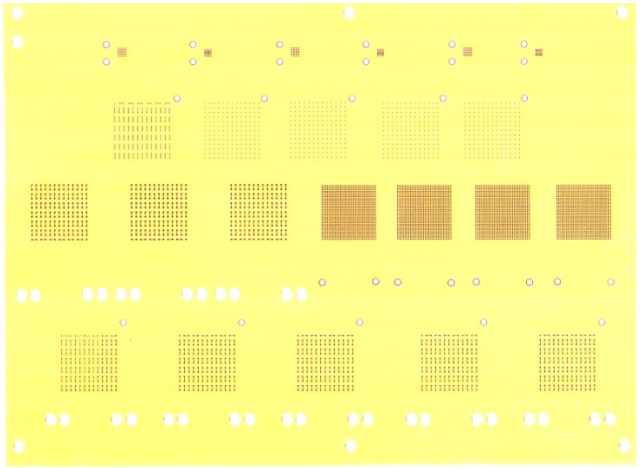
Adapt the test vehicle to resolve key implementation issues on specific applications



Work closely with customers to implement effectively in many different configurations

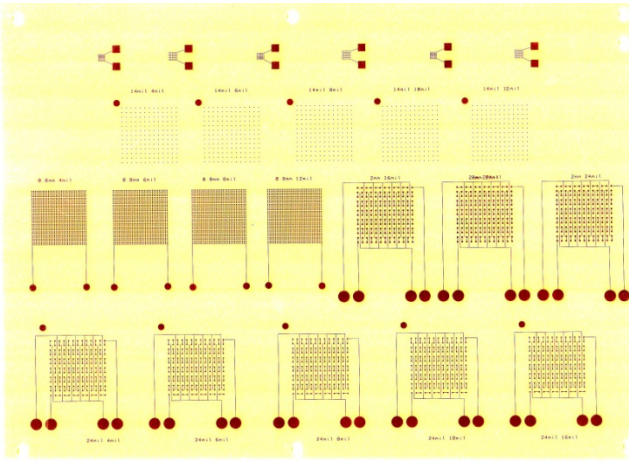
Collect and analyze data to refine key factors and develop improvements/best practices

A daisy chain test vehicle used for development of the TLPS paste via implementation



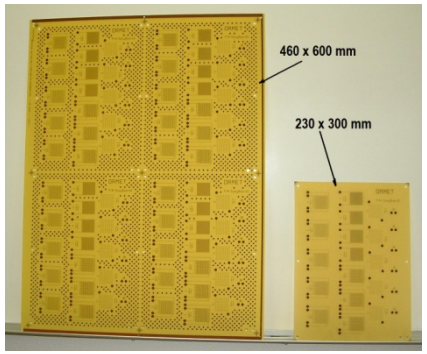
Layer 1 & 2

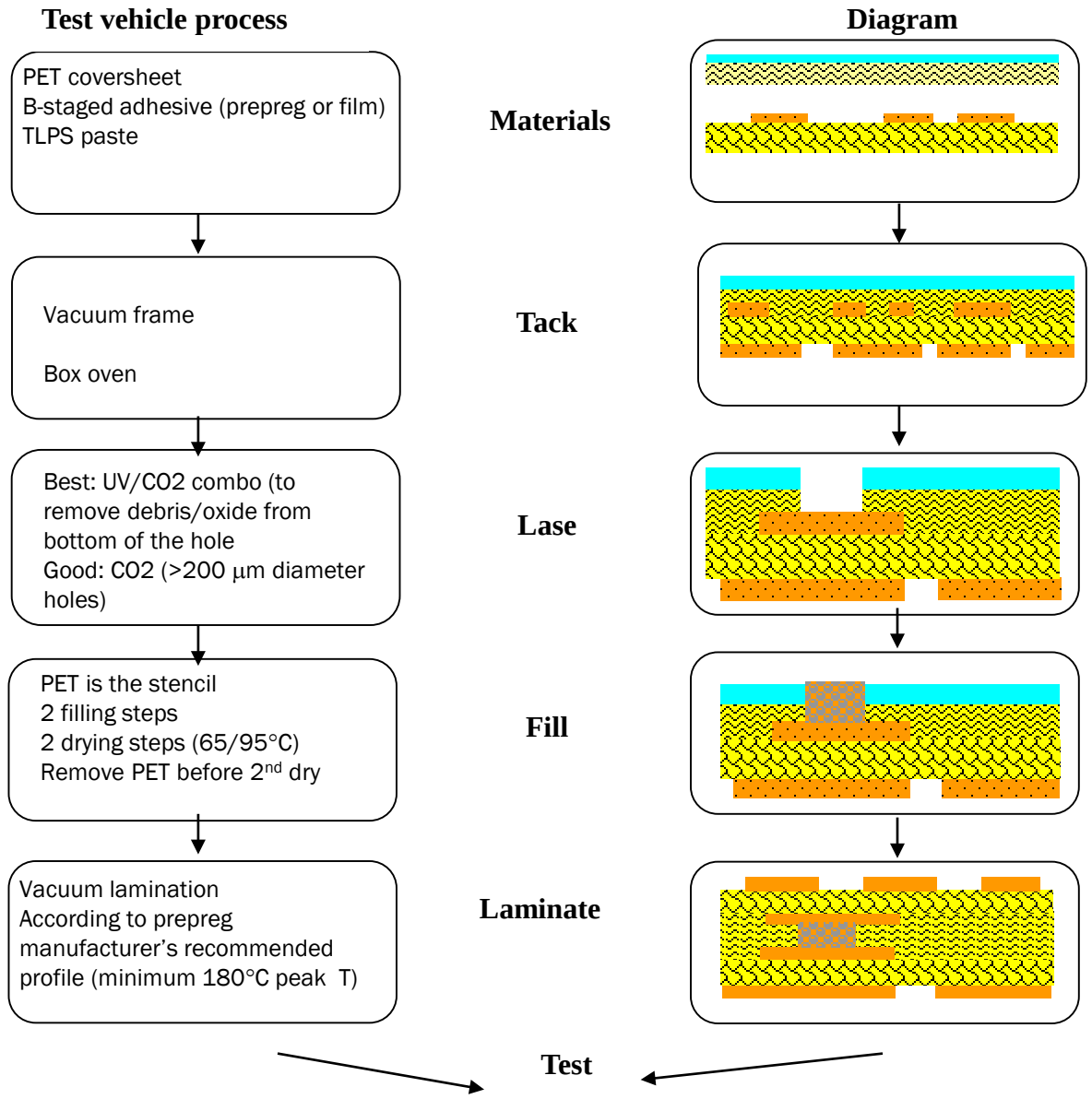
Filled microvia layer



Layer 3 & 4

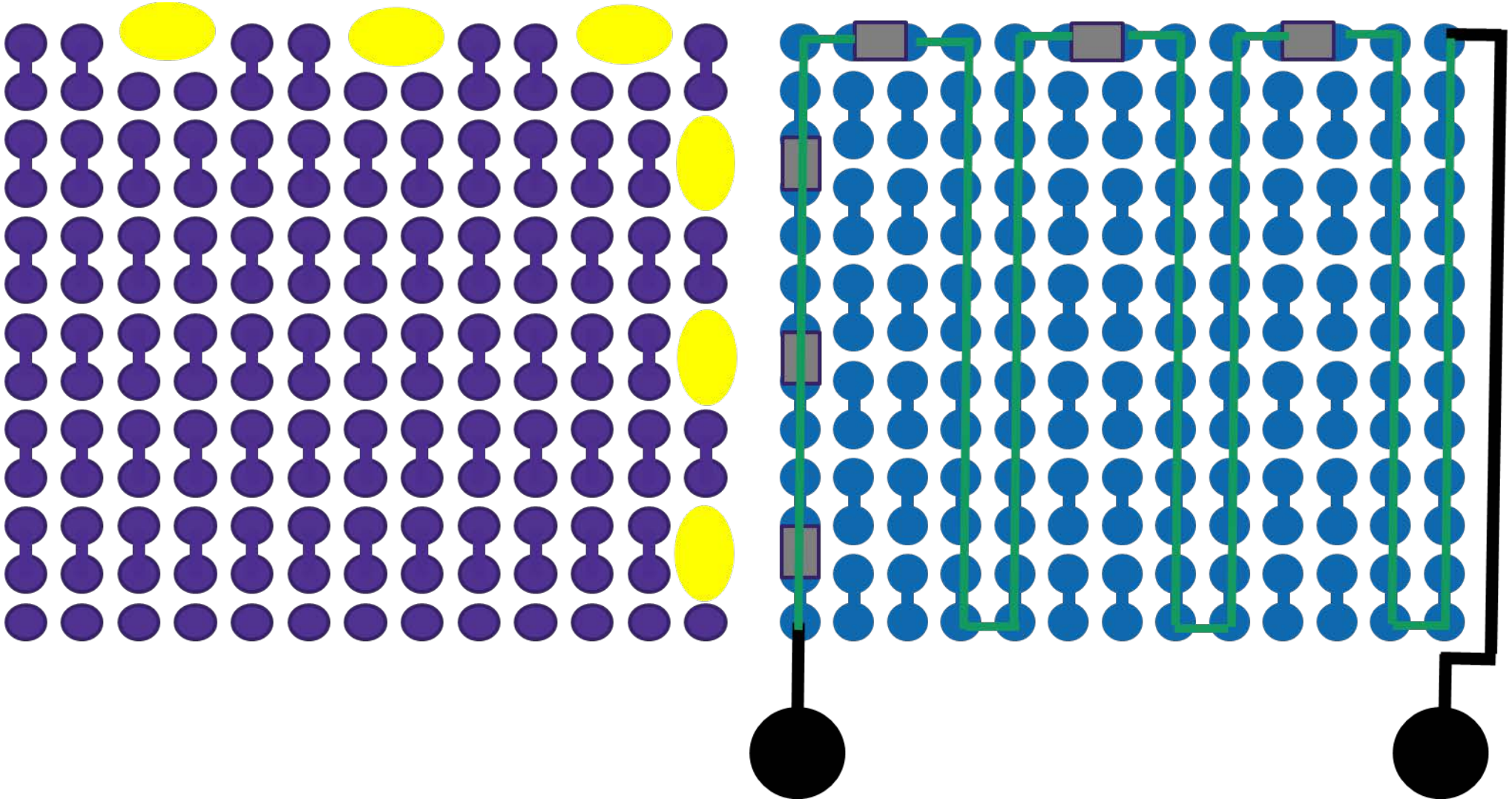
Standard 18” x 24” panel, 9” x 12” board →



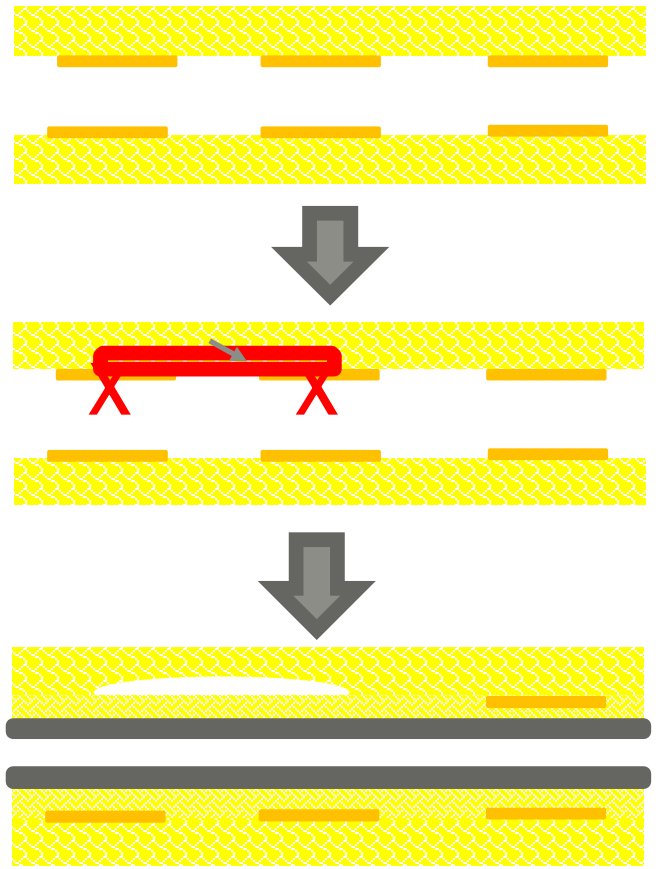


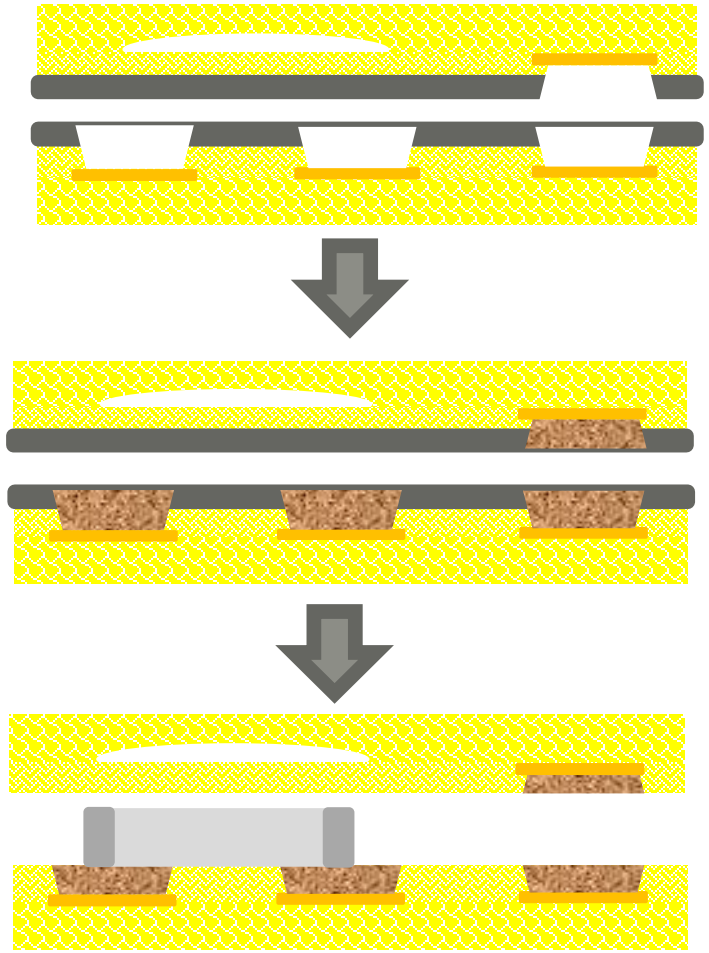
A typical process flow for implementing TLPS paste vias using the daisy chain test vehicle

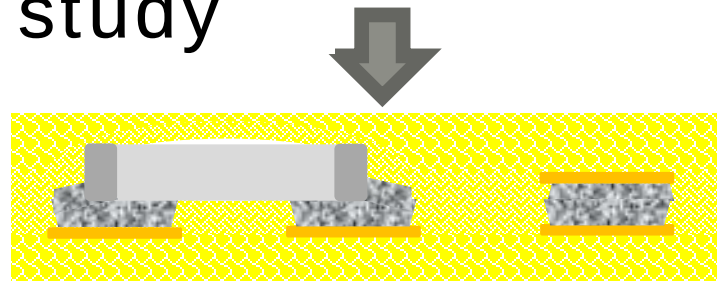
Modifications made to the daisy chain design



The process flow used in the initial feasibility study





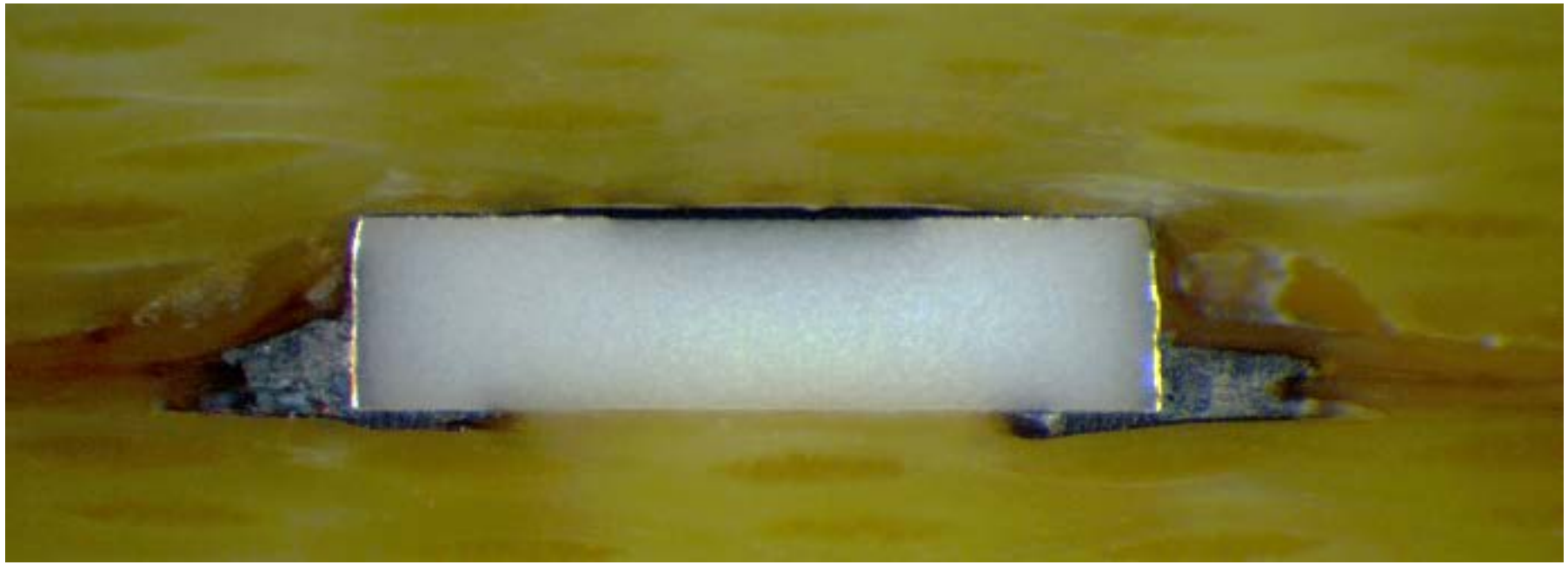


- Obtain cores
- Remove unneeded pads and route relief area for cap body
- Tack laminate adhesive and PET coversheet to both subs
- Laser ablate to accept paste via fill
- Doctor blade paste into openings and remove PET
- Place cap and laminate

- Issue: Relief cut insufficient and deformation around cap body

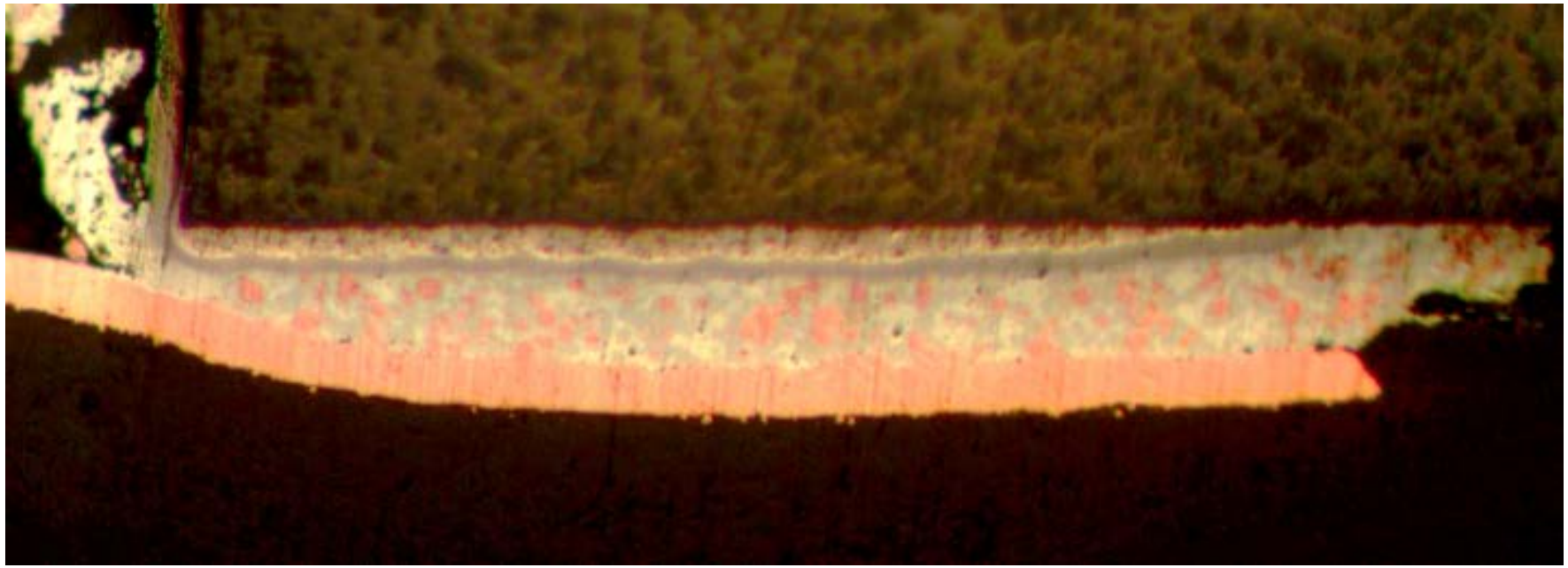
Discrete 0805 capacitors were successfully interconnected in the modified test vehicle

- Cross-sections reveal that good interconnects were formed
  - *The relief area provided for the cap body was insufficient resulting in a localized bulge*
  - *Some of the caps in the series-connected daisy chains cracked and therefore prevented electrical test*



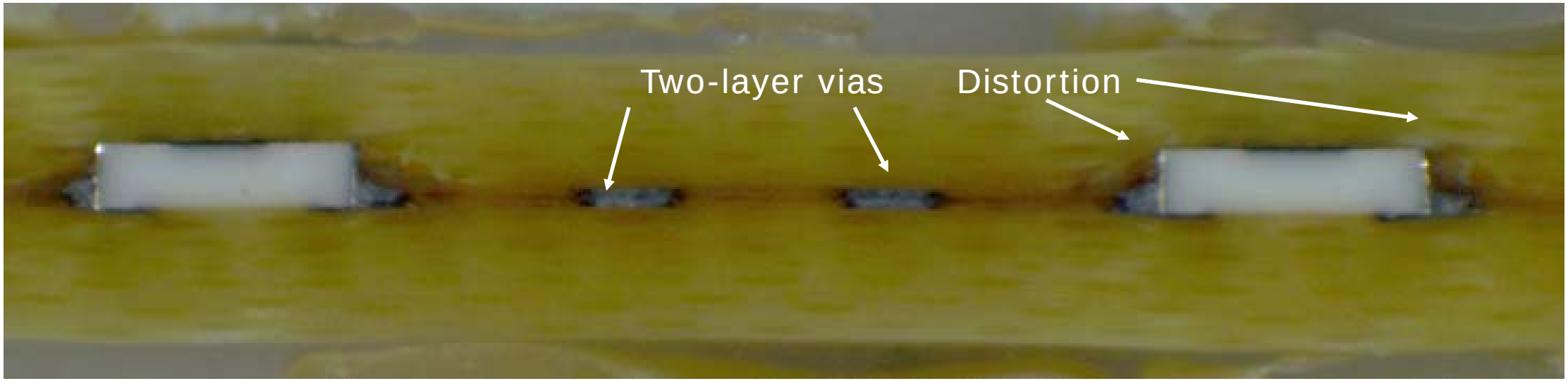
A solid metallic interconnect was formed by the TLPS paste

- A continuous metallic interface was formed at both the tin-plated capacitor termination and to the copper pad
  - *The copper pad has a standard oxide replacement treatment for adhesion to the prepreg*
- The metallic joint is nearly void free

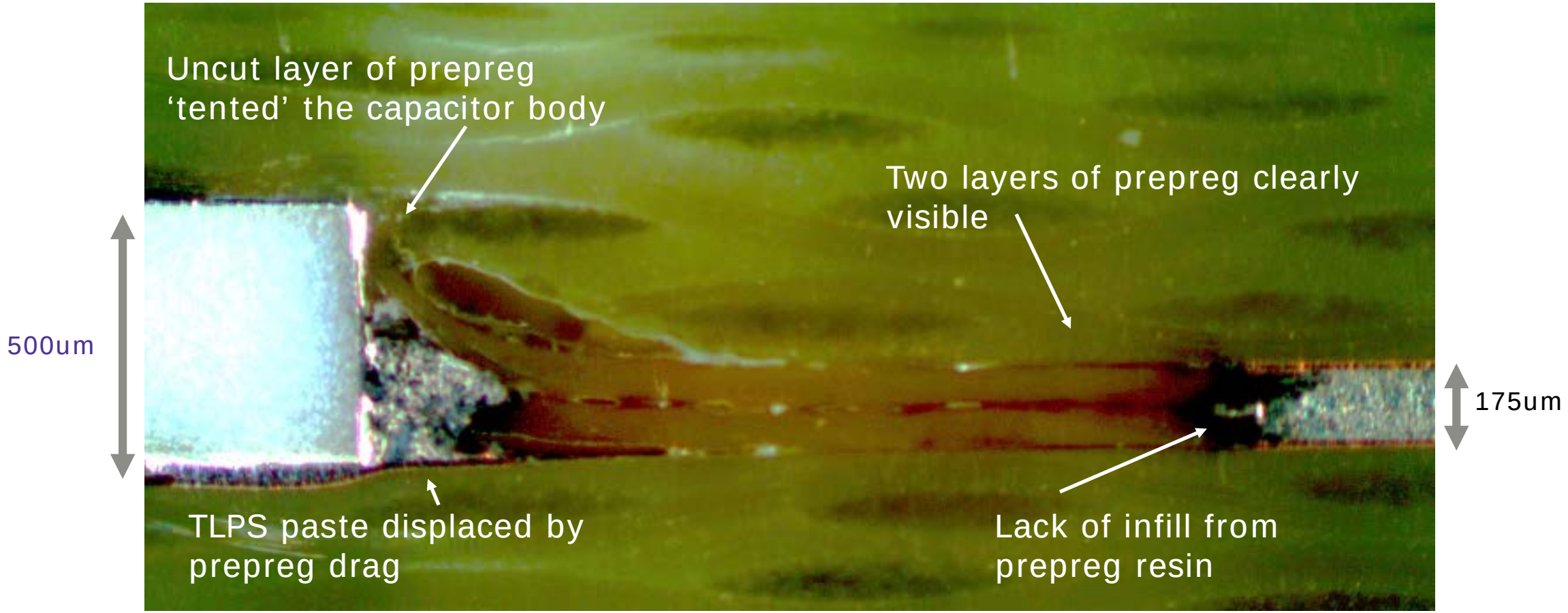


Z-axis interconnects between layers in the PCB were formed simultaneously with the capacitor interconnects

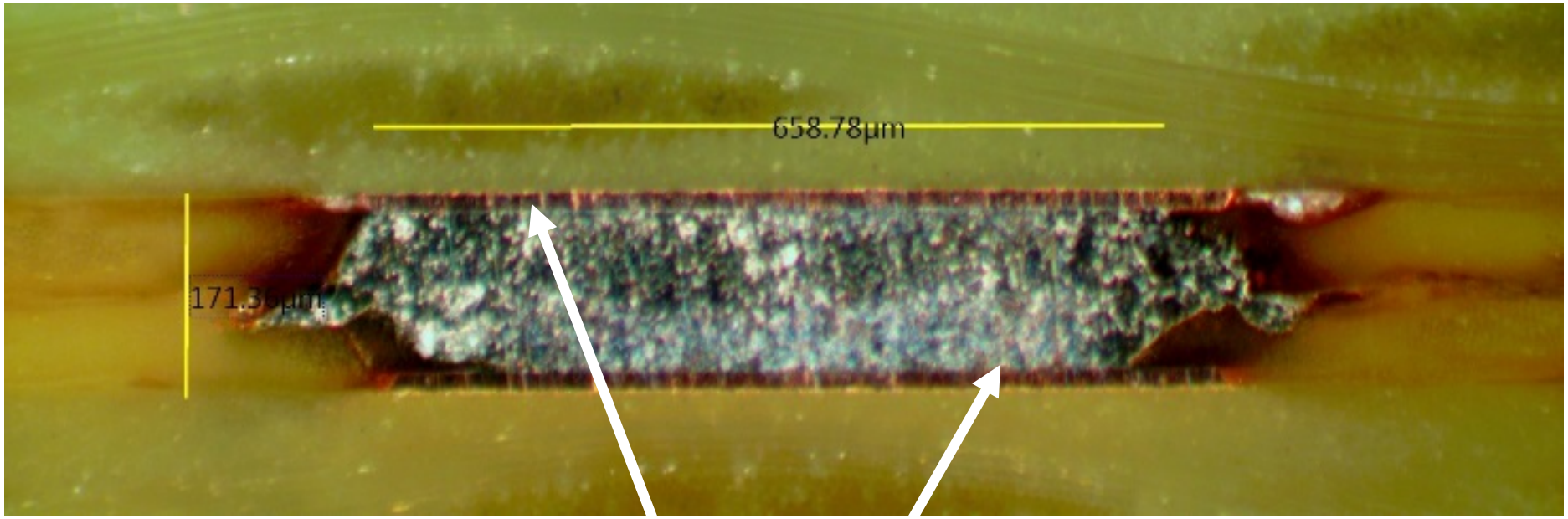
- Despite the localized distortion around the capacitor bodies, the nearby z-axis interconnects were successfully formed



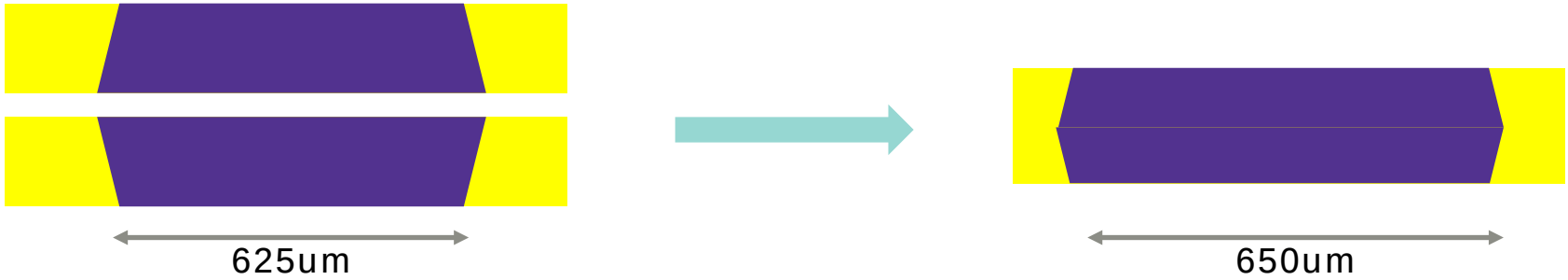
Despite the distortion and lack of in-fill of the prepreg resin, the TLPS joints maintained integrity and sintered well



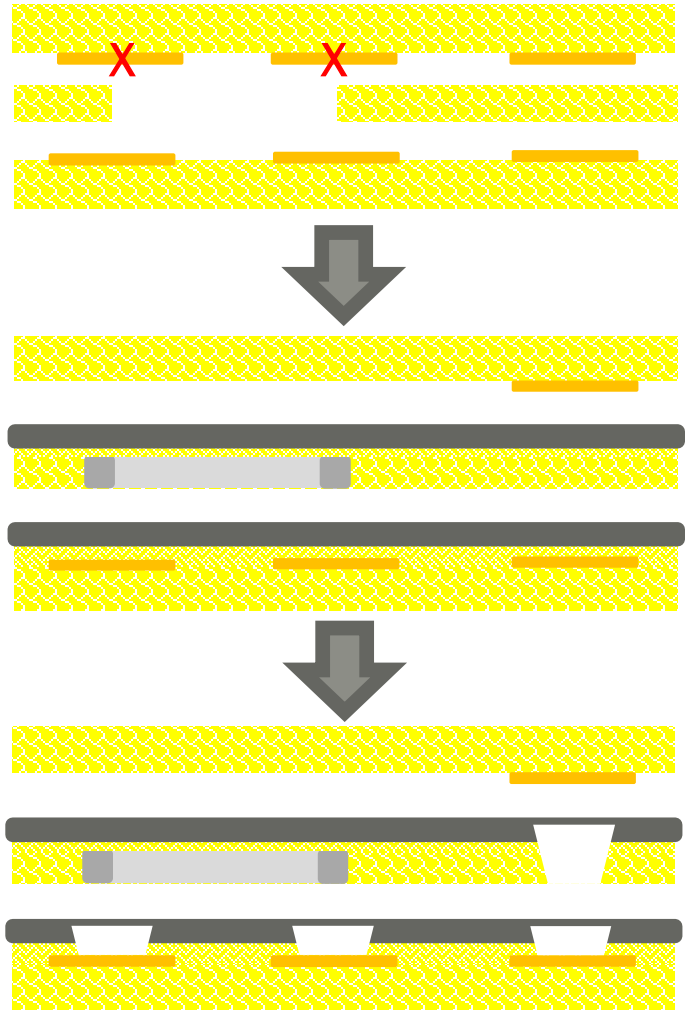
The TLPS paste installed into vias in opposing layers joined to form monolithic structures

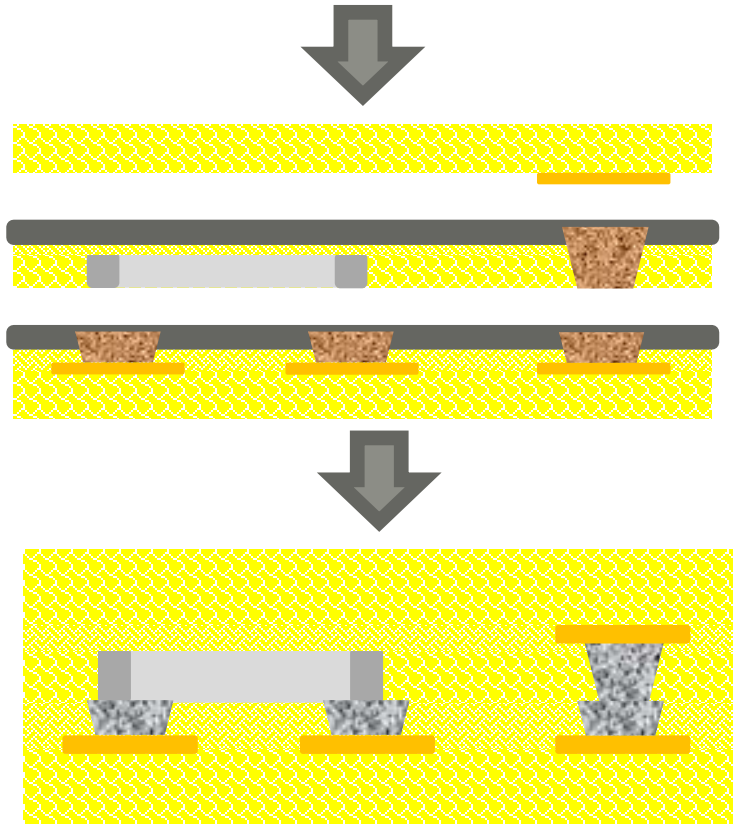


Good retention of via shape, consistent sintering throughout and to both interfaces



Next steps: Repeat the experiment with adequate relief for the capacitor bodies





- Obtain cores
- Remove unneeded pads on upper core
- Route a cavity in a thin interposer core to accept the cap
- Tack laminate adhesive and PET coversheet to the bottom sub and interposer (install cap to form a tack bond to the adhesive)
- Laser ablate to accept paste via fill
- Doctor blade paste into openings and remove PET
- Align and laminate

- Issue: Interposer core needs to be similar in thickness to the caps
- Issue: Will tack-bonded caps stay through handling processes of lasing, filling and lay-up?

Summary

- Embedded passives have long been desired in substrates to free up topside real estate and reduce parasitics
- Existing technologies to embed passives have limitations
  - *Layer types are cumbersome and provide only a limited range of values*
  - *Embedded discretes require a separate interconnect layer and exacerbate the sequential lamination problem*
- TLPS pastes interconnects have been used in z-axis joining operations for over two decades
- The use of TLPS pastes interconnects enables parallel fabrication
- The parallel fabrication strategy can potentially be used to incorporate discrete passives simultaneously with forming z-axis interconnects
- A feasibility study was conducted and simultaneous embedding of discrete passives and formation of z-axis interconnects was demonstrated
- Based on the results of the initial study, a refined embedding scheme has been proposed
- It appears feasible to use this type of methodology to embed discrete components

Thank You!