From leaded to Leadless SMD (DFN) packages. Enabling Automatic Optical Inspection (AOI) for Leadless (DFN) Packages via Side Wettable Flanks

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Abstract
Leadless semiconductor plastic packages (QFN) isa growing package category in terms of market share and diversity. This is also valid for low pin count semiconductors (e.g.: transistors and diodes). Several semiconductor companies offer a wide variety of leadless packages for such products. For small, low pin count products, these leadless packages are known as DFN (Discrete Flat No leads)packages. The diversity of DFN packages is still growing. There are several advantages of DFN packages compared to conventional leaded (SO) packages. A disadvantage is that the quality of the AOI inspection of the solder joint on the PCB is limited because the device terminals are only at the bottom of the products. The best way to inspect the soldering quality on PCB is x-ray inspection. However, especially automotive customers have requested suppliers to find a reliable alternative solution.In response to the requests to enable AOI (Automatic Optical Inspection) capability for leadless packages, side wettable flanks for DFN packages have been invented. With the help of side wettable flanks, a satisfactorywetting with solder during reflow soldering process at SMT can be guaranteed. The resulting solder fillet can be reliably inspected with AOI systems. An additional benefit is that the mechanical robustness on PCB could be improved (e.g.: higher device shear force). This paper describes the evolution from leaded to leadless semiconductor (DFN) low pin count packages. It will includea survey of standard semiconductor low pin count leaded and DFN packages. The realization and boundaries of side wettable flanks will be discussed.Focus is on side wettable flanks for 3 to 6 I/Os DFN packages. Alternatives for >6 I/Os packages are considered: e.g.: "dimple", saw plate saw and immersion Sn plating. Verification of AOI capability as done together with a leading AOI system supplier complete this paper.

Introduction
Even thoughintegration is continuously increasing there is and will be a growing demand for discrete semiconductors. Discrete semiconductors are defined as a single device, for example a transistor or a diode, in a package. However double transistors anddiodes, arrays of devices or a combination of single function chips (e.g. combining transistors, diodes and/or passive devices) arealso considered as discrete semiconductors.

Besides being used for debugging of failures in IC design the main driving factor for discrete semiconductors include:

- Driving high currents
- Dealing with high voltage
- Easier power dissipation
- IC protection against ESD pulses and surge currents
- Flexibility of designing electronic circuits

There is a broad variety of discrete semiconductor packages on the market, including packages with through hole leads. This paper concentrates on SMDpackages. The first SMDpackage which was developed around 1968 was the SOT23 (see figure 1).

Figure 1: SOT23 leaded SMD gullwing package

Over timevarious discrete semiconductor SMD packages with gullwing leads like SOT23 or flat leads like SOD323F (see figure 2) have been introduced. It is expected that the variety of such packages will continue to increase, be it at a slower rate in the future and mainly for medium power applications. However, they are still used in high and growing volume.

Figure 2: SOD323F leaded SMD flat lead package

The application area of leaded packages is for electronic devices which are not typically limited in terms of space e.g. consumer electronics like TV sets, monitors, radios, chargers and so on. Also in automotive applications, the leaded SMD packages are still commonly used because of its proven ease of use and board level reliability. One of their ease of use aspects is the AOI capability after soldering onto a PC board.

Other application fields require a high density of electronic components on PCBs because of space limitation. A good example of this are mobile devices like smart phones. Due to this fact, QFN (Quad Flat No lead) packages with connection pads only on the bottom have been established to reduce the required PCB area by eliminating the leads.These kinds of packages are also used in high volume for discrete semiconductors. The variety (e.g. because of miniaturization) as well as the volume are growing rapidly. Because of their small size and low number of I/Os for discrete semiconductors these packages are named DFN which stands for Discrete (or Dual) Flat No leads. An example of a DFN package is the DFN2020-6 as shown in figure 3. An explanation of the nomenclature of DFN package on the example DFN2020-6 is as follows: “2020” is the nominal x and y dimension, in this case 2.0 mm x 2.0 mm, the “6” means 6 I/Os.Because of its compact design DFN packages incorporate more advanced SMT technology compared to leaded packages. This technology is already widely established in the industry. A disadvantage in respect to ease of use of QFN/DFN packages is that the solder connection quality can only be fully inspected by x-ray, because the solder connection is only underneath the plastic body of the package.

Figure 3:DFN2020-6 as example for DFN packages

At this point it should be mentioned that because of space limitations, other packaging technologies have also been invented. For example, CSPs (Chip Scale Packages) which have either solder balls (also known as flip chip or WLCSP=Wafer Level

Chip Scale Package) or flat contacts (DSN packages =Discrete SiliconNo leads). These kinds of package usually come without a plastic body. The trend for this package categoryis that they will get a plastic protection at the side walls for some advanced applications. Beside the examples in figure 4 & 5 and some further remarks they are not in the scope of this paper.

Figure 4: Example of a WLCSP with solder balls

Figure 5:Example of a DSN diode package with flat contact pads

To complete the introduction of the DFN package and the variety of packages available, a package portfolio offered by a semiconductor standard product manufacturer is included in figure 6.

Figure 6: Extract of discrete semiconductor package variety

From leaded to Leadless SMD (DFN) plastic packages

As already mentioned in the introduction, leadless DFN packages are becoming ever more important to realize growing electronic functionality in compact devices. This section will focus on the driving factors for evolution of packages from leaded SMD to leadless DFN packages and on the advantages of DFN packages. The overall driving factor is space limitation. The primary driver is area but height can also be on major concern.As a first step, height reduction was the motivation to go from gullwing SMD packages to flat lead SMD packages. Due to the shorter distance from chip to PCB solder point, the package's thermal resistance could also be somewhat reduced with this package design. The next step in height reduction was made by implementing DFN packages. In addition, DFN packages also have the advantage of further reducing the distance from chip, which is the source of power dissipation/heat, to the solder connection,because the chip is directly positioned above the solder pad. Only the leadframe and die attach layer are between the PCB solder connection and the chip. With that the thermal path is reduced to a minimum. In addition, it is possible to maximize the size of the heatsink (solderable metal area) under the package. Figure 7 illustrates the evolution from a leaded gullwing package to a leadless DFN packages. In this context, it should be noted that theintroduction of CSP (DSN) packages has been the nextstep in the evolution. Besides the obvious advantages of DFN packages there is one drawback which is that the AOI inspection of solder connection is limited because the solder pads are only at the bottom of the package.

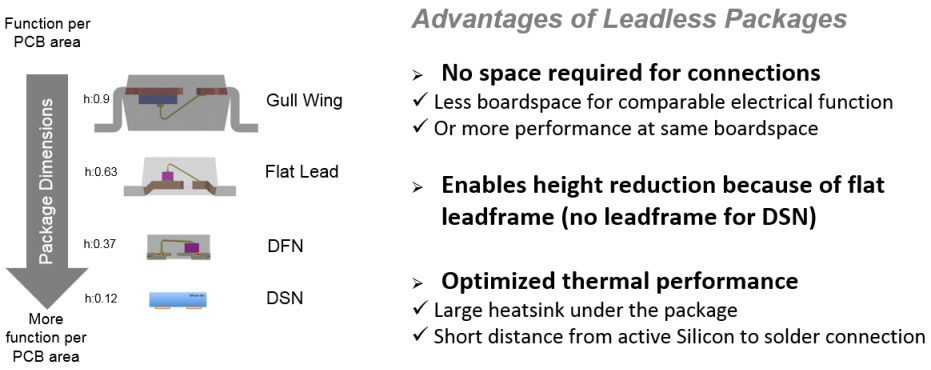

Figure 7 : From leaded to leadless packages

Construction and Manufacturing of Discrete Semiconductor Plastic Packages

In this section a description of themanufacturing process and an explanation will be given as to why the lead tips of leaded SMD packages and the side flanks of DFN packages are usually not plated with a metal layer which ensures solder wetting. The production flow of leaded semiconductor packages is based on a leadframe. The leadframe is made froma Cu alloy or NiFe material with Cu plating. It has several functions: It acts as a carrier for transport in production, as connection for chips and wire,and a part of it builds the leads of the final package. After the chip attach and wire bond the body of the package is created by epoxy plastic encapsulation of the chip and leadframe part which is inside the package. That means every package is formed by an individual cavity in the mold tool. The next production step for the packageis to have the leadframe electro galvanic plated with tin (Sn). This tin layer prevents the underlying metal, e.g. Cu, from oxidation and so guarantees a surface which is wettable by solder pasteduring the soldering process. Finally, the single packages will be separated by punching (trim) the leads out of the leadframe. Since the leadframe tin plating is done before singulation of the packages, the lead tips are not covered with Sn. Figure 8 illustrates the production process flow by example of reel to reel package assembly.

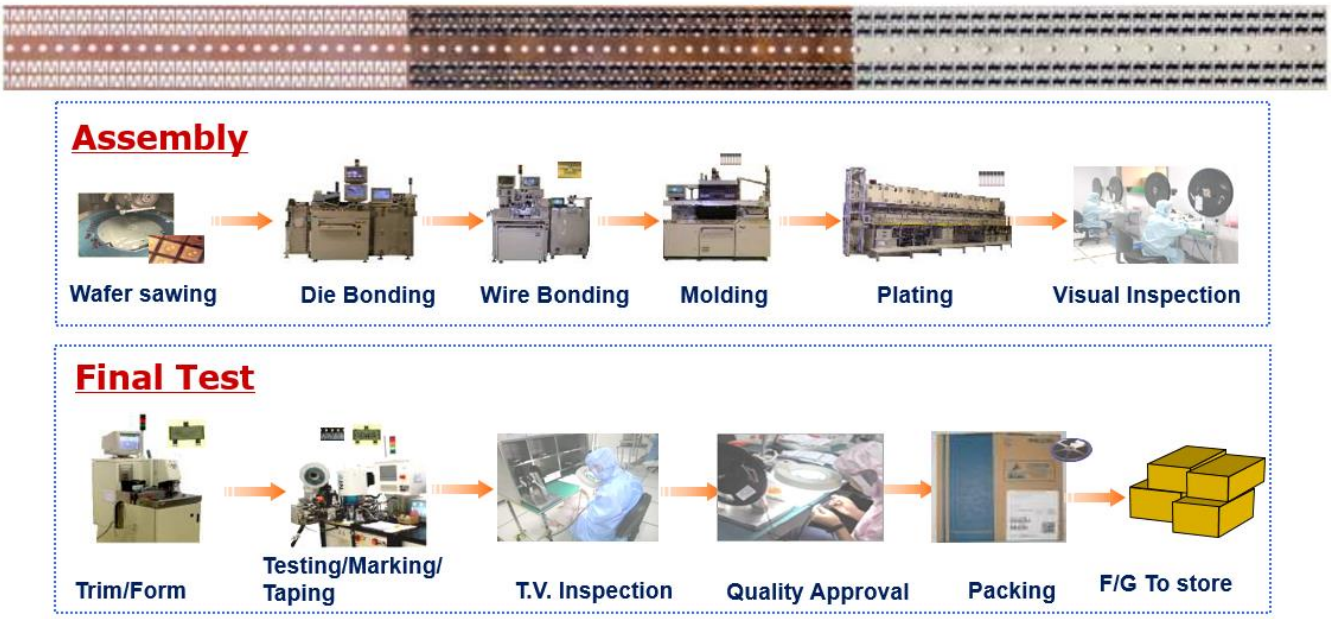

Figure 8:Discrete semiconductor assembly flow, example reel to reel production

DFN packages are assembled in a similar manner as leaded packages. However, a map (or group) of several products are molded with epoxy plastic in one shot. All QFN / DFN package leadframes consist of Cu alloy base material. A lot of them are plated with a NiPdAu layer stack which is already applied by the leadframe supplier and which guarantees an oxide free surface for chip attach, wire bonding and, on the connection pads, for wetting with solder. Optionally, the NiPdAu layer may be left as is or plated in addition with tin. Singulation into individual packages is done by blade sawing. In case tin is applied the singulation is done after electro galvanic tin plating.As a remark, the same diamond coated sawing blade used for wafer dicing are used for package singulation.Figure 9 shows two leadframe strips with four maps each which are molded in one shot and the principle of sawing singulation into individual packages. Of course, in this case Sn plating of the side flanksof the bottom padswhich are exposed after sawing singulation is not possible. The material of the side flanks of the DFN package pads is Cu alloy (leadframe base material) which may oxidize and so a wetting with solder in the reflow soldering process depends on storage condition and duration of the products and cannot be guaranteed.

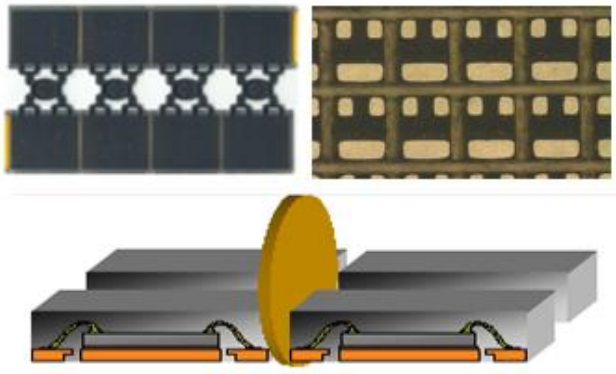

Figure 9: Mold maps and singulation of DFN packages

Side Wettable flanks to provide guaranteed solder wetting of side pads for low I/O DFN packages

To overcome the disadvantage thatthe solder wetting of the side flanks of DFN packagesis not guaranteed, a solution has been developedto also cover the side flanks with plated tin in the same electro galvanic plating step as used for the bottom pads [1].This technique is only applicable for DFN packages with up to four pads (can be more if multiple pads are fused to each other) and the pads need to be on two parallel opposite sides of the package. A plating of the pad´s side flanks on all four sidesof a DFN package is not possible with this method. The method relies on the fact that the solder pads of the

individual packages are connected by metal features,which are perpendicularto the I/O pad flanks, to the leadframe. These metal features will be separated at final singulation step. As example of a DFN package with wettable flanks refer to figure 3 and for detail view see figure 10 and figure 11.

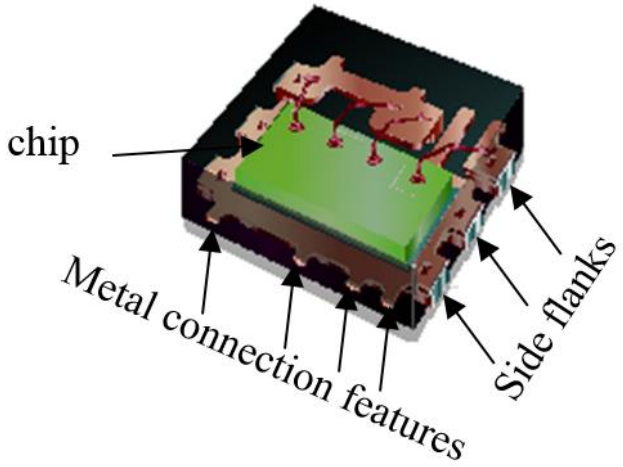

Figure 10: Transparent view of DFN2020-6 package

Figure 11: Detail view on side wettable flank feature of DFN2020-6 package

With the full tin-plated side wettable flanks it is guaranteed that the complete side pad surface will be wetted with solder during the reflow soldering process. An important advantage is that the plating layer on the side flank is as thick as on the bottom pads, which is around 10µm. With that a wettable surface can be guaranteedeven after long periods of storage. Two examples of optical appearance of side flanks after soldering are shown in figure 12 for a DFN2020-6 package with and without side wettable flanks and in figure13 for the two-pad DFN1608-2 package.

Figure 12: Example DFN2020-6 comparison of SWF versus bare Cu side flanks after soldering

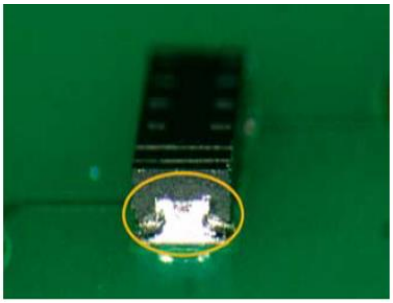

Figure 13: Example DFN1608 appearance of side wettable flanks after soldering

The height of the side wettable flanks of a DFN package which are plated with this method depends on the leadframe thickness. Usual leadframe thickness for DFN packages with a package height of h≥ 0.5mm up to 0.65 mm is 127µm (=5 mil) and for packages with package height h< 0.5mm it is 100µm (4 mil). The height of the side wettable flanks is higher than the leadframe thickness because some Cu burr will occur at sawing and this burr and the Sn plating thickness of the bottom pads will add to the height. Refer to the cross-section figure 14 for details.

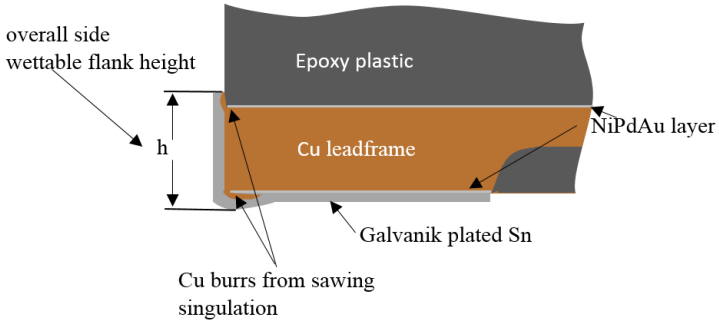

Figure 14: Height of side wettable flanks

Based on the explanation above the wettable flanks meets the requirement of a minimum height of 100µm as raised by some automotive customers [2].

AOI capability of low pin count DFN packages with side wettable flanks

The main purpose of the side wettable flanks is to enable a reliable AOI capability for DFN packages. Thus, the costly x-ray inspection process can be skipped.

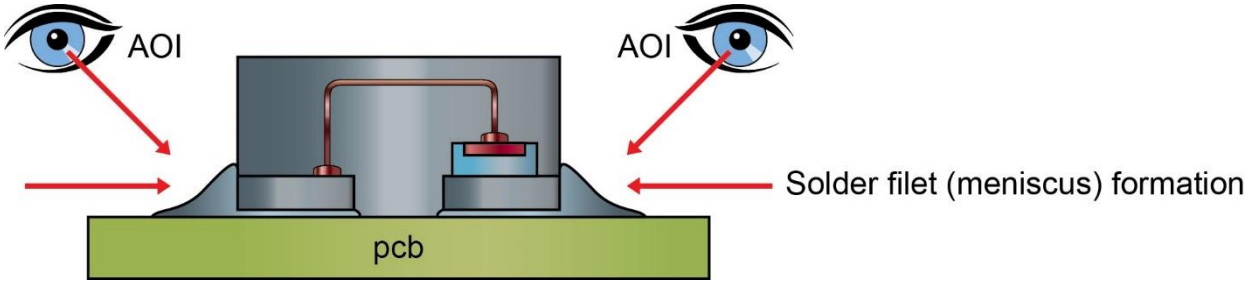

Figure 15 : AOI enabled DFN package with Side Wettable Flanks (SWF)

A boundary which needs to be considered is that the PCB solder pad size must be extended to be larger than the package dimension to give some space for the solder to build a meniscus or filet. The solder footprint recommendations of suppliers which offer packages with side wettable flanks include this extra space.

The effectiveness of the side wettable flanks for AOI inspection has been proven together with a leading AOI equipment supplier by evaluation of soldered DFN device equipped with SWF in comparison to corresponding DFN packages without

SWF. Multiple test boards were built on which the footprints were modified to accommodate the SWF package. The printed solder paste volume has been modified on purpose. E.g. on some PCB solder pads no solder was printed (see example figure 16). It could be confirmed that the DFN packages with SWF are suitable to reliably identify soldering failures with AOI on PCB after reflow soldering [4].

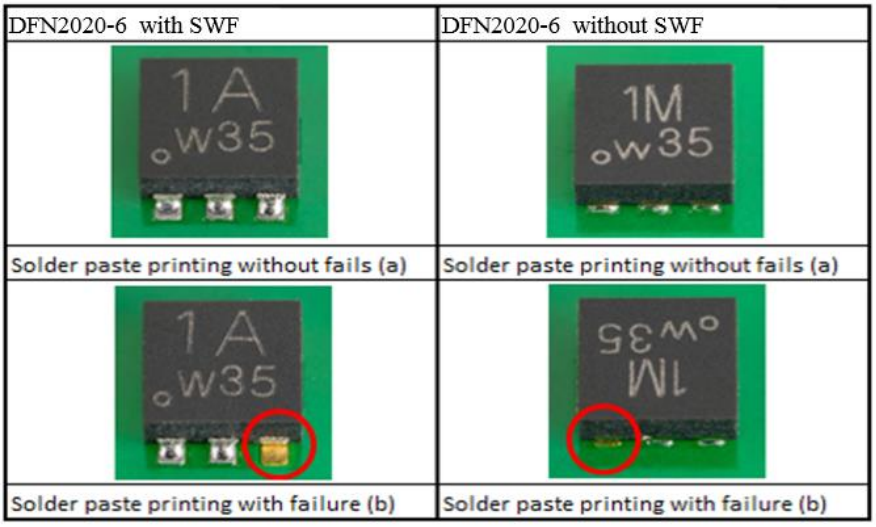

Figure 16: Example of solder failures on test board

Additional benefits of low pin count DFN packages with side wettable flanks

An additional benefit of side wettable flanks is that the mechanical robustness of the PCB bond is improved compared to DFN packages without SWF. For a survey of advantages refer to figure 17.

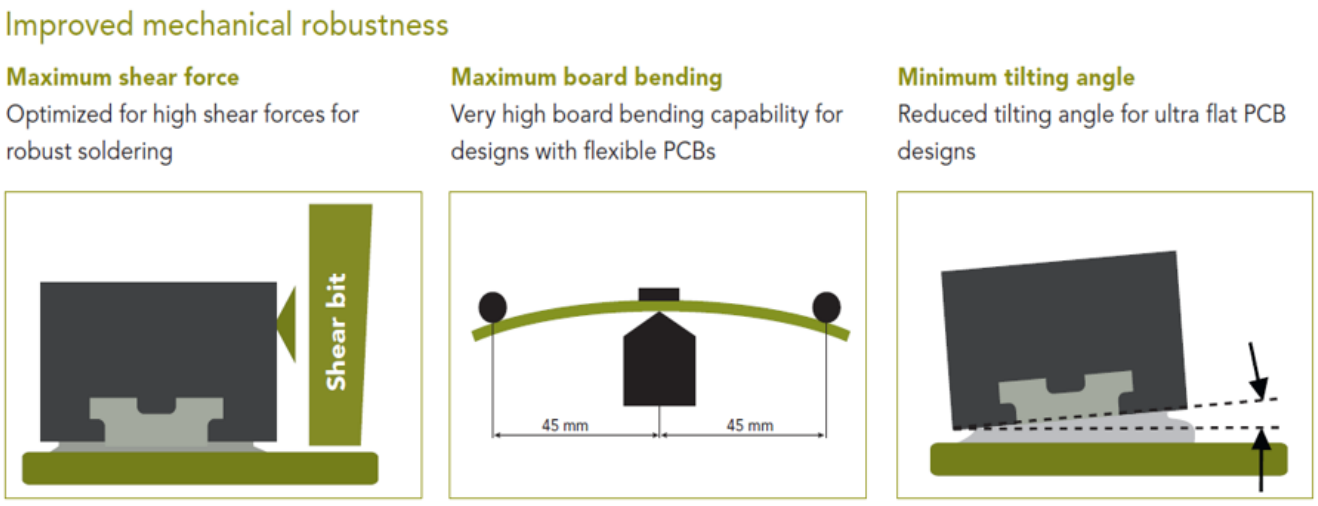

Figure 17: Board level robustness improvements of DFN with SWF

The shear force required to dislocate the package off the PCB is increased due to the meniscus that is formed after soldering.Shear force data for a DFN2020-6 package with and without side wettable flanks have been collected. Overall 80 samples each had been sheared on the PCB after soldering. The result is that shear force could be improved by about 10% with side wettable flanks as well as a reduction of the standard deviation of the shear values was observed. Refer to figure 18 for details. Important for a solid comparison is that the footprint, stencil apertures and solder paste type for both package variants are the same. The shear direction and height of the shear bit needs to be kept the same for all tests as well.

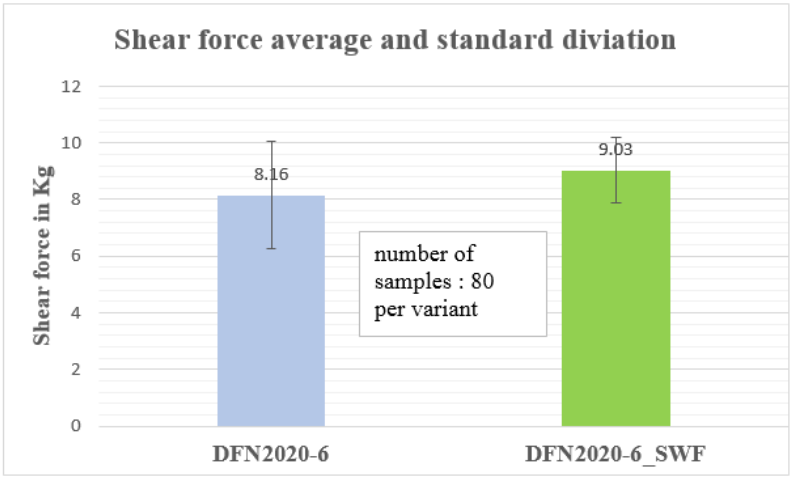

Figure 18: Shear Test on PCB for a DFN2020-6 package with and without Side Wettable Flanks (SWF)

The board bending test robustness could be optimized as well, which is given by additional features at the package solder pads to achieve a better anchoring to the plastic body. For verification board bending tests were performed for DFN1006-2 packages with and without side wettable flanks. Over time 120 board bend test results per package variant following IEC60068-2-21 have been gathered. Because tests were done at different times the impact of process and material variations are eliminated. Summarizing all the data it could be proven that board bending depth for the DFN1006-2 package with SWF is up to 14 mm. For the data as displayed in Figures 19 and 20 the number of package cracks after board bending have been counted. Electrical testing of all samples are still pass even though the packages show cracks. Already tiny cracks as shown in figure 21 are counted. The bending robustness of both DFN1006-2 package variants is > 4mm and with that the package robustness is better than for passive chip components of same size for which the bending depth is often specified with 1mm.

Row Labels	Sum of Qty	BBT 4mm	BBT 8mm	BBT 14mm
DFN1006-2				
2016Q1	20	0	4	18
2016Q2	20	0	20	20
2016Q3	20	0	10	20
2016Q4	20	0	9	17
2017Q1	20	0	0	0
2017Q2	20	0	11	20
DFN1006-2 Total	**120**	**0**	**54**	**95**
DFN1006-2_SWF				
2016Q1	20	0	0	1
2016Q2	20	0	1	8
2016Q3	20	0	0	0
2016Q4	20	0	0	0
2017Q1	20	0	1	6
2017Q2	20	0	0	0
DFN1006-2_SWF Total	**120**	**0**	**2**	**15**

Figure 19:Board Bending Test (BBT) results (=number of package cracks) of DFN1006-2 with and without Side Wettable Flanks (SWF)

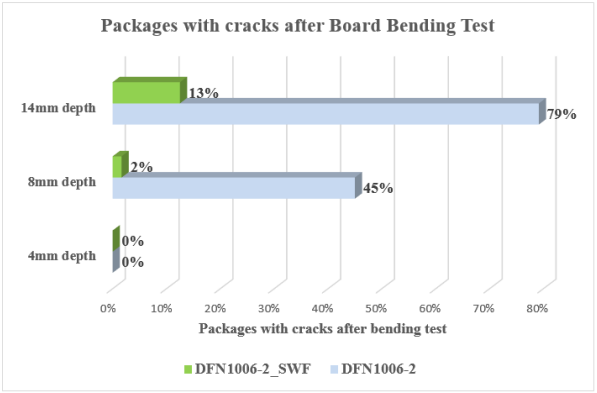

Figure 20:Board BendingTest result DFN1006-2 with and without Side Wettable Flanks (SWF)

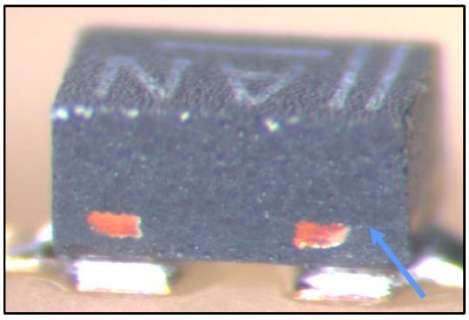

Figure 21: Example of plastic body crack after board bending

An advantage mainly relevant for 2 I/O DFN packages with side wettable flanks is that the tilting after soldering is reduced. In figure 22 is an example of package tilting angle of DFN1006-2 packages with and without side wettable flanks. It should be mentioned at this point that for a proper comparison the solder volume needs to be controlled carefully to be the same for both package variants. Otherwise this will be easily the dominating factor for tilting.

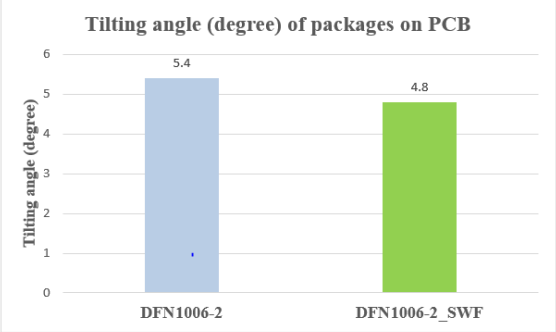

Figure 22: Tilting angle on PCB of DFN1006-2 packages without and with Side Wettable Flanks

Alternative Side Wettable Flank solutions for DFN packages with more than 6 I/Os

One alternative is to use dimples on side pads for DFN/QFN with multiple I/Os and leadframe thickness of ≥ 200µm. Dimples are already etched and NiPdAu plated together with the bottom pads at the leadframe supplier. Sawing singulation is done between two adjacent packages in the middle of the etched dimples. The wettable feature size formed by the dimples is smaller than for the galvanic tin plating solution described previously. Usually packages with SWF made in this way will be delivered with NiPdAu pad plating, that means without additional tin plating on the pads. Figure 23 gives an example of such a package without, on the left, and with the dimple feature, on the right picture.

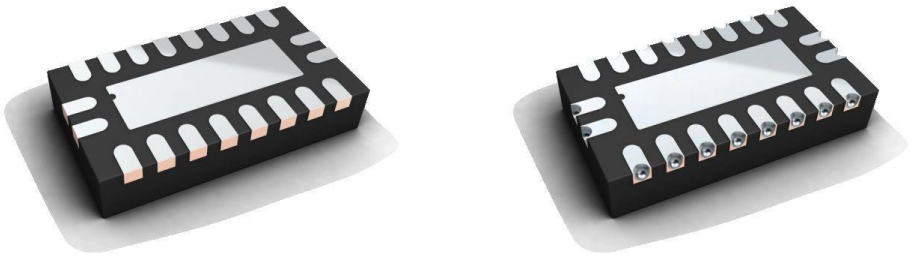

Figure 23: Example of multi I/O DFN/QFN package with dimples to achieve wettable flanks

Another alternative is partial sawing of the DFN packages prior to tin plating, also known as the “saw plate saw” method. After map molding, sawing is done, but not completely, just to a depth to expose the side flank partially. The clue is that the pads are still connected by the remaining metal part of the pad flanks which are not separated. By this method, the continuity

of the leadframe is maintained for the galvanized plating process. Full singulation, with a thinner sawing blade than used for partial cut, is done after Sn plating. Due to the involved sawing tolerances, this method is the same as the dimples alternative, only suitable for ≥ 200µm thick leadframes and as shown in figure 24 not the complete height of the side flank is covered with tin.

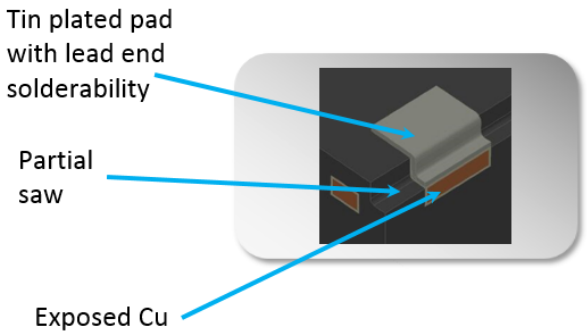

Figure 24: SWF realization by saw plate saw process

Outlook: E-less Sn plating as universal alternative for multi I/O package

An upcoming option is to apply e-less (immersion) tin plating to realize side wettable flanks as for the galvanic plating solution for low I/O count DFN packages, the e-less tin plating covers the side flanks in complete height (≥ leadframe thickness, refer to figure 14). It allows plating of multiple pads which can be arranged on all four sides of the DFN/QFN packages. The individual DFN/QFN package can be fully separated prior to e-less immersion tin plating. Unlike barrel plating, a good layer thickness conformity can be achieved by fixation of the packages in the immersion Sn plating process on a carrier (e.g. dicing foil). A disadvantage of immersion tin plating is that the growth rate of the tin is slow and getting slower with increasing Sn thickness. The achievable Sn layer thickness is less than 3µm. However, plating chemistry suppliers offer new immersion Sn plating systems including surface treatments to provide as good wetting as plated and after storage.

Summary/Conclusion

The described galvanic tin plating method of side wettable flanks ensures solder wetting of the side flanks after storage. With current leadframe height a side wettable flank height of minimum 100µm can be achieved. DFN packages with side wettable flanks combine advantages of packages with and without leads in respect to AOI capability and board level robustness. The AOI capability on PCB is proven by a leading AOI system supplier. To realize side wettable flanks for multi pad packages (≥ 6 I/Os) e-less tin plating of side flanks will be evaluated.

General References

[1] Martin Ka Shing Li, Max Leung, Pompeo Umali, “Singulation of IC packages, plating contact pads of the leadframe, and including contact pad edge regions formed by the first series of cuts”, US Patent 13/876,819, 19 August 2014

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[3] NXP / Nexperia „Application Note AN10365 “Surface mount reflow soldering” Rev 6.0, “2012

[4] Detlef Beer, Hans-Juergen Funke, Application Report, AOI Inspection of DFN Devices, 23 October 2013

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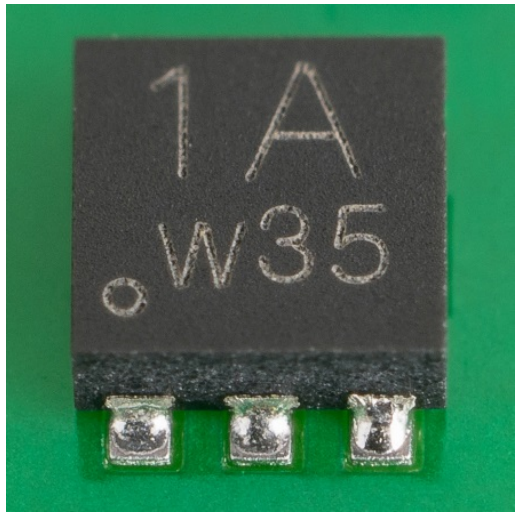
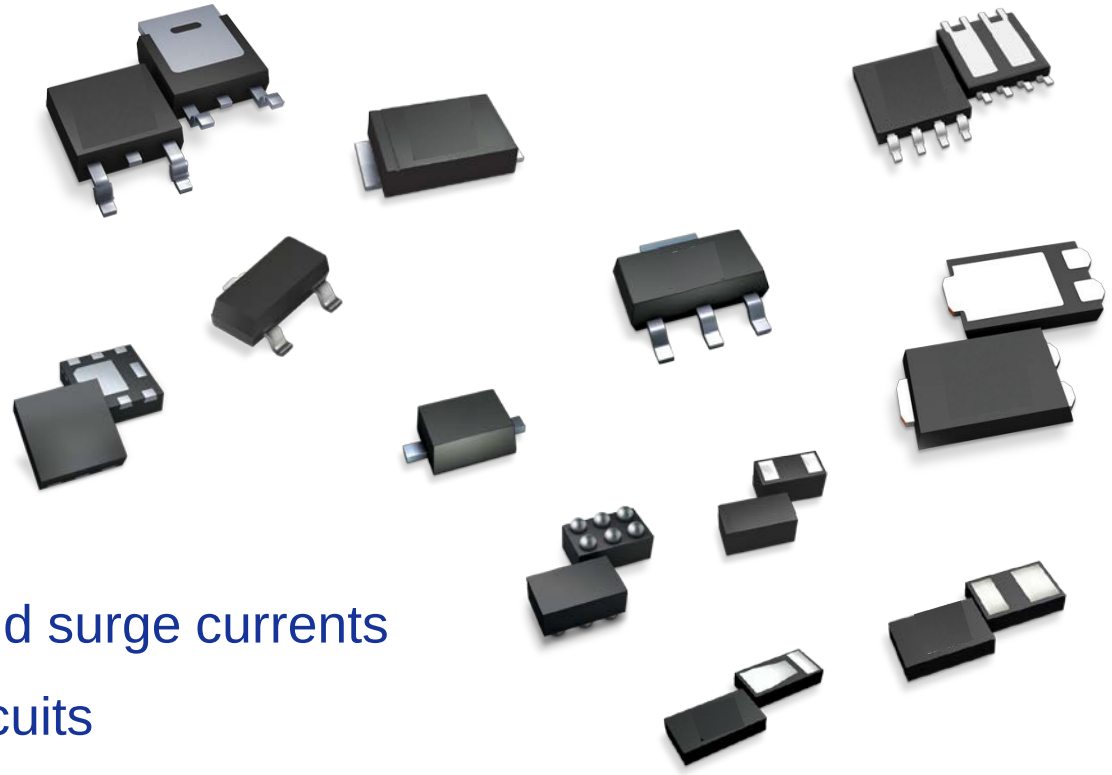


Introduction, Why Discrete Semiconductors



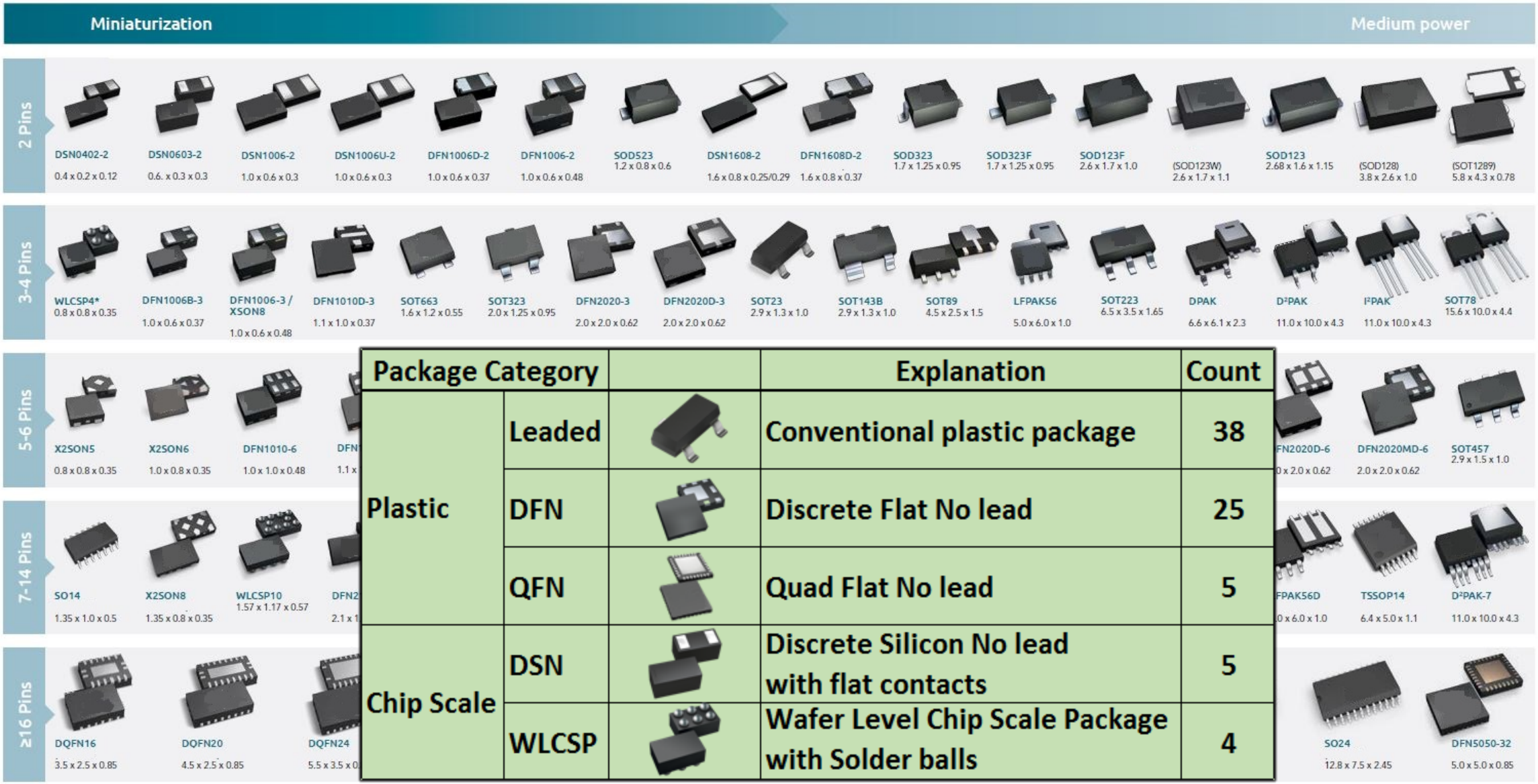
- Debugging failures in IC design
- Driving high currents
- Dealing with high voltage
- Easier power dissipation
- IC protection against ESD pulses and surge currents
- Flexibility of designing electronic circuits

Worldwide Production Volume of Discrete Semiconductors > 400 billion pieces / year

Discrete Semiconductors Packages, Portfolio Example

Miniaturization → Medium power

Discrete Semiconductors Packages, Portfolio Example



Package Category			Explanation	Count
Plastic	Leaded		Conventional plastic package	38
	DFN		Discrete Flat No lead	25
	QFN		Quad Flat No lead	5
Chip Scale	DSN		Discrete Silicon No lead with flat contacts	5
	WLCSP		Wafer Level Chip Scale Package with Solder balls	4

Discrete Semiconductors Package Platforms

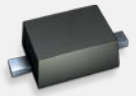
Leaded
Wire bonded

Small-signal

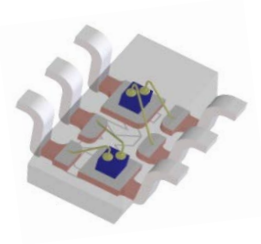
Medium-power

Power

Small-signal flat lead

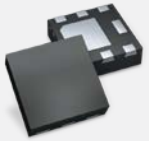


Gullwing



Leadless plastic

DFN

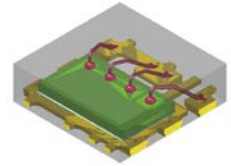


DQFN

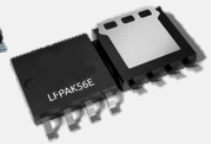
DFN2111-7

X2SON

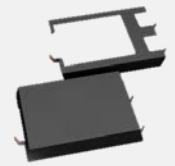
With side wettable flanks option



Leaded
Copper clip

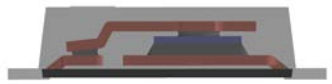


LFPAK family



Clip flat family

Gullwing



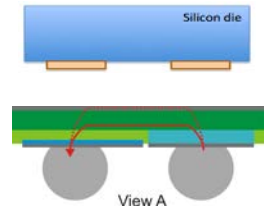
DSN & WLCSP

DSN1608-2

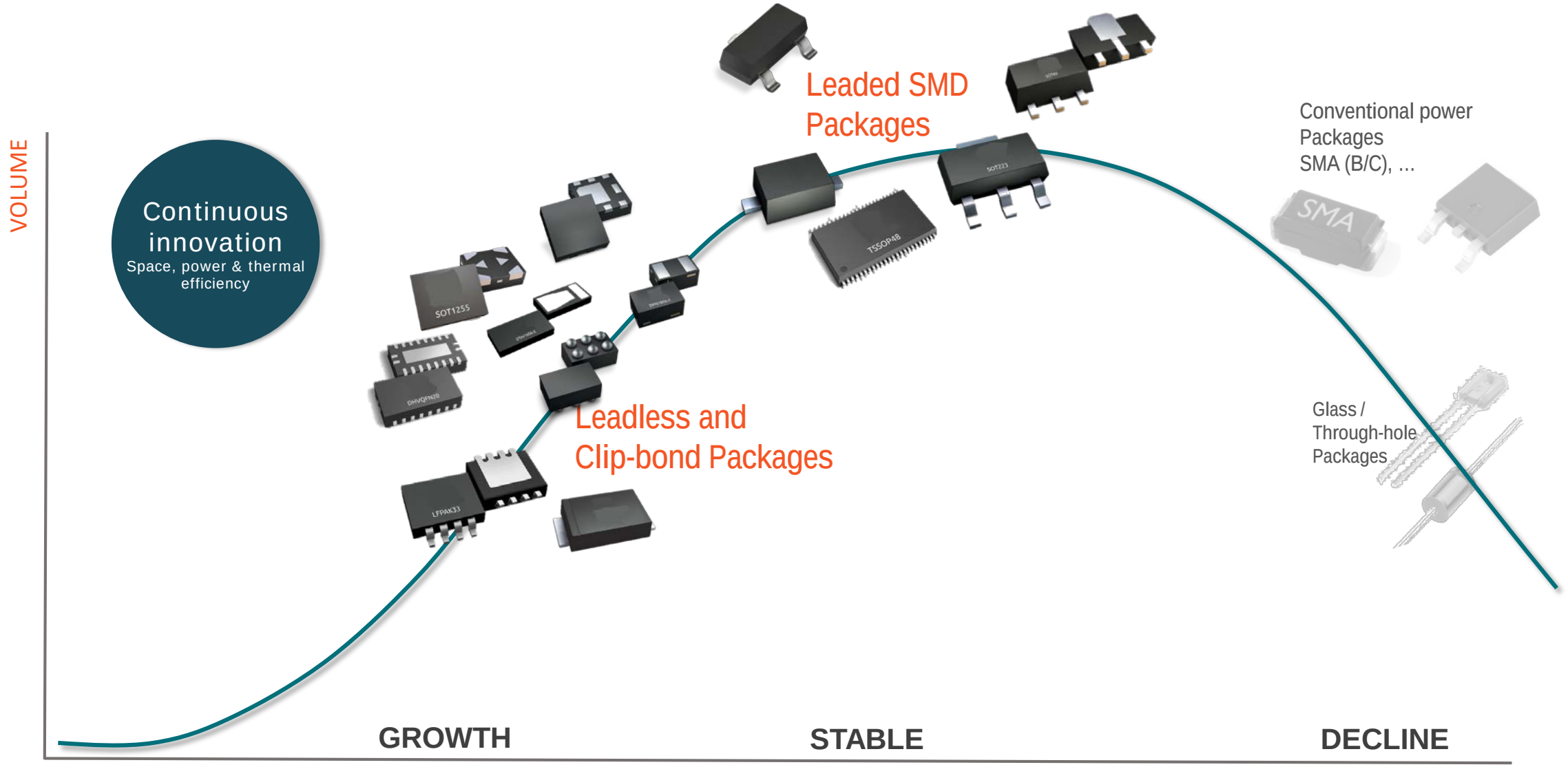
DSN1006-2

WLCSP15

WLCSP6



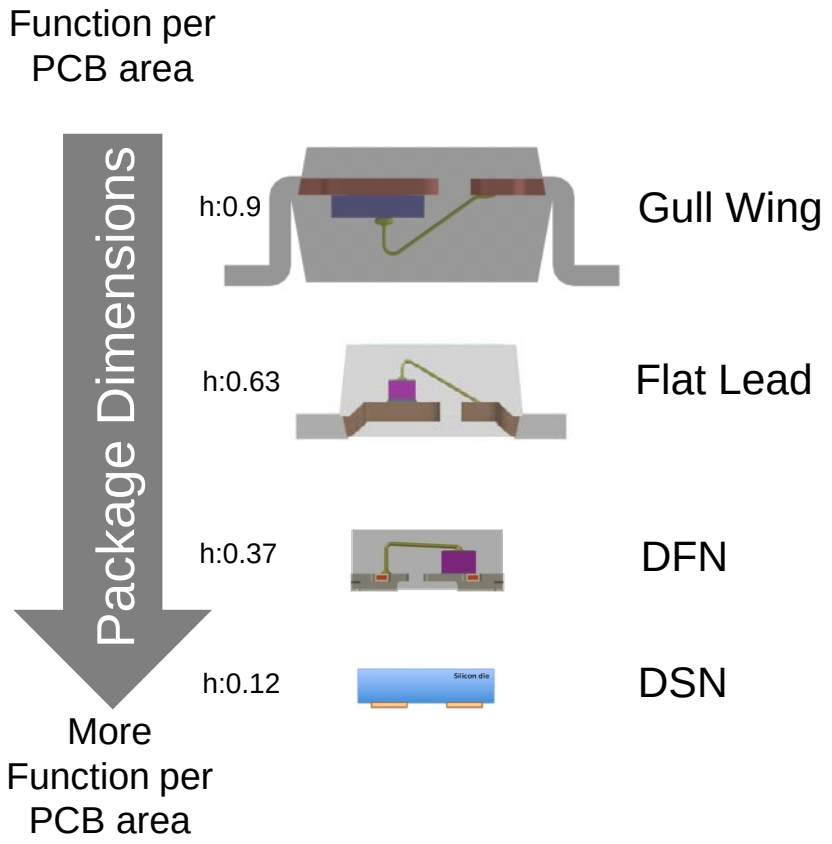
Discrete Semiconductors Package Trends



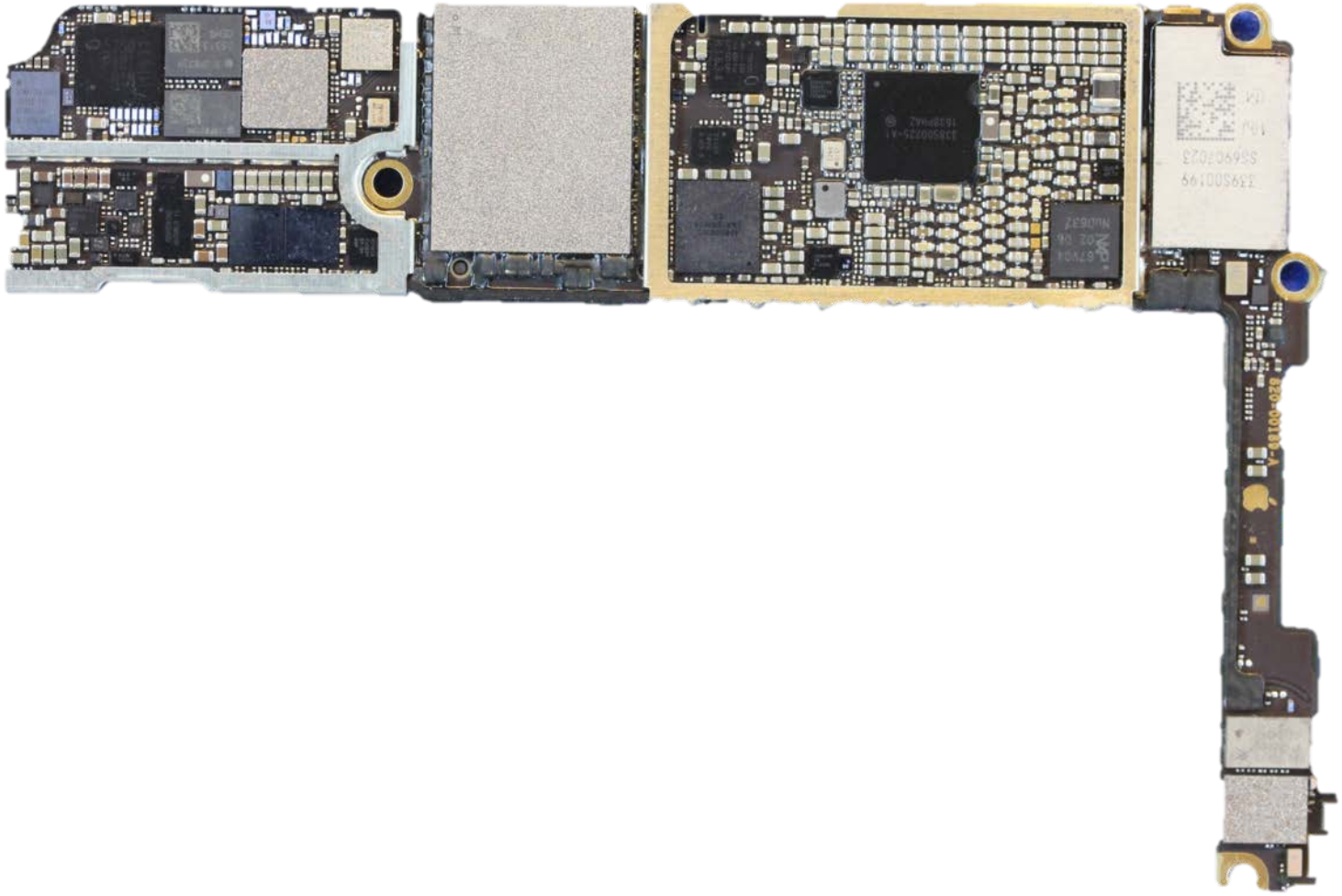
Driving factors for Leadless Packages

Advantages of Leadless Packages

- No space for leads needed
  - *less PCB space for same electrical function*
  - *or more performance on same PCB area*
- Enables height reduction due to flat leadframes
- Optimized thermal performance
  - *large heatsink under plastic body possible*
  - *short distance from active silicon to PCB solder pad*

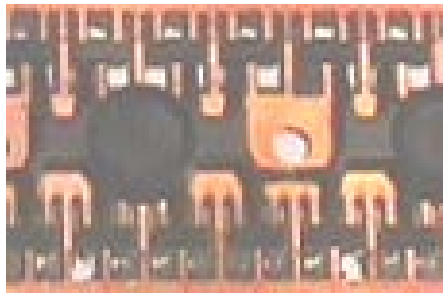


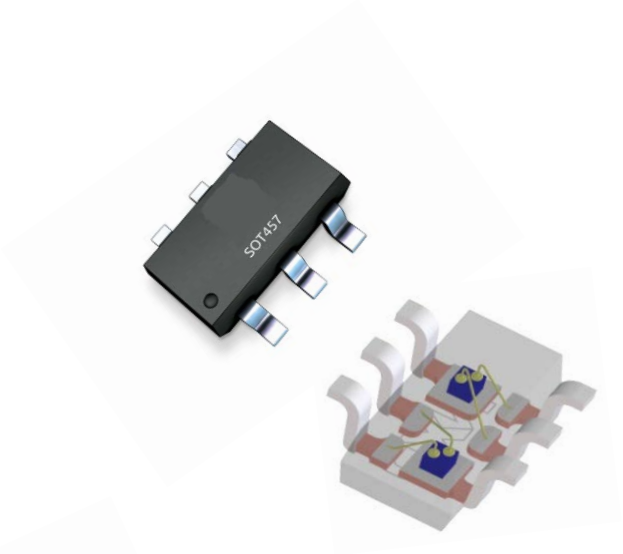
Driving factors for Leadless Packages

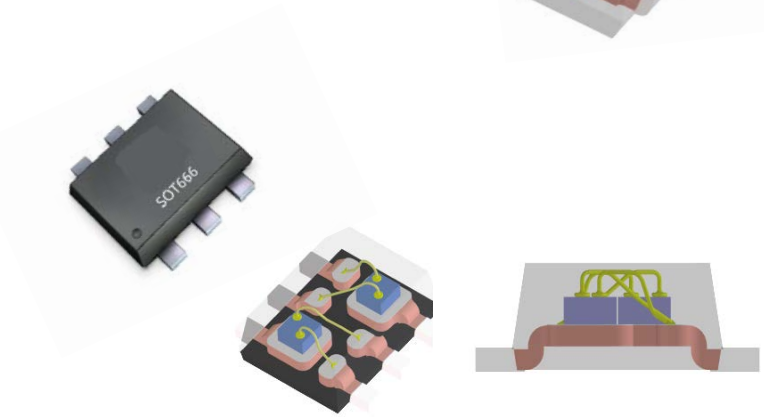


Leaded SMD Packages
- Package Characteristics / Build up

- Leadframe based plastic packages
- Reel-to-reel or strip leadframe
- Die attach: eutectic (mainly) and epoxy glue
- Ball / wedge wire bonding (Cu or Au wires)
- Single cavity transfer molding
- Lead finish:
  Electro-galvanic Sn plating



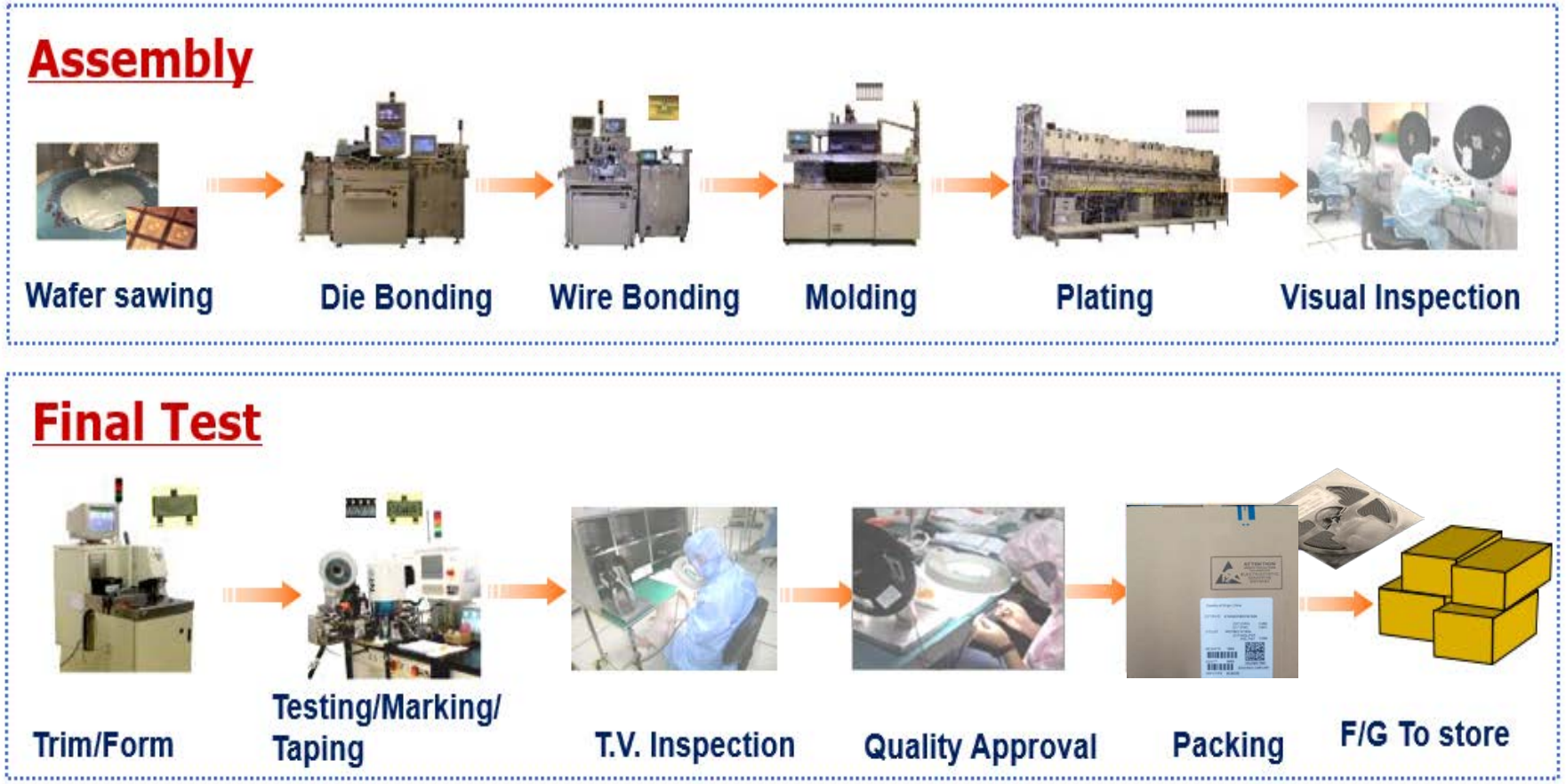




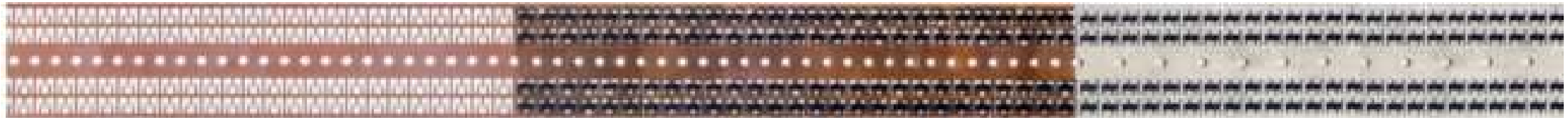
Leaded SMD Packages
- Assembly Flow, Example Reel to Reel

Example :

- Reel to reel SOT23 production



Leaded SMD Packages
- Assembly Line, Example Reel to Reel



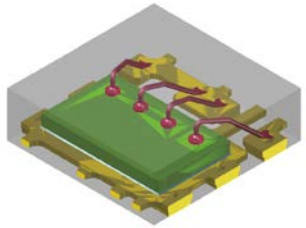
Die-& Wire Bond

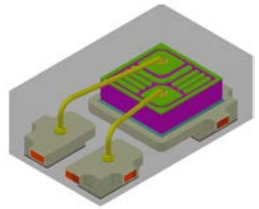
Molding

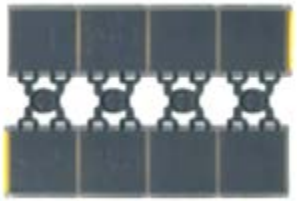
Sn Plating

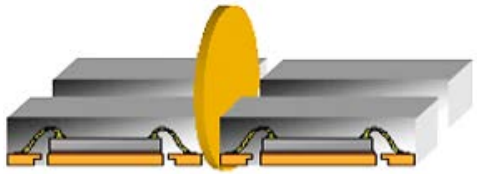
Leadless Packages (DFN/QFN)
- Package Characteristics / Build-up

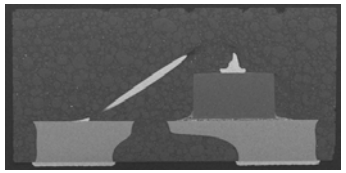
- Leadframe based plastic packages
- Strip leadframe
- Die attach: epoxy glue
- Chip front contacts: Cu or Au wires
- Map molding (transfer molding)
- Lead finish:
  Electro-galvanic Sn or NiPdAu plating
- Package singulation: sawing

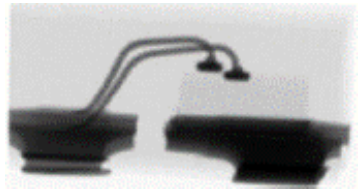




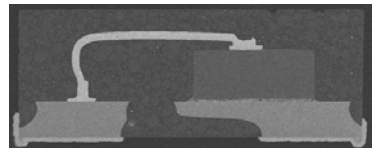


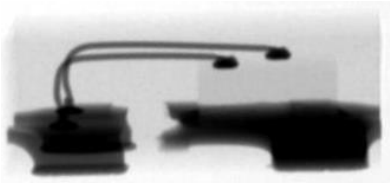




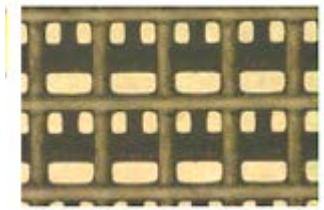


Normal wire loop
ball wedge





Reverse wire loop
for thin packages



Leadless Packages (DFN/QFN) - Assembly Line Set-up

Wafer sawing

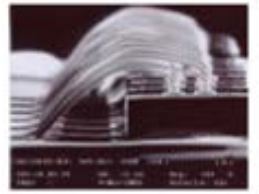
Die attach

Glue curing

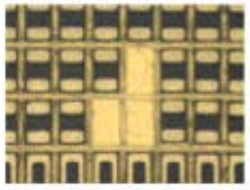
Plasma cleaning

Wire Bonding

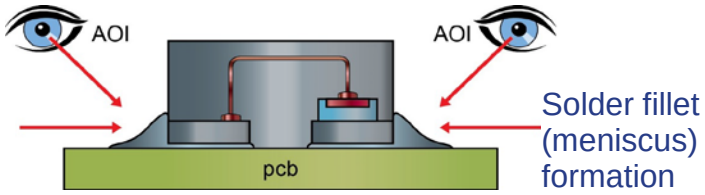
Die attach to leadframe → Glue curing for glue bond → Plasma cleaning for W/B → Wirebond to leadframe →



Leadless Packages (DFN/QFN) - Assembly Line Set-up

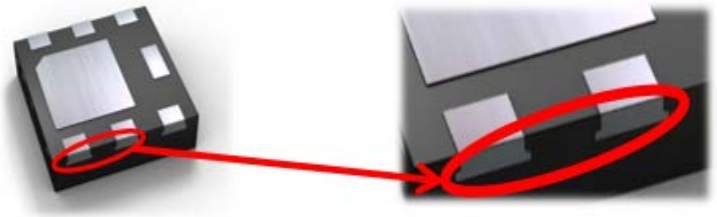
Molding	Post Mold cure	Tin plating	Package sawing	Testing / Marking / Taping
				
Encapsulation	Plastic body curing	Tin plating for solder pads	Sawing for singulation	2 x 100% electrical test
				

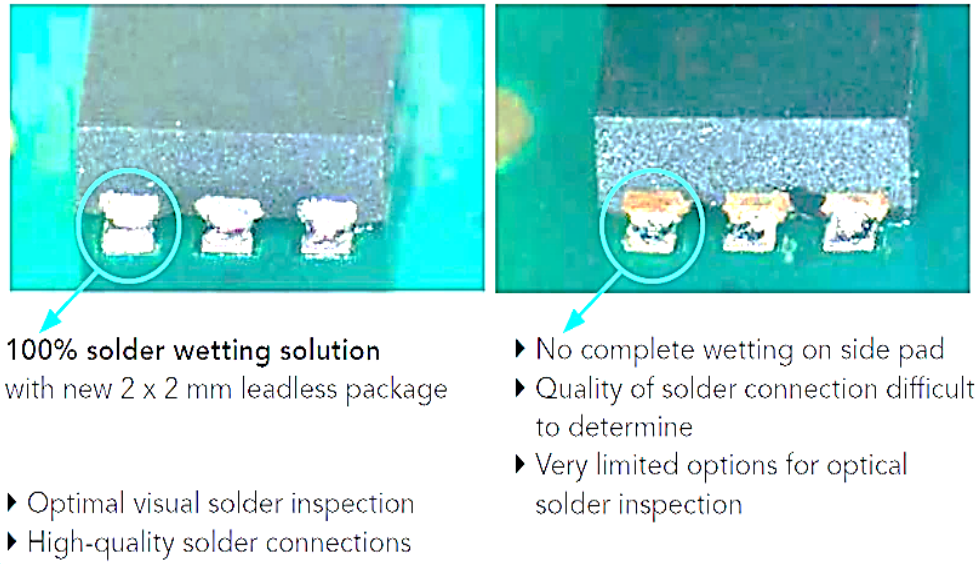
Side Wettable Flanks for low I/O DFN Packages



Example 1 : DFN2020-6 (SOT1220)

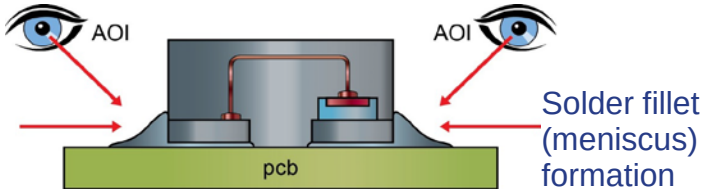
- Exposed side pads are Sn plated =SWF (Side Wettable Flanks)
- Results in easily wetting with solder
- Enables visual inspection of solder connection on PCB by AOI
- Combines advantages of packages with and without leads

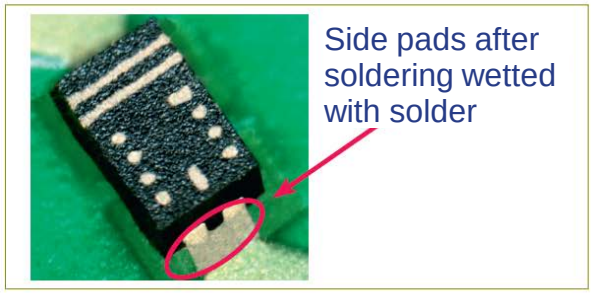




DFN2020-6 comparison of SWF versus bare Cu side flanks after soldering

Side Wettable Flanks for low I/O DFN Packages



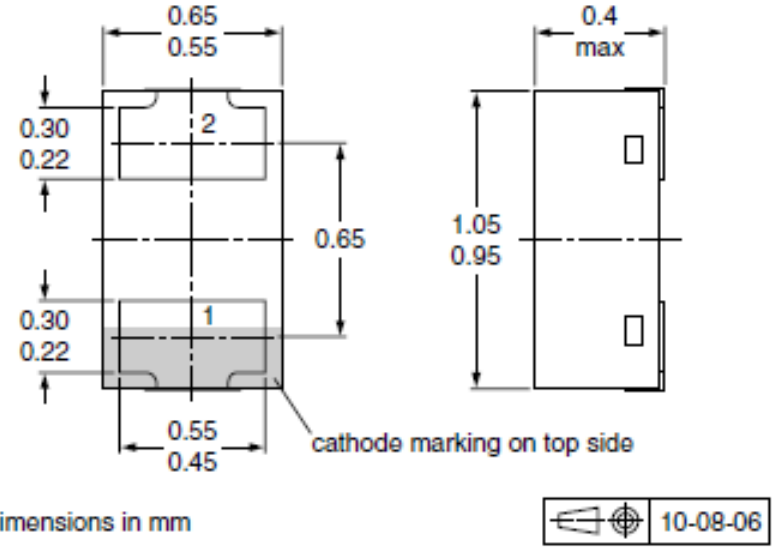


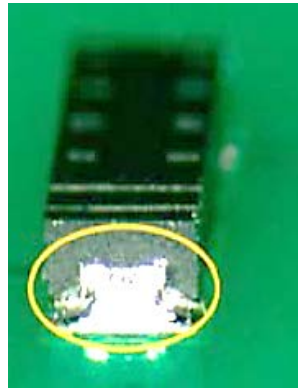
Example 2 : DFN1006 (SOD882D)

- Exposed side pads are Sn plated =SWF (Side Wettable Flanks)
- Results in easily wetting with solder
- Enables visual inspection of solder connection on PCB by AOI
- Combines advantages of packages with and without leads

DFN1006
SOD882D

Mounted on PCB

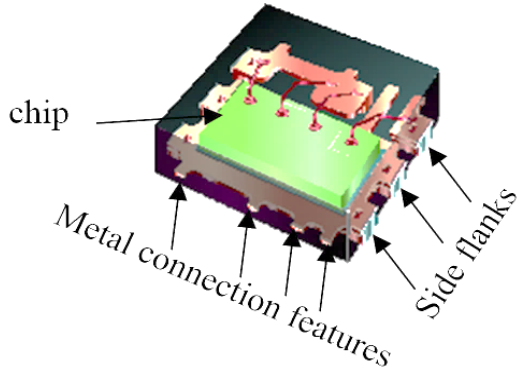


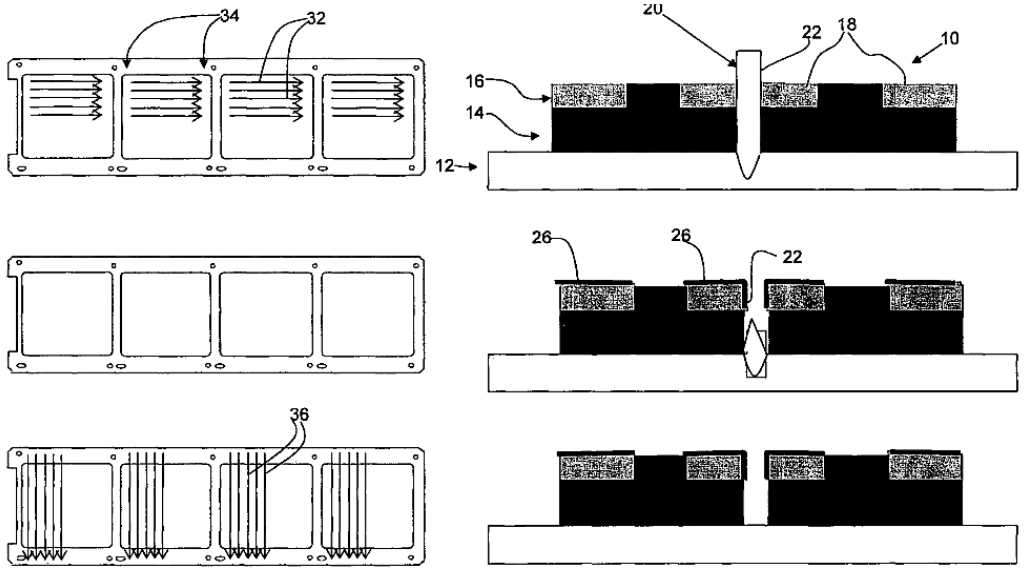


Side Wettable Flanks for low I/O DFN Packages Realization

Electro-galvanic tin plating of bottom and side pads:

- Exposure of side flanks by sawing
- Bottom pads and side flanks plated in same process
- Final package singulation after plating



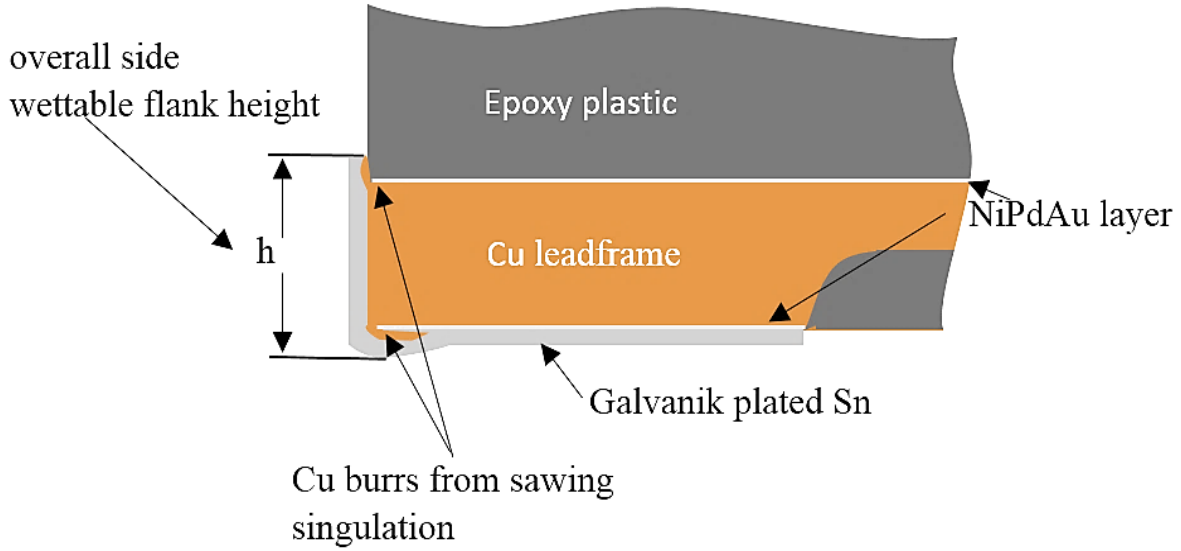


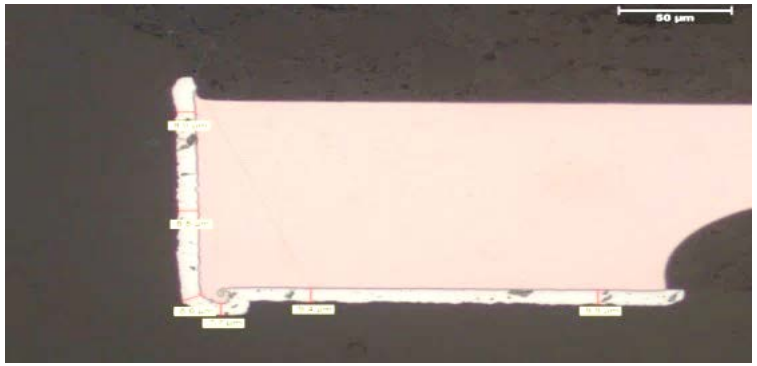
[1]

Side Wettable Flanks for low I/O DFN Packages

Requirement for ≥ 100µm SWF height

- Usual leadframes thickness:
  - *for packages with h ≥ 0.5mm : 127µm*
  - *for packages with h < 0.5mm : 100µm*
- Sawing burr and Sn plating thickness guarantees ≥ 100 µm SWF height also for packages < 0.5mm height





Side Wettable Flanks for low I/O DFN Packages

Verification of Effectiveness

- AOI capability has been verified in cooperation with a leading AOI equipment supplier
- Test board with footprints of various DFN packages has been realized
- Solder paste volume has been varied by purpose:
  E.g.: ± 50% more or less solder volume
  No solder paste printed at some pads

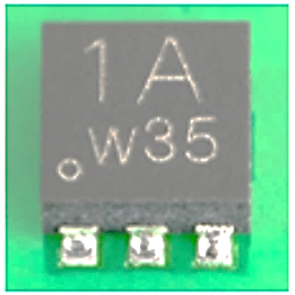
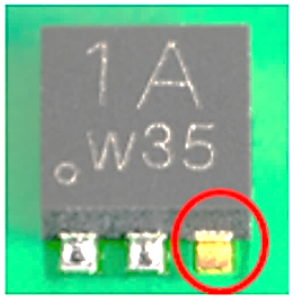
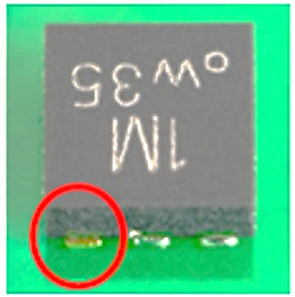
Packages with solderable (Sn plated) side pads						Corresponding Packages without solderable side pads					
Package	SOD/SOT number	length in mm	width in mm	height in mm	picture	Package	SOD/SOT number	length in mm	width in mm	height in mm	picture
DFN1006-2	SOD882	1.0	0.6	0.37		DFN1006-2	SOD882	1.0	0.6	0.5	
DFN1608-2	SOD1608	1.6	0.8	0.37							
DFN1010-3	SOT1215	1.1	1.0	0.37		DFN1010-6	SOT1216	1.1	1.0	0.37	
DFN2020-6	SOT1220	2.0	2.0	0.65		DFN2020-6	SOT1118	2.0	2.0	0.65	

Side Wettable Flanks for low I/O DFN Packages

Verification of Effectiveness

- AOI capability has been verified in cooperation with a leading AOI equipment supplier
- Test board with footprints of various DFN packages has been realized
- Solder paste volume has been varied by purpose:
  E.g.: ± 50% more or less solder volume
  No solder paste printed at some pads

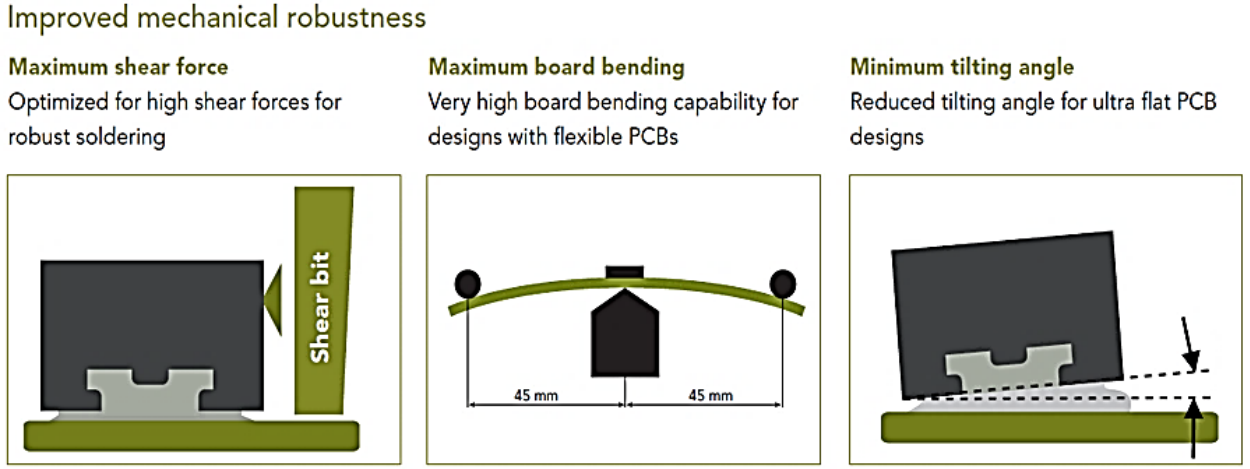
➔ It could be confirmed that DFN packages with SWF enable reliable AOI of solder connection quality

DFN2020-6 with SWF	DFN2020-6 without SWF
	
Solder paste printing without fails (a)	Solder paste printing without fails (a)
	
Solder paste printing with failure (b)	Solder paste printing with failure (b)

Side Wettable Flanks for low I/O DFN Packages

Additional Benefits compared to DFN w/o SWF

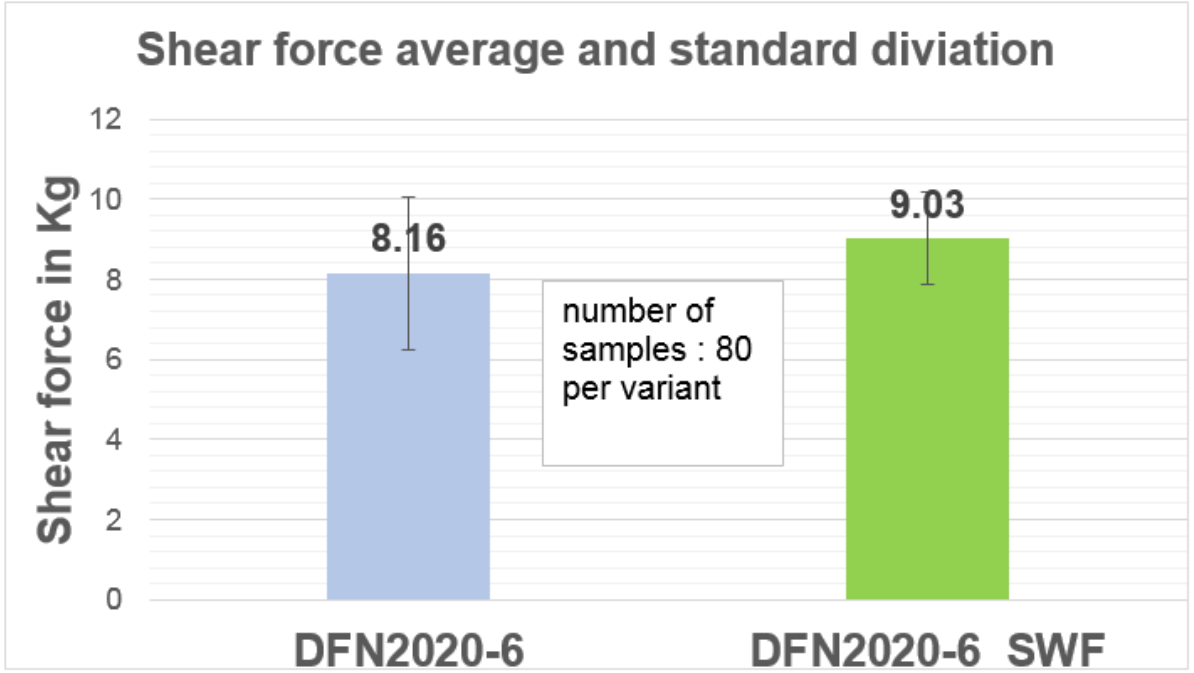
- Maximized shear force of packages on PCB
- Maximized board bending robustness
  Together with smart leadframe design:
  up to 14 mm bending depth according to IEC60068-2-21
- Minimized tilting of packages after soldering
  Particularly for 2 I/O packages

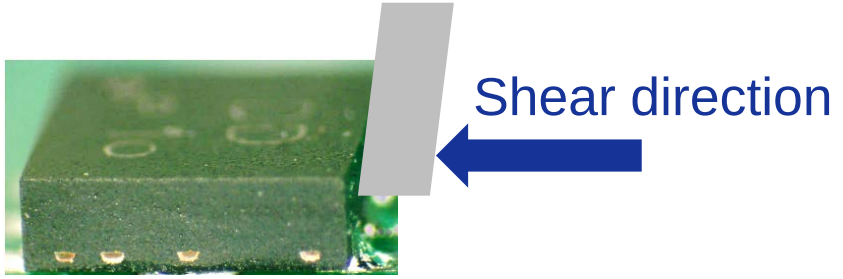


Side Wettable Flanks for low I/O DFN Packages

Maximized shear force of packages on PCB

- Shear test according to IEC 62137-1-2
- Important to be controlled for comparison:
  - *PCB pad layout, stencil dimensions and solder paste type*
  - *Shear direction and shear bit height*
- Example for DFN2020-6 package:
  - *Shear test on PCB with 80 samples each with and without SWF*
  - *SWF result in 10% higher shear forces*
  - *SWF reduces the variation of shear forces*

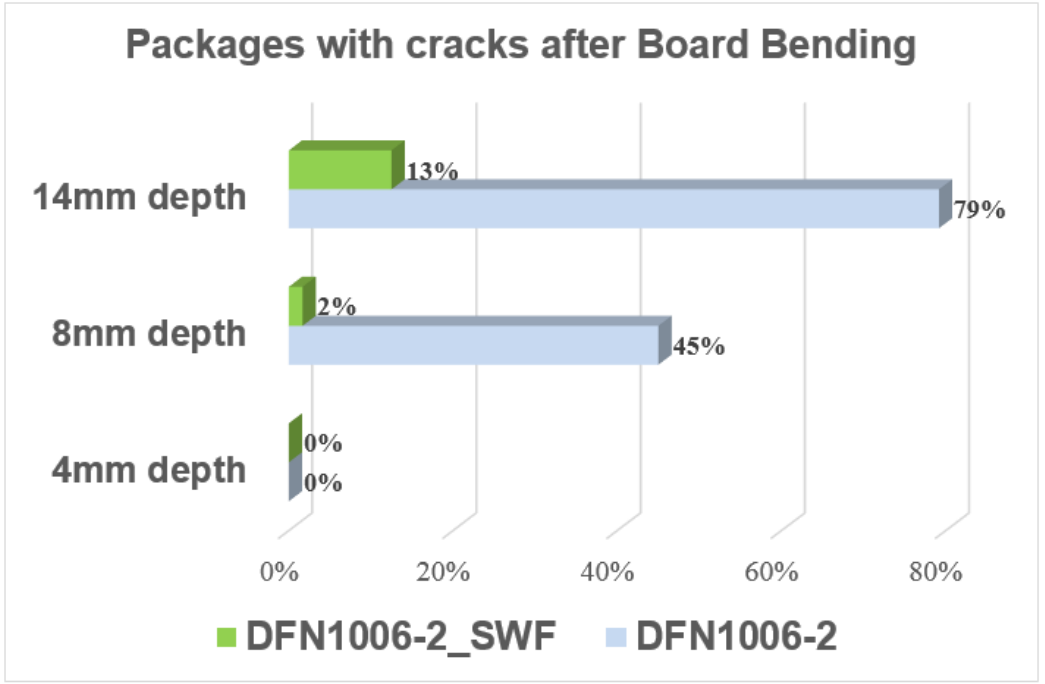


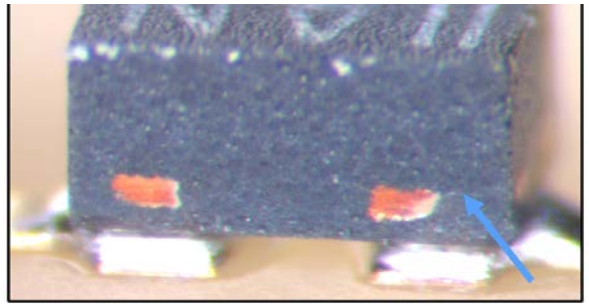


Side Wettable Flanks for low I/O DFN Packages

Maximized board bending robustness

- Board bending test according to IEC60068-2-21
- Bend test performance improved by inner package design, e.g. Leadframe anchoring features
- Example for DFN1006-2 package:
  - *Bending test on PCB with 120 samples each with and without SWF*
  - *All tested samples passed electrical insitu test*
  - *SWF samples passed up to 14mm bending without any visual defect*
- As reference: Chip capacitors in same size often specified with 1mm bending depth

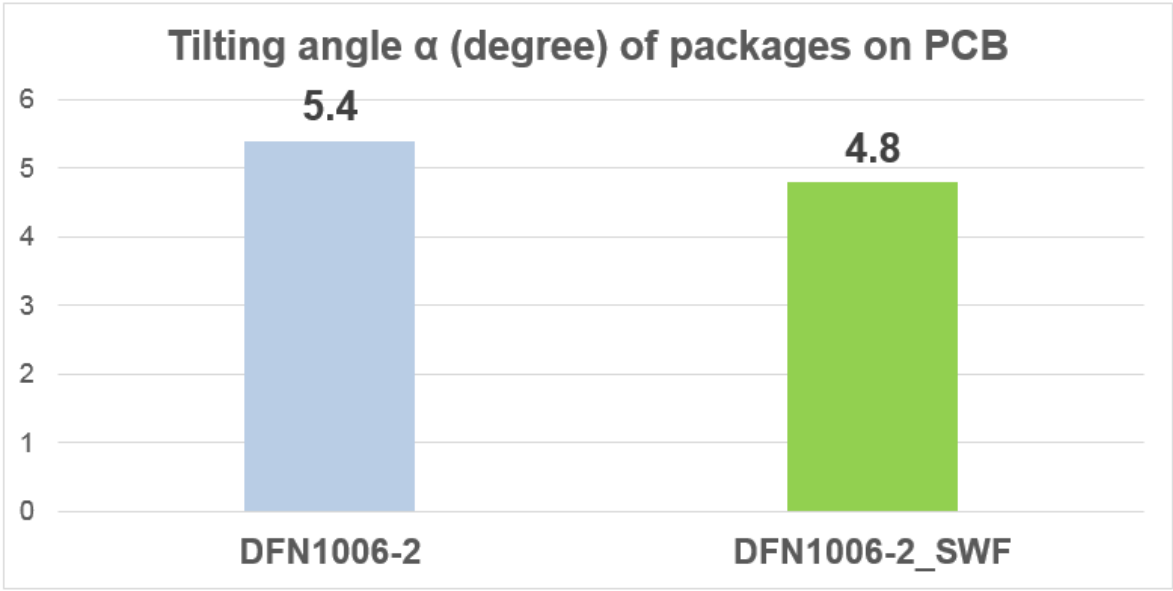


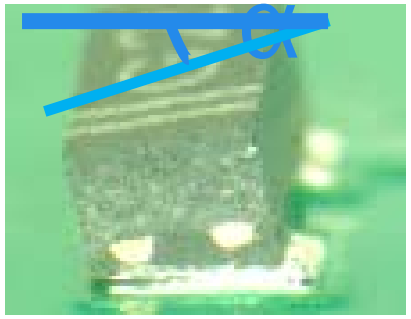


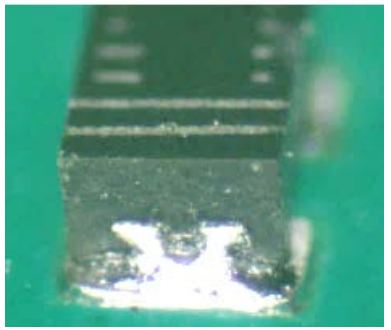
Side Wettable Flanks for low I/O DFN Packages

Reduced tilting after soldering on PCB

- Tilting of Packages after soldering
- Important to control for comparison:
  - *PCB pad layout, stencil dimensions and solder paste type*
  - *Reflow soldering conditions*
- Example for DFN1006-2 package:
  - *Tilting measurements on PCB with 40 samples each with and without SWF*
  - *Tilting angle reduced by ~10% with SWF*



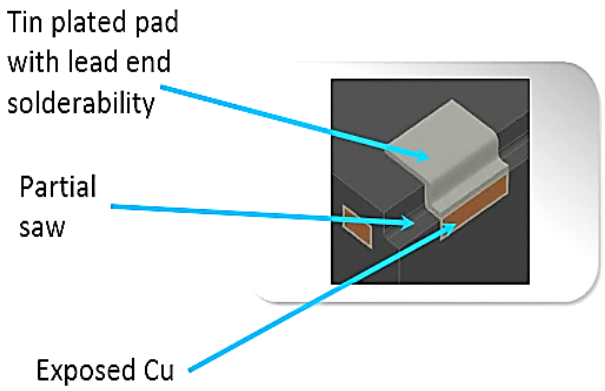




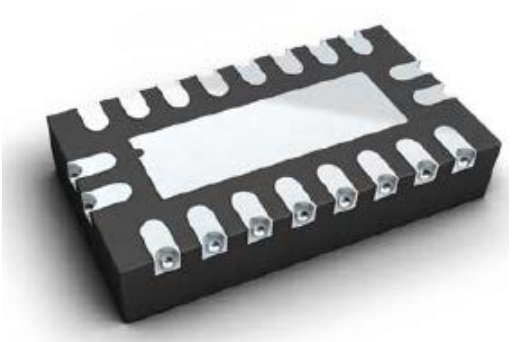
Side Wettable Flanks for QFN and DFN Packages

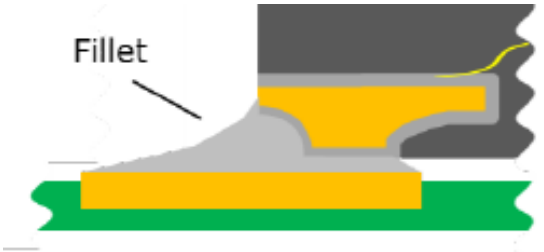
Examples of alternative SWF Solutions

- Saw plate saw
  - *Partial sawing of the DFN packages (leadframe) after molding prior to e- Sn plating*
  - *Final singulation after Sn plating*



- Dimples
  - *Etched during leadframe manufacturing*
  - *Plated with NiPdAu as the bottom pads*
  - *No Sn plating at package assembly*





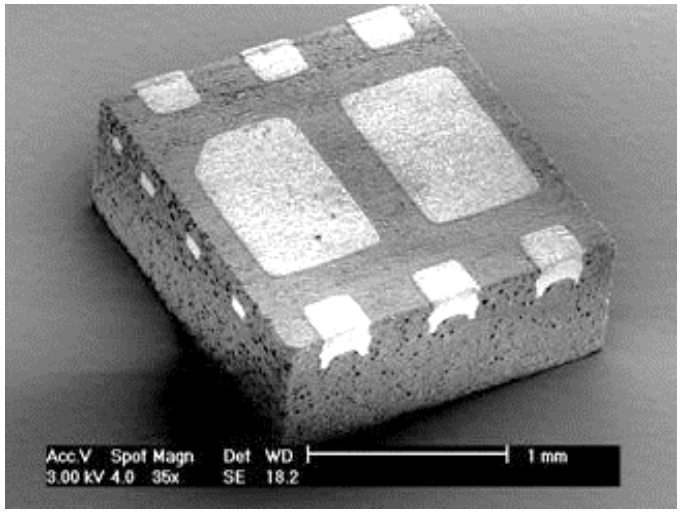
Advantage : Allow to realize SWF for packages with multi I/Os

Disadvantage : Only possible for ≥ 200µm thick leadframe

Side Wettable Flanks for QFN and DFN Packages

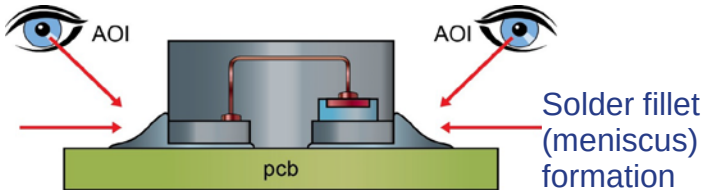
Outlook : Immersion Sn Plating as universal Solution

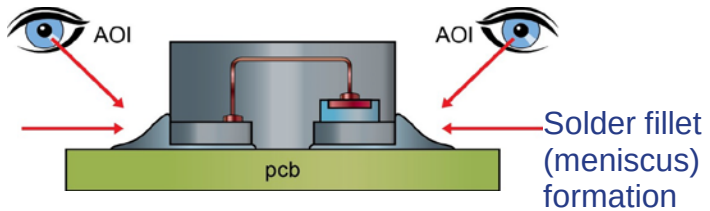
- E-less, immersion Sn plating can be applied after full singulation of packages
- In opposite to barrel plating the packages are fixed on a carrier or still in leadframe
  This enables a good layer thickness conformity
- Disadvantage is the slow growth rate of Sn in this process, layer thickness will be < 3 µm
- Plating systems and surface treatments which still guarantee good wetting after storage have been developed by chemistry suppliers
- Height of SWF will be ≥ leadframe height , > 100 µm



Summary and Conclusions

- The described galvanic tin plating method for SWF ensures solder wetting of side flanks after storage
- With current leadrame thicknesses a SWF height of ≥ 100 µm can be achieved
- DFN packages with SWF combine advantages of packages with and without leads
- AOI capability of DFN packages with SWF was proven by a leading AOI equipment supplier
- DFN packages with SWF give additional benefits in mechanical robustness
- To realize SWF for multi I/O packages (≥ 6 I/Os) e-less (immersion) Sn plating will be evaluated





Thank you for your attention

Questions?

References

[1] “Martin Ka Shing Li, Max Leung, Pompeo Umali, “Singulation of IC packages, plating contact pads of the leadframe, and including contact pad edge regions formed by the first series of cuts”, US Patent 13/876,819, 19 August 2014.