Fill the Void IV: Elimination of Inter-Via Voiding

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ABSTRACT
Voids are a plague to our electronics and must be eliminated! Over the last few years we have studied voiding in solder joints and published three technical papers on methods to "Fill the Void." This paper is part four of this series. The focus of this work is to mitigate voids for via in pad circuit board designs.

Via holes in Quad Flat No-Lead (QFN) thermal pads create voiding issues. Gasses can come out of via holes and rise into the solder joint creating voids. Solder can also flow down into the via holes creating gaps in the solder joint. One method of preventing this is via plugging. Via holes can be plugged, capped, or left open. These via plugging options were compared and contrasted to each other with respect to voiding. Another method of minimizing voiding is through solder paste stencil design. Solder paste can be printed around the via holes with gas escape routes. This prevents gasses from via holes from being trapped in the solder joint. Several stencil designs were tested and voiding performance compared and contrasted.

In many cases voiding will be reduced only if a combination of mitigation strategies are used. Recommendations for combinations of via hole plugging and stencil design are given. The aim of this paper is to help the reader to "Fill the Void."

Key words: voids, solder joints, via holes, via-in-pad, stencil design, QFN thermal pad

INTRODUCTION
Voiding in solder joints is an ongoing issue for electronics manufacturers. Bottom terminated or "no-leaded" devices such as Quad Flat No-Lead devices (QFN) are becoming commonplace. This type of device is vulnerable to voiding due to low standoff heights and relatively large mass of solder paste applied to the thermal pad. QFN thermal pads are frequently designed with via holes to help transfer heat away from the components. Via-in-pad designs tend to generate unacceptably high voiding levels and therefore make a good test vehicle for voiding studies.

This study is a continuation of previous work on voiding [1, 2, 3]. In the previous work several parameters were varied and their effects on voiding summarized. A variety of water soluble and no clean lead-free solder pastes were compared. A range of solder powder particle sizes and solder alloys were tested with respect to voiding. The stencil design of QFN thermal pads was varied and differences in voiding levels were noted. Two different circuit board surface finishes were compared with respect to voiding performance. Several different convections reflow profiles were used and their effects on voiding compared. Convection reflow with a nitrogen atmosphere and vapor phase reflow with vacuum were compared and contrasted. Differences in voiding were noted and the size of the largest voids was also analyzed with respect to some of the variables. The voiding levels for all of these variables were compared and contrasted using statistical analysis techniques. The previous work was concluded with recommendations to help the reader "Fill the Void".

This investigation includes QFN thermal pads with via-in-pad designs and methods of mitigation of voids for these designs. The list below shows the variables which were tested with respect to their effects on voiding.

- Via-hole plugging (3): not plugged, solder mask tent, and non-conductive via fill.
- Stencil designs (2): solder paste printed directly over the via holes, and a modified stencil design with paste printed around the via holes including gas escape routes.

Analysis of the voiding data was done using statistical analysis techniques. Box and whisker plots were used to show the data populations. Tukey-Kramer honest significant difference (HSD) testing was used to determine if the data sets were significantly different. Voiding images were compared and contrasted to demonstrate the differences in voiding behavior. Conclusions were drawn for each set of variables, and from these conclusions a set of recommendations were made.

METHODOLOGY

Materials

The circuit board used for this experimentation is shown below (Figure 1). This circuit board is made of FR4 material, plated copper pads and via holes, and electroless nickel immersion gold (ENIG) surface finish.

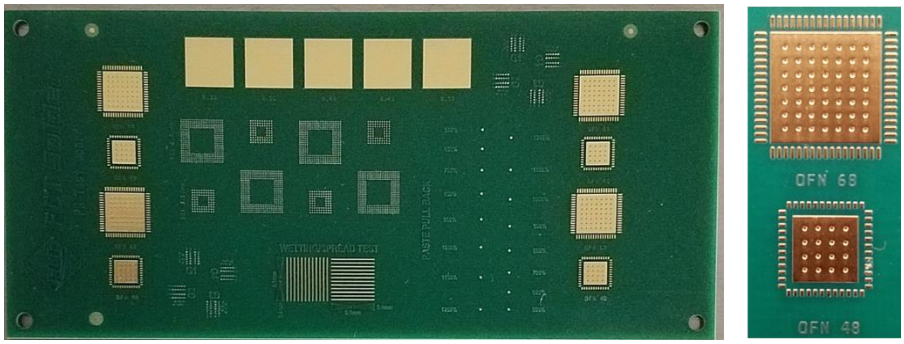


Figure 1 –Test Circuit Board for Voiding with Via-in-Pad Designs

The via holes were built on a grid as recommended by the QFN component manufacturer. The larger QFN had a grid of 7 x 7 via holes and the smaller QFN had a grid of 4 x 4 via holes. The drilled hole size was 0.30 mm (0.012 inches) and the finished hole size was 0.25 to 0.28 mm (0.010 to 0.011 inches) for both sizes of QFN components.

Two different via plugging options were used on the circuit boards. The first via plugging option was a solder mask tent applied to the bottom side of the circuit board. The via holes are open at the top side of the board. The solder mask tent did not completely cover the holes. Some openings are visible in solder mask over the holes (Figure 2)

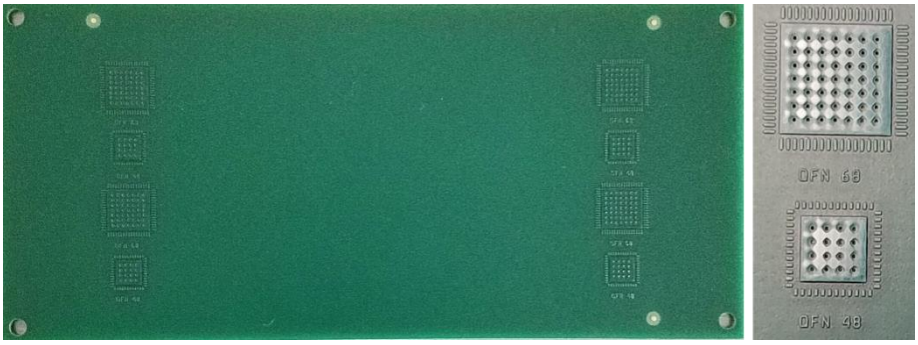


Figure 2 – Test Circuit Board with Solder Mask Tent on the Bottom Side

In the 2nd plugging option, the via holes were filled with a non-conductive polymer (Figure 3). The plugged vias were plated over with the ENIG finish.

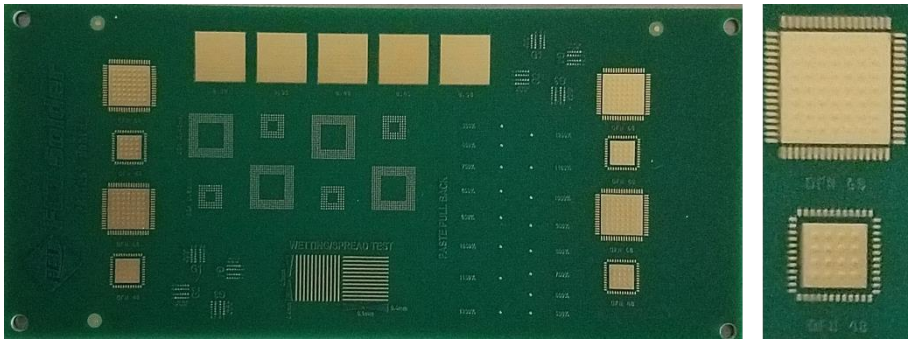


Figure 3 – Test Circuit Board with Non-Conductive Polymer Hole Fill

The QFN thermal pads were used for void measurements. The QFN components used were dummy components of two different sizes. The larger QFN had 68 perimeter leads on a 0.5 mm pitch, a 10 mm body size, and a matte tin finish. The smaller QFN had 48 perimeter leads on a 0.5 mm pitch, a 7 mm body size, and a matte tin finish (Figure 4).

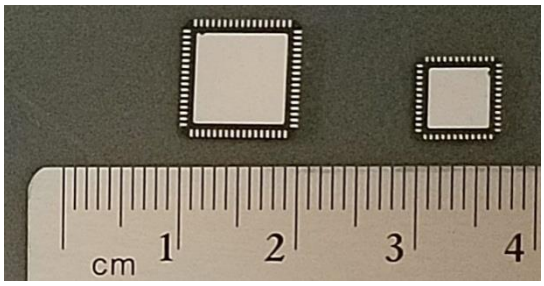


Figure 4 – QFN Dummy Components

The standard stencil design was similar for each size of QFN (Figure 5). In each case the solder paste coverage was approximately 65% of the thermal pad area.

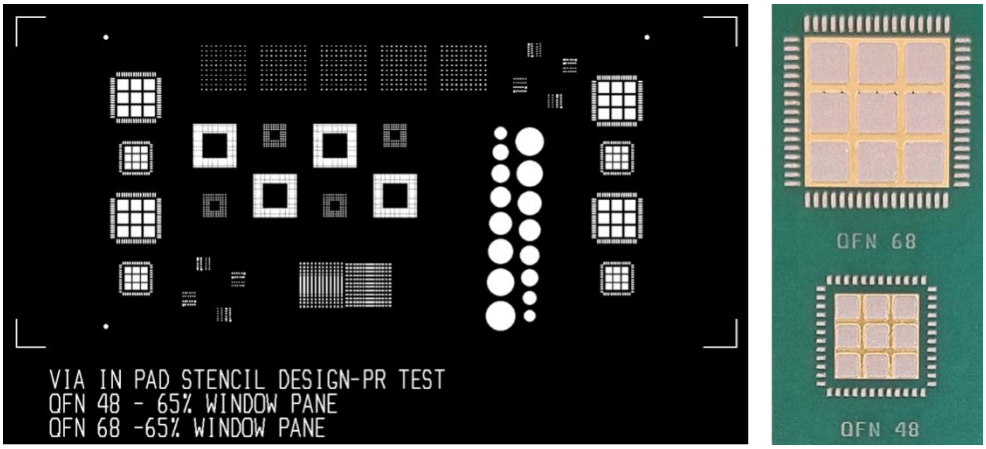


Figure 5 – Standard Stencil Design for QFN Thermal Pads

The standard stencil design included window pane designs with 9 panes. The web width of the larger QFN window panes was 0.51 mm (20 mils). The web width of the smaller QFN window panes was 0.38 mm (15 mils). The solder paste was printed directly over the via-holes with no consideration for via location.

A modified stencil design was made with clearances around the via holes and gas escape routes from the via holes to the outside of the thermal pad. Solder paste was printed around the via holes (Figure 6).

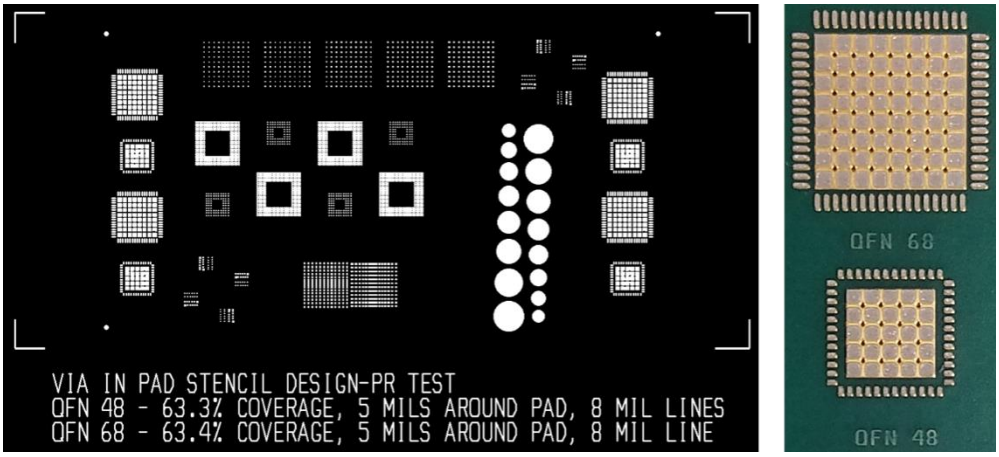


Figure 6 – Modified Stencil Design to Print Solder Paste Around the Via-Holes

This modified stencil design gave approximately 63% area of printed solder paste coverage. The web width was held constant at 8 mils for each size of QFN. The clearance of the printed solder paste around the via-holes was kept at 5 mils.

The solder paste used was a no-clean lead free solder paste that typically gives "ultra-low" voiding results. Tin (Sn) / Silver (Ag) 3.0% / Copper (Cu) 0.5% alloy was used and is commonly referred to as SAC305. The solder powder particle size was IPC Type 3 (25 to 45µm).

Convection Reflow Profile

Reflow was done in a 10-zone convection reflow oven. A linear ramp-to-spike (RTS) type profile was used (Figure 7).

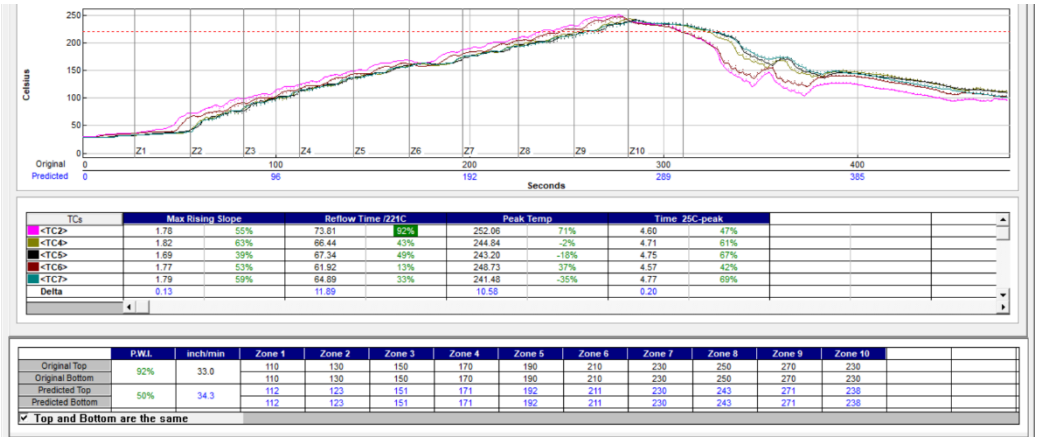


Figure 7 – Linear Ramp to Spike (RTS) Reflow Profile

The parameters for the profile are summarized below (Table 1).

Table 1 – Reflow Profile Parameters

Setting	RTS Profile
Ramp rate	1.7 – 1.8 °C/sec
Reflow Time (>220 °C)	61 – 67 sec
Peak temperature	241 to 248 °C
Profile length (25 °C to peak)	4.70 minutes

Experimental Procedure and Statistical Analysis

10 circuit boards were run for each variation. Voiding area and largest void size was measured for each QFN thermal pad resulting in 4 measurements per circuit board for each QFN size. The total number of measurements for each experimental variation was 40. This was done in order to generate statistically significant data. Representative images of each voiding variation were captured.

Tukey Kramer honest significant difference (HSD) testing was done on the data sets to compare and contrast the data. Tukey Kramer HSD analysis determines whether multiple data sets are significantly different, or statistically similar. This test is similar to Student's t-test used to compare means. The output of the Tukey Kramer HSD test is a chart that shows the data sets,several data calculations and reports (Figure 8).

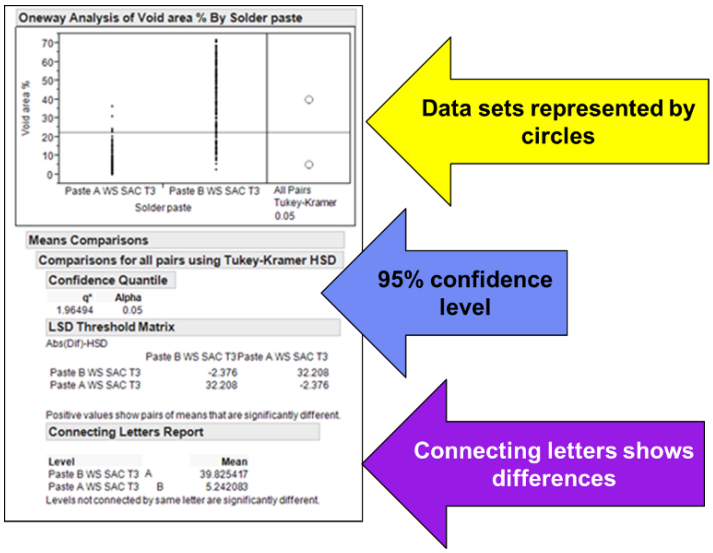


Figure 8 – Explanation of Tukey Kramer HSD Report

The Tukey Kramer HSD analysis shows whether the data sets under comparison are significantly different. This analysis is used to draw general conclusions.

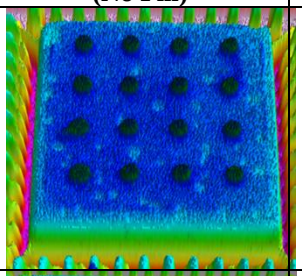
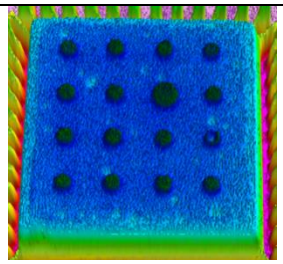
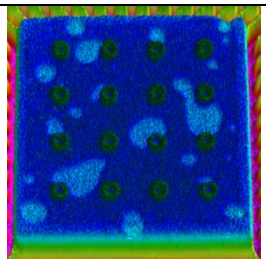
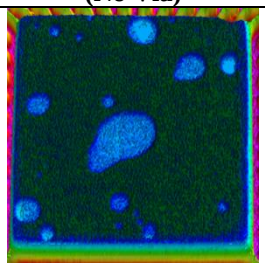
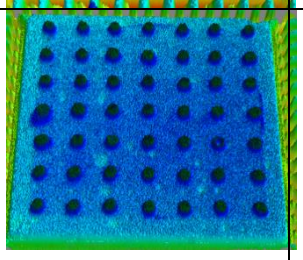
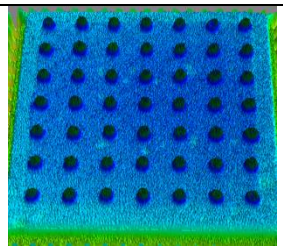
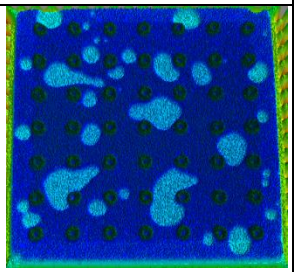
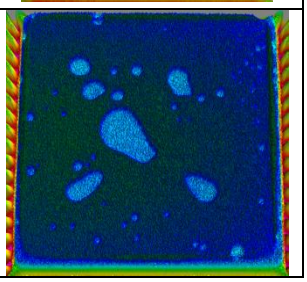
RESULTS AND DISCUSSION

The results of the voiding investigations are broken out below by variable. The results for each comparison are discussed within each section below.

Voiding Comparison of the Via Fill Options with the Standard Stencil

The different via fill options showed different voiding behavior with the standard cross hatch stencil. The X-ray images are 3D renderings which show voiding more clearly than the x-ray images themselves. The images are sorted by QFN size (7 mm and 10 mm body) and by via fill option (Table 2).

Table 2 – Voiding by Via Fill Option with the Standard Stencil

	Open Vias (No Fill)	Solder Mask Tent	Complete Plug	Flat Thermal Pad (No Via)
QFN7				
QFN10				

The 3D X-ray images show the voiding as light blue spots on the dark blue background. The darkness of the blue background is proportional to the amount of solder under the component. The lighter blue background of the open vias indicates less solder is present on the thermal pad (lower standoff height) as compared to the darker blue background of the flat thermal pad (taller standoff height). The via holes appear as dark blue to black colored dots. The open vias and solder mask tented vias showed similar voiding performance with very low voiding. The plugged vias and the flat QFN ground

pads without via holes showed much higher voiding behavior. This is similar to the results reported by Lifton [4], where higher voiding was found with plugged vias on several different component types as compared to open vias.

Analysis of the size of the largest voids shows some statistical differences in the voiding behavior of the different via plugging options (Figure 10).

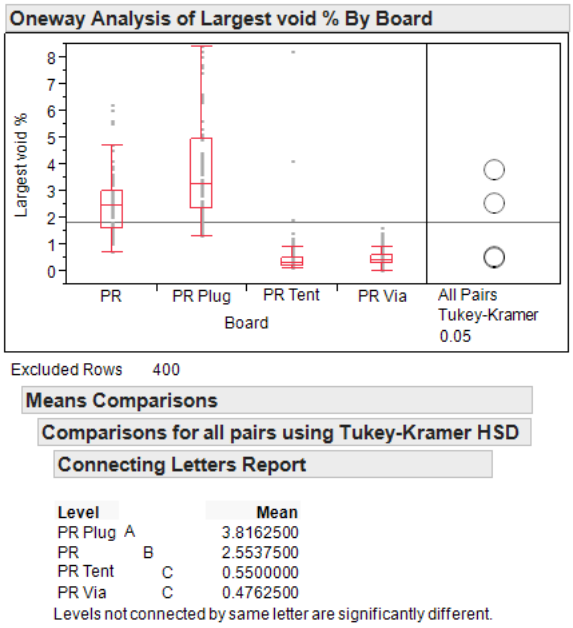


Figure 10 –Largest Voids by Via Fill Option

Larger voids were observed with completely plugged vias (PR Plug) and the flat thermal pad with no via holes (PR). The tented (PR Tent) and open vias (PR Via) showed significantly smaller voids. Visual inspection of the bottom of the circuit boards shows clearly that solder flows down the open and tented vias but not through the completely plugged via holes (Figure 11).

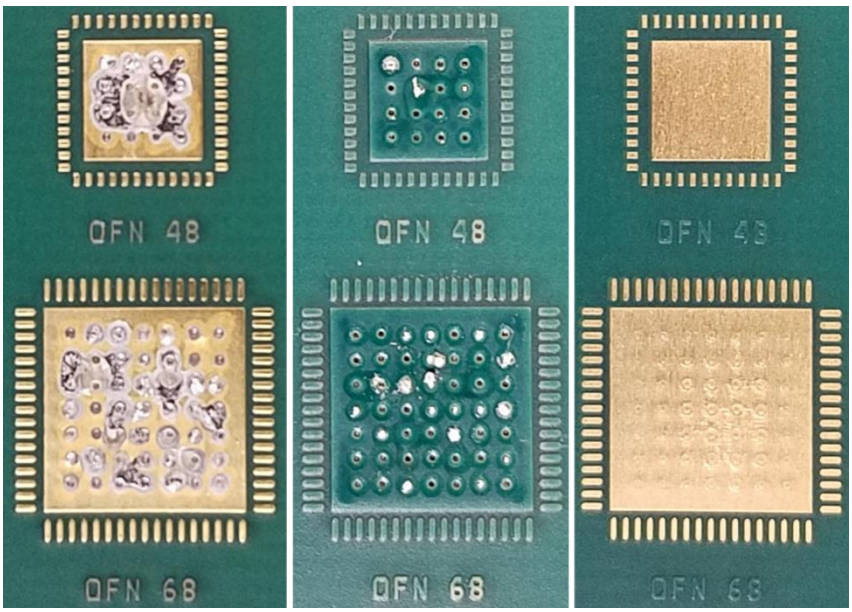


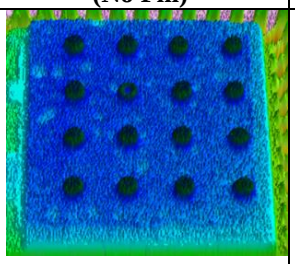
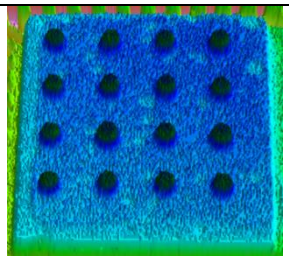
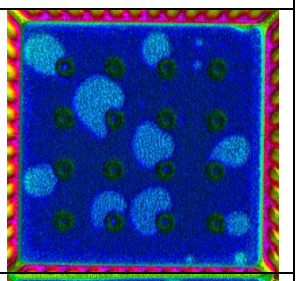
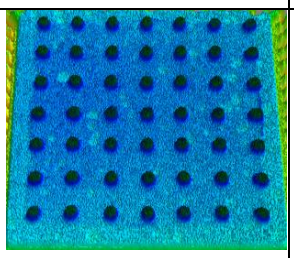
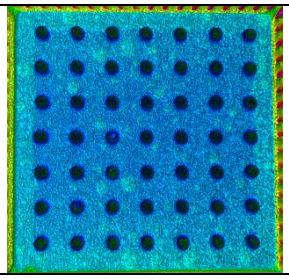
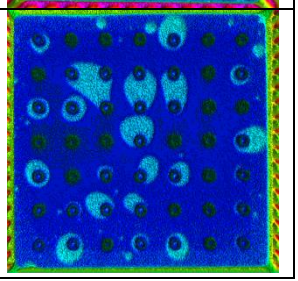
Figure 11 – Solder Flow Down to the Bottom of the Circuit Board.
Open (Left), Tented (Center), Plugged (Right)

Based on these results, solder flow down into the open vias and the tented vias tends to reduce void size. Perhaps the downward flow of solder through the via holes carries some voids out of the solder joint.

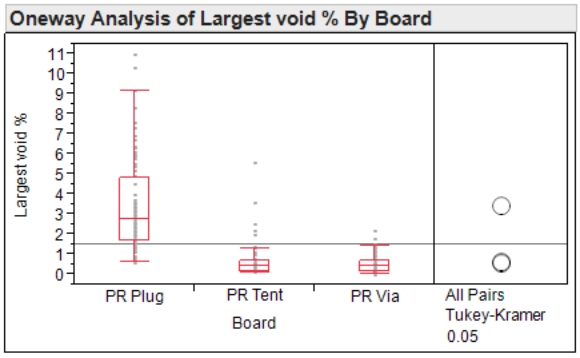
Voiding Comparison of the Via Fill Options with the Modified Stencil

The modified stencil design (Figure 6) printed solder paste around the via holes. This did not dramatically change the voiding behavior as compared to the standard stencil. Representative voiding 3D images are shown in Table 3 below.

Table 3 – Voiding by Via Fill Option with the Modified Stencil

	Open Vias (No Fill)	Solder Mask Tent	Complete Plug
QFN7			
QFN10			

The open and tented via holes showed much lower voiding than the plugged via holes with the modified stencil. Voids also appeared near the completely plugged via holes. This may be due to cool spots created by the heat sinking effect of the plugged via holes. It is possible that the solder paste near the plugged via holes reflows more slowly than the bulk of the solder paste. This could cause localized voiding at the plugged via holes. These void results are similar to what was seen with the standard window pane stencil. An analysis of largest void size again shows some statistical differences (Figure 12).



Excluded Rows 480

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level		Mean
PR Plug	A	3.4425000
PR Tent	B	0.6375000
PR Via	B	0.5575000

Levels not connected by same letter are significantly different.

Figure 12 –Largest Voids by Via Fill Option for the Modified Stencil

The plugged vias (PR Plug) resulted in larger voids than the tented (PR Tent) and open vias (PR Via). This is identical to the voiding results found with the standard stencil. Solder flow down into the via holes was affected by the stencil design. Less solder flowed to the bottom side of the boards with the modified stencil (Figure 13).

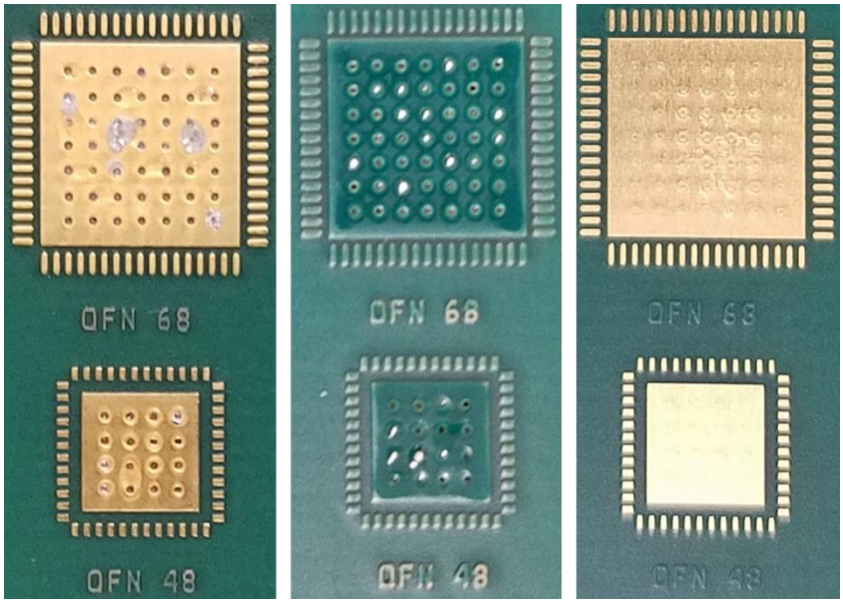


Figure 13 – Solder Flow to the Bottom of the Board for the Modified Stencil. Open (Left), Tented (Center), Plugged (Right)

Modification of the stencil design to print around the via holes definitely reduced flow of solder down the holes. Less solder flowed down the via holes with the modified stencil design, but void size was reduced in similar fashion to the standard stencil. The voids that remain trapped in the solder joint are correspondingly much smaller than what is seen with plugged via holes or a flat thermal pad without vias.

Voiding Comparison by Stencil Design

The size of the largest voids was compared by stencil design and broken out by via plugging option (Figure 14).

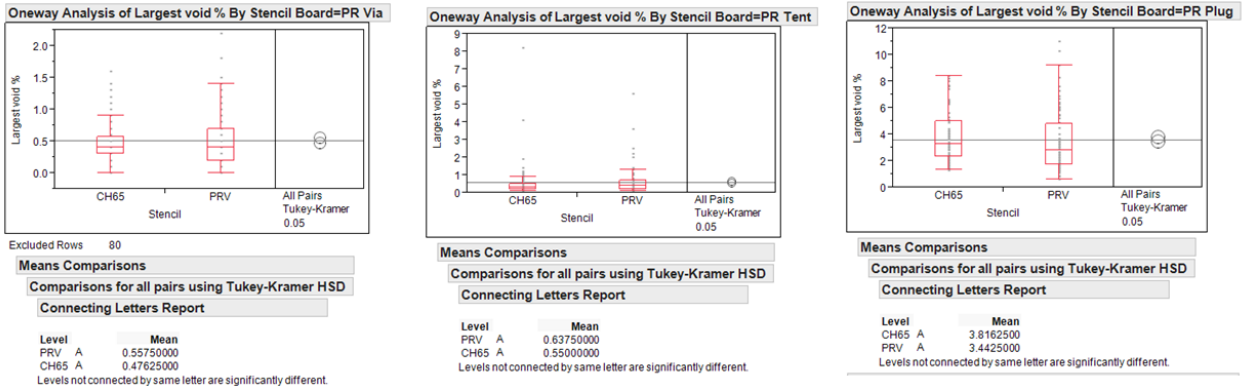


Figure 14 –Largest Voids by Stencil Design for Each Via Type. Open (Left), Tented (Center), Plugged (Right)

The Tukey Kramer analysis shows that the size of the largest voids was not affected by stencil design. This is true for each via plugging option. It is apparent from this data that the presence of open via holes in the QFN thermal pad reduces the size of the voids regardless of stencil design.

Voiding Behavior by QFN Size

The size of the QFN has an effect on size of the largest voids (Figure 15).

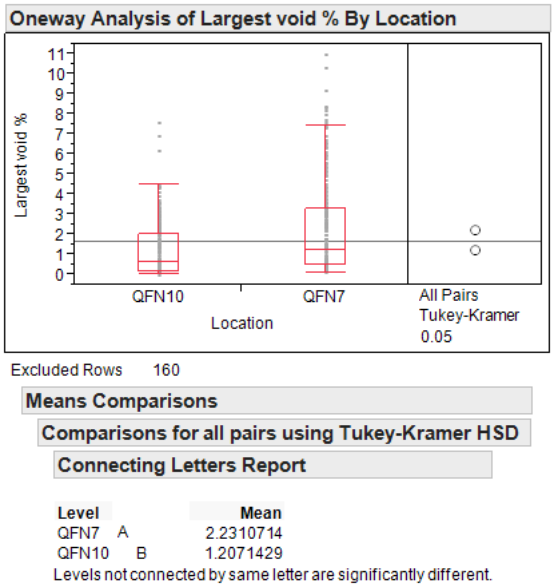


Figure 15 –Largest Voids by QFN Size

Voids were larger for the 7 mm body QFN than for the 10 mm body QFN. This is true regardless of the different via in pad plugging options. The overall void area also varied by QFN size (Figure 16).

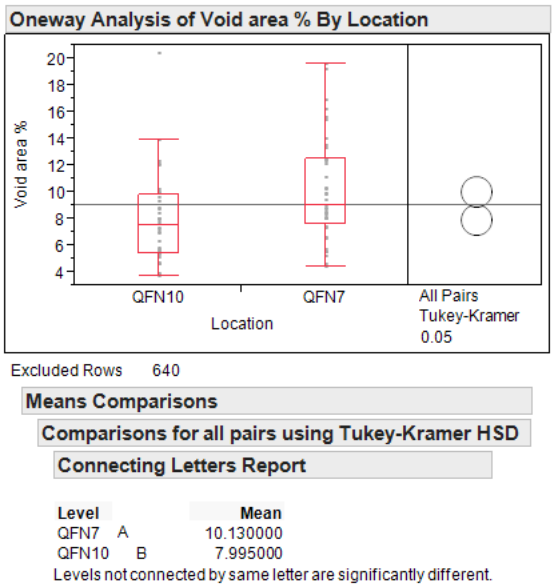


Figure 16 –Void Area by QFN Size

This analysis was run on the test boards with flat QFN pads (no via holes) and the standard stencil design with 65% area. It is apparent that the 7 mm QFN gives higher void area than the 10 mm QFN. Void size was also larger for the 7 mm QFN.

Recommendations to "Fill the Void"

Based on the data presented in this paper, here are some recommendations to fill the void.

- Void size can be reduced through the use of via holes in QFN thermal pads.
- Modifications to the stencil design limits the amount of solder that flows down through the via holes.
- Use of larger QFNs may result in lower overall voiding area.

CONCLUSIONS

Voiding in QFN thermal pad solder joints is affected by via holes in the thermal pad. Open or tented via holes tend to reduce void size. Plugging the vias tends to give slightly larger voids than a flat thermal pad without via holes. Modification of the

stencil to print solder paste around the via holes limits the amount of solder that flows down into the via holes, but did not affect void size. Due to the commonplace use of bottom terminated components, it is clear that voiding will be an issue that many must address. The authors will continue to study factors that influence voiding in an effort to help the reader to "Fill the Void".

FUTURE WORK

Work to find mitigation strategies to lower voiding in solder joints is ongoing. Data will be presented at future technical conferences.

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FILL THE VOID IV: ELIMINATION OF INTER-VIA VOIDING

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OUTLINE

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- Methodology
- Voiding Results
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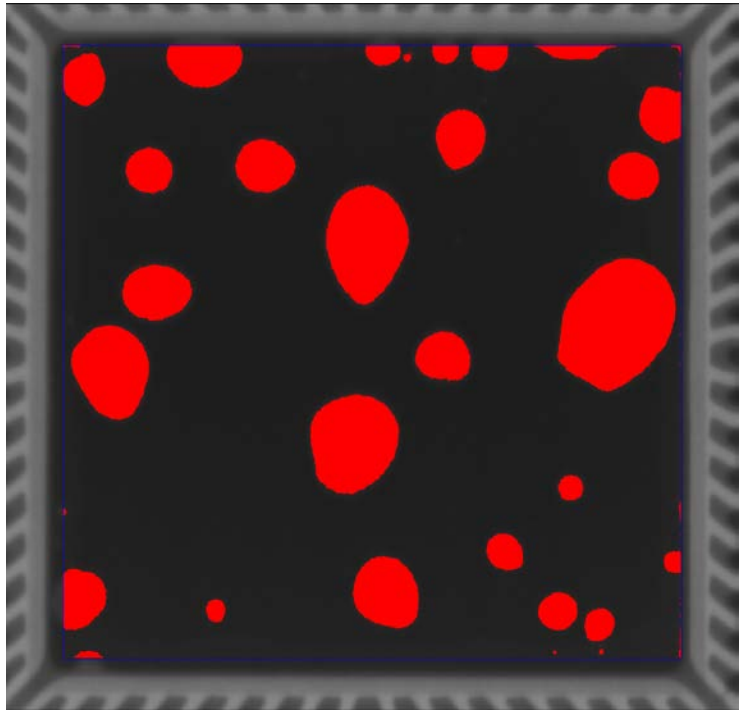
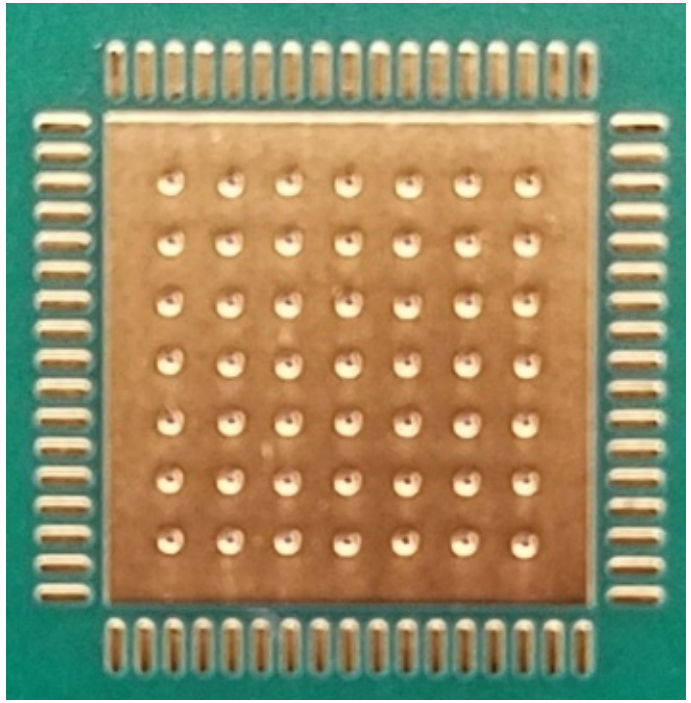
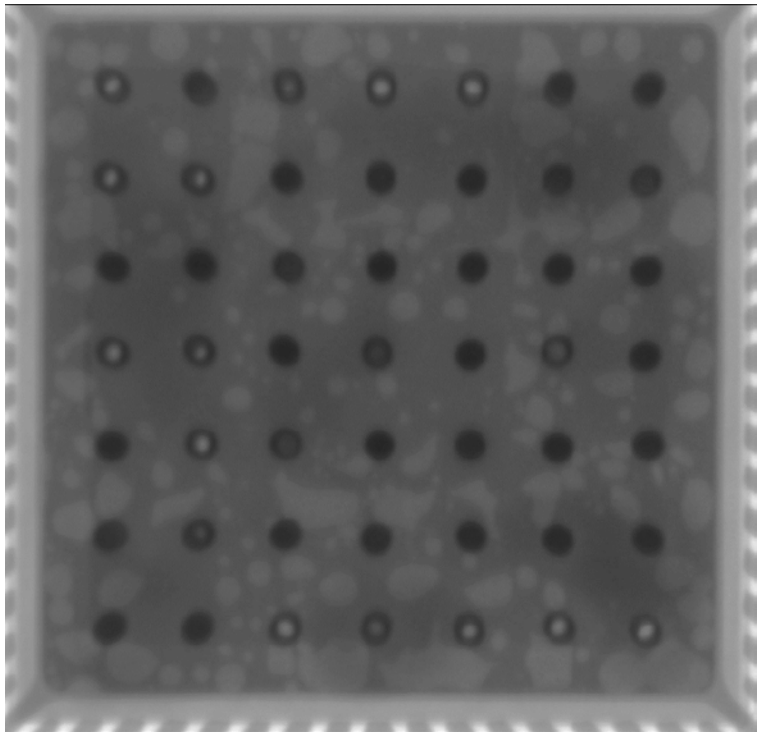
- Thank You & Questions

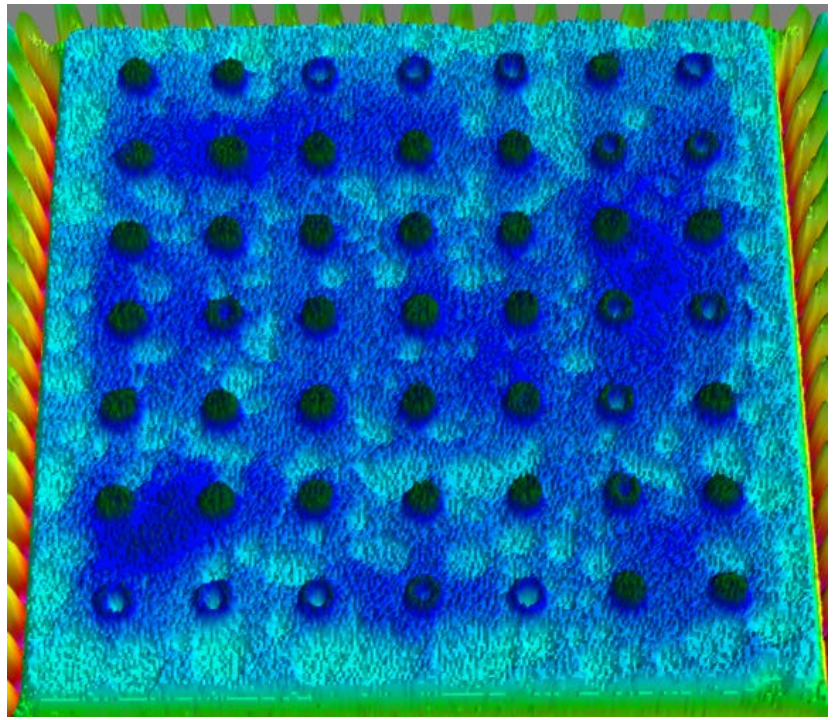


INTRODUCTION

INTRODUCTION ON VOIDING

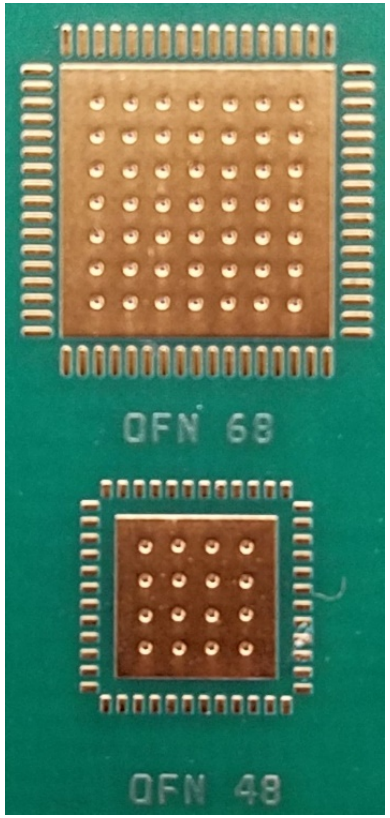


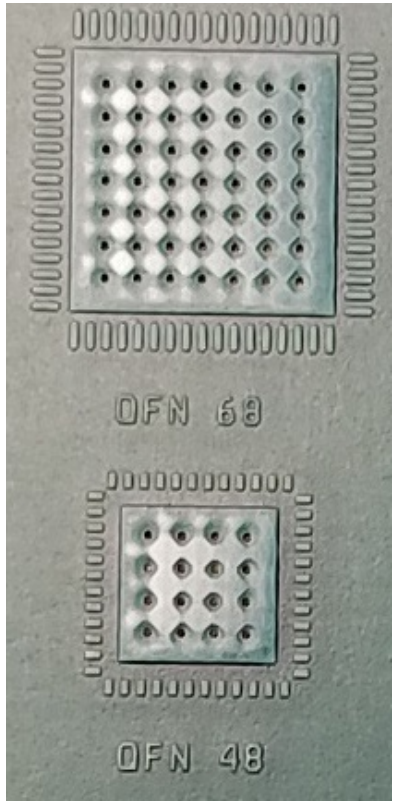


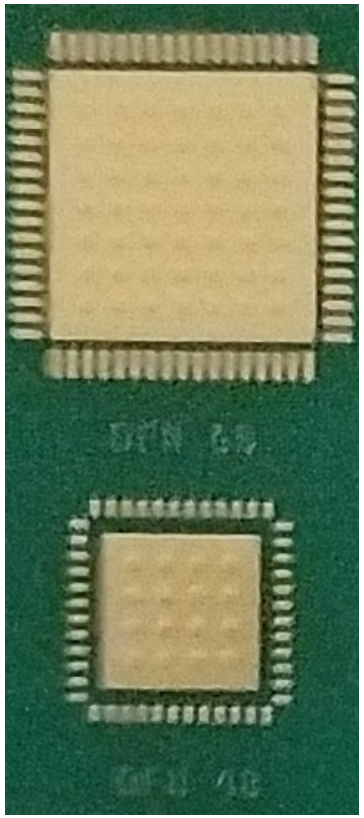


Voiding is Common for QFN Thermal Pads with Via Holes

FACTORS THAT INFLUENCE VOIDING FOR VIA-IN-PAD DESIGNS

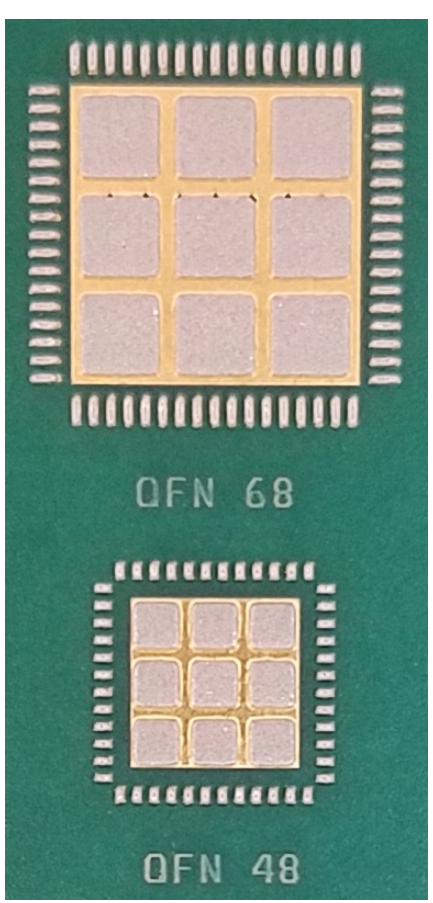


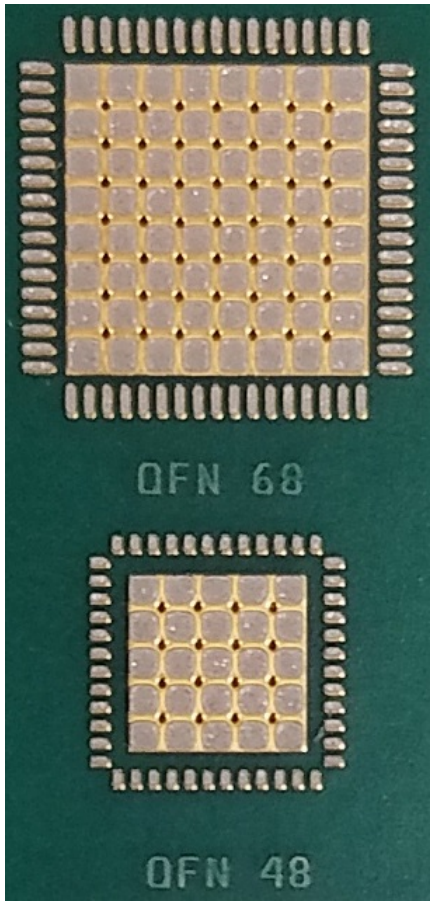




Via Hole Plugging Options: Open, S/M Tent, Plugged

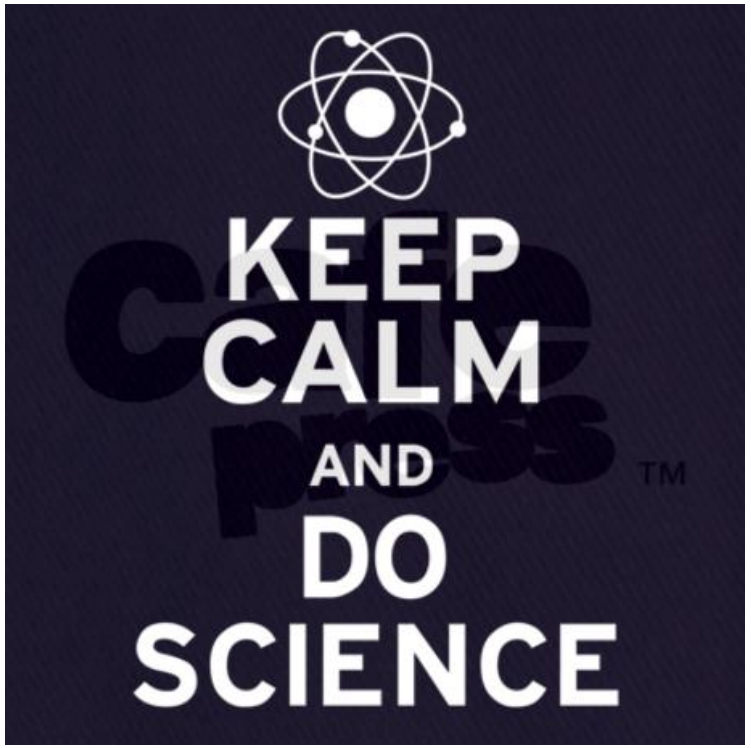
FACTORS THAT INFLUENCE VOIDING FOR VIA-IN-PAD DESIGNS



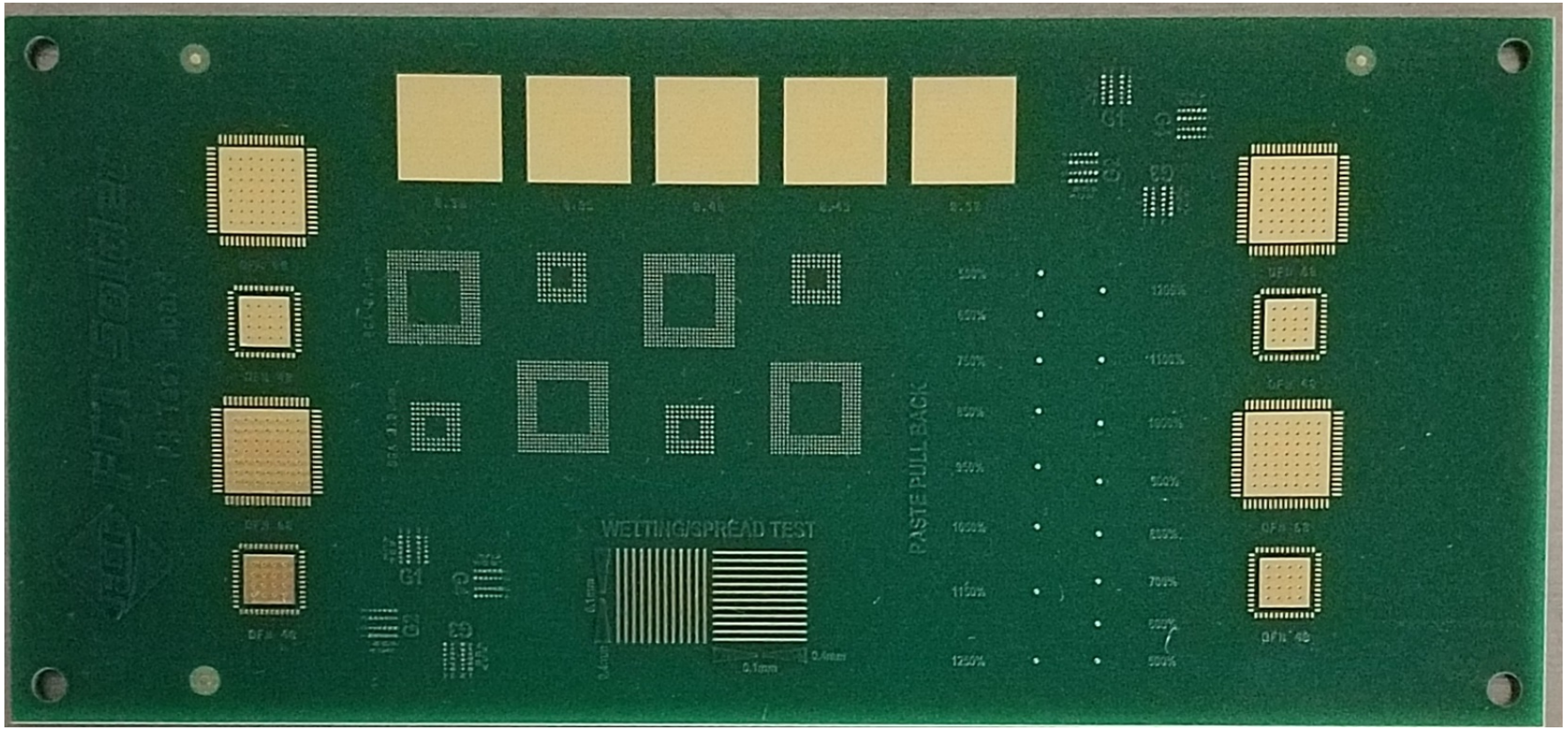


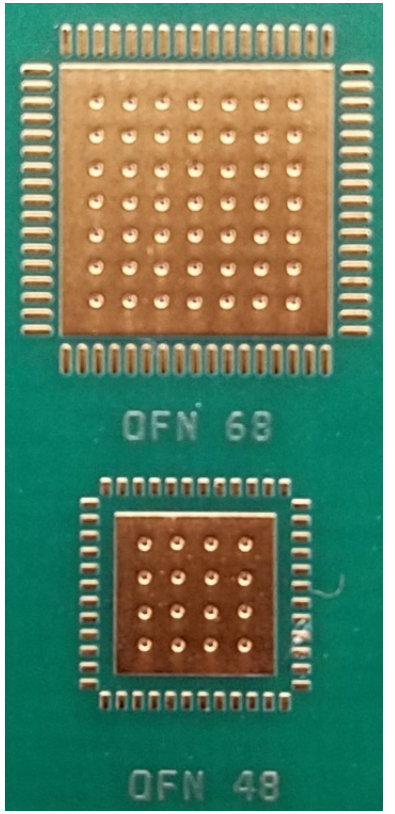
Solder Paste Print Options: Print over Vias, Print around Vias

METHODOLOGY



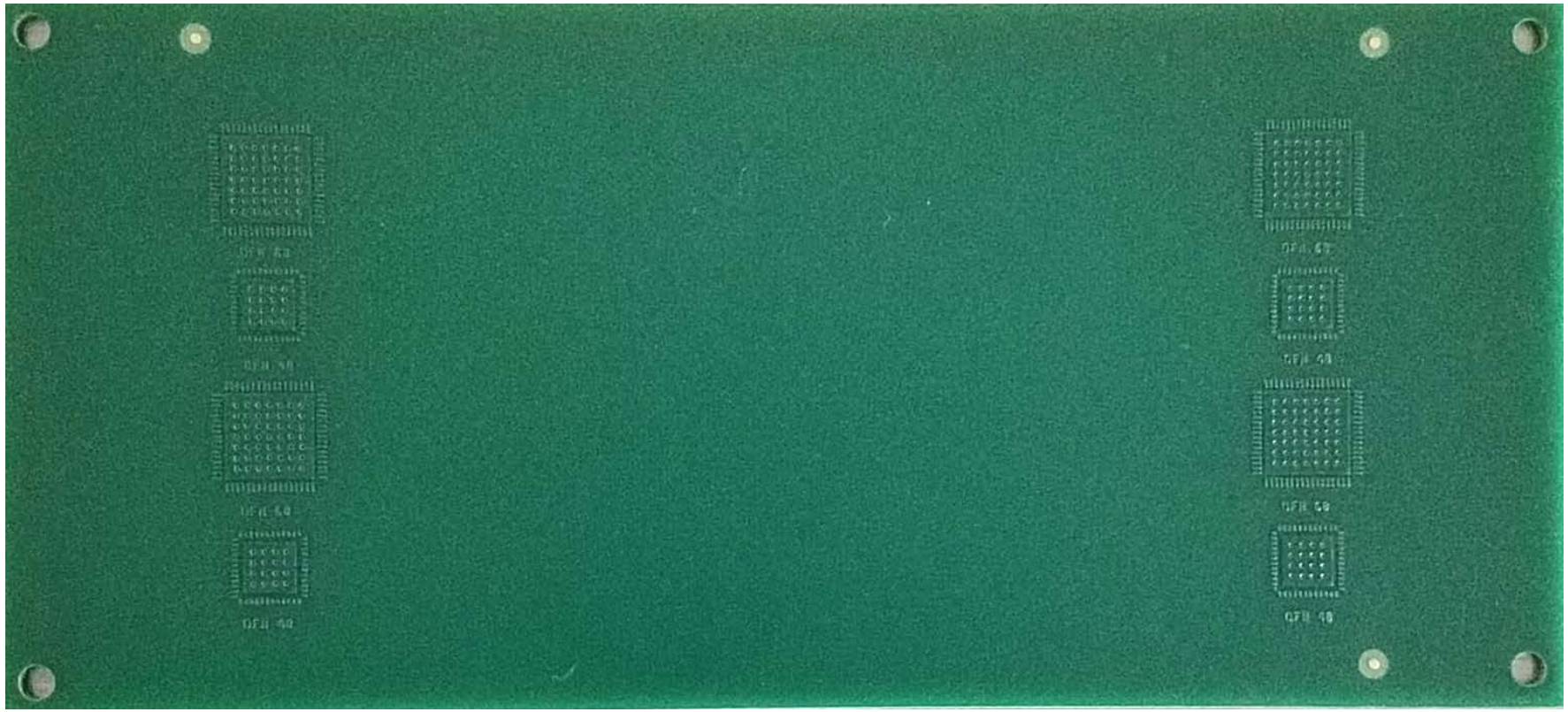
METHODOLOGY – CIRCUIT BOARDS

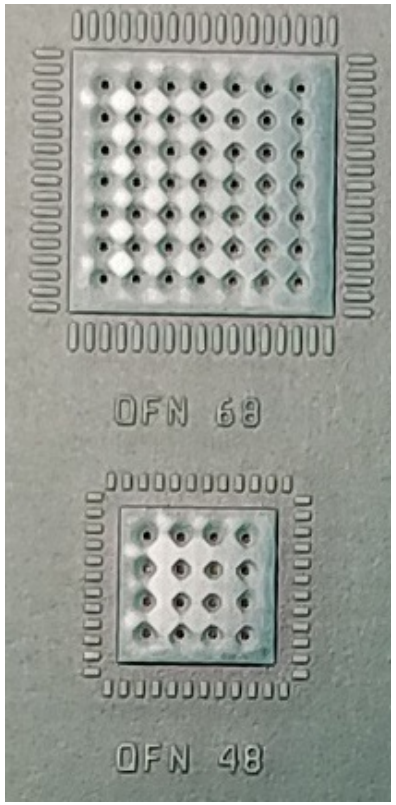




PR Test Board with Via in Pad (0.3 mm = 12 mil vias), Plated with ENIG

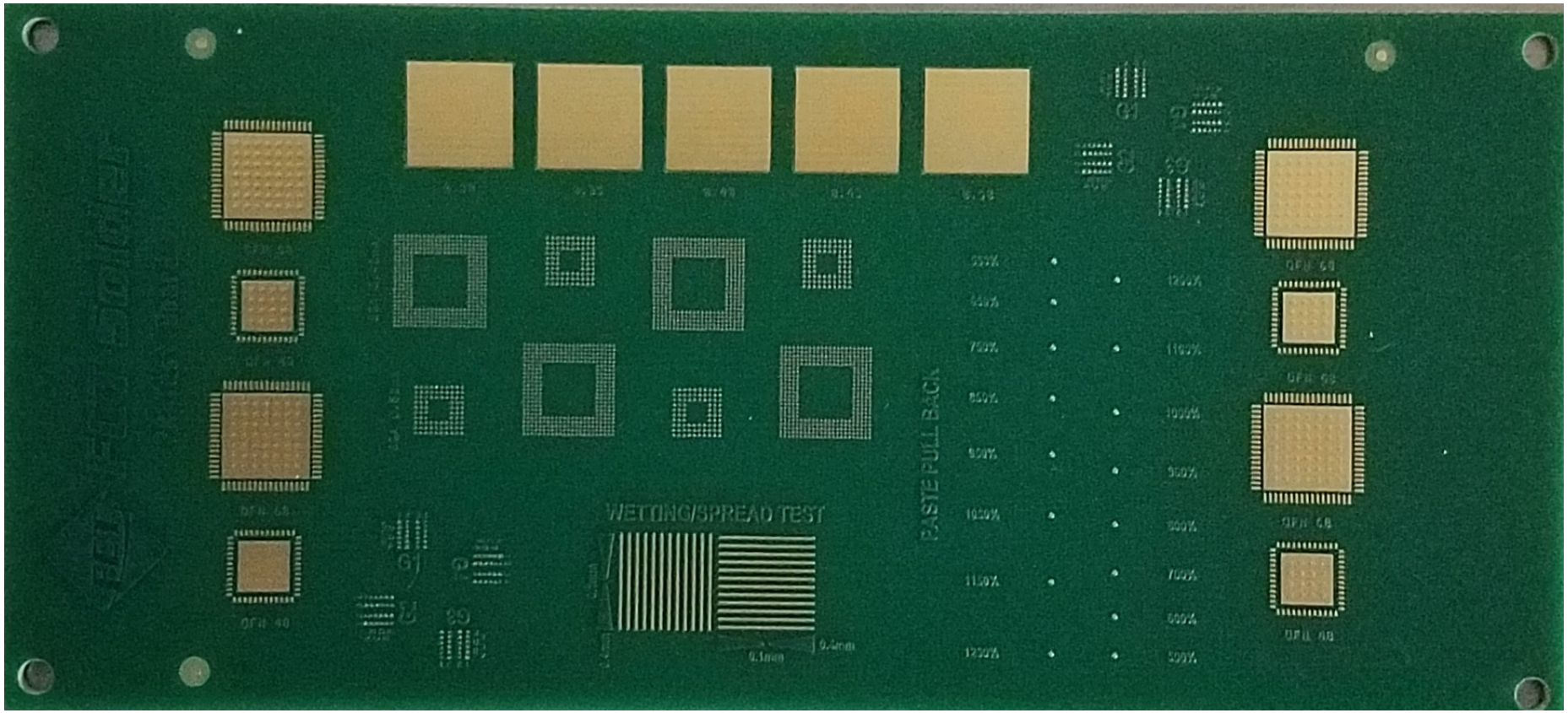
METHODOLOGY – CIRCUIT BOARDS

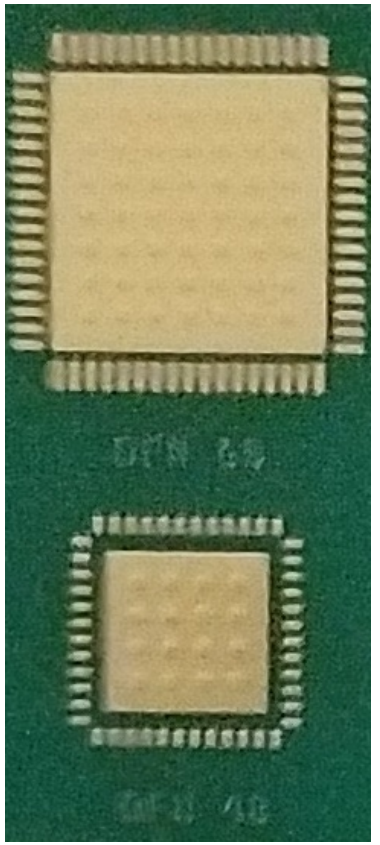




PR Test Board with a Solder Mask Tent on the Bottom Side

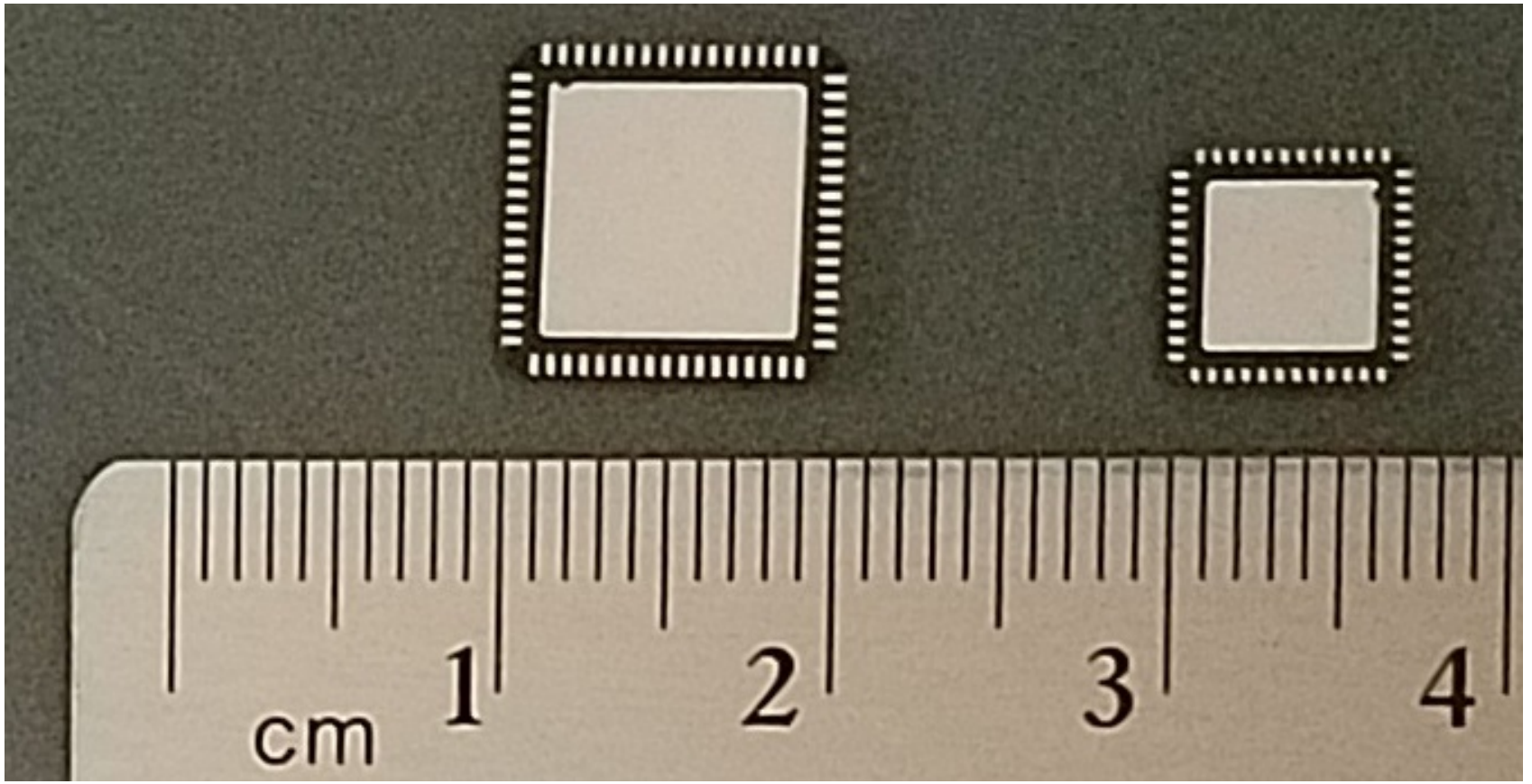
METHODOLOGY – CIRCUIT BOARDS





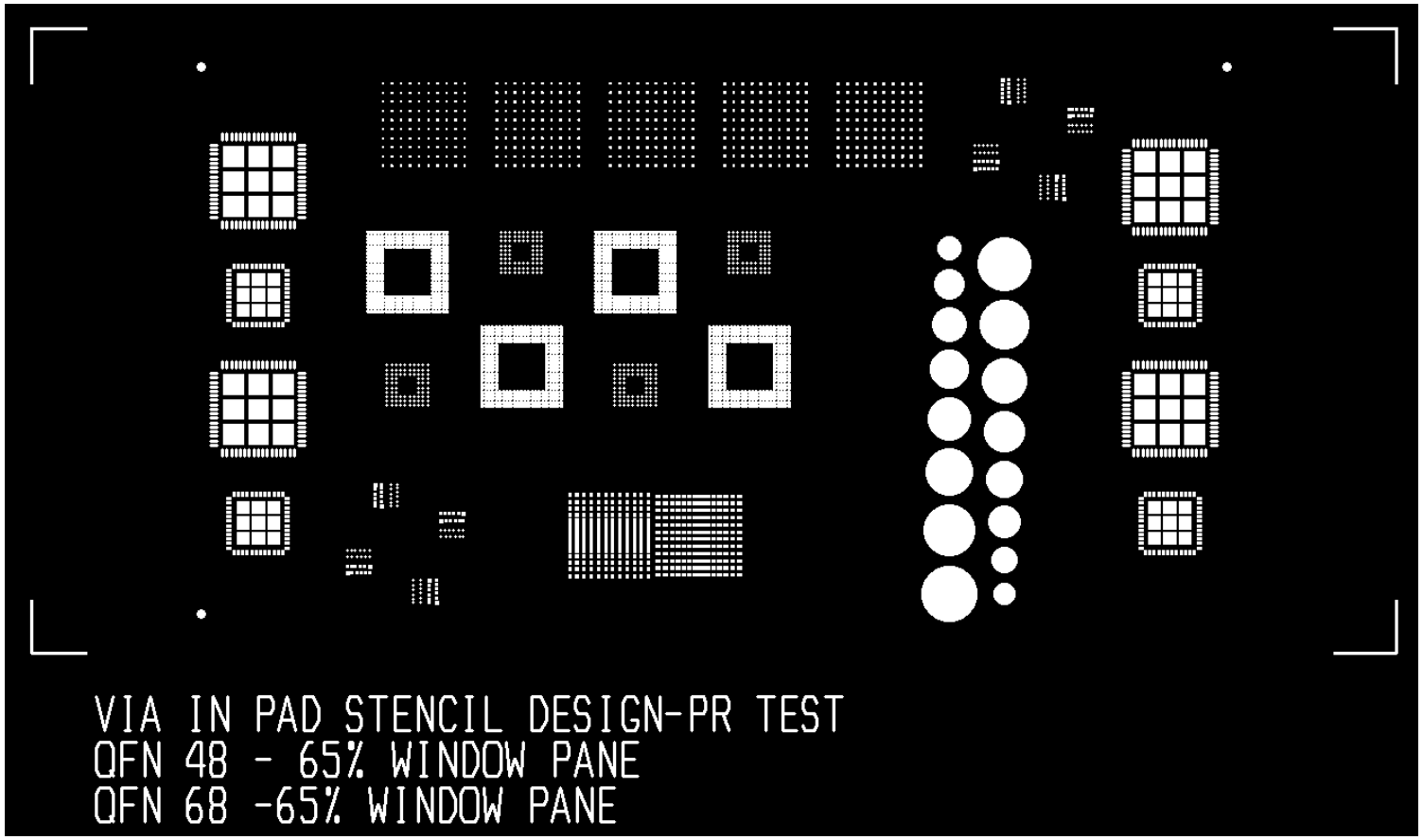
PR Test Board with Non-Conductive Via Fill, Plated with Cu and ENIG

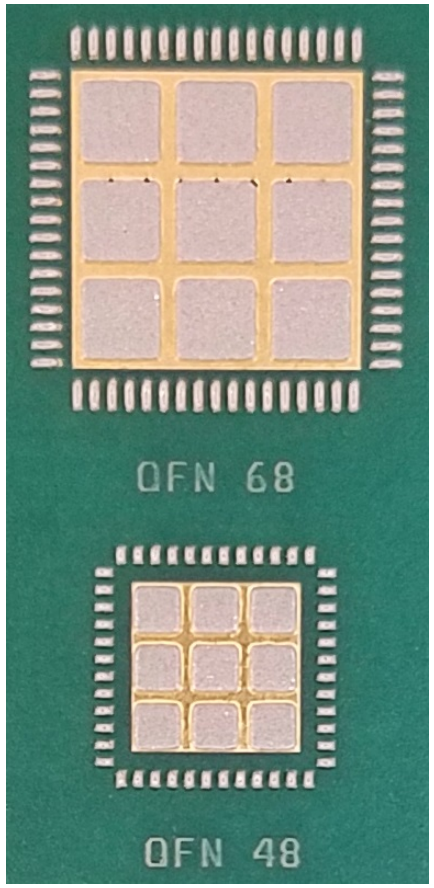
METHODOLOGY – QFN COMPONENTS



QFN Components: 10 mm body (68 lead) and 7 mm body (48 lead). Matte Tin Finish

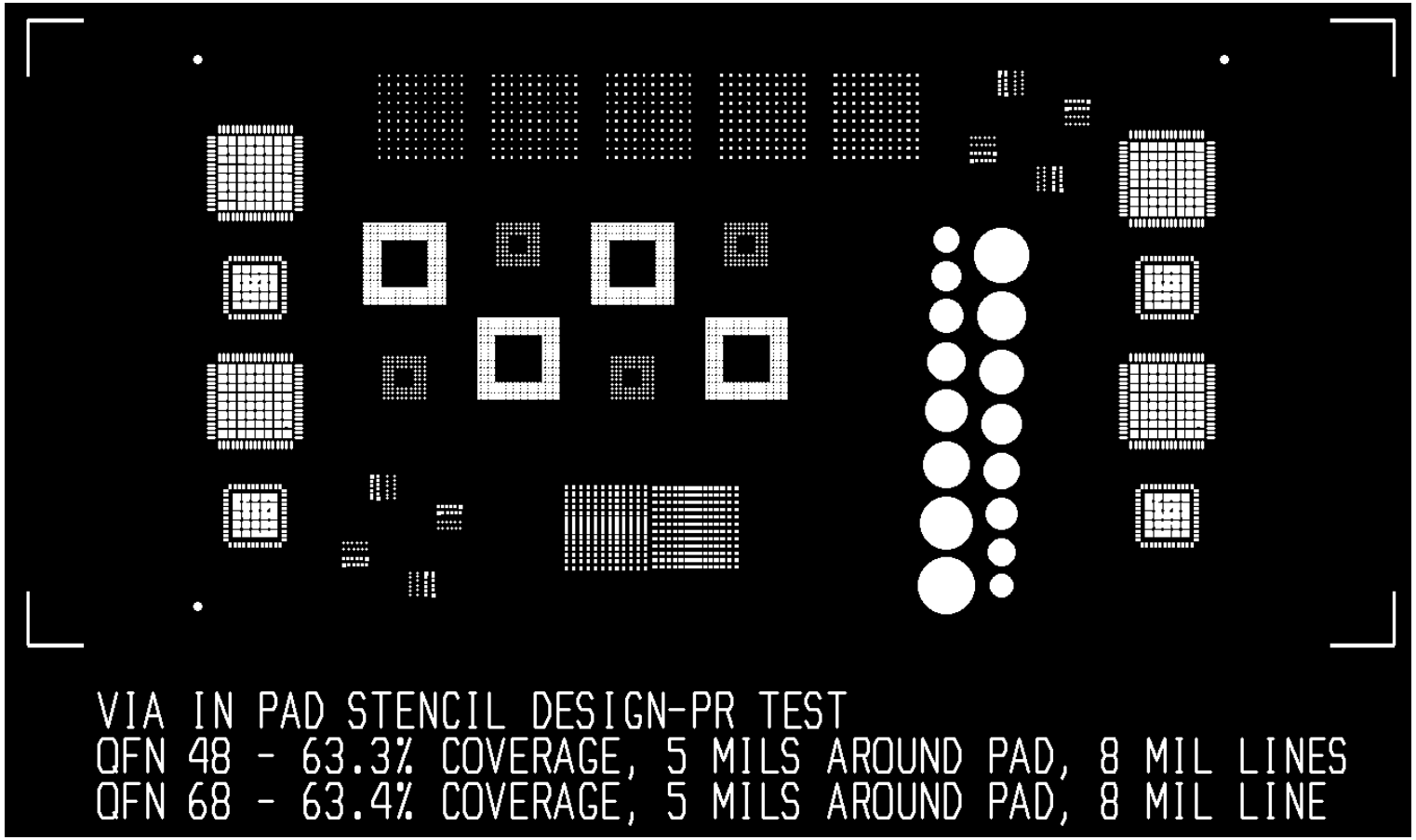
METHODOLOGY – STANDARD STENCIL

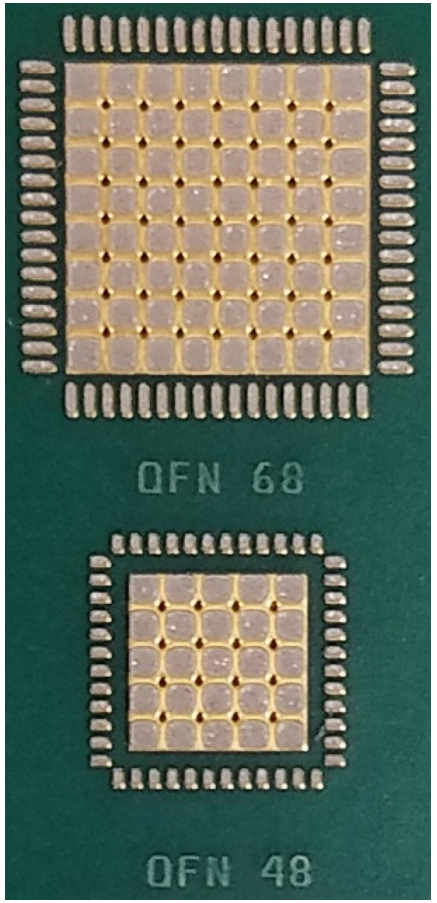




Standard Solder Paste Print: 65% Area Window Pane. Printed Over Via Holes

METHODOLOGY – MODIFIED STENCIL

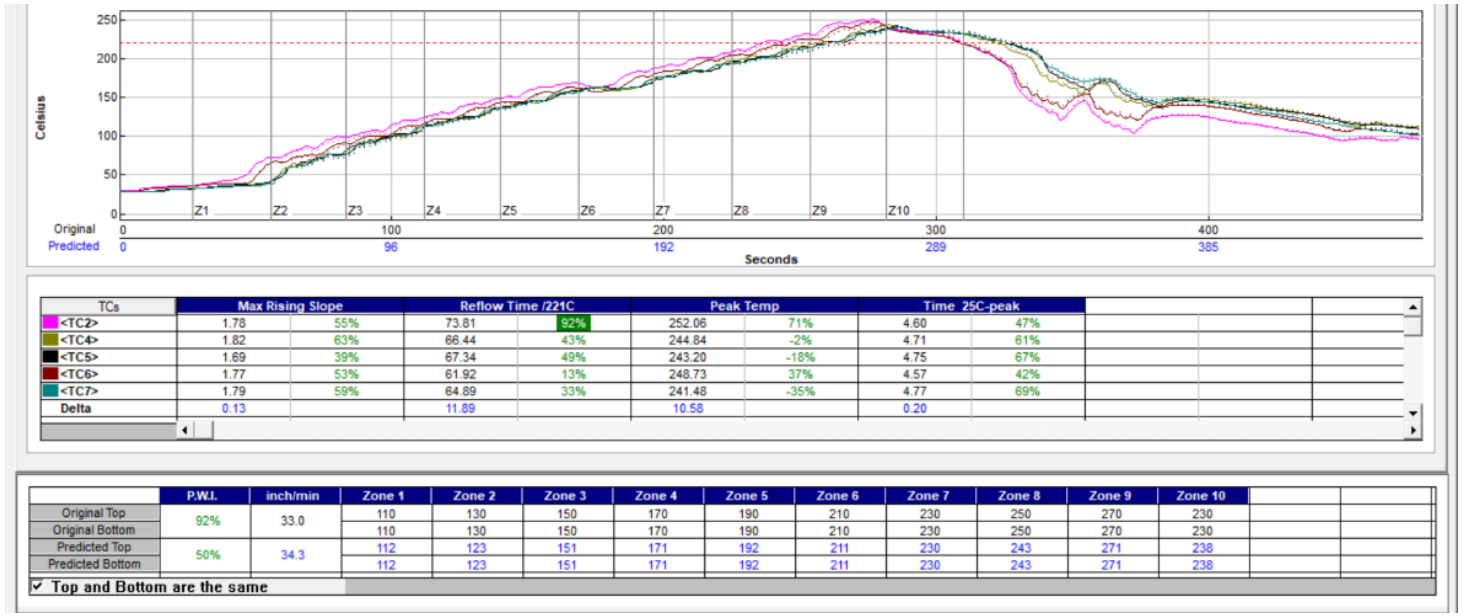




Modified Solder Paste Print: 63% Area Grid. Printed Around Via Holes

METHODOLOGY – SOLDER PASTE AND REFLOW

No Clean SAC305 Type 3 Solder Paste



TCs	Max Rising Slope		Reflow Time /221C		Peak Temp		Time 25C-peak	
<TC2>	1.78	55%	73.81	92%	252.06	71%	4.60	47%
<TC4>	1.82	63%	66.44	43%	244.84	-2%	4.71	61%
<TC5>	1.69	39%	67.34	49%	243.20	-18%	4.75	67%
<TC6>	1.77	53%	61.92	13%	248.73	37%	4.57	42%
<TC7>	1.79	59%	64.89	33%	241.48	-35%	4.77	69%
Delta	0.13		11.89		10.58		0.20	

	P.W.I.	inch/min	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6	Zone 7	Zone 8	Zone 9	Zone 10
Original Top	92%	33.0	110	130	150	170	190	210	230	250	270	230
Original Bottom			110	130	150	170	190	210	230	250	270	230
Predicted Top	50%	34.3	112	123	151	171	192	211	230	243	271	238
Predicted Bottom			112	123	151	171	192	211	230	243	271	238

☑ Top and Bottom are the same

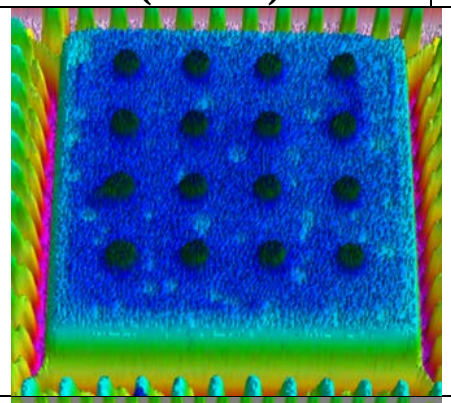
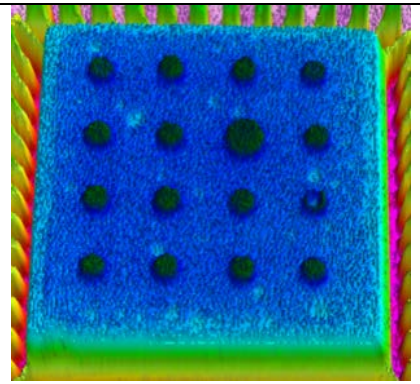
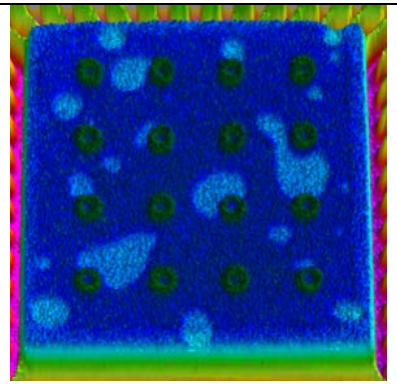
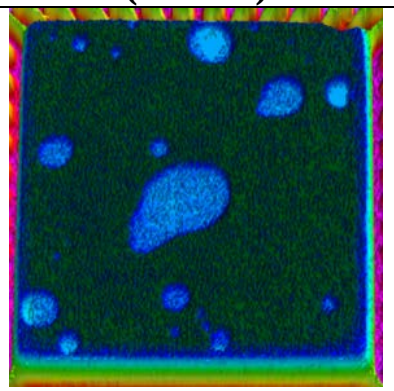
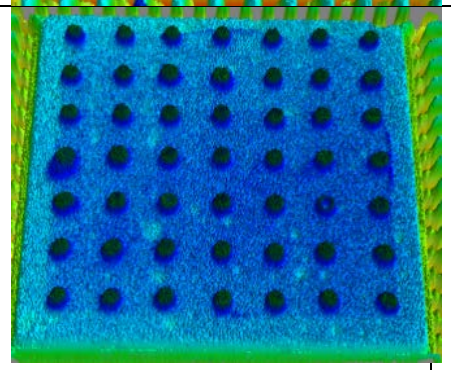
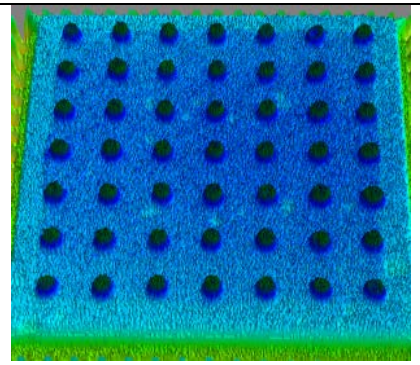
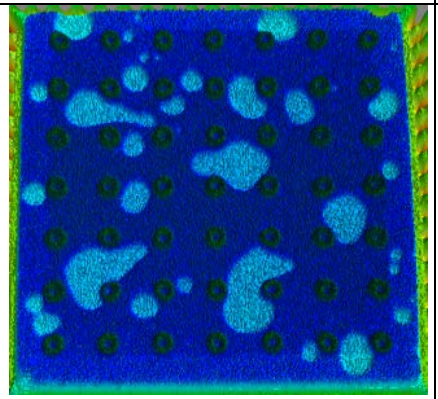
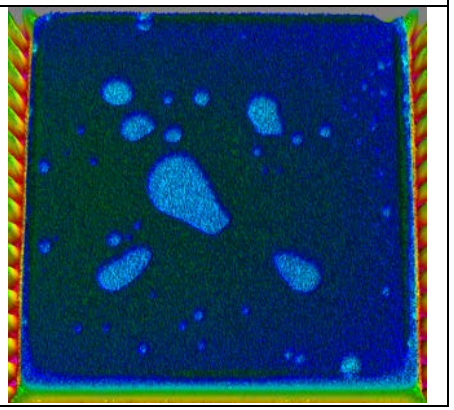
Setting	RTS Profile
Ramp rate	1.7 – 1.8 °C/sec
Reflow Time (> 220 °C)	61 – 67 sec
Peak temperature	241 to 248 °C
Profile length (25 °C to peak)	4.70 minutes

METHODOLOGY – EXPERIMENTAL PROCEDURE

- 10 Circuit Boards For Each Variation
- 4 of Each QFN Size Placed and Boards were Reflowed
- Void Area and Largest Size Measured on Each QFN
- Images were Taken of Representative QFN Voiding
- Data was Analyzed and Statistics Generated

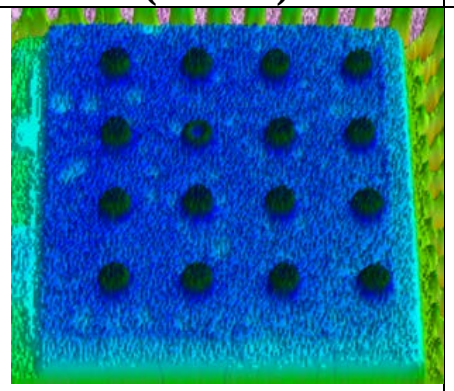
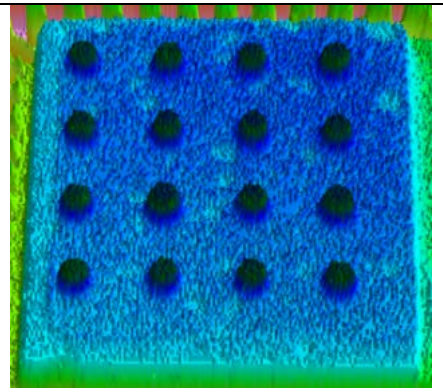
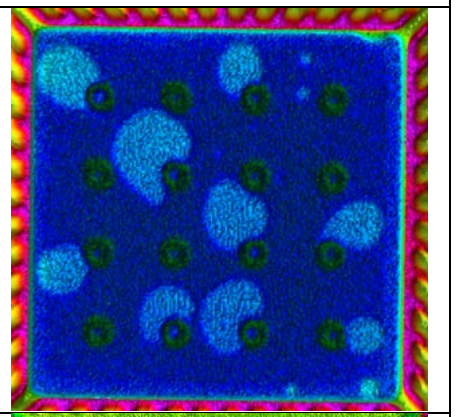
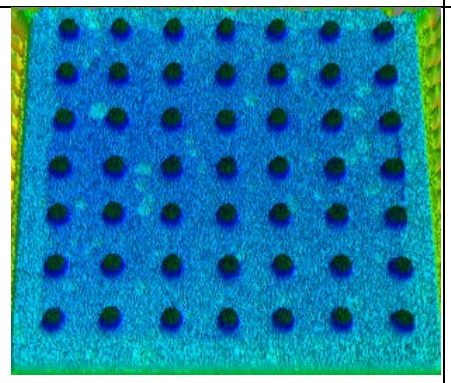
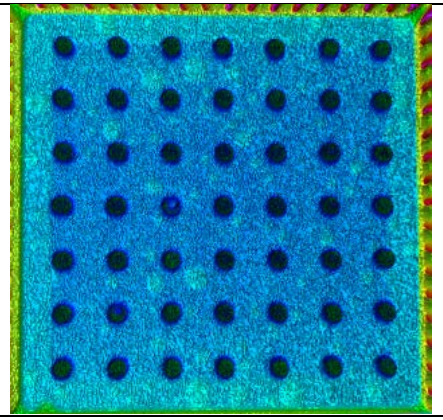
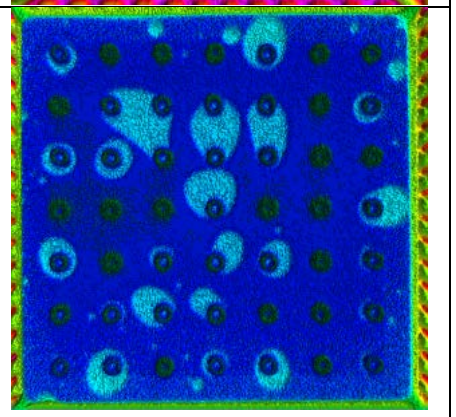
VOIDING RESULTS

VOIDING RESULTS – VIA FILL OPTIONS, STANDARD STENCIL

	Open Vias (No Fill)	Solder Mask Tent	Complete Plug	Flat Thermal Pad (No Via)
QFN7				
QFN10				

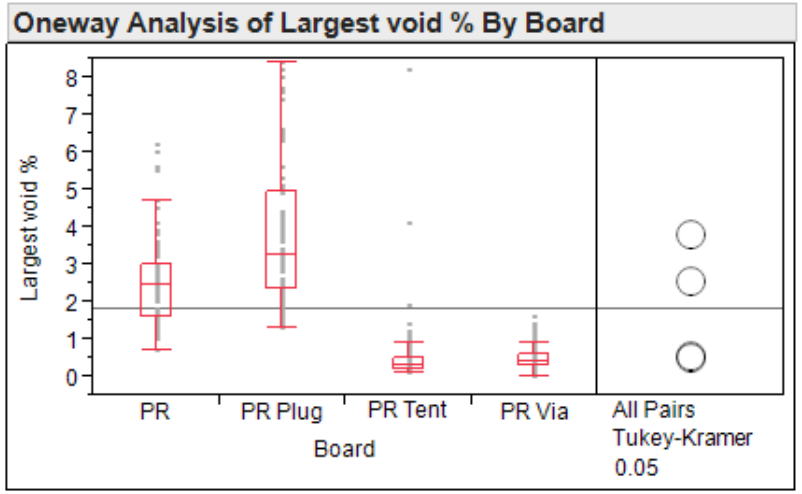
3D Voiding Images: Open Vias = Lower Voiding, Plugged and No Vias = More Voiding

VOIDING RESULTS – VIA FILL OPTIONS, MODIFIED STENCIL

	Open Vias (No Fill)	Solder Mask Tent	Complete Plug
QFN7			
QFN10			

3D Voiding Images: Open Vias = Lower Voiding, Plugged Vias = More Voiding

VOIDING SIZE – BY STENCIL



Excluded Rows 400

Means Comparisons

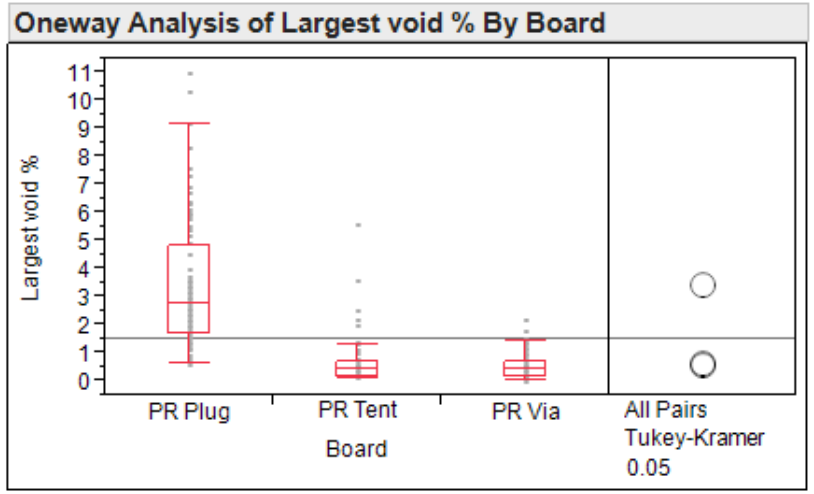
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level		Mean
PR Plug	A	3.8162500
PR	B	2.5537500
PR Tent	C	0.5500000
PR Via	C	0.4762500

Levels not connected by same letter are significantly different.

STANDARD STENCIL



Excluded Rows 480

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

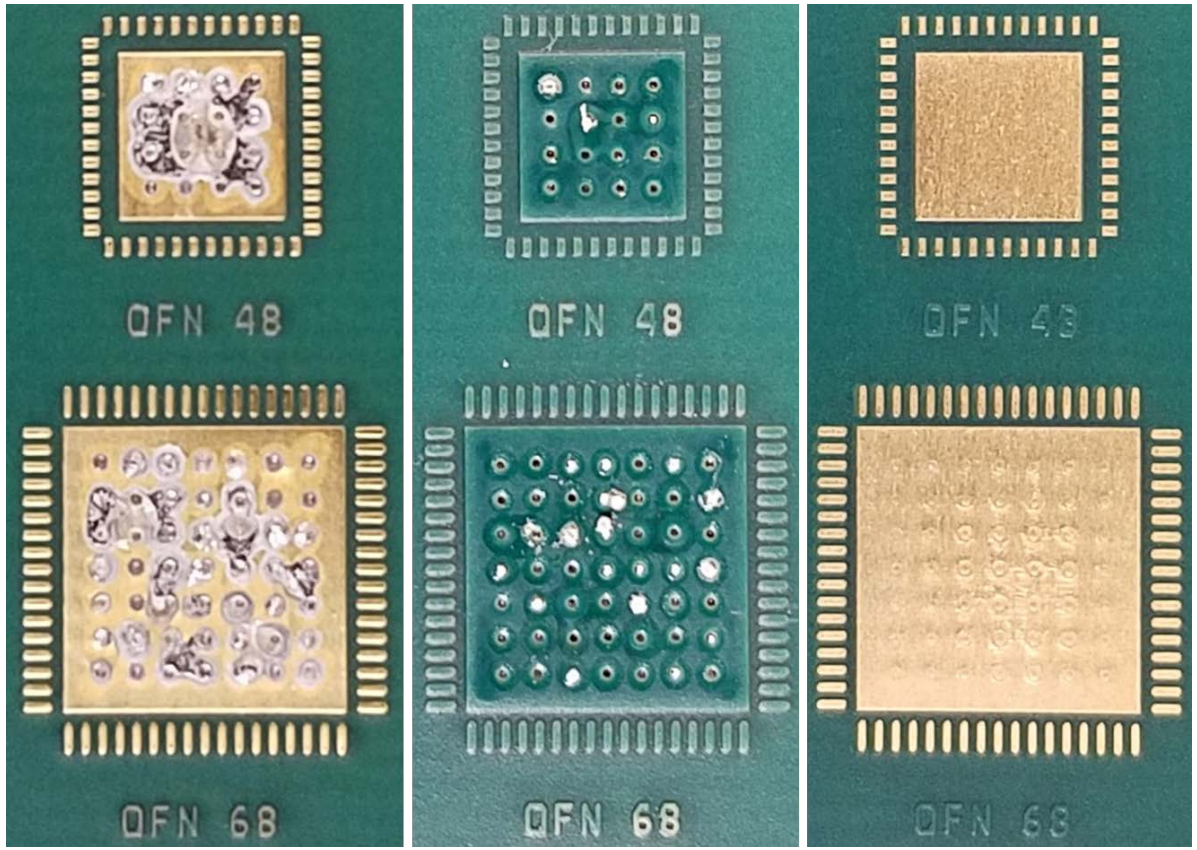
Level		Mean
PR Plug	A	3.4425000
PR Tent	B	0.6375000
PR Via	B	0.5575000

Levels not connected by same letter are significantly different.

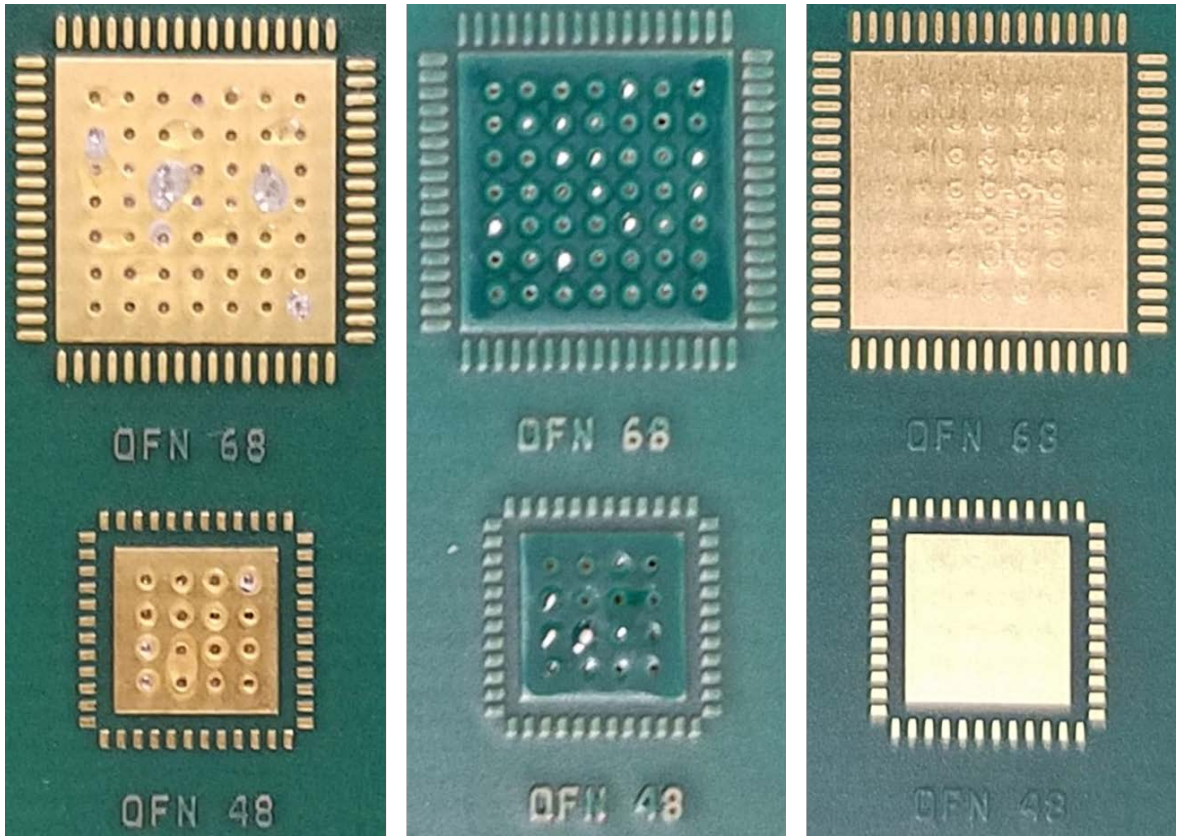
MODIFIED STENCIL

PR = Flat Pad (No Vias)
PR Plug = Plugged Vias
PR Tent = S/M Tented Vias
PR Via = Open Vias

SOLDER FLOW TO THE BOTTOM OF THE BOARD

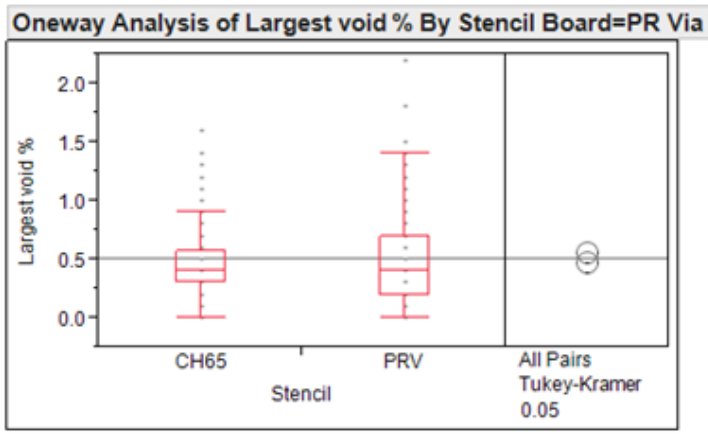


STANDARD STENCIL



MODIFIED STENCIL

VOIDING SIZE BY STENCIL DESIGN FOR EACH VIA TYPE



Excluded Rows 80

Means Comparisons

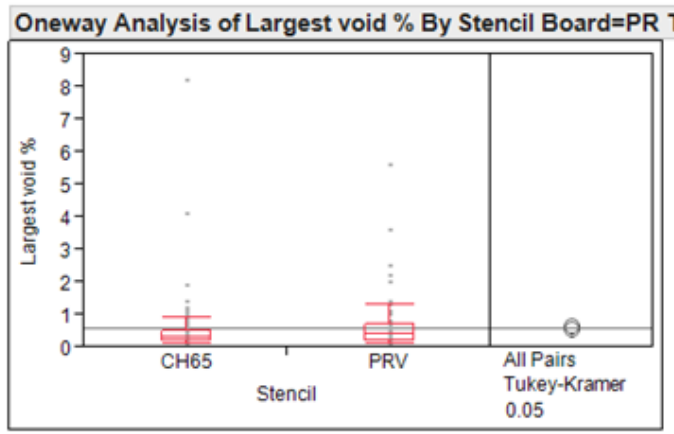
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level		Mean
PRV	A	0.55750000
CH65	A	0.47625000

Levels not connected by same letter are significantly different.

OPEN VIAS



Means Comparisons

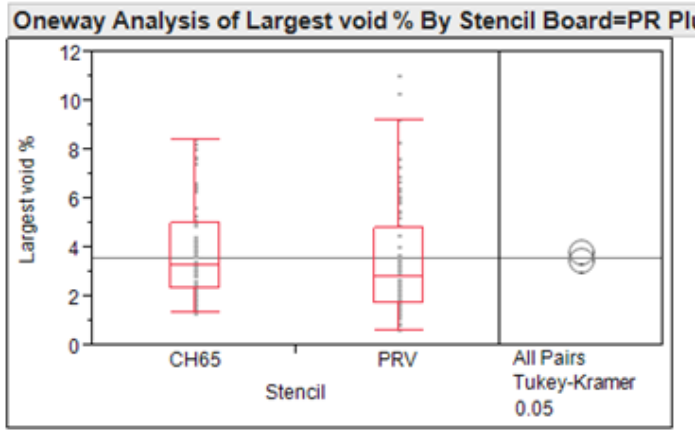
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level		Mean
PRV	A	0.63750000
CH65	A	0.55000000

Levels not connected by same letter are significantly different.

TENTED VIAS



Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

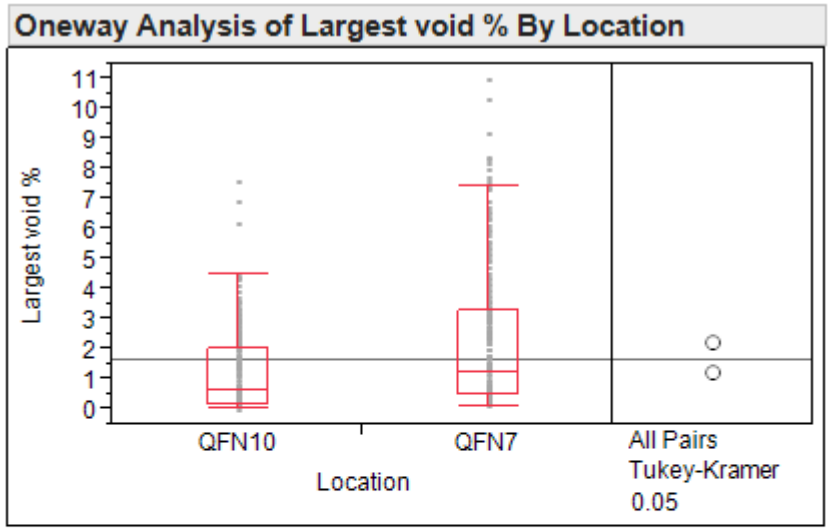
Connecting Letters Report

Level		Mean
CH65	A	3.8162500
PRV	A	3.4425000

Levels not connected by same letter are significantly different.

PLUGGED VIAS

VOIDING BY QFN SIZE



Excluded Rows 160

Means Comparisons

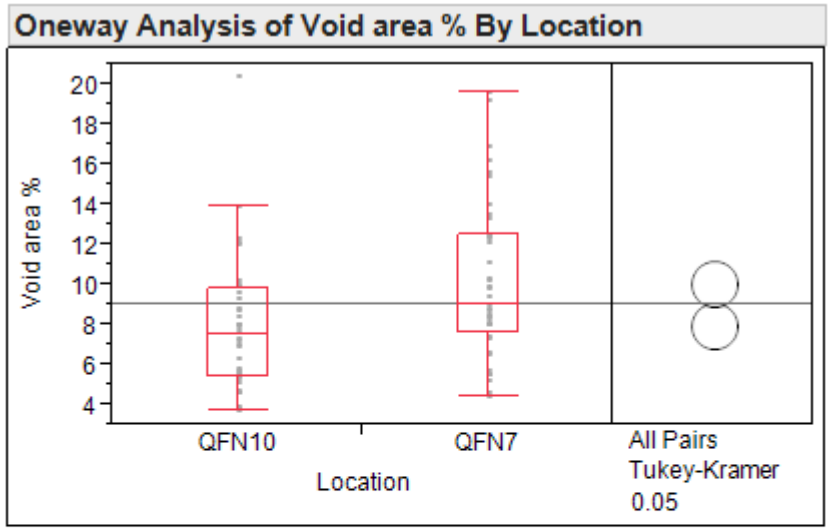
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level		Mean
QFN7	A	2.2310714
QFN10	B	1.2071429

Levels not connected by same letter are significantly different.

LARGEST VOID SIZE



Excluded Rows 640

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level		Mean
QFN7	A	10.130000
QFN10	B	7.995000

Levels not connected by same letter are significantly different.

VOID AREA

Standard Stencil (65%)
Flat QFN Pads – No Vias
QFN10 Mass = 2x QFN7

FILL THE VOID

RECOMMENDATIONS TO FILL THE VOID

- Void size can be reduced using via holes in QFN thermal pads.
- Modifications to the stencil design limits the amount of solder flow through the via holes.
- Use of larger QFN's may reduce overall voiding.

Via holes in QFN thermal pads certainly influence voiding!

FUTURE WORK

Work on mitigation strategies to reduce voiding is ongoing.

Data will be presented at future technical conferences.

ACKNOWLEDGEMENTS

Greg Smith with BlueRing Stencils designed and supplied the stencils used in this work.

Tony Lentz

FCT Assembly

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