Voids in SMT Solder Joints – Myths Revisited

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1 Introduction

Since the introduction of lead-free soldering technology, voids in solder joints have been a topic of intensive investigations and discussions. One issue of detailed investigations is the formation mechanism of voids in solder joints. The objective of these activities is the assessment, if and how voids can be reduced to a low or at least acceptable level. The second question for deeper analyses is the effect of voids on solder joint reliability. If the potential for elimination or reduction of voids in solder joints is found to be low, this question comes automatically into focus. Especially within the automotive industry or other business sectors with high reliability requirements for electronic assemblies the relevance of voids for product reliability is still a matter of debate. This is why this paper tries to give a general overview of mechanisms governing void formation, an assessment of the relevance of different influencing parameters on void formation as well as an assessment of the effects of voids on solder-joint reliability. Widely known facts or findings from other studies are combined with additional studies on issues of special interest.

The whole paper wants to explain current understanding of solder joint voiding, primarily as an insight on this topic from the perspective of an automotive supplier, but in a next step also as a statement and input for further discussions within scientific and technological working groups dealing with this issue.

2 Void formation

Generally, voids are gaseous inclusions within the solder joints containing organic substances. These inclusions may have different origins, but most of the macroscopic voids visible in X-ray analysis are caused by evaporation of solder flux ingredients or by thermal degradation of flux constituents during the reflow process. During the cooling phase in the reflow process, when the solder alloy solidifies, most of these gaseous species condense and cover the inner surfaces of a void as an organic film. This could be proven by SEM-EDX and ToF-SIMS investigations of sliced voids [1].

Further sources of gaseous inclusions are organic residues from PCB or component surfaces, which may have different origins, e.g. residues from pre-processing or galvanic plating processes. Since this kind of organic impurities often consists of low volumes, the voids generated by this mechanism may reach only very small size in the range of a few µm diameter. These small voids are often called planar micro voids or “champagne” voids and are not visible in standard 2D-X-ray analysis due to limited resolution. The third reason for voiding can be outgassing of organic materials from component terminations. One example is the release of gaseous substances from improperly covered soft terminations of chip resistor or capacitor components during the reflow process.

An important aspect affecting voiding is the outgassing of gas bubbles during reflow. Buoyancy force calculation for gas bubbles of realistic size within the molten solder alloy shows that their rising velocity is high and most of the relevant bubbles can leave the solder joints within less than one second, if coverage of solder joint by components is neglected. It means that all voids without contact to a PCB or component surface have almost no chance to stay within the bulk material of the solder joint for a longer time during the melting phase. This is confirmed by cross sections showing that almost all voids found within vertical cross sections are attached to any surface. To look deeper at relevant parameters for void formation a comprehensive experimental analysis was done [2]. Most relevant parameters applied in this study are listed in Table 1.

Table 1 - Standard test parameters of investigations

PCB material	standard FR4 material
PCB metallization	bare Cu, Cu OSP, iSn, ENIG, HAL (lead-free)
Solder pads	80 pads of size 1.4 x 1.1 mm; 40-80 pads/ variant analyzed
Solder paste alloy	Sn95.5Ag4.0Cu0.5 ("SAC"), type 3
Solder paste flux	base variants standard fluxes for leaded soldering (low activity), lead-free soldering (mean activity)
Stencil	stainless steel 150 µm thickness
Assembly	no component placement, only open solder pads
Reflow profile	time until cooling ~300 s, T_{max} ~245°C, with preheating
Void analysis	2D X-ray and image evaluation by production software

From all results of this experimental study the following four main parameters influencing void formation could be identified:

1. The type or especially the **thickness of PCB metallization**. PCB surfaces like HAL (hot air leveling) with Sn layer thickness in the range of 10 or 20 µm has been frequently used in combination with leaded solder alloys. With lead-free alloys and higher melting temperatures the thermal load on the PCB material was significantly increased and therefore the use of HAL has been abandoned in many cases. Alternative PCB surfaces for lead-free applications like immersion tin (iSn) and Cu OSP show significantly lower thickness in the range of 1 µm or some hundred nm, which is also advantageous for miniaturization of assemblies and components.

   For voiding phenomenon these differences are highly relevant since voids are normally attached to surfaces as explained above. If thick HAL layers are melting during reflow, this connection of flux residues to the PCB surface is lost and gaseous flux residues can rise easily through molten solder. For thinner lead-free surfaces this mechanism does not work since especially with the beginning of IMC formation within the iSn layer the remaining amount or thickness of melting Sn is too low to release the flux residues from the surfaces. For OSP there is no release effect at all. This effect can explain at least to some extent by the significantly increased void level of lead-free solder joints.

2. Another relevant parameter for voiding is the **grain size** of the solder paste alloy. A clear correlation between solder ball diameter and void number as well as void-area percentage was found in various experiments. Other investigations do not show this clear trend or even arrive at different results [3, 4], but internal investigations showed a significant tendency for uncovered soldered pads as well as for solder joints with assembled components on a broad statistical basis [2]. As mentioned in some of these studies this effect may vary for different solder pastes and thus these results are valid only for investigated solder paste fluxes.

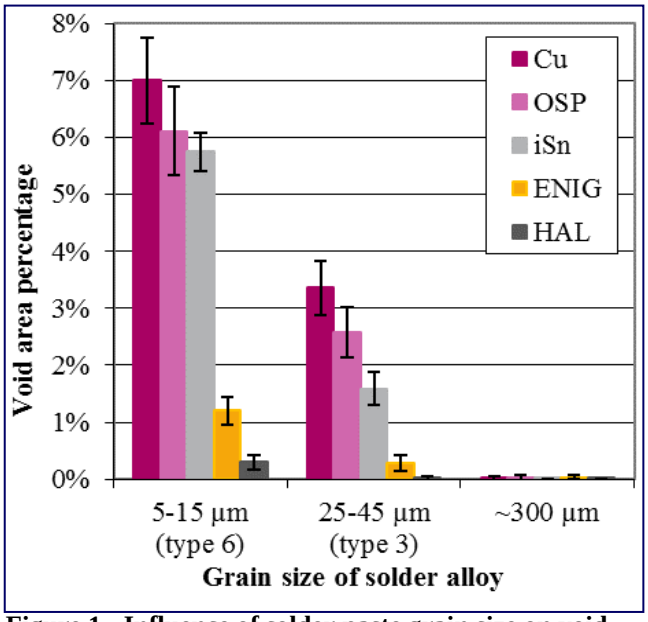


Figure 1 - Influence of solder paste grain size on void percentage for SAC solder alloy with open solder joints

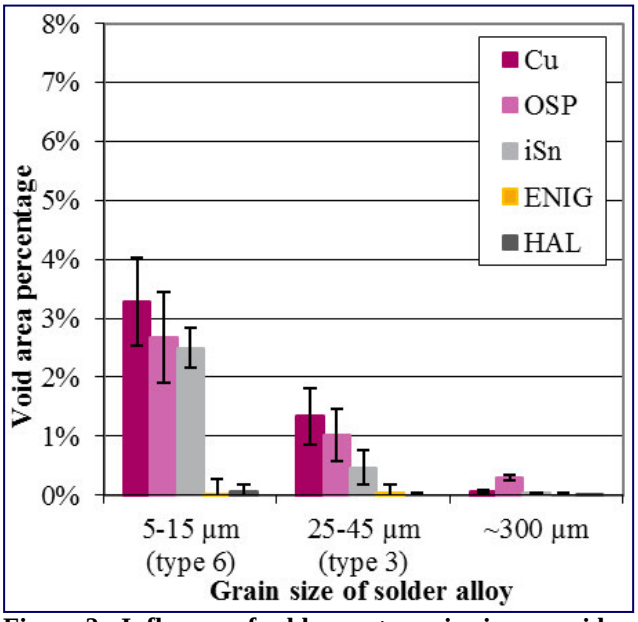


Figure 2 - Influence of solder paste grain size on void percentage for SnPb solder alloy with open solder joints

The tendency could be confirmed for SAC as well as for SnPb solder pastes (Figure 1 and 2). Further investigations with component assembly showed the same tendency, but due to coverage effect and lower variation of solder particle diameter the difference was not as significant as with uncovered solder pads.

3. The third parameter with high influence on voiding is the **solder alloy** itself. Leaded Sn63Pb37 solder alloy was found to have better spreading on standard PCB surfaces than lead-free high Sn alloys like SnAg4Cu0.5. One explanation for this behavior could be the inhibition of intermetallic phase formation by Sn with Sn63Pb37 due to the diffusion mechanism. Good wettability is clearly correlating with low voiding since flux residues are removed more easily from wetted surfaces [2].. The difference of void level between SAC and SnPb can be seen clearly by comparison of results from Figures 1 and 2 and is often in the range of 50 % and more.

4. Another parameter of high relevance is the flux chemistry of the solder paste, especially the **flux activity**. This can be influenced by acid number, but also by the type and composition of the acidic ingredients. Since it is difficult to condense this activity to one parameter only this overall description is limited to a comparison of three different fluxes from one supplier with different activity levels. Results are shown for combination with SAC and SnPb solder alloys in Figure 3. The activity of three fluxes is increasing from A to C.

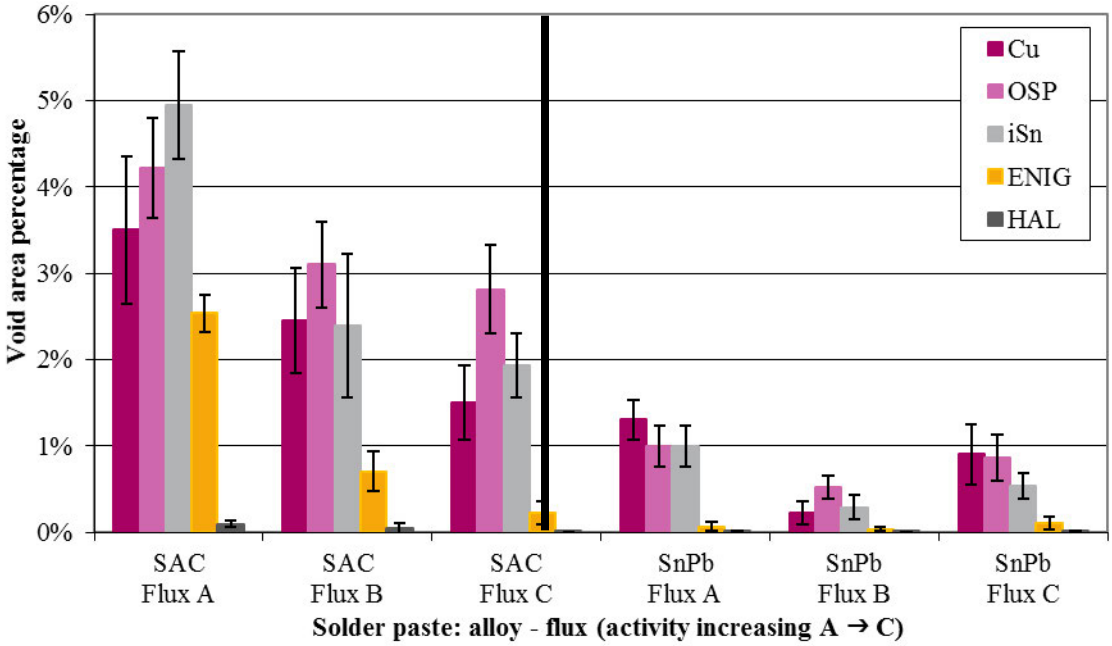


Figure 3 - Influence of solder paste flux activity on solder joint voiding

Relatively low influence on void percentage was determined for a variation of the reflow-temperature profile. The variations were made for level and time of peak zone as well as for level of ramp up. The realized changes are shown in Table 2 and resulting void percentages in Figure 4.

Table 2 - Overview of reflow profile variations

T-t profile	preheating	T-peak	peak time
A	std	-15K	std
B	std	-15K	+180s
C	std	std	std
D	std	std	+180s
E	std	+15K	std
F	std	+15K	+180s
G	-20K	Std	std
H	+20K	Std	std
I	ramp	std	std

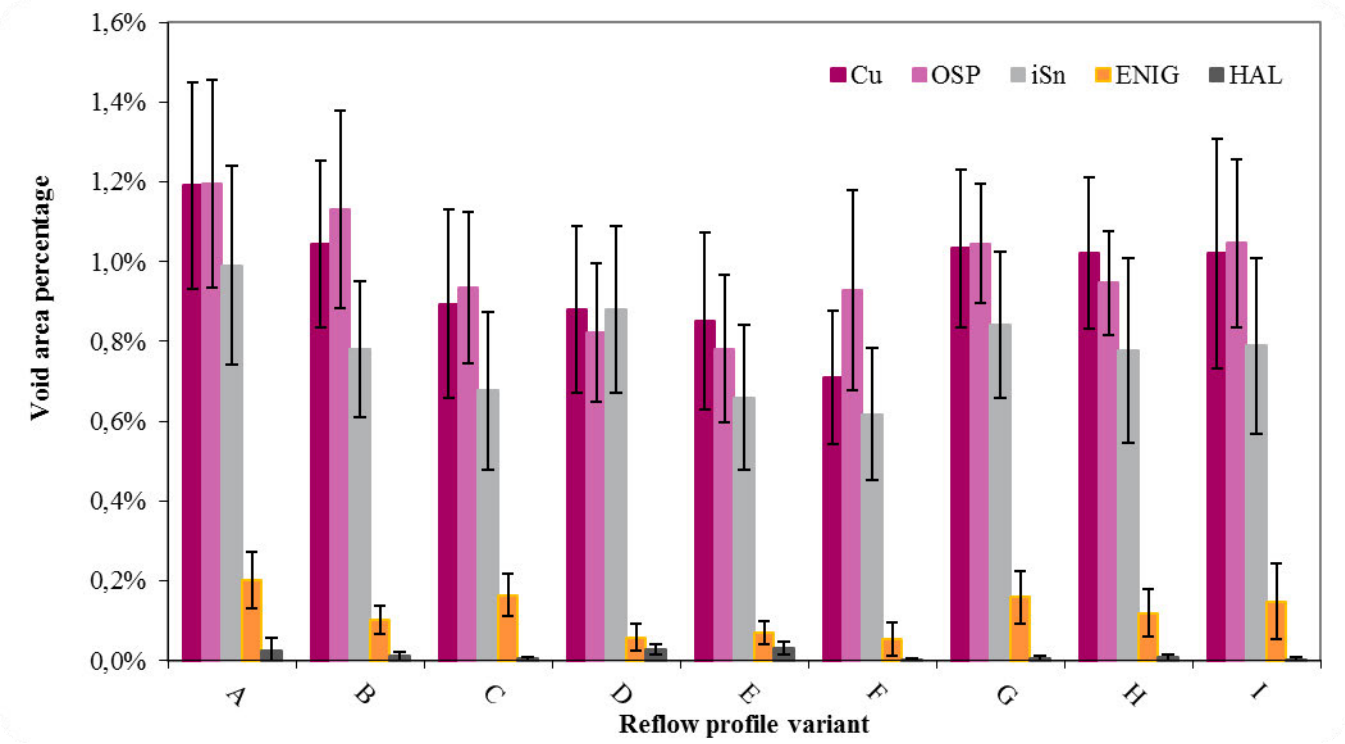
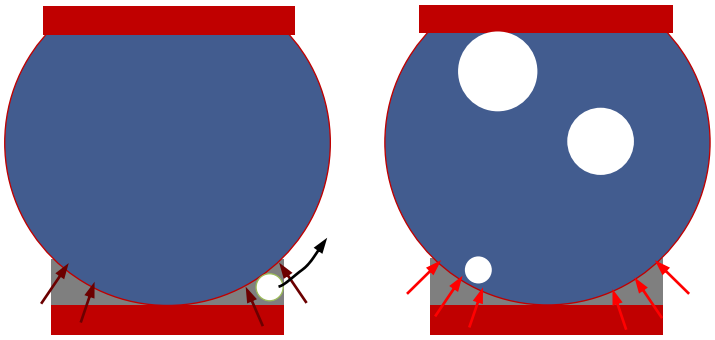


Figure 4 - Influence of reflow temperature profile variation on solder joint voiding

Some reduction of voiding can be observed mainly with increasing peak temperature. But the difference between low and standard temperature (which is ~ 245°C) is higher than between standard and high temperature. This means that temperature should not be too close to the melting temperature, but very high reflow temperatures do not improve voiding significantly.
As a remark it must be admitted that the transferability of these results to other solder pastes is not guaranteed. Due to chemical complexity of reaction and outgassing processes and limited availability of detailed information about chemical compositions the chemical processes during reflow process are unknown and can only be investigated on an empirical basis. Thus results may differ from presented correlations with different solder pastes and reflow profiles generally should be well adapted to solder paste as recommended in other studies [5], but influence of temperature profile is widely accepted as relatively low compared to the parameters mentioned above.

These results concerning influence of flux activity and reflow temperature profile are valid for open solder paste deposits and quantitatively also for small standard SMT solder joints. For BGA solder joints a different behavior was observed regularly. With pre-balled components high flux activity and high peak temperature or temperature gradient caused high voiding levels.



Low flux activity/
Low temperature gradient
⇨ **Low voiding**

High flux activity/
High temperature gradient
⇨ **High voiding**

Figure 5 - Theoretical model for voiding behaviour pre-balled components

This phenomenon can be explained by a simple model as shown in Figure 5, even if there is no complete proof for correctness of this model. The assumption is that there is some kind of more or less stable "skin" of the BGA ball, which could be an oxidation layer or some phase separation effect at the ball surface. This "skin" is stable during the reflow process until it is penetrated by thermal convection, wetting forces or flux activity. Up to this moment of penetration all gaseous evaporations from solder paste pass along the ball and will easily leave the solder joint. As soon as the skin is cracked a significant share of rising gases enter the ball so that bubbles are captured within. The cracking is accelerated by higher temperature gradient or higher flux activity resulting in higher final void content of the solder joint. Since this behavior of pre-balled components is different from standard SMT components, a general void reduction strategy for panels with mixed component spectrum is limited. In these cases void reduction for one component may increase void level for other. A reasonable compromise for the whole product needs to be found. Especially for exposed pad solder joints voiding is enhanced if solder volume is too low to fill the whole potential solder joint volume determined by z-position of pins and exposed pad. But not only is solder paste volume relevant, the paste deposit geometry in large area solder joints defined by stencil design also might influence the void level [5].

All these findings show that voiding can be reduced to a certain level, but not reduced to zero with normal convection reflow processes. If material and process parameters can be kept very stable, the variation of this void level can also be kept under control, since sensitivity of void level to process parameters was found not to be very high.

But additionally, there is an effect that makes it difficult to keep strict void limits: Online X-ray analysis during reflow processes have shown that void formation during reflow is a quite dynamic process. Gas bubbles are generated, grow and leave the solder joints. A few seconds later new bubbles are forming often at the same location from flux residues not visible in X-ray inspection as visible from online X-ray analysis like the images of open solder pads in Figure 6. Thus, the void level in a solder joint during the melting phase of a reflow process may look like an irregular saw tooth cycle.

For the final state of solder joints this behavior means that the overall void level may be quite stable, but the real void level distribution may cover a wide range of void values.

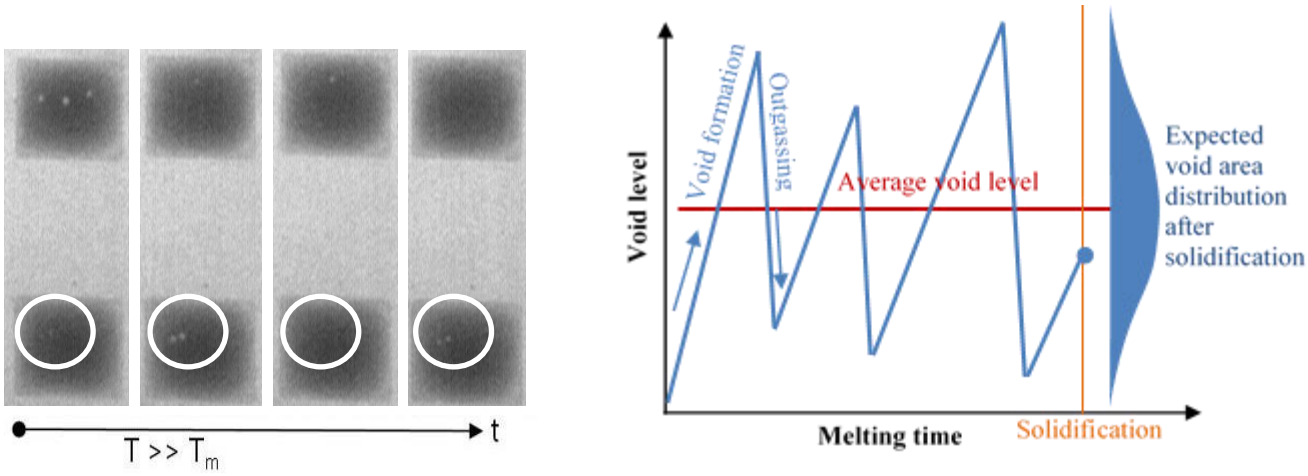


Figure 6 - Online X-ray images and sketch of principal course of void level during the melting phase

3 Void limits and void influence on solder joint reliability

Currently there is only one rigid void specification in international standards. IPC-A-610 F defines void percentage of BGA balls as acceptable for class 1, 2, 3, if its void area is lower than 30% of the ball area in 2D X-ray inspection. For all other components there may be some recommendations, but no specifications. Void evaluation of test boards with standard process and material parameters (SAC solder paste) show that this level is normally kept in series production with sufficient statistical safety. 99.7% of void values in this investigation were below 10% void area (Figure 7).

A more detailed c_{pk} prognosis of limit violations is difficult since the void percentage variation is often not compatible with standard statistical distributions. The X-ray images for BGA balls illustrating different void levels have been produced by soldering tests with worst case conditions making use of knowledge explained in Section 2. For other components than BGA no specifications are valid due to different reasons. X-ray control of these components is not as common as for BGAs, since further solder joint quality can widely be controlled by optical inspection. Additionally, BGAs are more critical with respect to temperature cycling reliability than many other components. Thus, this type of component is worth to have a closer control.

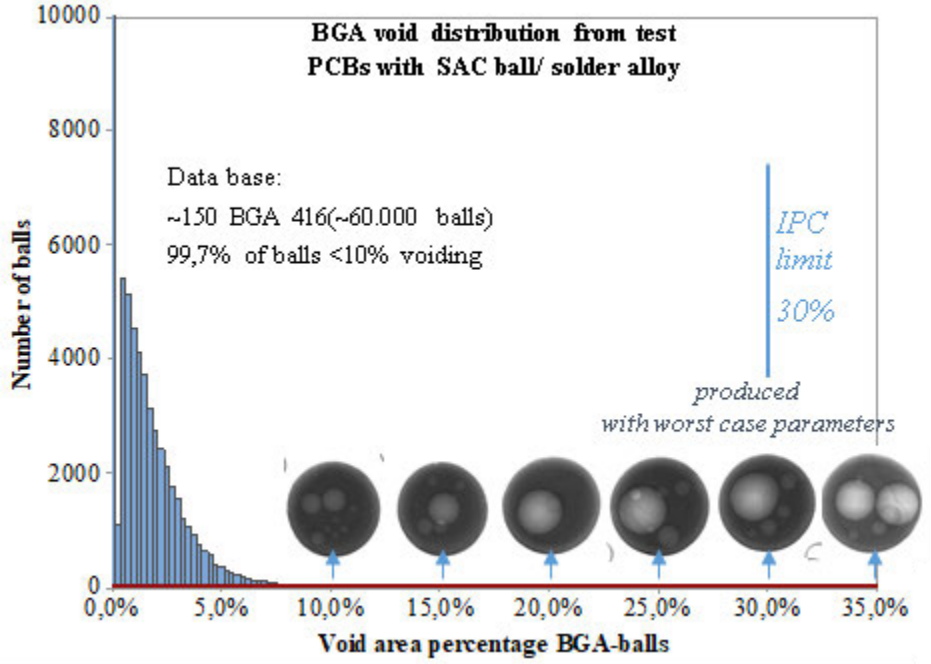


Figure 7 - Standard void distribution for BGA 416 component with examples of X-ray images for different void levels

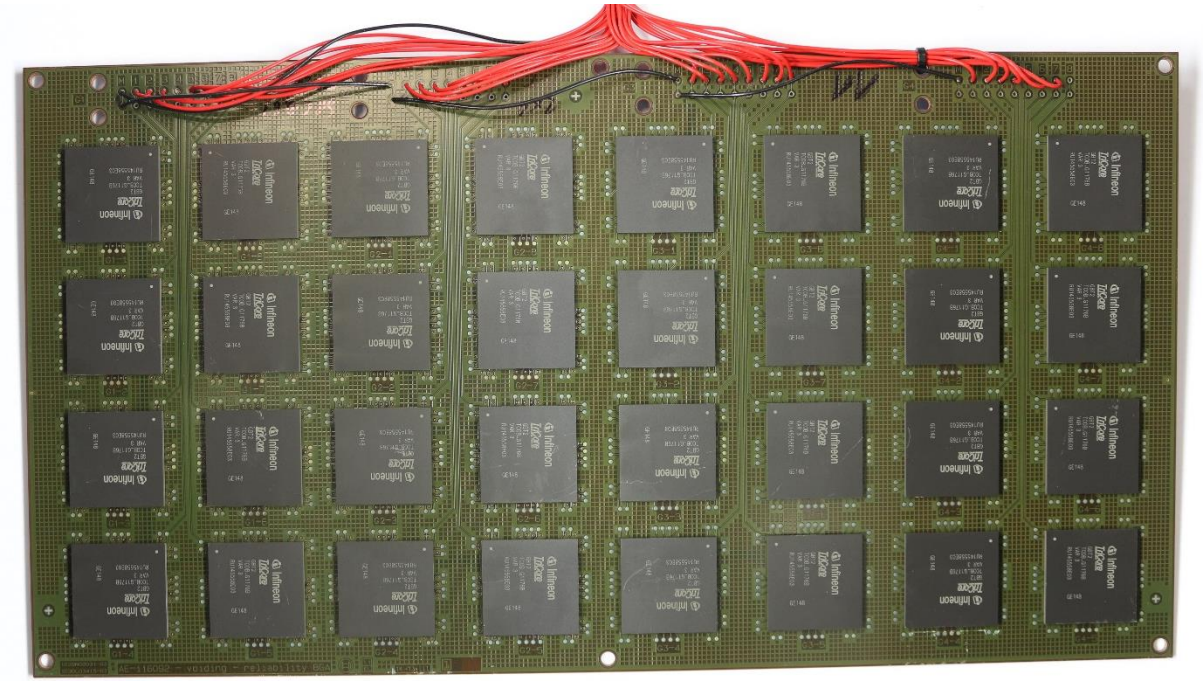


Figure 8 – Test board with 32 BGAs and electrical connections for online measurement

To investigate the influence of BGA voids on TC reliability a lifetime study with electrical online measurement during temperature cycling has been performed. Many other studies on investigation of reliability influence of BGA components by experimental analysis or by FEM simulation have been published [6, 7, 8, 9]. Most of them try to identify a direct correlation between void rate and crack behavior within single balls. Positive as well as negative effects of voids on reliability, mainly depending on size and positions of voids within the ball, have been reported. But from our simulations and theoretical considerations it was also clear that interactions between different balls are relevant for overall reliability of the whole BGA. Voids within one ball may reduce strength of this solder joint to a certain extent, but also enhance flexibility of this connection so that stress may be partially transferred to neighboring balls. The overall effect of voids on reliability is difficult to analyze. To cover this effect the reliability of the entire BGA was measured and taken as relevant criterion.
Together with further variations 6 boards each with 32 BGAs have been assembled (Figure 8).
The following experimental parameters have been applied:

- Component: BGA 416, pitch 1.0, daisy chain layout
- Ball alloy: SnAg4Cu0.5
- Solder alloy: SnAg4Cu0.5
- PCB: production halogen-free FR-4 base material, 6 Cu layer
- PCB surface: iSn
- Assembly: one side
- Reflow process: 2x standard profile (second reflow: board turned upside down)

To realize low and high void levels for direct comparison of BGA reliability the reflow peak temperature, grain size of solder paste alloy and flux activity was varied for minimum and maximum voiding according to findings explained above.

Temperature cycling was done in a temperature cycling shock chamber with min/max temperature of -40°C /+125°C and total cycle time of ~50 minutes. Electrical lifetime was tracked as permanent or third interrupt of the daisy chain for each BGA. The testing was stopped at 9000 cycles and to all BGAs without failure at 9000 TC an artificial lifetime value of 9500 cycles was assigned at least for direct correlation of void values and TC. From several experimental and mainly simulation studies in the literature it is well known that not only the 2D area percentage of voids is relevant for reliability, but also the number and the individual 3D positions of all voids. Since these parameters are difficult to measure and to correlate, the simple approach with only 2D X-ray evaluation of void area percentage was chosen.

Results of this investigation are shown in a graph as TC lifetime over void level, where void level can be average level (Figure 9) and maximum void level (Figure 10). The IPC void limit for BGA is defined as the maximum void level of any BGA ball so it can only be applied to Figure 10. Other correlations of reliability with average void number, void level at the edges and spreading of void values of a BGA have also been checked, but the regression quality was no better than for the presented ones.

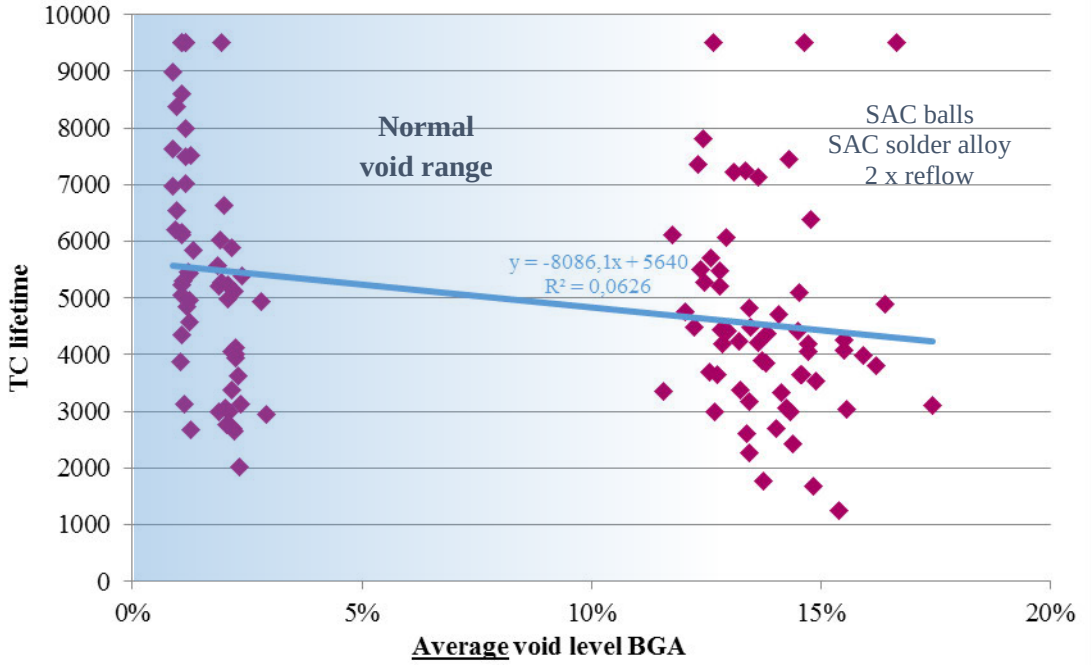


Figure 9 - Correlation average voiding – lifetime BGA

Especially the average void values in Figure 9 show that variation of the three parameters for void level adjustment was very efficient and the two groups low and high voiding are clearly distinguishable. Standard production parameters show average voiding in the range of 1-3 %, worst case parameters result in void levels between 11 and 18%. For maximum void percentage the difference is not so clear, but BGAs with standard parameters can fulfill the IPC limit (Figure 10).

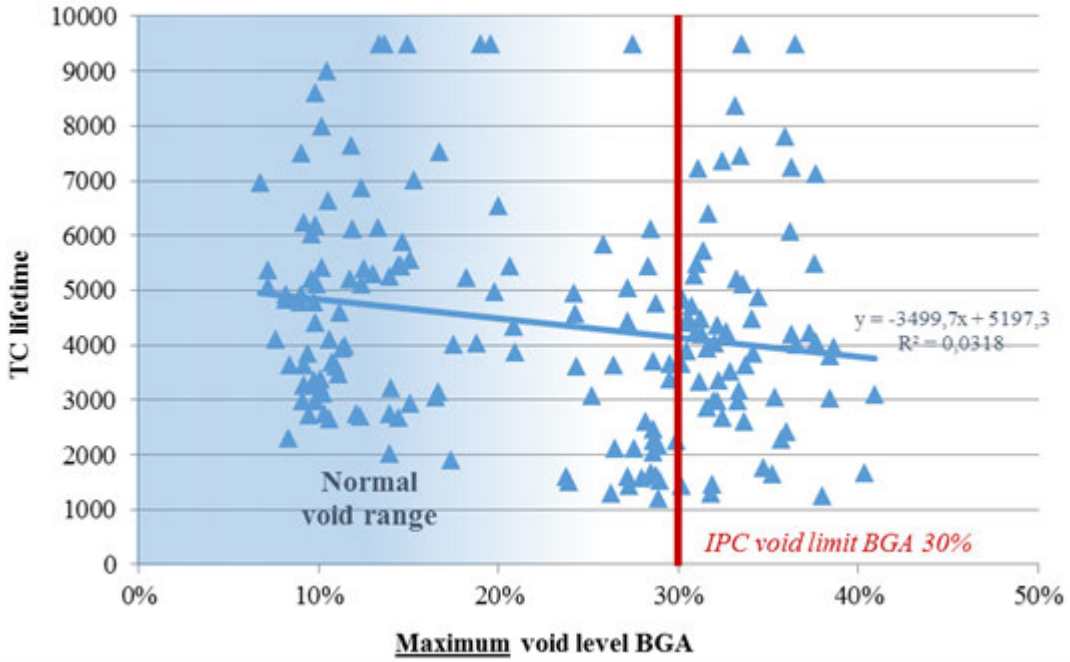


Figure 10 - Correlation maximum voiding – lifetime BGA

The lifetime results show that there is a slight but visible influence of voiding on TC reliability of BGA. The correlation is similar for average and maximum voiding, so that it can not be concluded that only the largest void is relevant for reliability of the entire BGA. Apart from voiding there are many other factors influencing TC lifetime, since variation of TC values is very high at all void levels. Thus, voiding is only one of many other factors with reliability relevance. The moderate influence of voids together with void values for standard parameters show that the IPC void limit of 30% for the most affected ball BGA components is a reasonable specification which inhibits critical void percentages and is achievable in series production. Nevertheless, this definition cannot guarantee a certain lifetime value, since voiding is only one factor of limited influence.

For other standard SMT component types the influence of voids on TC reliability is also a topic of discussion. Thus, void distribution for 7 of these component types (QFP, SOT23, QFN, quartz, SOP8, ELKO (Electrolytic Capacitor), chip resistor 0603) and standard production parameters have been analyzed on series boards by X-ray control with part volumes between 100 and 450. The relative void histograms (Figure 11) show that there are more than 97% of all void percentages lower than 10% and only 0.2% higher than 20% area percentage. These distributions might be only random results but show at least the range of what is common in lead-free series production. In real series production sometimes, additional effects like surface quality variations may increase the average void level to some extent.

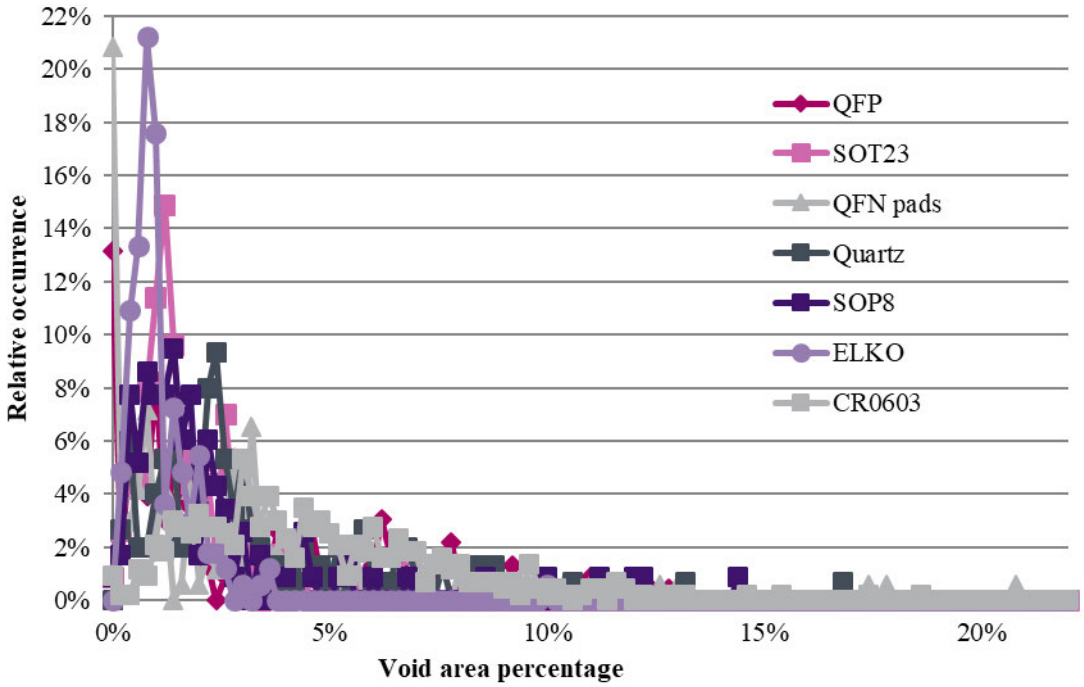


Figure 11 - Typical void distributions for standard SMT component types

So the question for product reliability is how critical this void level or also higher values might be for TC lifetime of SMT components. To evaluate void influence on TC lifetime of standard SMT solder joints another study was performed. Since large chip resistors are known to be some of the lifetime determining components on a board a special CR1206 type was selected for investigation, where void level was known to be relatively high due to termination outgassing effects. Normal void percentages within the standoff area for these components are in the range of 0-20% as shown above, whereas here void values up to ~40% could be measured. The meniscus area was neglected since void level in this area was very low and X-ray analysis was not feasible in an acceptable quality. Therefore, only the standoff area is taken into account.
Further experimental parameters are below:

- Component: 250 chip-R 1206 with soft termination
- Solder alloy: SnAg4Cu0.5
- PCB: production high Tg FR-4 base material, 4 Cu layer
- PCB surface: iSn
- Assembly one side
- Reflow process: 1x standard profile

Boards were aged in 5 classes of temperature cycles -40C/ 125°C (0/ 500/ 1000/ 1500/ 2000 cycles). Each class contained 50 components. After ageing component reliability was tested by shear testing with 0.167 mm/s shear speed. Shear force values have been correlated with average void percentage for both standoff areas. The result is shown with shear force values separated for the 5 TC classes in Figure 12.

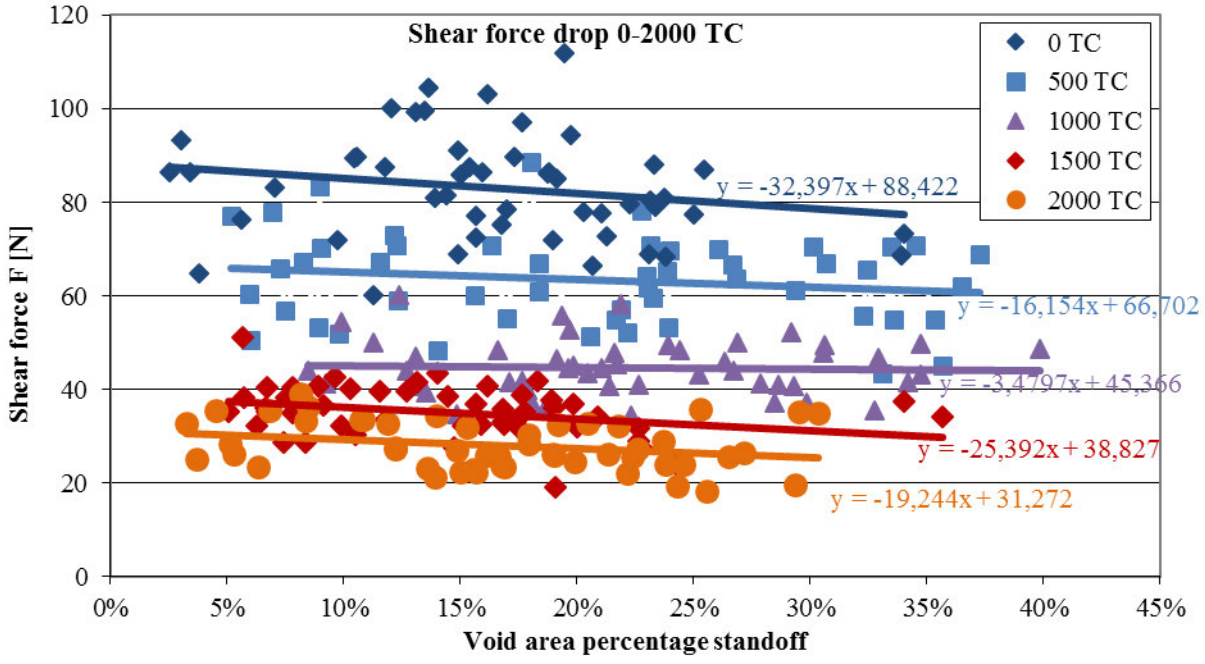


Figure 12 - Correlation shear force – void level within standoff area for CR1206 components and different TC ageing classes

Shear force values already show that influence of voids on reliability is quite low, since all trend lines show low and similar gradients over void percentage. This is already a valuable and important result, but to derive an overall conclusion it would be important to know how final lifetime values depend on void values. To generate this correlation a second evaluation step was applied where shear force values have been used for extrapolation of TC lifetime. For each void class of 5% width separate average gradients of shear force drop for standoff and meniscus crack were used to make a prognosis for TC lifetime values with 80% solder joint crack. With these assumptions the specific lifetime of each component is defined as the cycle number reaching a remaining solder joint area of 20%. Figure 13 shows the result of this so called "Perlschnur" evaluation.

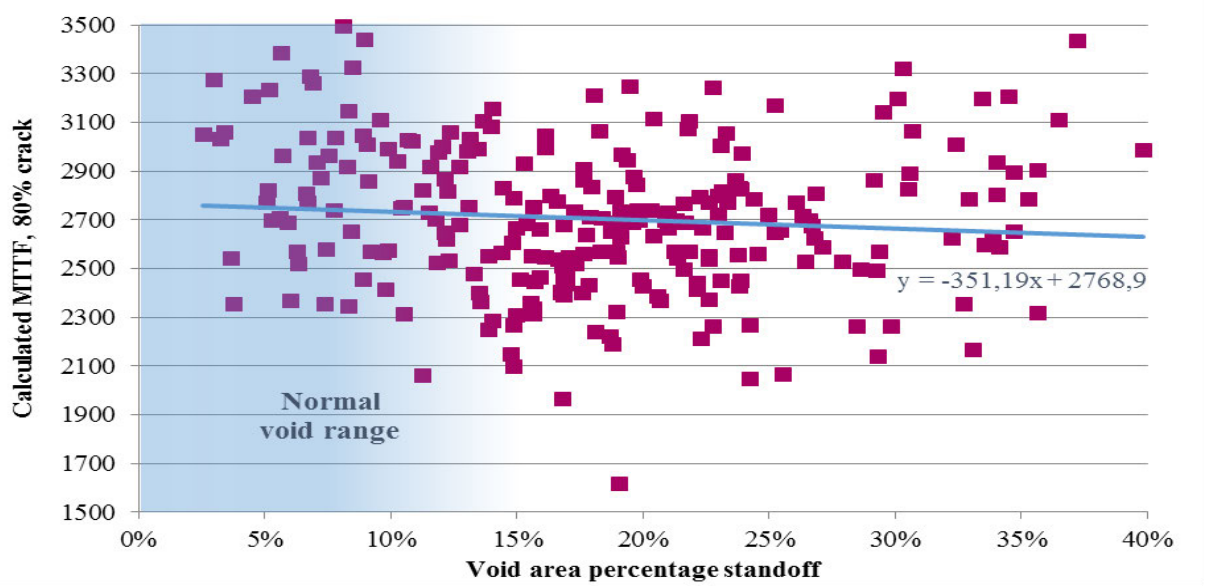


Figure 13 - Correlation void percentage with TC lifetime for CR1206 calculated by Perlschnur evaluation

Calculated TC values range from 1500 to 3500 TC but there is no clear trend visible for lower lifetime with higher voiding, even if the range of void percentages is significantly larger than in normal production so that this analysis also covers worst case conditions. Similar to BGA results this diagram shows that there is high variation of lifetime values, indicating that there are many other parameters influencing lifetime of components. These results show that even for these worst-case parameters and boundary conditions with high voiding level void influence is low or even can be neglected. For a realistic range of series production, it can be concluded that there is a large safety margin and slight changes of average void level occurring due to process and material variations are not critical for overall TC reliability.

Another concern in the context of voiding is a potential heat transfer reduction for large thermal pads, referred to as exposed pads. Within these large area solder joints void content is normally significantly higher than in small standard SMT solder joints. The range which usually can be found with standard production parameters is between 10% and 50%, sometimes up to ~60% void percentage. The question is if this void rate may reduce heat transfer in the vertical direction. To answer this a simple thermal resistivity calculation was performed.

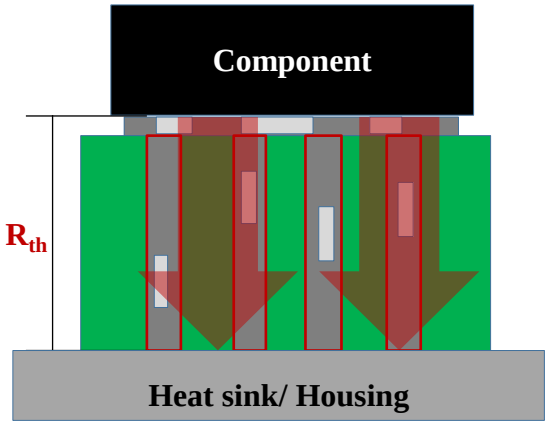


Figure 14 - Sketch of heat transfer with exposed pad solder joints

A sketch of the simplified model behind this calculation is shown in Figure 14. The overall heat resistivity between component surface and heat sink or housing surface on the other PCB side is calculated for the whole exposed pad area.
For a 30 mm^2 solder area with 25 through hole vias of 0.5 mm diameter the influence of void content within the soldered area on vertical thermal resistivity of solder joint plus PCB is calculated as illustrated in Figure 15. Since via filling may reduce thermal resistance of PCB and enhance void influence, this effect was also considered.

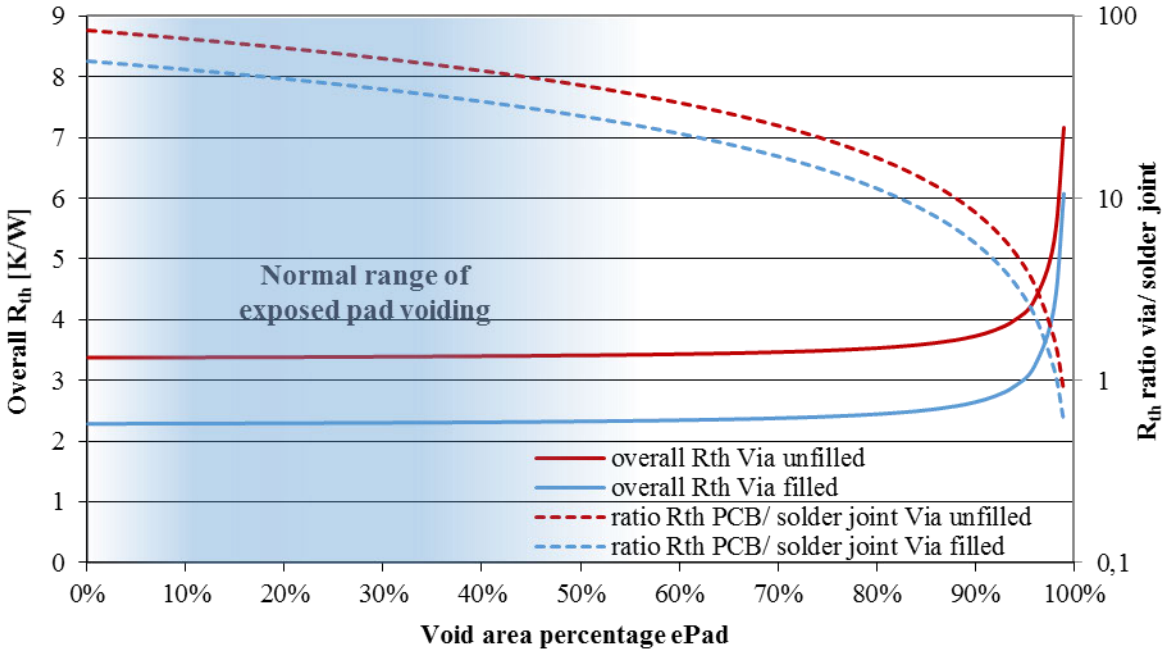


Figure 15 - Calculation of void influence within exposed pads on overall R_{th}

This calculation clearly shows that solder joints of exposed pads on standard PCBs are not sensitive to voiding up to about 80% or even 90% area percentage. The main bottleneck of heat transfer is the PCB base material, even if a high number of vias is supporting the vertical transfer of heat through the PCB. Solder filling of vias also does not change the situation generally. The influence of high void level within exposed pads on TC lifetime was not investigated, but from serial production experience it is known that this kind of solder joint is not an issue for reliability. Thus at least the normal range of void values up to about 60% void area can be accepted as uncritical. This may be different only if the solder joint is positioned on thick or massive copper (DBC). In this case the base material is no longer the bottleneck for heat transfer and voids show increased influence on thermal resistivity. For these applications vacuum soldering is known as an effective method for void reduction.

As an overall conclusion for the reliability issue, voiding may have negative influence on TC reliability for high percentages, but for the investigated reliability relevant components normal series void level including a sufficient safety margin was found to be uncritical.

After specific reliability investigations some general considerations concerning voids and solder joint reliability are presented. From the author's understanding all voiding concerns concentrate on reliability issues and risks are seen that voids may reduce the lifetime of solder joints, components and products with in some cases high risk level even for human life, like in the automotive industry. But reliability of the solder joint is a highly complex topic with many different influencing parameters.

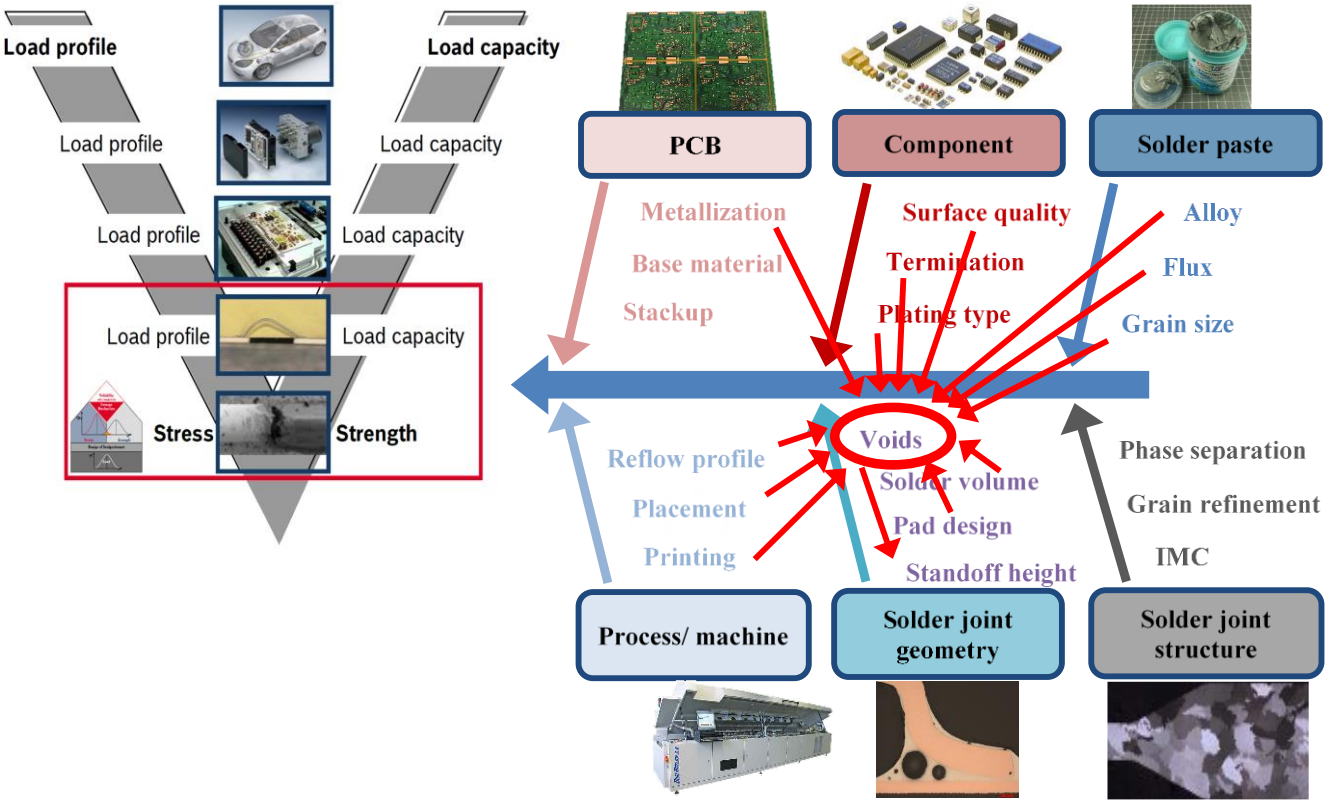


Figure 16 - Solder joint reliability and influencing parameters

Figure 16 tries to demonstrate this complexity. On the left side the principle of reliability is illustrated. Stress profiles and strength of design elements have to be adjusted to each other, not only on the product level, but likewise also on more refined levels like PCB, electrical component, solder joint and grain structure. For all real constellations load level should be lower than load capacity of design elements, even respecting real distributions. The strengths of solder joints on the right side is defined by many parameters like PCB materials and built-up, component materials and quality, solder paste, process and machine parameters, general and individual solder joint geometry and solder joint material structure. Voiding is only one

parameter out of the solder geometry parameters, but it is not independent of all the other parameters and is influenced e.g. by solder paste or component termination as explained above. In such a complex system it is not said that a reduction of void level by varying some of these parameters automatically enhances overall reliability. In most cases this may be right, but there can also be circumstances where void reduction means reliability reduction, not improvement.

Two examples for such behavior related to the solder alloy and component selection are explained. As an alternative for standard lead-free SnAg4.0Cu0.5 solder alloy, high reliability alloys such as SnAg3.8Cu0.7Bi3.0Sb1.5Ni0.15 are available on the market. This alloy can improve TC reliability significantly by a factor of 1.5 or even 2, but also tends to have slightly higher voiding. If product development focuses only on void reduction or even is forced to reduce voiding down to a very low level by customer or international void limits, it may lose the chance of applying the high reliability alloy. Finally the selected standard alloy solution would show lower voiding and better optical appearance of solder joints, but would not optimize overall solder joint reliability as originally intended.

The same situation can be found for soft terminated chip components as already used for void evaluations. At least some of these type of components tend to have higher voiding due to termination issues, but still show higher TC performance compared to components with standard terminations.

These examples show that always overall solder joint reliability must be the main focus of improvement and void reduction should be looked upon critically if it really improves solder joint reliability.

The final remark of this paper is about dealing with capability of void measurement by X-ray. It is well known that measured void values depend on X-ray parameters. High voltage or high current means a bright picture where solder joints are reduced in size, but voids are enlarged compared to reality. For low current/ voltage the effect is vice versa. To quantify this effect an analysis has been made with one BGA region analyzed applying different X-ray parameters. The results are shown as measured void percentage versus $I * U^2$ in Figure 17.

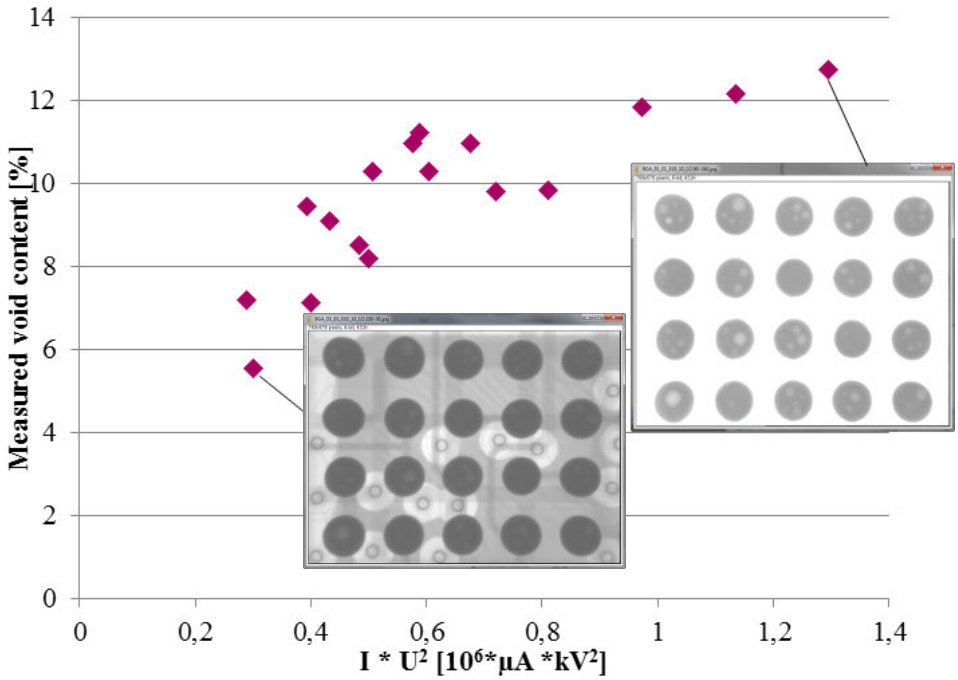


Figure 17 - Void measurement of BGA region with varying X-ray parameters

From this investigation it can be concluded that there is high uncertainty of void measurement, especially if performed on different X-ray machines. There might be a factor of 2 only from X-ray analysis alone without taking into account the influence of image processing, which may have an uncertainty of similar size. For direct comparison with the same materials, machines and parameters the differences are much lower and can be used for void influence investigations as within this and many other studies. But if X-ray measurement is used for control of void limits in production, this low level of measurement capability must be taken into account, especially since there is currently no reproducible measurement

reference available to overcome this drawback. Thus, for further work on void reduction and control an improvement of X-ray quality is crucial.

4 Conclusions

Looking at the different aspects of voiding some general findings can be concluded:

1. Some parameters with high influence on solder joint voiding could be identified, but most of them are widely fixed by further constraints like environment legislation (lead-free solder pastes and as a consequence PCB metallization) and miniaturization trends (grain size, also PCB metallization).
2. Other parameters like reflow profile or flux activity have relatively low effect on voiding or show different tendencies for different types of components. Thus, voiding can be reduced to certain extent, but significant void levels which depend on component type (pad area) and solder paste has to be accepted for lead-free soldering.
3. The average void level can be kept sufficiently stable by adjusting and controlling material and process parameters in series production. Additional statistical variation of void level is process inherent and can not be avoided completely.
4. The influence of artificially enhanced worst case void level on temperature cycling reliability was investigated for most critical components by cross sections or electrical online measurement. Especially for BGA components some slight influence on lifetime could be observed, but within the IPC specification for BGA solder joints no significant effect is expected. For chip resistors no significant influence could be detected.
5. Combining these findings, the overall conclusion is that with controlled series production parameters there is no significantly increased risk due to voiding in solder joints. Void level should not run out of control, but this can be assured by stable and clearly defined processes and materials.
6. Concentration on void issues and introduction of further strict void limits may even lead to negative and not intended effects for TC reliability. Thus, the first objective of product improvement must be always the overall product reliability. Voiding is only one of many other aspects and should be treated like this.
7. For further investigations on voiding and especially for void control under series production conditions an improvement of X-ray analysis is crucial to achieve reliable results.

5 References

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Voids in SMT Solder Joints – Myths Revisited

Dr.-Ing. Norbert Holle, Dr.-Ing. Thomas Ewald, Dr.-Ing. Udo Welzel

Robert Bosch GmbH – Stuttgart, Germany

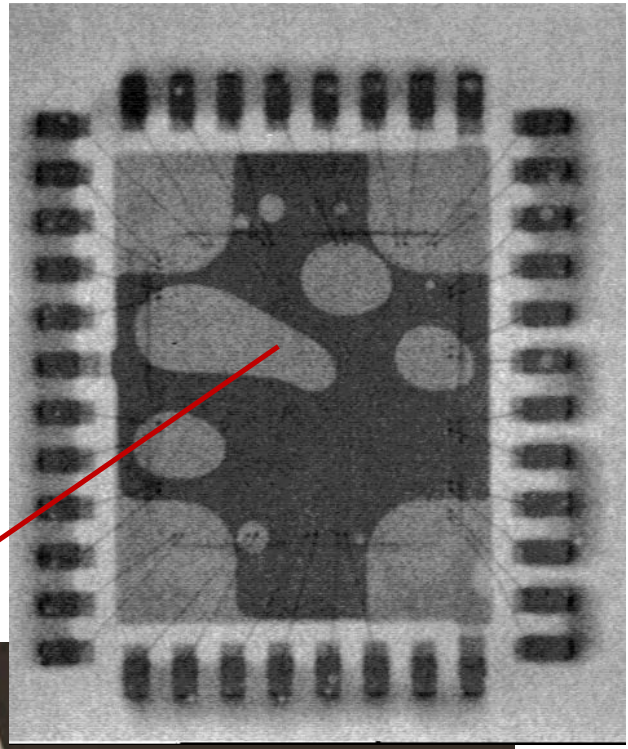
Overview

- Appearance and root causes for voiding in solder joints
- Main influence parameters and special effects
- Influence of solder joint voids on temperature cycling reliability
- Influence of solder joint voids on heat balance
- Voiding within general context of solder joint reliability
- Void measurement by 2D X-ray
- Conclusion

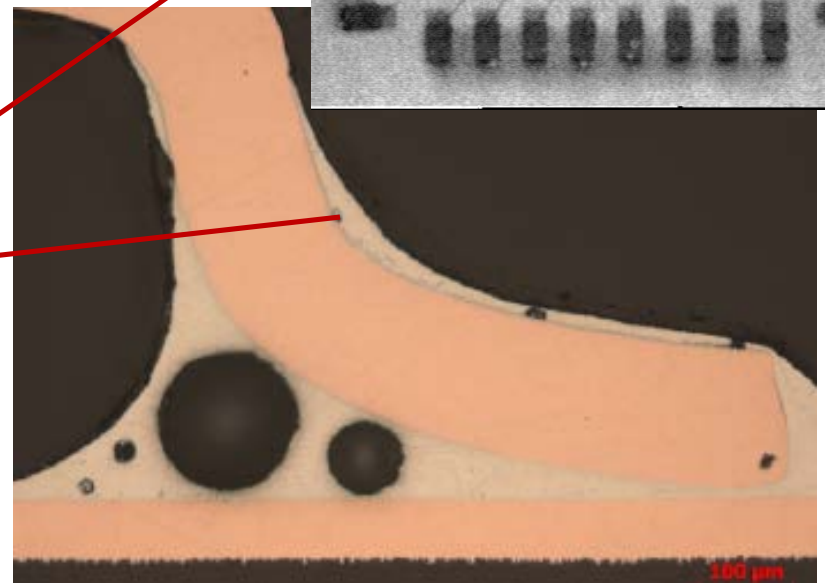
Appearance of voids

"Voids are gaseous inclusions within solder joints"

- Possible sources of gaseous inclusions are
  - ***Flux ingredients*** *or reaction products of thermal degradation*
  - ***Organic residues*** *on PCB or component surfaces (e.g. from galvanics)*
  - *Evaporations from organic materials within* ***component plating***
- **Size of voids** may reach from <1 µm (e.g. "champagne" voids at galvanic surfaces) to few mm (e.g. large voids in e-pads)
- Voids are normally **attached to** PCB or component **surfaces**



X-ray image of QFN e-pad voiding

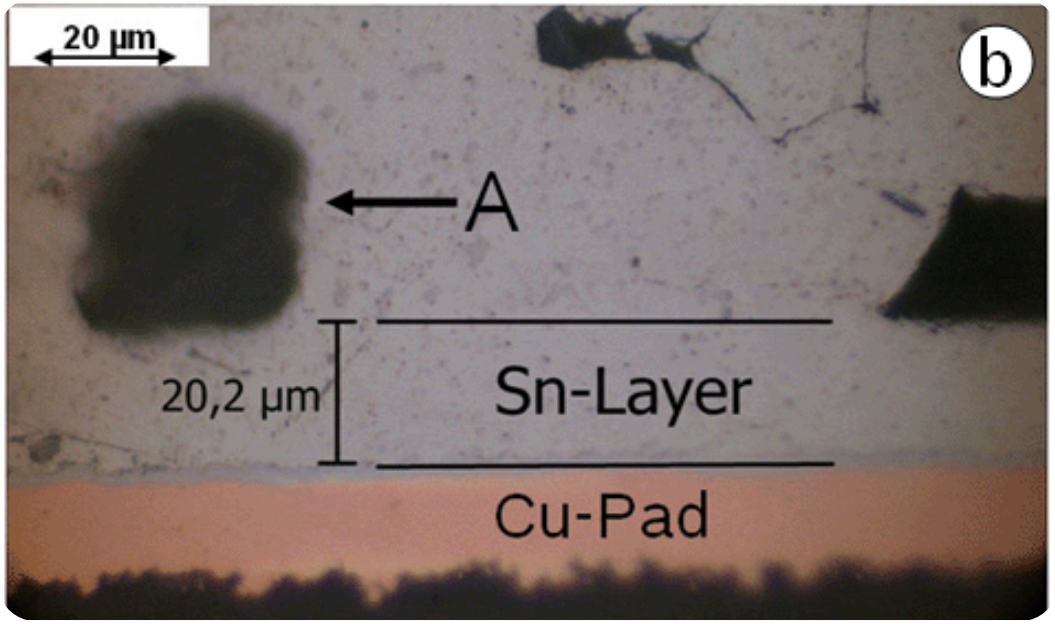


Microsection of gullwing solder joint with voids

Root causes for voiding

"Voiding is a normal phenomenon especially of lead free soldering"

- Most relevant parameters for void formation:
  - Thickness of **PCB metallization**:
    thick ↘ (HASL) ⇔ **thin ↗** (iSn, OSP)
  - **Grain size** of solder alloy: standard type 3
    large ↘ (type 2) ⇔ **fine ↗** (type 5)
  - Solder **alloy**: less voids with
    leaded ↘ compared to **lead free ↗** alloys
    due to higher wetting tendency/ lower surface tension
  - **Flux (activity)** and **process parameters** can have opposite effects
    for different component categories (standard SMD ⇔ BGA/ pre-balled)



*Voids on top of HASL surface are positioned **within** liquid bulk material after melting*

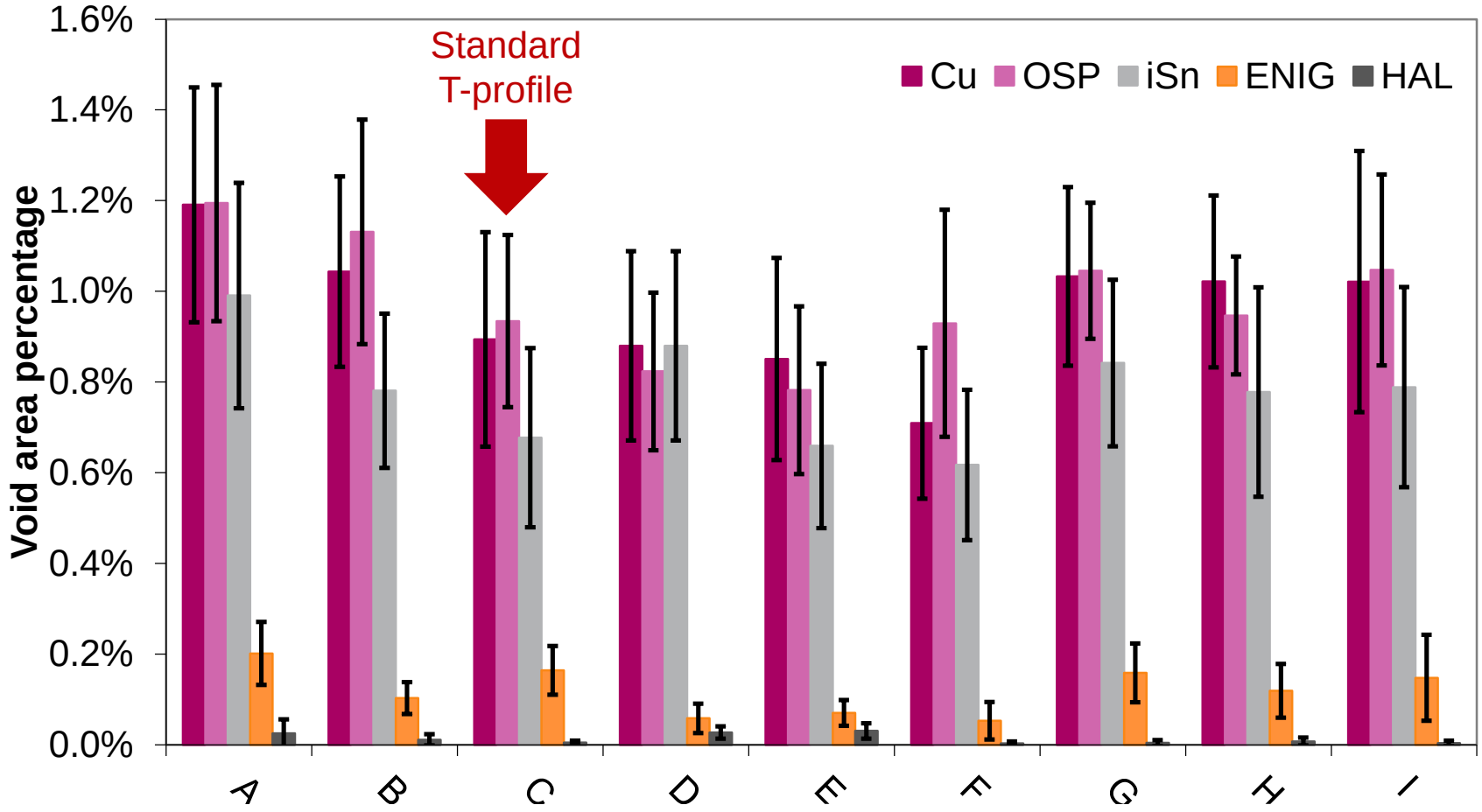
⇨ Void level normal even with optimized lead free processes

Influence parameters voiding: Reflow profile

T-t profile	pre-heating	T-peak	peak time
A	std	-15K	std
B	std	-15K	+180s
C	std	std	std
D	std	std	+180s
E	std	+15K	std
F	std	+15K	+180s
G	-20K	std	std
H	+20K	std	std
I	ramp	std	std

T-t profile variations

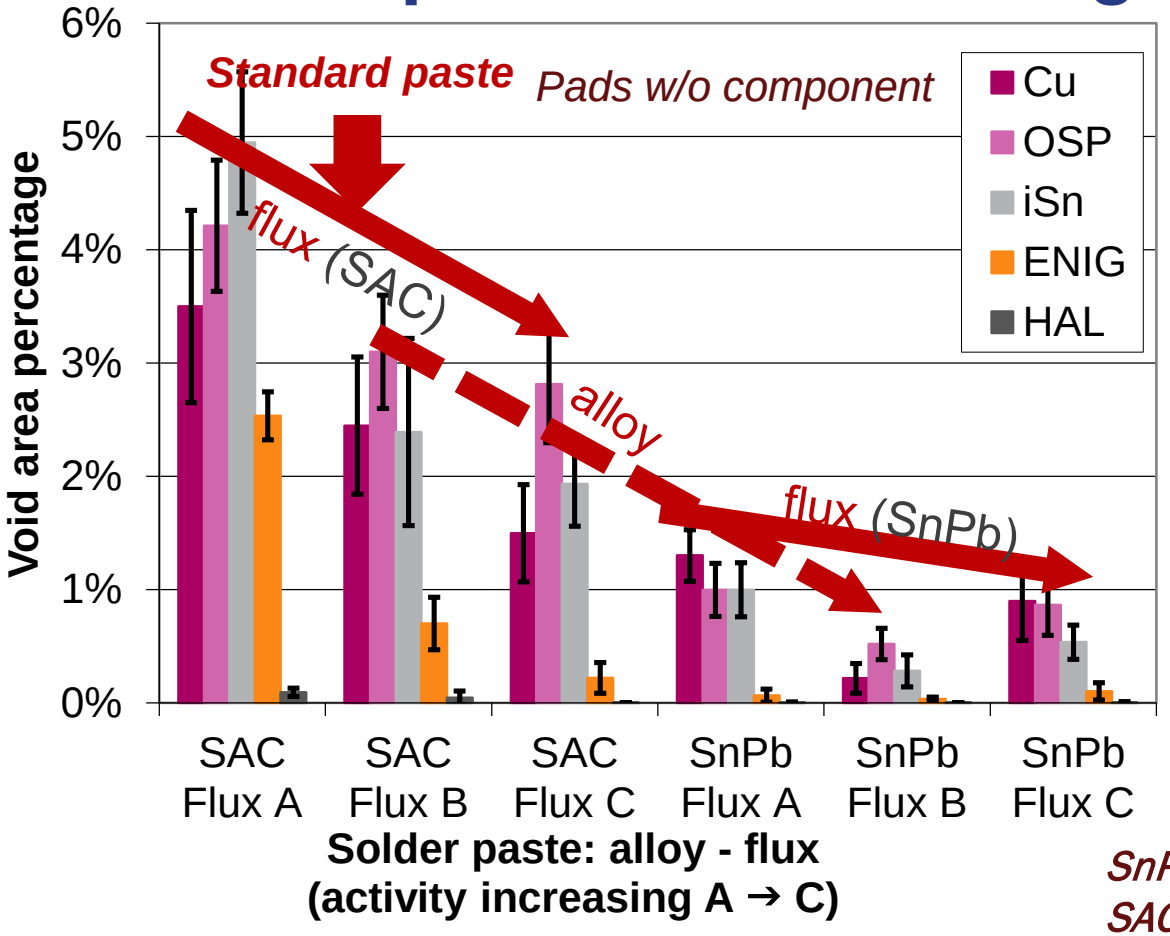
Pads w/o component

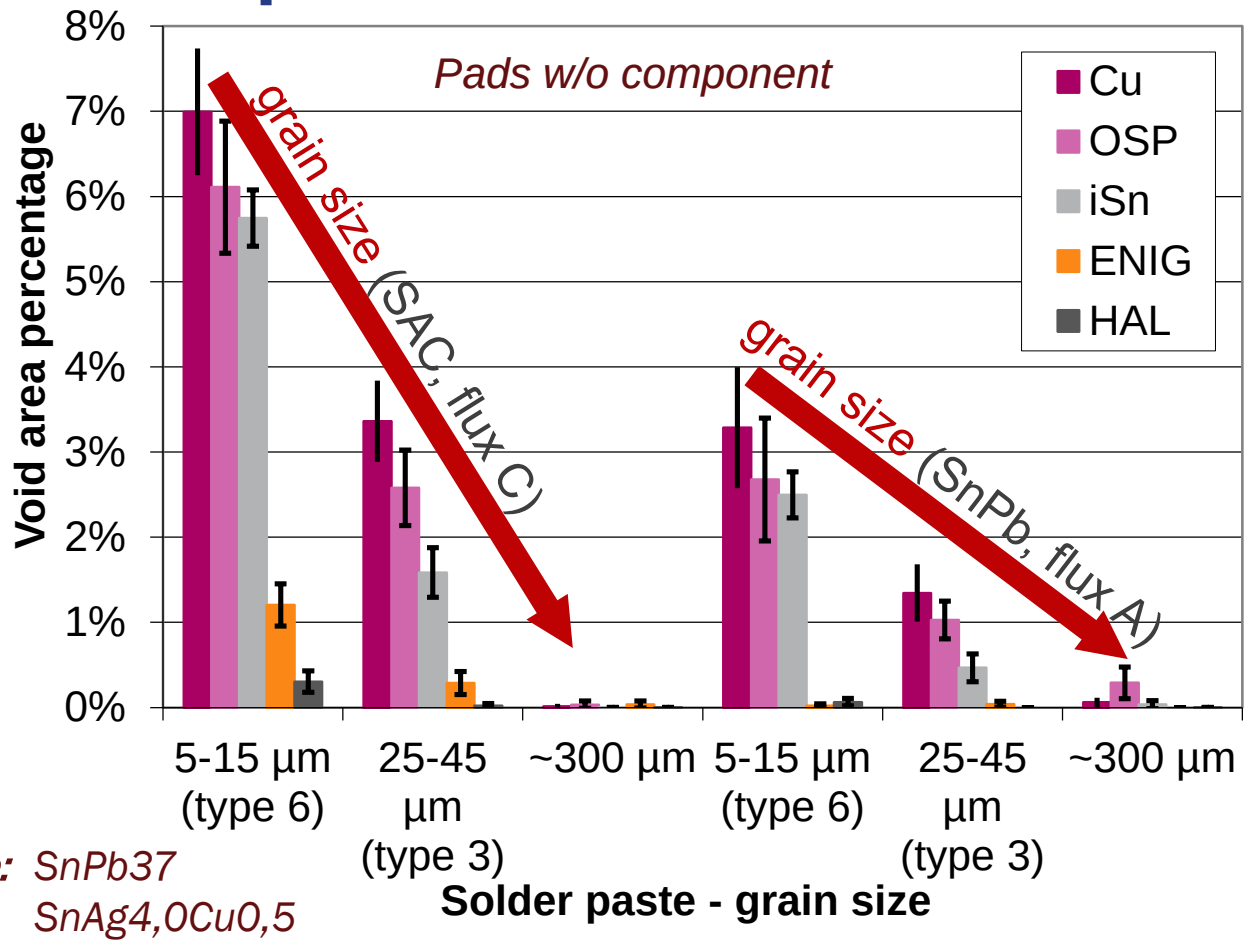


- Strong variation of preheating, peak temperature, peak time investigated

⇨ Only minor influence of T-profile on voiding, low potential for improvement

Influence parameters voiding: Solder paste





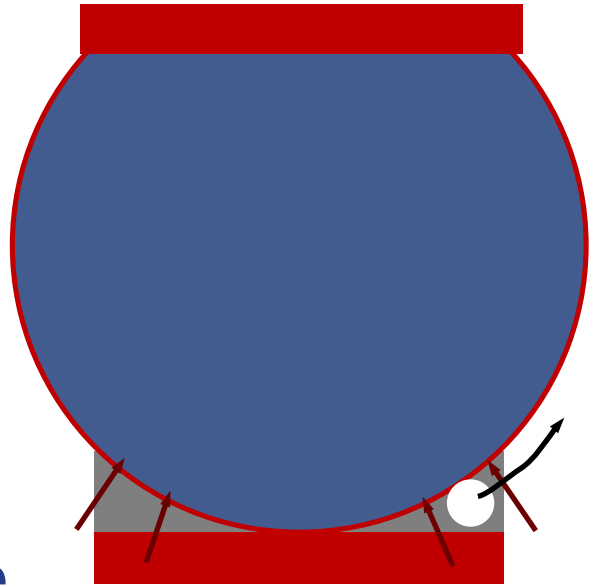
SnPb: *SnPb37*
SAC: *SnAg4,0Cu0,5*

- Evaluation relevance of paste parameters: grain size > alloy > flux

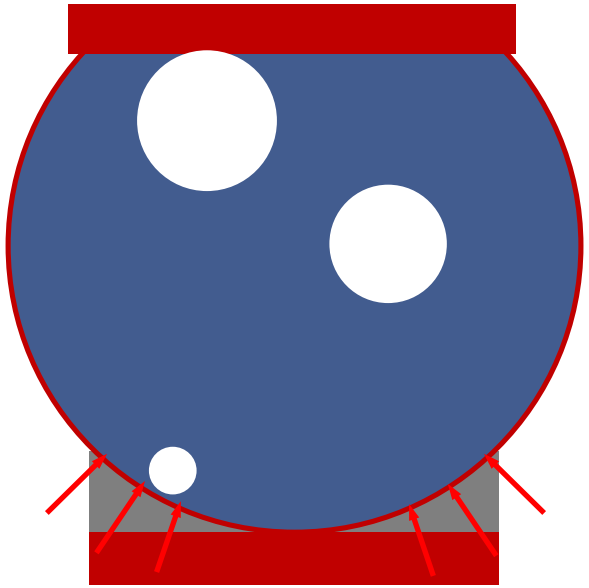
⇨ Solder paste influence relatively high but normally low space for modification

Void formation BGA balls

- **Special voiding mechanism BGA:**
  Effect of flux activity and reflow temperature different for standard SMD and BGA (pre-soldered components)
- **Model voiding mechanism BGA:**
  - During a first melting phase gases pass along outer, still stable „skin“ of BGA ball (oxidized layer)
  - Within a second phase flux activity and temperature is opening this skin
  - High flux activity or temperature gradient is accelerating second phase
    ⇨ Higher percentage of gases is captured within ball during soldering



Low flux activity/
Low temperature gradient
⇨ **Low voiding**



High flux activity/
High temperature gradient
⇨ **High voiding**

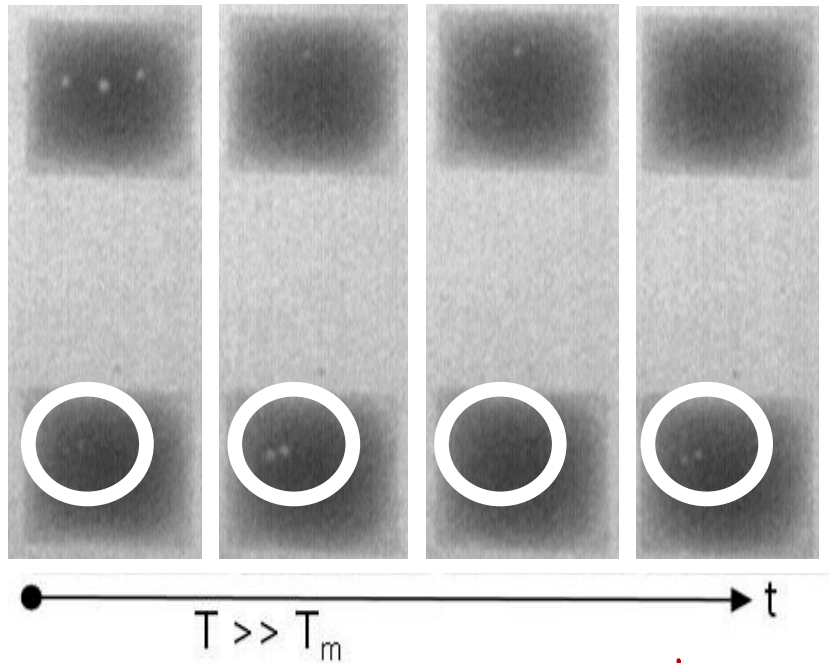
⇨ Voiding countermeasures may differ depending on component type

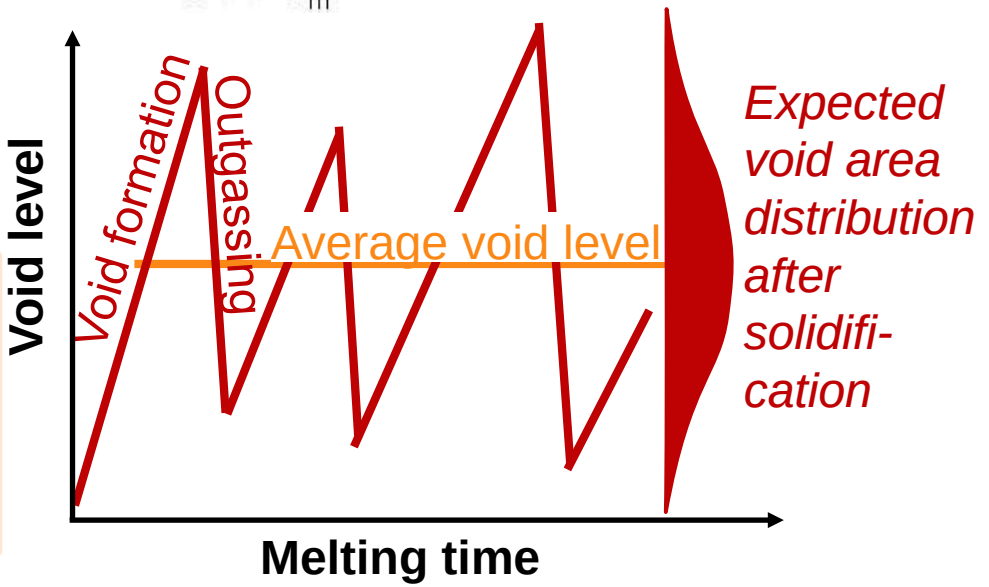
SMT process quality assurance

- Low variation of void relevant material and process parameters together with low sensitivity of void formation results in **stable average void level**
- Observation online X-ray analysis: Arbitrary void formation effects like repeated outgassing of bubbles from solder joint during melting period lead to **overlaying high void distribution** (often not normal distributed)

⇨ **Strict voiding levels hard to ensure**

⇨ **Regular quality check of processes and materials in series production recommended**





International voiding specification

- IPC limits only existing for **BGA: max. 30% voids** relative to ball size in 2D X-ray (IPC-A-610 F):

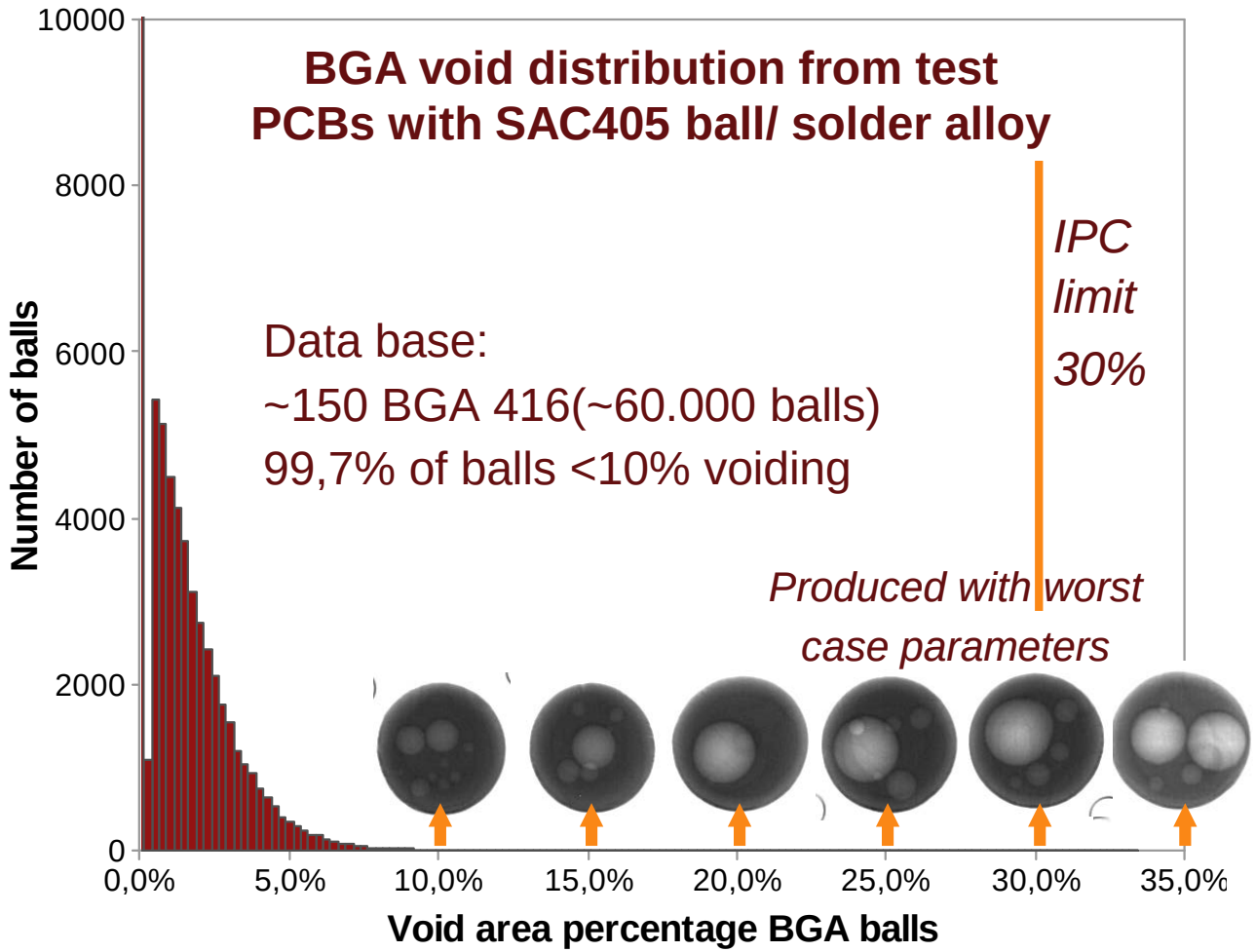
Acceptable – Class 1,2,3

- 30% or less voiding of any ball in the x-ray image area.

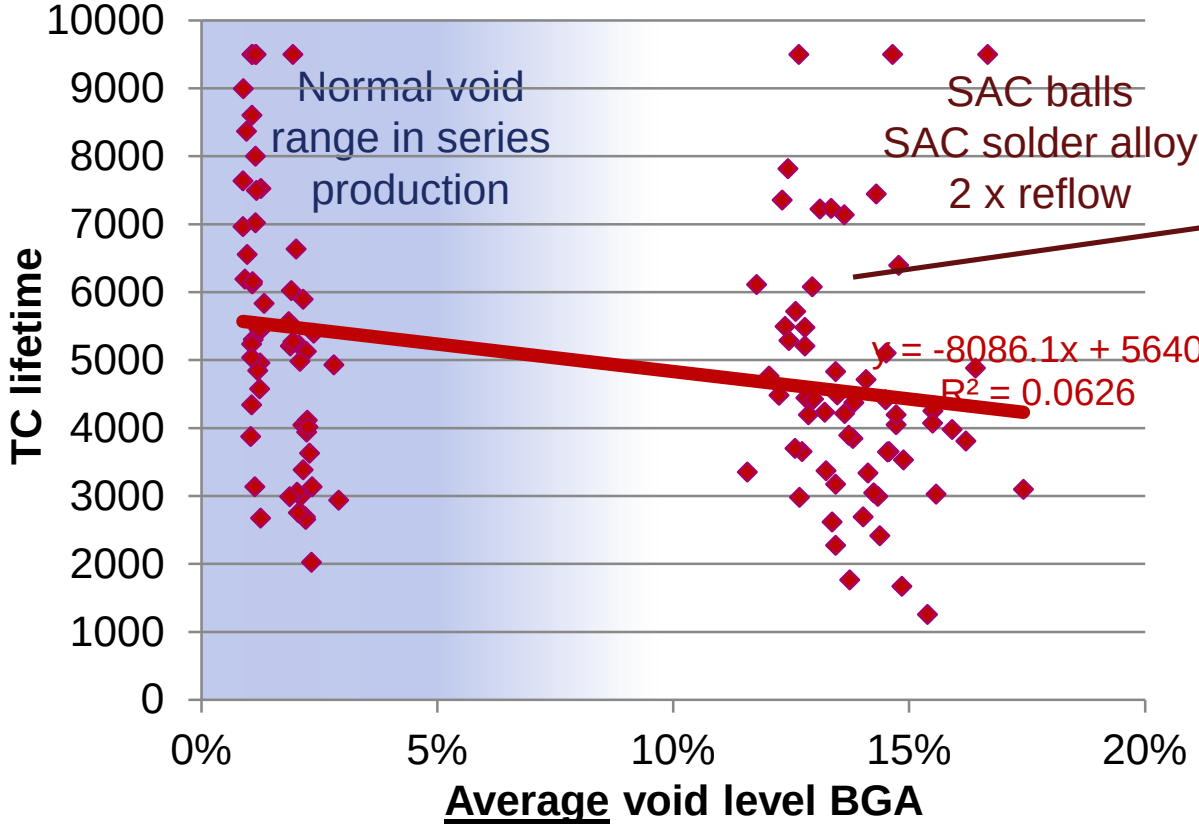
Defect – Class 1,2,3

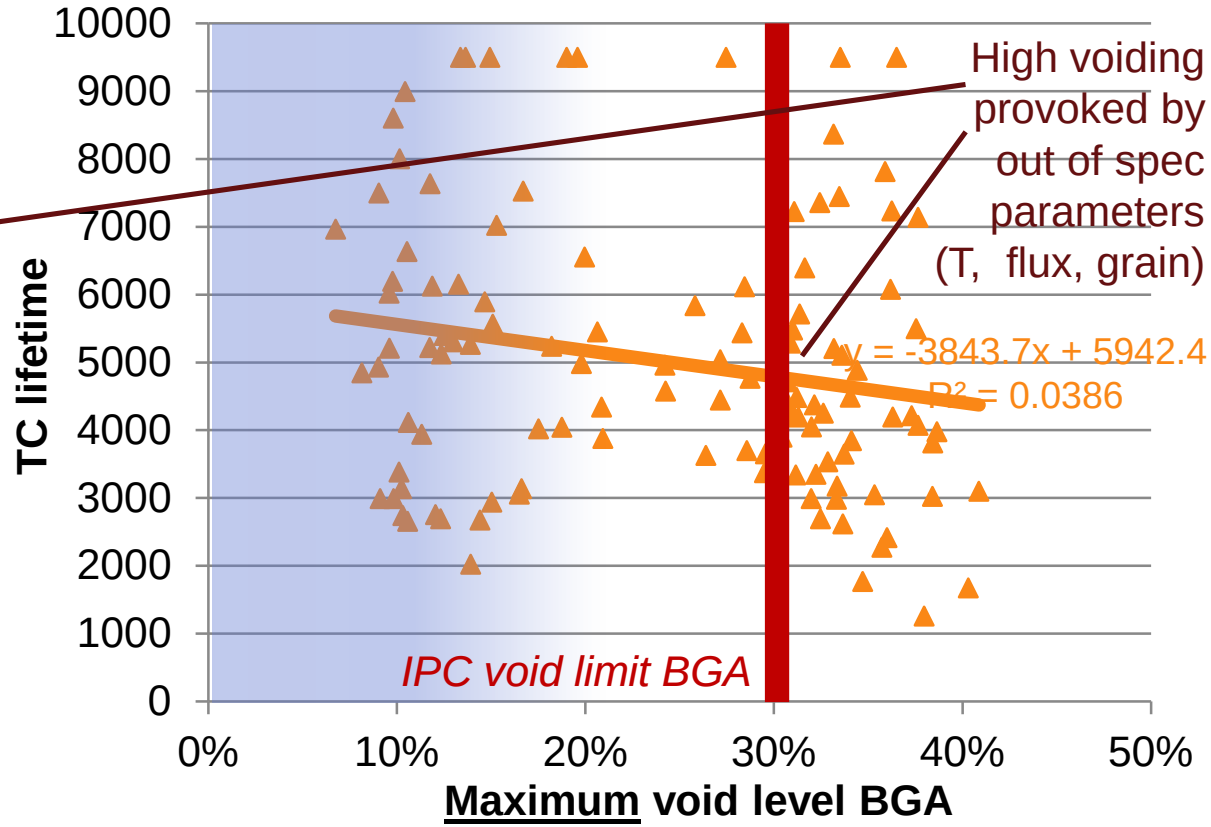
- More than 30% voiding of any ball in the x-ray image area.

- Average void area percentage BGA in series production normally < 5%
- Cpk-prognosis difficult (no normal distribution of void values)
- No limits and no control defined for other components/ solder joints



Influence of voids on TC reliability: Evaluation BGA 416

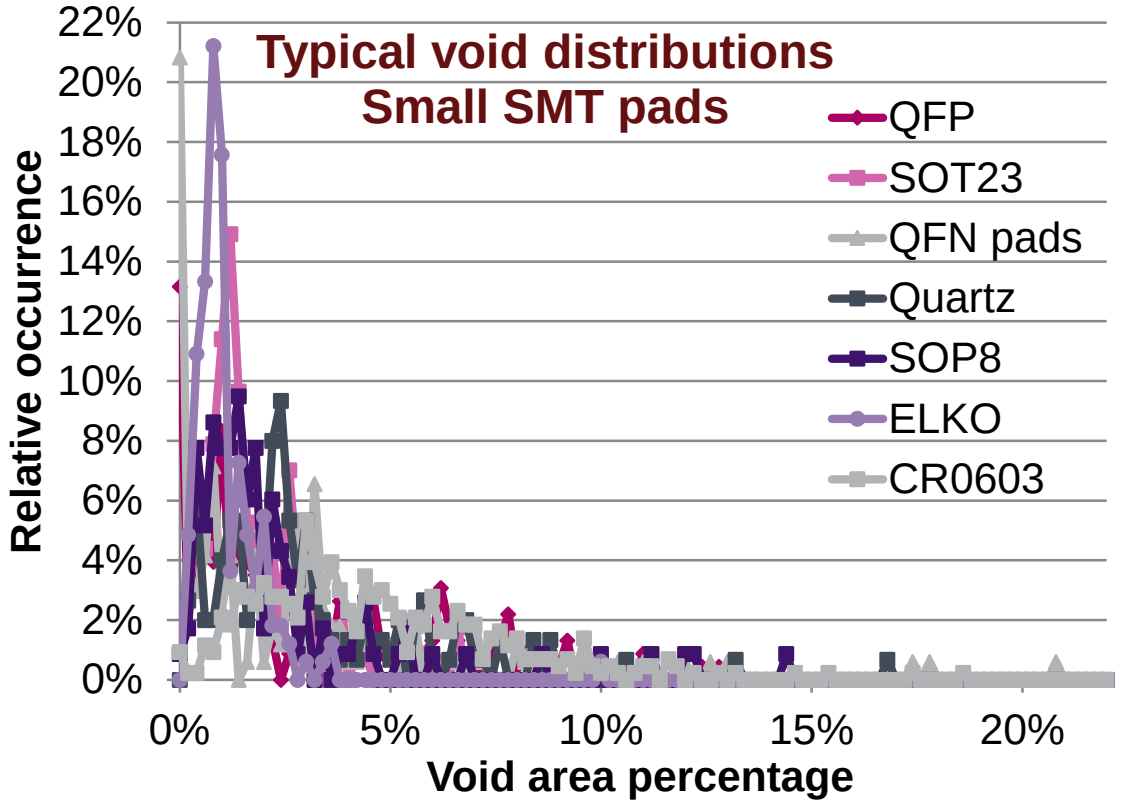


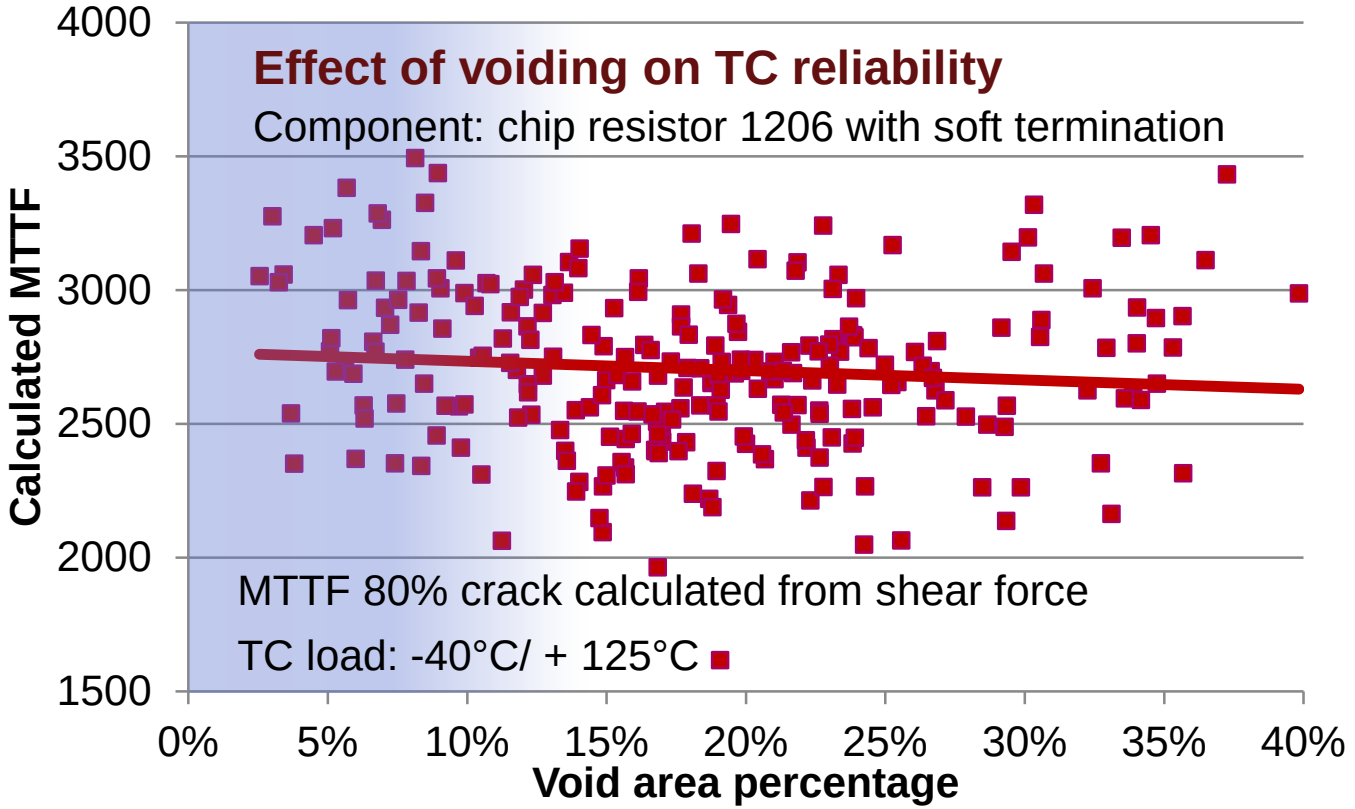


- High variation of TC values independent of void level
- Only slight influence of average and max void level on solder joint reliability

⇨ Current IPC BGA void limit reasonable for processability and reliability

Influence of voids on TC reliability: Small SMT pads





- Mean void level of small SMT solder joints in series production < 10%
- Only few values > 20%

TC reliability of CR with high void level:

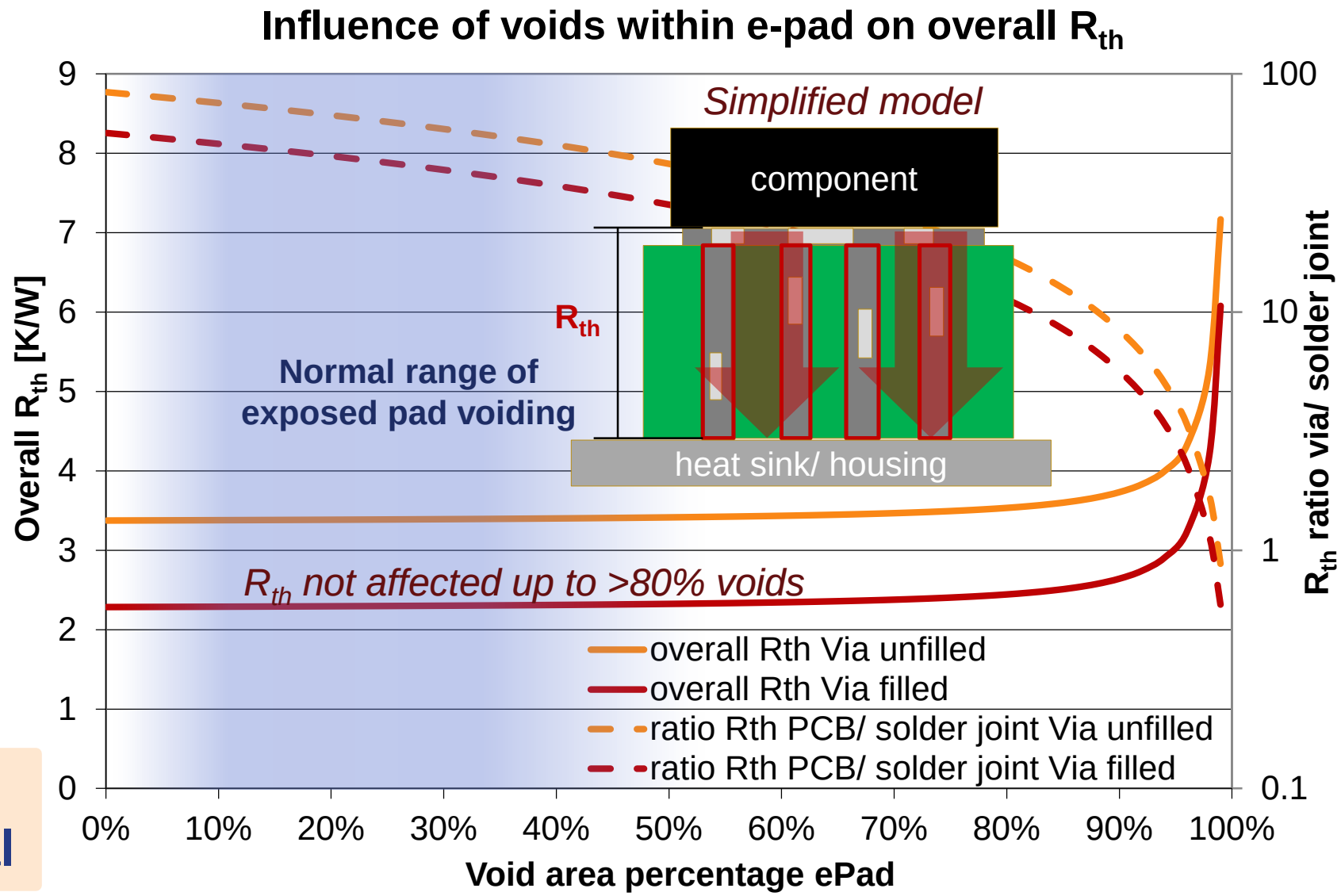
- High variation independent of voids

⇨ No significant reliability influence of standard void level

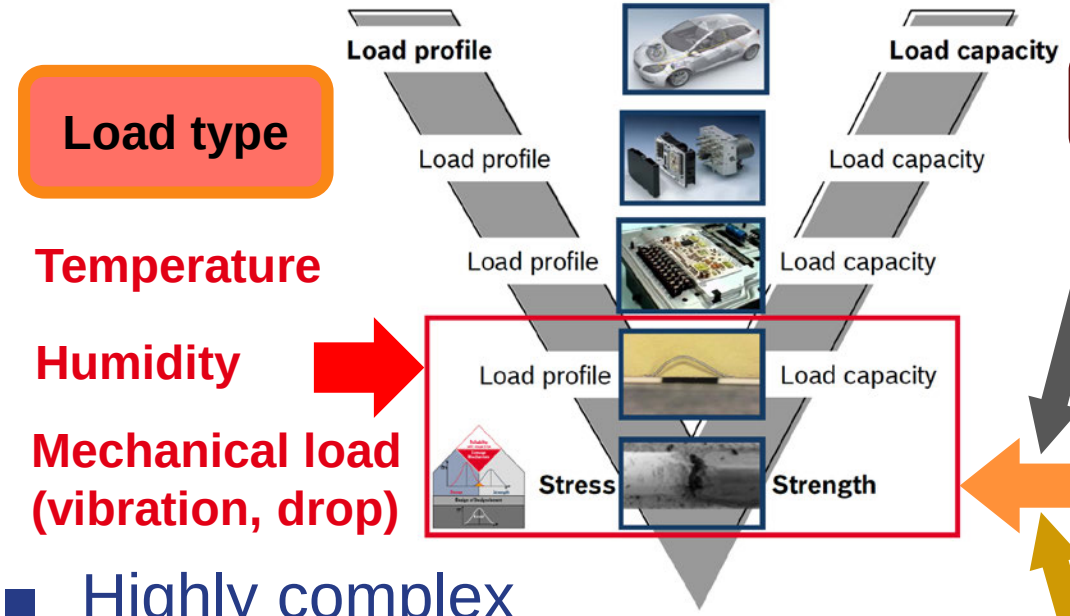
Influence of voids on thermal resistivity: R_{th} calculation e-pads

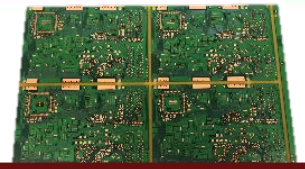
- No IPC limit for exposed pads
- Calculation of thermal resistivity R_{th} for exposed pads on **standard PCB**: Heat flow dominated by PCB and vias, even if solder-filled
- Exposed pads not critical concerning TC reliability

⇨ Normal voiding of exposed pads uncritical



Solder joint reliability





PCB

Component

Solder paste

Stackup

Base material

Metallization

Surface quality

Termination

Plating type

Alloy

Flux

Grain size

Reflow profile

Placement

Printing

Voids

Solder volume

Pad design

Standoff height

Phase separation

Grain refinement

IMC

Process/ machine

Solder joint geometry

Solder joint structure

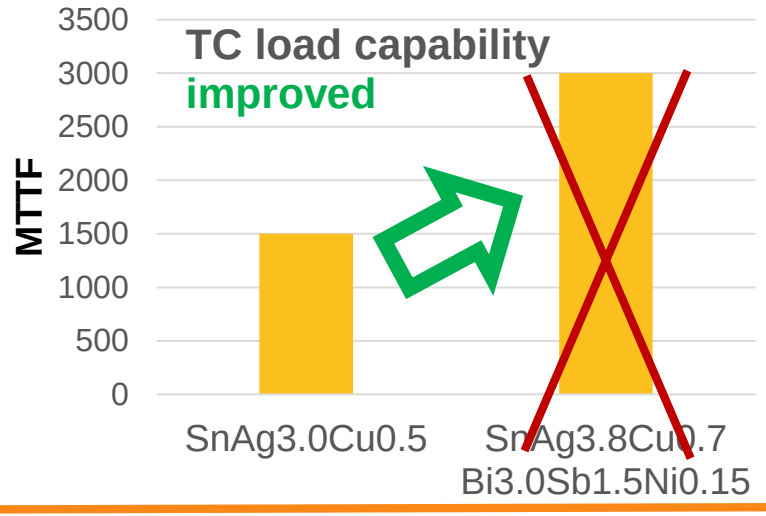
- Highly complex and interactive system
- Voiding only one aspect of solder joint reliability
- Void formation affected by many other reliability relevant parameters

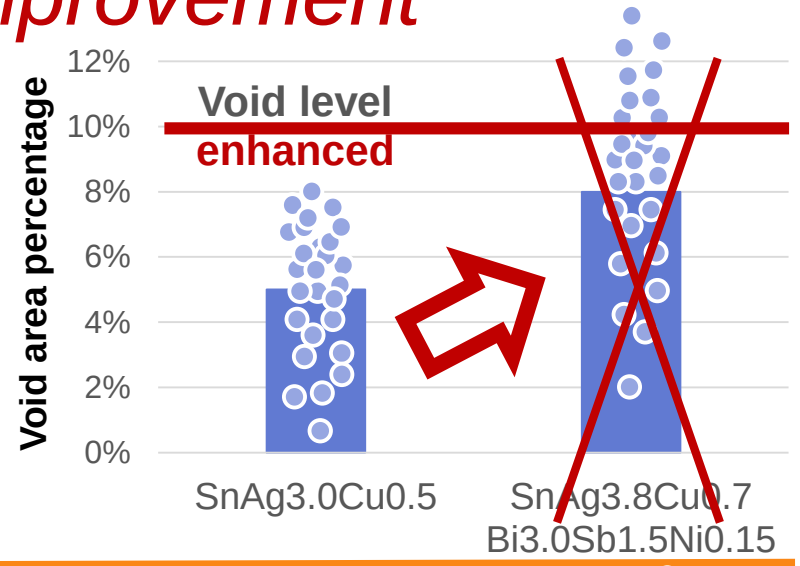
⇨ **Voiding optimum ≠ reliability optimum**

Consequences of void optimization

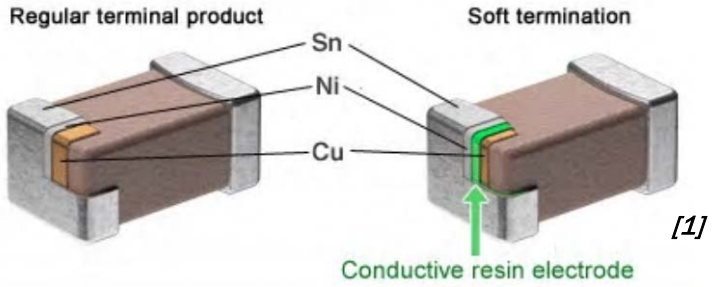
"Void limits may impede reliability improvement"

- Example 1:
  solder alloy:
  SnAg3.0Cu0.5/
  SnAg3.8Cu0.7
  Bi3.0Sb1.5Ni0.15





- Example 2:
  chip resistors with
  hard/ soft termination



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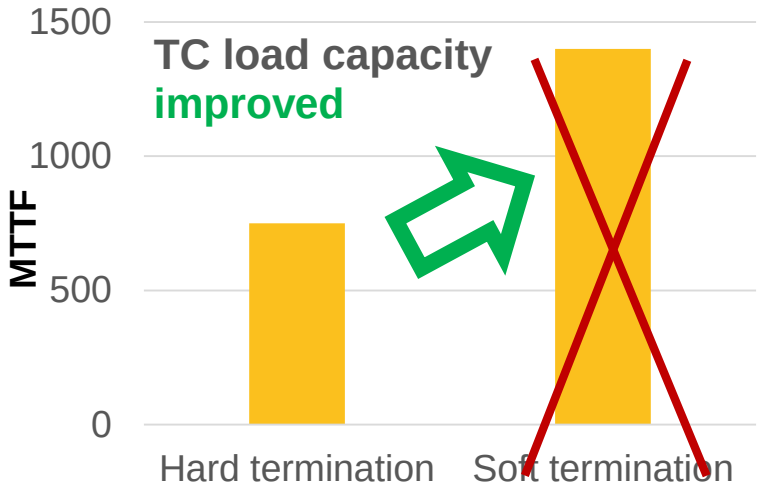
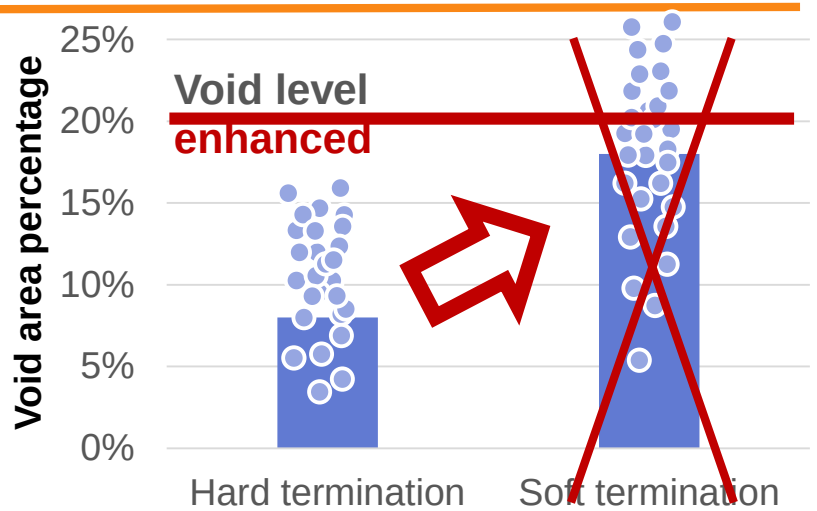




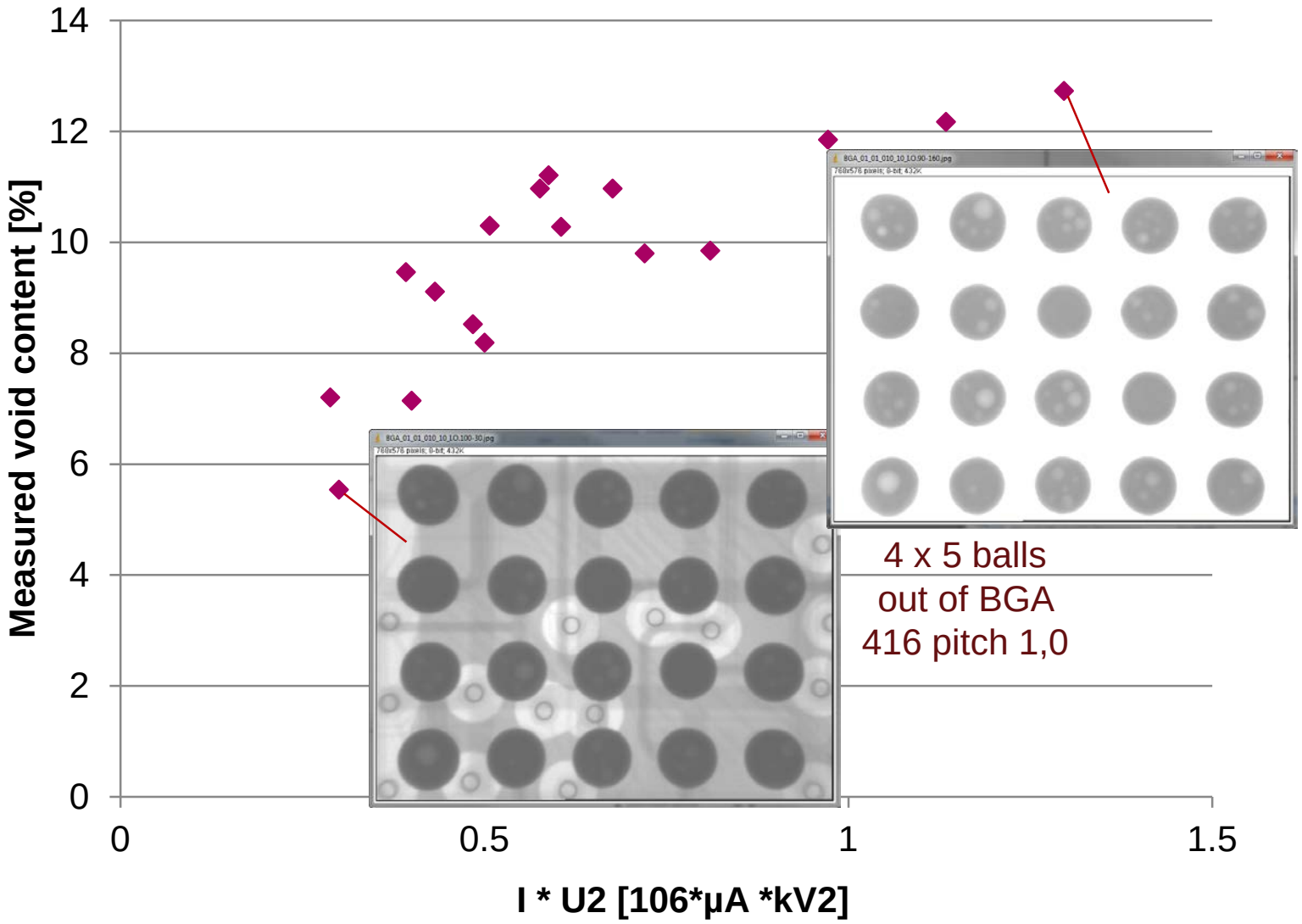
Consequences of void optimization

Void evaluation with different X-ray parameters (U/I):

- Void measurement highly depending on machine adjustment and image evaluation (each ~factor 2)
- Measurement standard not available

⇨ **Measuring capability not given**

⇨ **High effort for increased X-ray void control not justified**



Conclusion

- ⇨ Void formation is highly process intrinsic for lead free soldering
- ⇨ Void level can be controlled by stable material and process parameters
- ⇨ No significant influence of normal, controlled void level on product reliability
- ⇨ Void measurement not capable
- ⇨ Further void limitation not useful

References

- [1] ***Source: mouser.co.uk***

Thank you!