SLP+

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Multek

Abstract

As the IoT market demands higher data rates and processing, the PCB technology is driving for smaller form factors, higher signal densities, and advanced material solutions. Miniaturization has been a common trend. Besides reduction in transmission-line and space widths, higher density and bump pitches down to 200 microns, as well as smaller diameter microvias down to 50 microns will be required. The finer features challenge suppliers of equipment, chemistry and materials to find solutions to support the PCB fabrication requirements. This presentation addresses the science and technologies developed in collaboration with supply partners to understand, develop and deliver a 10-layer "substrate-like PCB +" (SLP+) with 50 micron diameter stacked microvias, transmission line and space of sub-25 microns and full array 200 micron pad pitch circuit technology solution to enable the next generation of IoT PCB requirements. This SLP+ technology goes beyond the MSAP/SLP technology that several suppliers are currently implementing. The sub-25 µm line and space is achieved with a modified semi-additive process (MSAP) that electroplates copper through openings in the dry-film, instead of using the dry-film as an etch resist. The initial SLP+ designs with leading smartphone customers and M2M modules are in the development phase. The extension of this technology drives feature sizes down to sub-25 micron line/space and 200 micron solder-bump pitch and below. This technology allows down to 200 µm pitch ICs to be directly attached to the PCB, thereby eliminating the need for a BGA substrate. Without the BGA substrate, reductions in z-height are achieved. The thermal resistance to the PCB plane and any rear heatsink is reduced by eliminating the BGA substrate. Similarly, signal integrity is improved by removing impedance discontinuities at the additional interfaces of the BGA substrate. Consumers will see their devices shrink beyond the current state-of-the art, and with performance improvements. The presentation will demonstrate 'advanced high-density interconnect' produced in high volume in collaboration with suppliers. The interconnect solutions include a single line between pads at 200 µm-pitch, and two lines between pads at 250 µm-pitch. Thermal cycling (air-to-air and liquid-to-liquid), and 10X solder reflow reliability test results will be presented.

Introduction

Virtually all modern electronic devices require interconnects to connect between active semiconductor devices, passives, communication devices and antennas, and HMI devices. For high-end electronics, a BGA substrate fans out the fine-pitch array of a semiconductor die to standard pitches that can be mass-produced with existing PCB manufacturing technology. However, with continued trends toward miniaturization in smartphones, tablets, and wearables, every cubic micron of saved space leaves more room for battery or reduced weight and volume. The PCB industry therefore has a compelling incentive to support direct-attach, wafer level packages (WLP) to a PCB without the need for a BGA substrate, even for devices with a high I/O count. Advances in PCB technology will allow direct-attach WLP with solder-ball pitch of 200 µm to be in mass production by 2019 as shown in Figure 1 below. [1]

Design

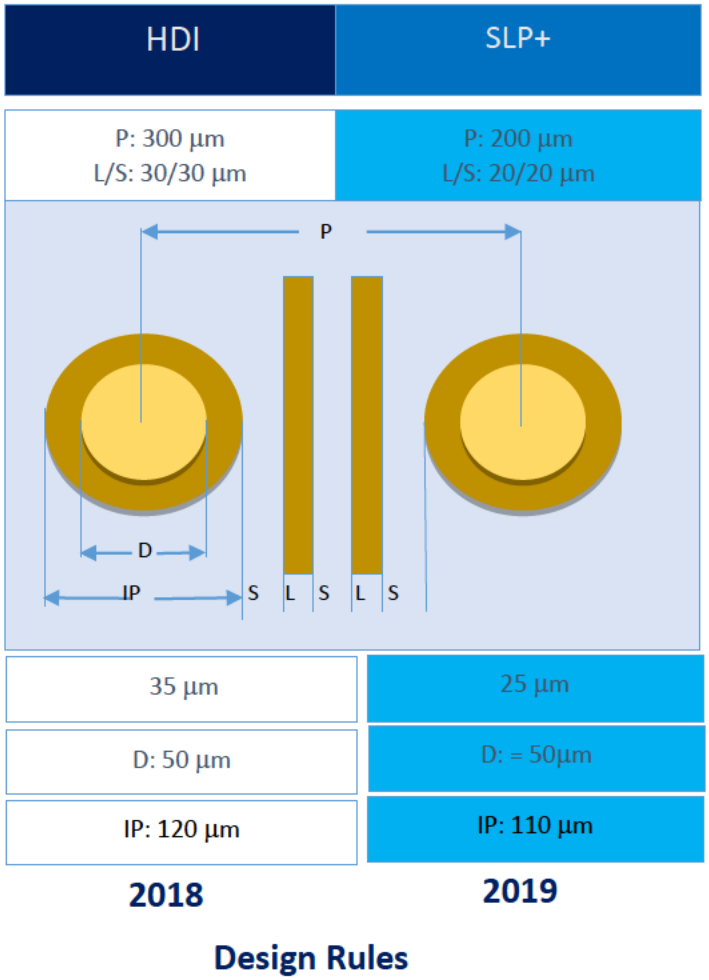


Figure 1: Reductions in line, space, via diameter, and registration tolerance to 200 µm solder-ball pitch with two traces between pads on inner layers.

BGA Routing:

BGA routing is the process of connecting the power, ground, and signal pads in a BGA to connections outside of the device. Typically, routing out from a fine-pitch BGA package is the most difficult part of PCB layout, and determines the number of layers and the level of technology that will be used. For fine-pitch BGAs (<=0.4mm), it is generally not possible to route traces between pads using conventional PCB fabrication technologies. This means all signal pads on inner rows of the array must use via-in-pad to drop down to the lower layer and then escape outward. The ability to rout signal lines between BGA pads could provide greater routing flexibility for the designer and potentially reduce the layer count. At the outer row of pads, signals from at least one signal per pad can escape the package, but inside that region traces must be routed between pads. The number of traces that fit between pads for a given pitch is a key number that determines the number of required layers of a PCB, and is determined by the pad size, drill-to-copper clearance, trace, and space dimension. The pad size is a function of the laser via drill diameter and registration tolerance of the fabricator. Therefore, it is necessary to reduce via diameter, linewidth, spacing, and the registration error between layers. Typically, routing between pads is not permitted on the outer layer to prevent topography on the soldermask that might interfere with assembly.

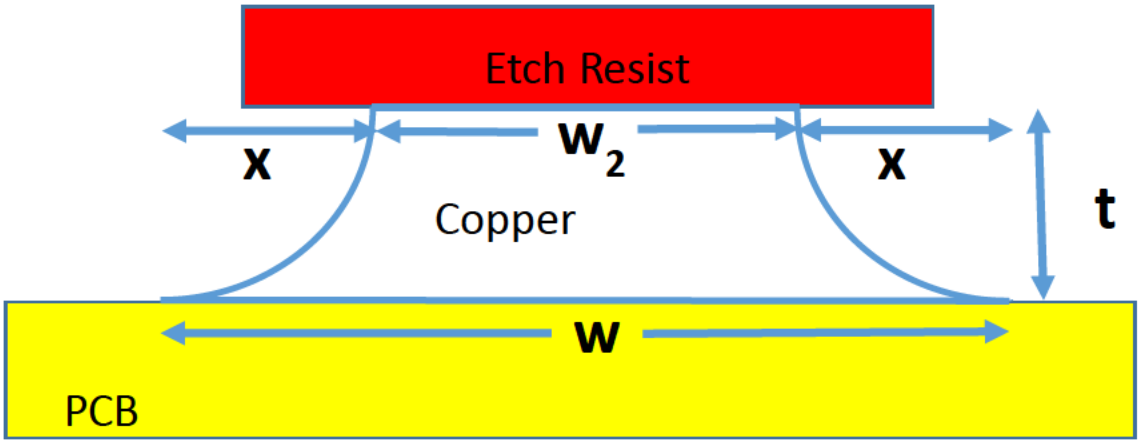
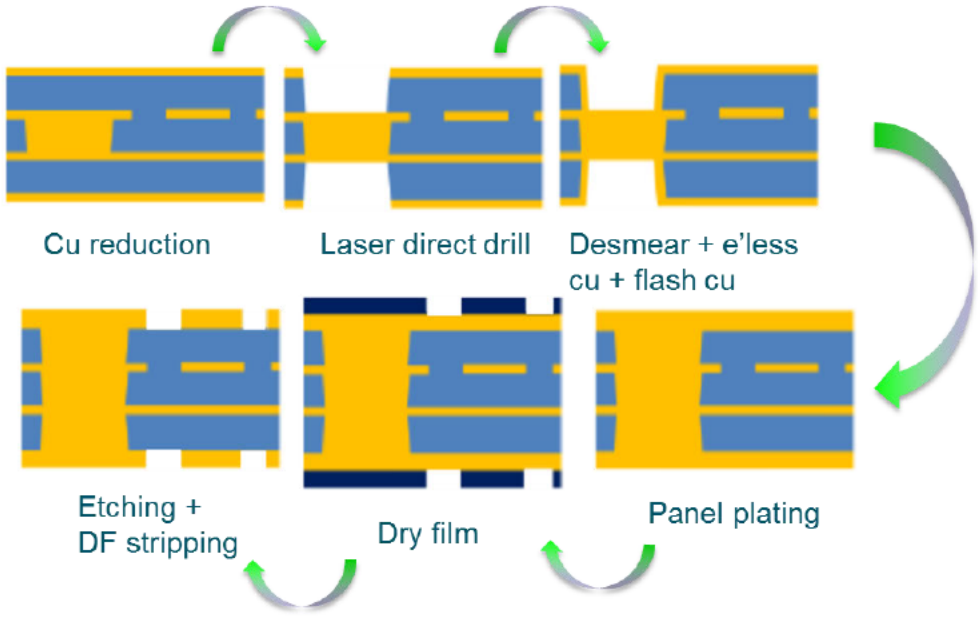


Figure 2: Typical copper undercut in a subtractive process

Limitations to achieving finer line and space:

In a typical HDI process, copper is etched subtractively to form the circuit pattern. In this process, the trace is subject to undercut due to inevitable lateral etching by the solution in addition to the desired vertical direction. The undercut is quantified with the etch factor, which is the ratio of the copper thickness to the undercut. As shown in Figure 2, the etch factor is t/x, and the higher the etch factor, the more precise the circuit definition. To attain high yield, the PCB fabricator must ensure that adjacent copper traces do not complete the circuit and produce a short. The undercut variability means that the patterned feature must be kept a greater distance apart to prevent faults, and makes fine lines easier to attain than fine spaces. Higher resolution is attainable with thinner copper, but copper thicknesses of 12 µm or greater are typically required to minimize resistive losses, avoid laser via punch-through, and to fully copper-fill laser vias.

Process



Traditional PCB Manufacturing Process Panel Plate

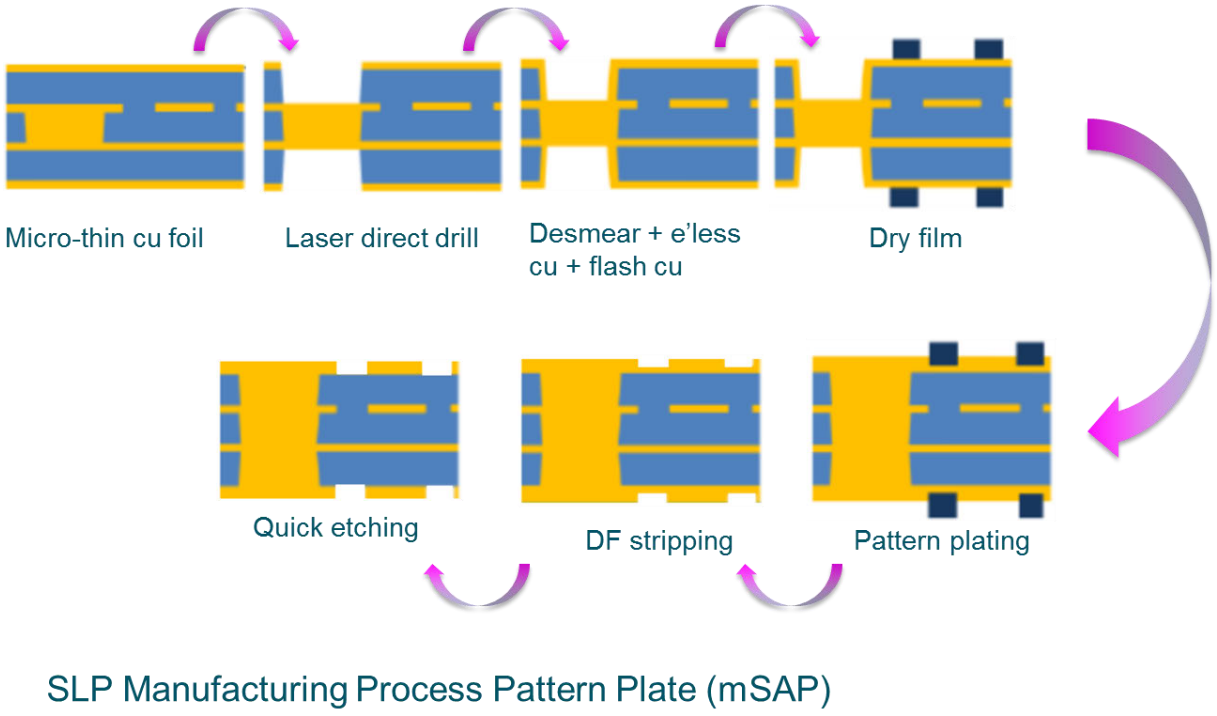


Figure 3: Traditional and mSAP processing compared

Hybrid Designs:
The fine-line MSAP process is higher cost than anylayer processing because of micro-thin copper foil prices, higher-end processing equipment, higher cleanliness standards, even more expensive laminates with greater dimensional stability to enable pad size reduction. Smaller vias also requires lower z-expansion laminate material and are at present more expensive to form. Therefore, hybrids stack-ups allow designers to put fine features only key routing layers for cost reasons.

MSAP Process:
With the modified semi-additive process (MSAP), a thin foil with a fine tooth is used as a seed layer for electroplating. After lamination, laser vias are drilled, cleaned with a desmear process, treated with a palladium catalyst, plated with electroless copper, and then electroplated with flash electrodeposited copper to protect the electroless copper. Dry film photoresist is laminated to the panels on both sides, and the dry-film photoresist is patterned with a laser direct imaging system (LDI), and developed. The vias and the traces are electroplated at the same time, the dryfilm is removed, and the copper foil electroplating seed layer is removed in a wet etch. The wet etch to remove the seed also etches the traces and pads vertically and laterally, however it does so uniformly, and maintains the vertical sidewalls.

MSAP Etch Compensation:

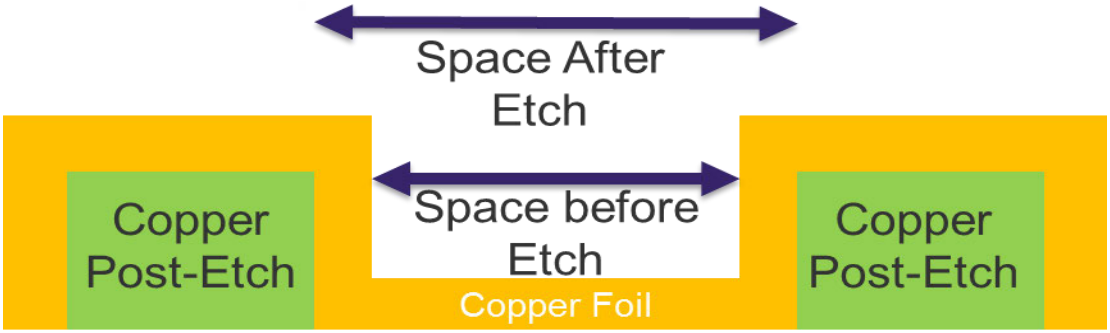


Figure 4: Etch Compensation and Minimum Feature Size

During copper foil seed removal, the etched distance (etching time x etch rate) is the sum of the thickness of the foil (minus copper removed in oxidation or cleaning), the electroless copper, the foil tooth, and a safety factor to account for the variability in etch rate (including the oxidation and cleaning steps) and the aforementioned thicknesses. It is therefore advantageous to have thin, low profile copper, and very uniform electroplating and etching, to minimize the amount of required etching. The width of the final space is increased by 2X the etch distance. For example, if there is an etch distance of 5.5 µm, and the laser direct imaging (LDI) system has a minimum line (which becomes a space because no electroplating can occur where there is photoresist) of 10 µm, the minimum space is 21 µm. Therefore, to define a 21 µm space, the artwork should define a 10 µm space.

Materials

There are two key CTE mismatches in a PCB: between the copper vias and the glass-reinforced resin, and between the PCB and the attached components. In order to further miniaturize the PCBA, greater effort must be expended to minimize the CTE mismatch strain.

Material CTE for IC Durability:

The coefficient of thermal expansion (CTE) of typical FR4 PCB laminate ranges from 6 to 30 ppm/°C in the plane of the laminate (warp or fill), compared with the CTE of silicon, which is 2.6 ppm/°C. As the part heats up and cools down, thermal mismatch between the laminate and copper pattern and the semiconductor die can either fracture the semiconductor die or the solder joint. A key challenge is that pre-preg made of thin glass (1027 and below), has dramatically higher CTE than the thicker weaves that the datasheet CTE values are based. A very common approach to minimize this stress is to use underfill, which is a ceramic filled polymer that is injected adjacent to the die and wicks under the die from capillary forces. The underfill serves to reduce the stress concentration at the solder-joint, and improves drop test and thermal cycling reliability [2]. However, the use of underfill requires a keep-out area between components to allow room for the underfill needle. In some applications, components spacing is so close that it is difficult to use underfill because of the keep-out area required for the needle. In cases where no underfill is allowed, it is important to use materials with lower CTEs, especially in the outer layers close to the die.

Material CTE for Via Size Reduction:

To enable smaller laser vias, the Z-axis CTE of the material must be engineered to be closer to copper over the expected temperature range. Polymers have a non-linear dependency of CTE as a function of temperature, which is approximated by a CTE below Tg (α_1) and above Tg (α_2). A typical IC substrate material (T_g of ~270°C) has a Z-axis α_1 values of 10-15 ppm/°C and α_2 values of 70-90 ppm/°C. More conventional and lower cost HDI materials (T_g of ~170°C) have a Z-axis α_1 values of 40 ppm/°C, and α_2 values of 200 ppm/°C above T_g, which leads to much more thermal expansion during reflow.

Laser Via Size Reduction:

Reducing the laser via size leaves room for more traces between pads or a reduction in pitch. However, a reduction in laser via size reduces the via contact area, which can be vulnerable to delamination during reflow due to z-axis expansion if not managed properly. To mitigate this strain, we need to utilize laminates with either higher glass transition points (T_g) or lower CTEs in those layers. Multiple laminate suppliers have developed material for the IC Substrate market with T_g in the range of 270-290°C, so that the material never exceeds T_g, even during lead-free solder reflow, and therefore does not exceed the lower α_1 CTE range. A typical HDI targeted laminate has an IPC 2.4.24 Z axis expansion of the order of 2.4 %, while an IC substrate targeted laminate has one of 0.3 %, almost an order of magnitude lower.

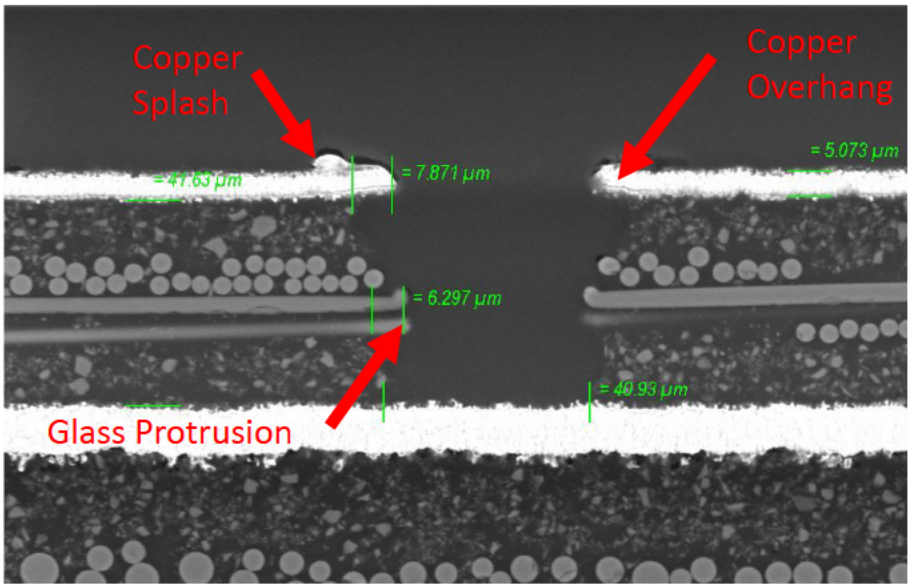


Figure 5: Laser via cross-section

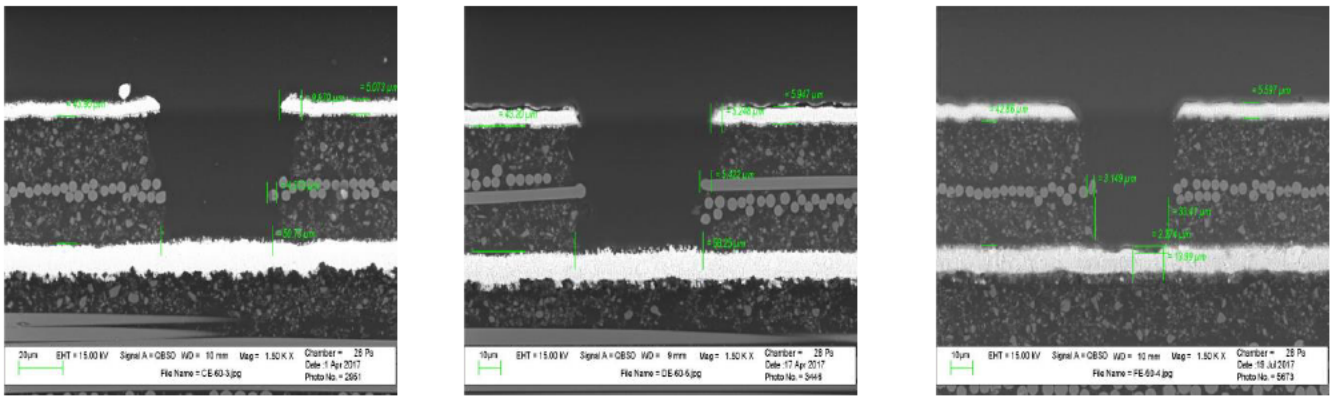


Figure 6: Representative samples of 50-micron diameter vias drilled with CO_2, UV +CO_2, and Picosecond Green Laser.

Moreover, as via diameters decrease, it becomes increasingly difficult to reliability electrodeposit copper with the solid via filling process into the hole without creating voids. Voids further reduce the effective via-cross section and become crack-initiation points. The bath chemistry in the mSAP process is carefully engineered with levelers and brighteners to electroplate copper more quickly in the hole than on the surface to minimize surface dimples. However, even the best bath electrochemistry cannot only accommodate a limited amount of copper splash, copper overhang, and glass protrusion, which is shown in Figure 5. While CO_2 direct laser drilling is the standard for high volume PCB production because of its high throughput, it leaves a copper overhang that increases the probability of voids, and splash that results in surface non-uniformities. New drilling technologies have been developed that cut a smoother hole, and therefore have lowered the incidence of voiding, but the tradeoff is slower drilling speeds and thus lower throughput. These via formation technologies include UV-CO_2, UV, and Pico-second lasers as shown in **Error! Reference source not found.**. By minimizing the copper overhang, the incidence of voiding is reduced, which can become crack initiation points.

Reliability Testing

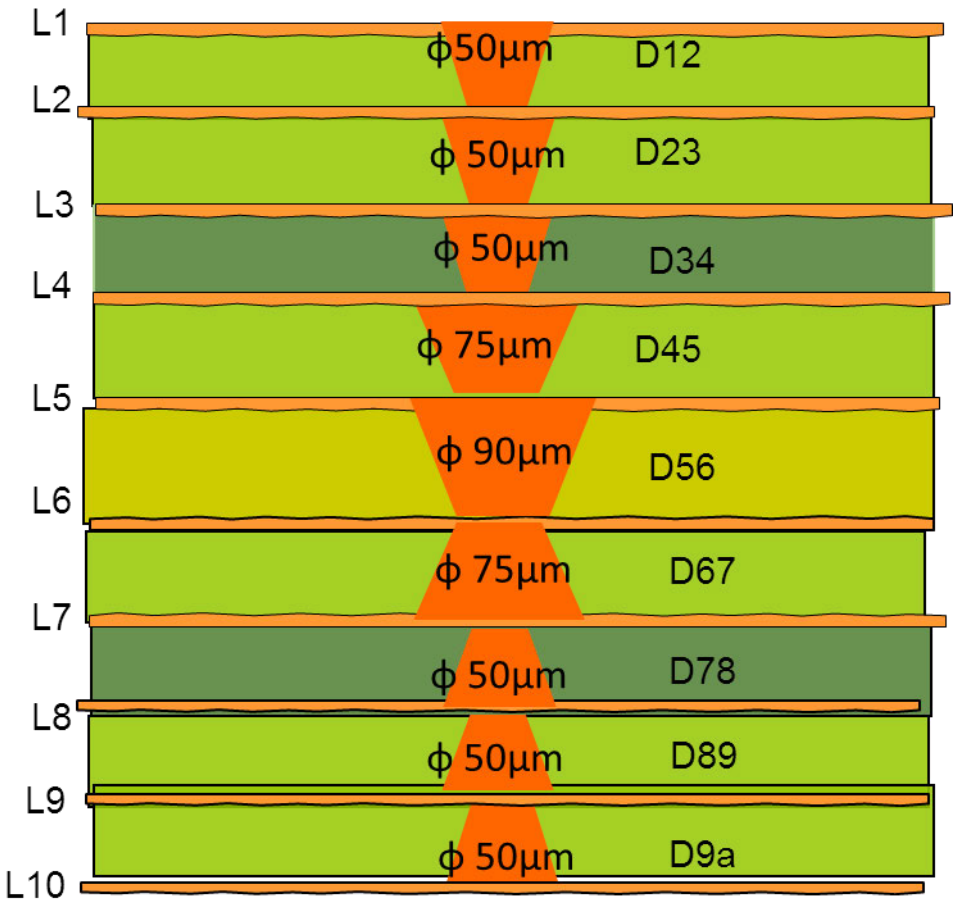


Figure 7: Stack-up of via reliability test vehicle: Layers with via diameters of 50 um are produced with substrate-like materials (T_g of ~270°C, Z-axis α_1 values of 10-15 ppm/°C). All other layers are made with conventional HDI materials (T_g of ~170°C, Z-axis α_1 values of 40 ppm/°C, α_2 values of 200 ppm/°C above T_g).

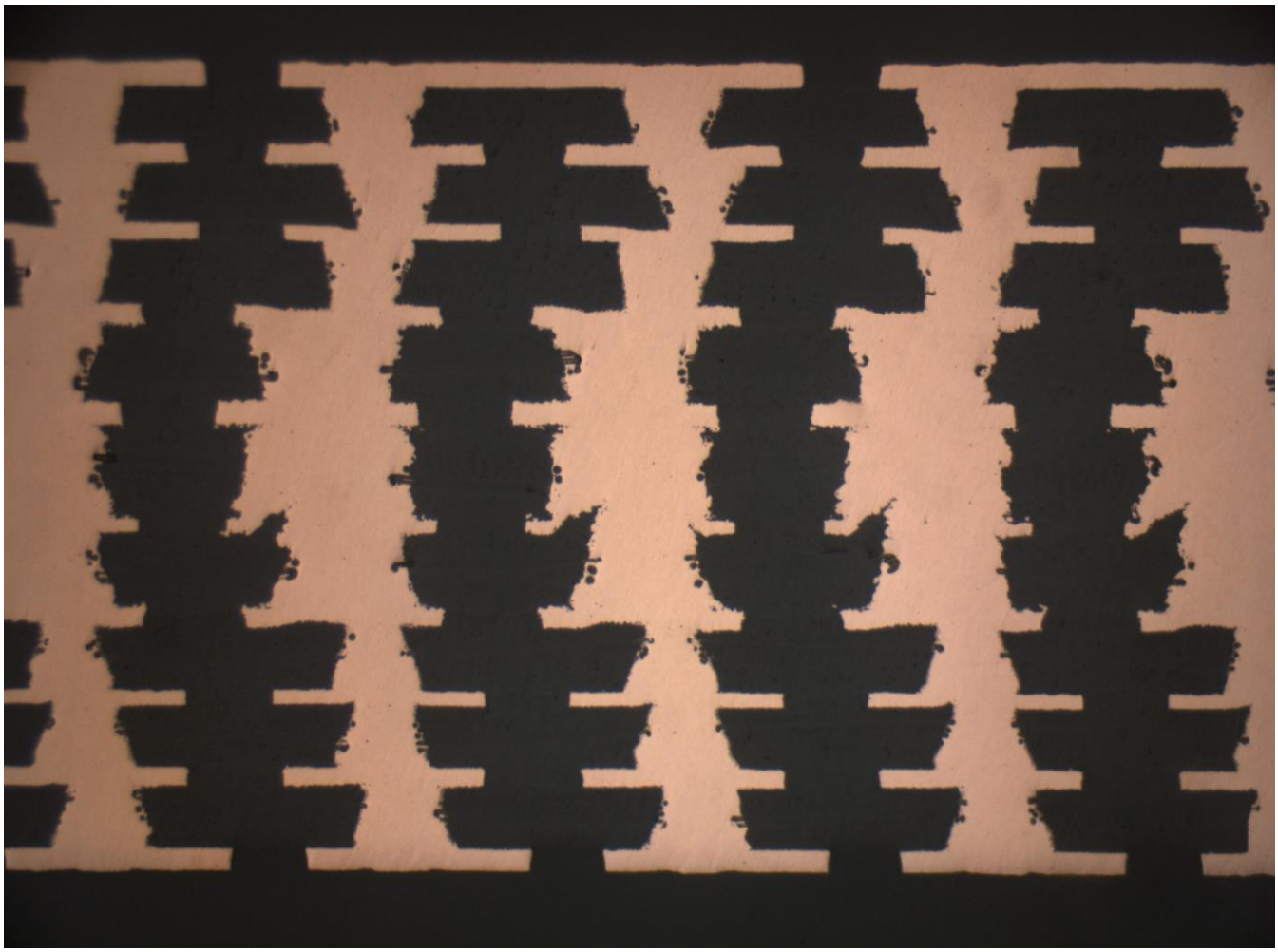


Figure 8: Cross-section of stack-up after 10X reflow testing.

Testing the Reliability of Small, Stacked uvias: Compared with conventional 100um uvias, the small contact area of a 50um uvia makes these features vulnerable to separation from the target pads due to z-axis expansion of the laminate material during reflow. The CTE mismatch between copper and laminate can result in thermal mismatch stresses at the junctions, in particular the bottom of laser vias. To test this reliability, test the bare boards with 10 lead-free solder reflow cycles, which is the largest temperature excursion a PCB will encounter. In the typical assembly of a PCB, it will experience 2 reflow cycles to solder components on the top and bottom. A PCBA may encounter additional cycles if rework is performed. Most OEMs require 6X solder reflow testing, but we have increased that to 10X to establish a safety factor with the profile shown in Figure 9. In addition, to solder reflow, some PCBs also encounter thermal cycling during use. Therefore, we test bare PCBs shown in Figure 7 with both Air-to-Air and Liquid-to-Liquid testing. The liquid-to-liquid temperature ramp is only 15 seconds. For the testing, any resistance change greater than 10% is considered a failure. If there is voiding caused by poor hole formation, poor chemistry, or poor agitation, it concentrates the force into a smaller area, which can result in crack formation.

The bare PCBs tested were 10 layers with stacked vias going from L1 to L10 as shown in Figure *7* and Figure 8.

Conclusions:

Using state-of-the-art laser drilling and high-Tg materials, we have reduced via, trace, and pad sizes to deliver a 200 µm-pitch BGA. Trace size has been reduced with a MSAP process that improves the trace profile and resolution. Via size has been reduced with improved laser via formation, and improved materials with lower z-axis expansion to improve reliability of the small via. The finer pitch allows the removal of the BGA substrate even for ICs with greater I/O count, and the utilization of WLCSP, to reduce the interconnect footprint in X, Y, and Z dimensions.

The 200 µm-pitch interconnect solution passes 10X solder reflow and 1000 cycles of air-to-air and liquid-to-liquid thermal cycling.

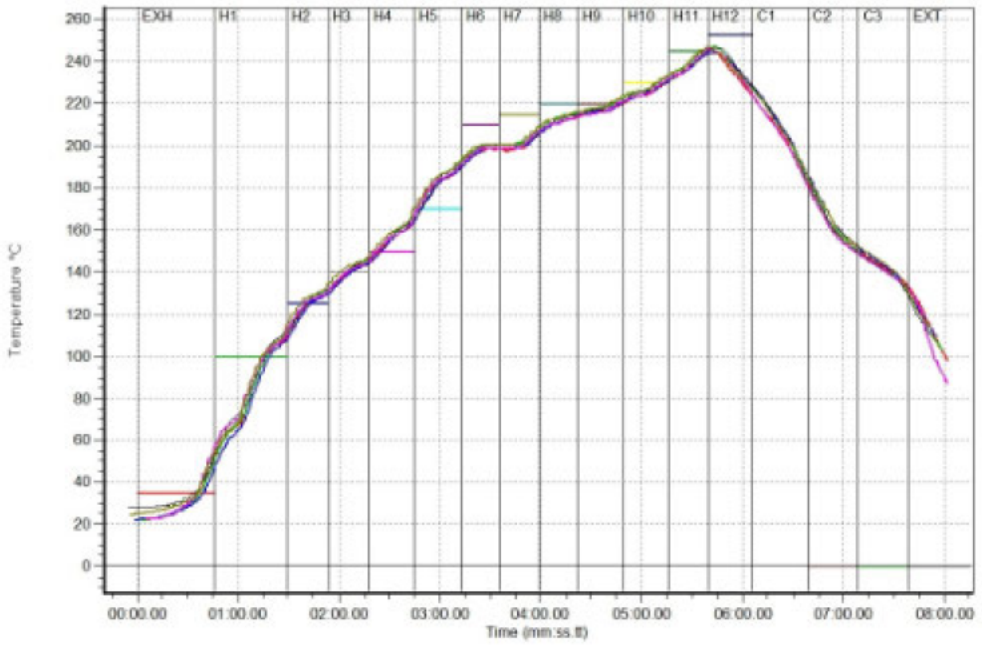


Figure 9: Lead-free solder reflow profile

- LLTS condition - 5X reflow cycles (preconditioning) + 1000 cycles (-55°C / 125 °C, 5 / 5 min dwell time,15 sec transition)
- Air-to-air condition - 5X reflow cycles (preconditioning) + 1000 cycles (-55°C / 125 °C, 10 / 10 min dwell time)

Table 1: Summary of Reliability Results

Laminate	Pitch (µm)	Reflow	Air-to-Air Cycling	Liquid-to-Liquid Cycling
HDI / IC Substrate Material Hybrid	200, 250, 300	Passed 10 cycles	Passed 1000 cycles	Passed 1000 cycles

References

[1] S. Qu and Y. Liu, Wafer-Level Chip-Scale Packaging, Springer, 2015.

[2] K. Mishiro, S. Ishikawa, M. Abe, T. Kumai, Y. Higashiguchi and K.-i. Tsubone, "Effect of drop impact on BGA/CSP package reliability," *Microelectronics Reliability,* 2002.

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SLP+

Michael Glickman, PhD.

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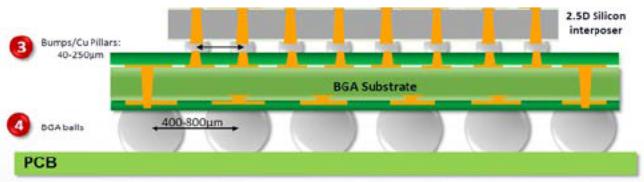
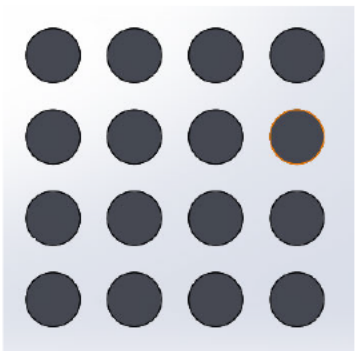
Multek

MOBILE	IoT MODULES	AR/VR

Industry Standard

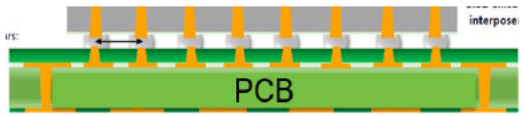


Cross-section: w/ BGA substrate



Top View: 400 µm pitch

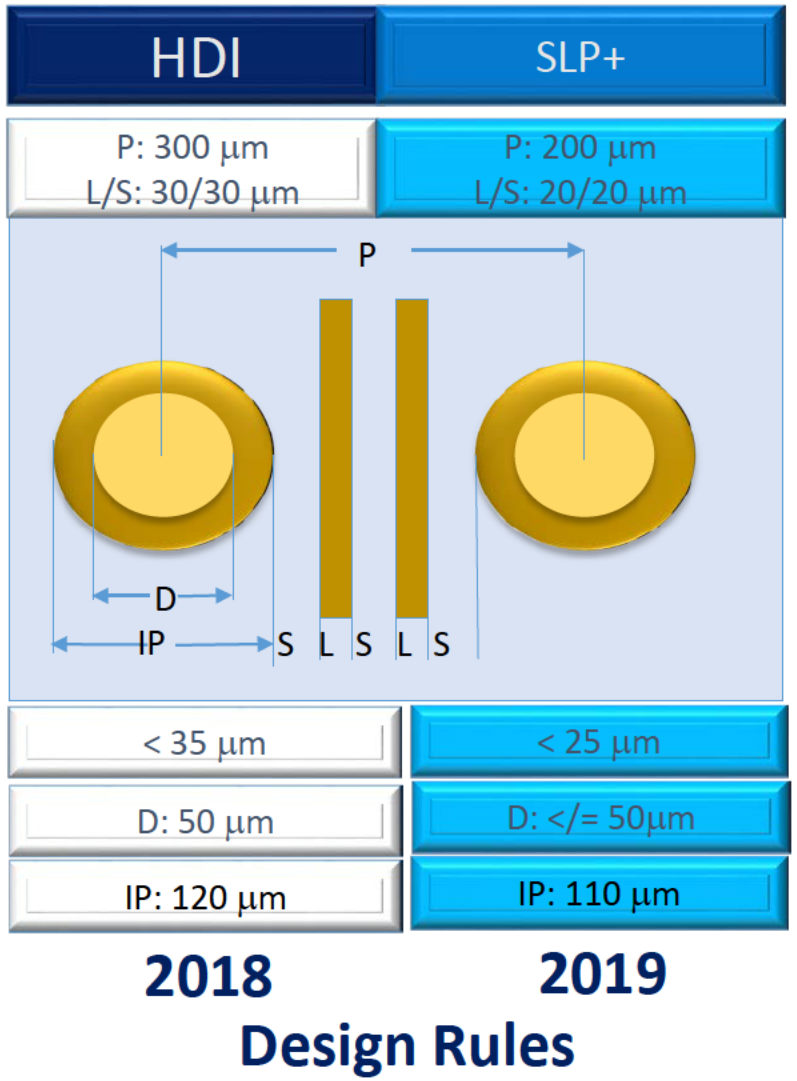
SLP+ Volume Reduction



Cross-section: BGA Substrate Removed

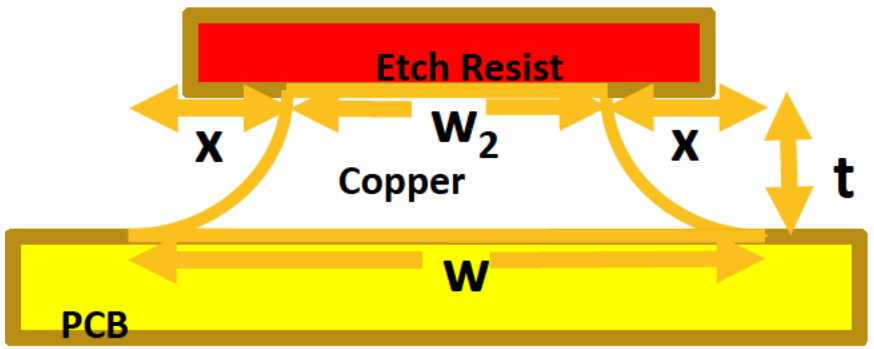
Top View: 200 µm pitch

- 25% height reduction
- 40% higher density
- Removes BGA Substrate Cost



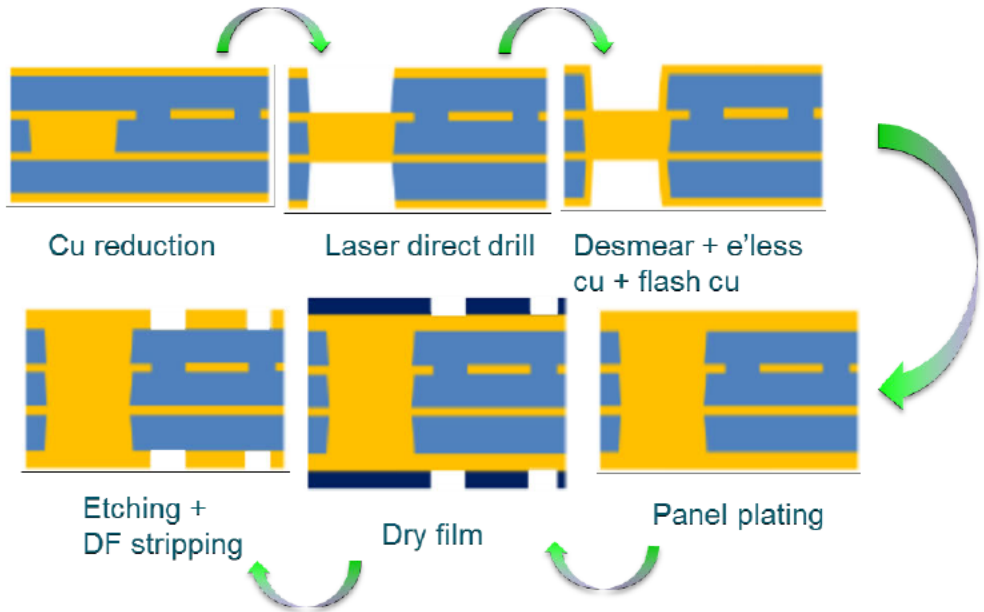
- Reduction in pitch
- Reduction in line-width
- Reduction in landing pad

Finer Circuit Patterns



- Etch Factor: t/x
- Limits minimum space and line control

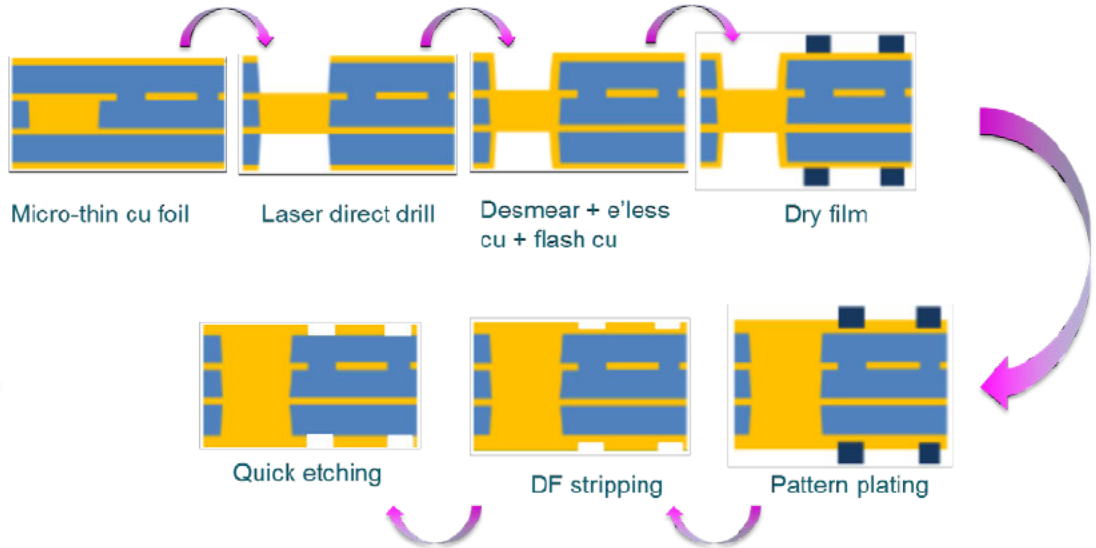
Traditional Subtractive Process:



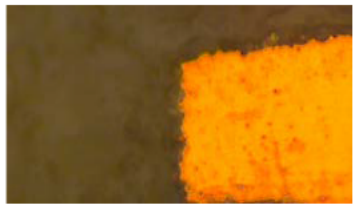
40 um Line
30 um Space

Example Profile

MSAP Process:



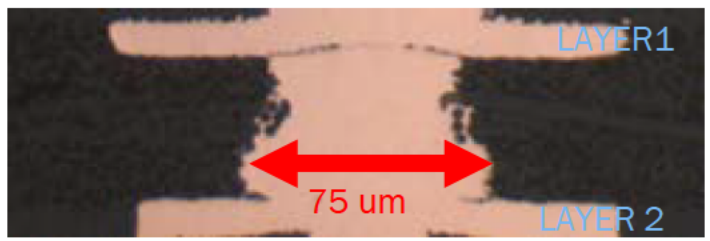
20 um Line
20 um Space



Example Profile

Via Size Reduction

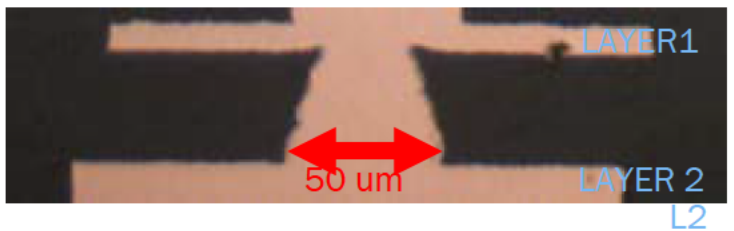
Standard



Via Cross-section

- Vias made with CO_2 LDD
- Aspect ratio of 0.8

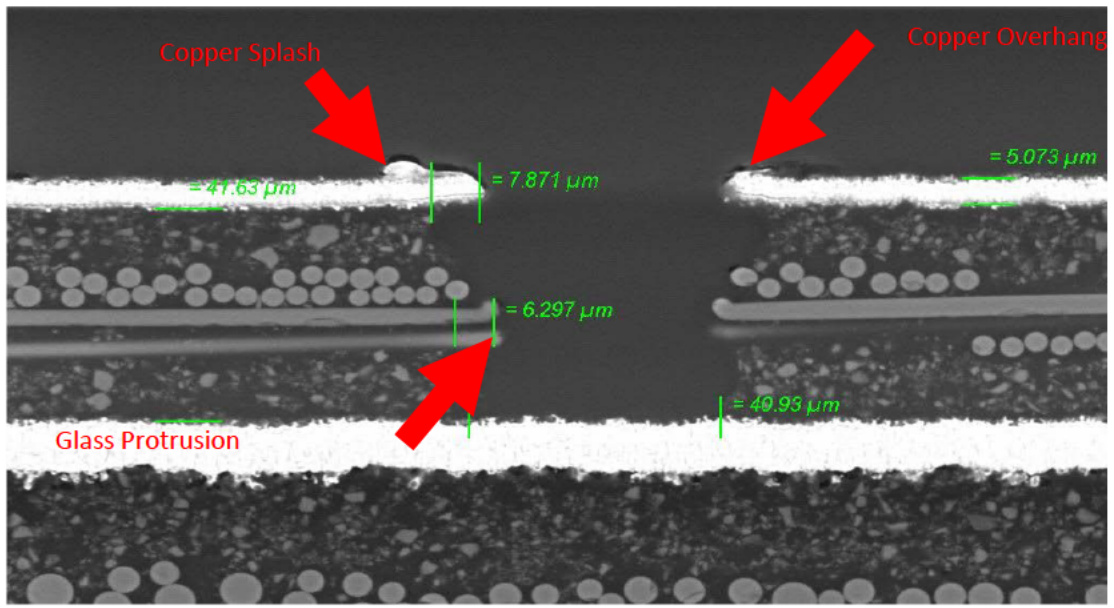
Our SLP



Via Cross-section

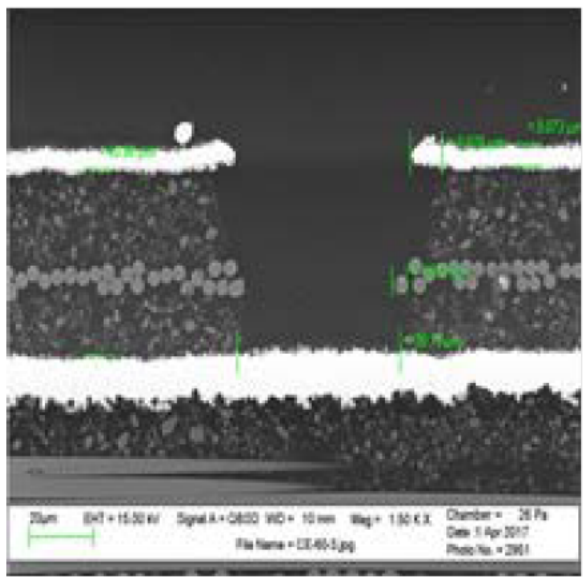
- Vias formed with UV-CO_2
- Smaller vias enable smaller pad sizes
- Aspect ratio of 0.8

Small Laser Via Formation Challenges

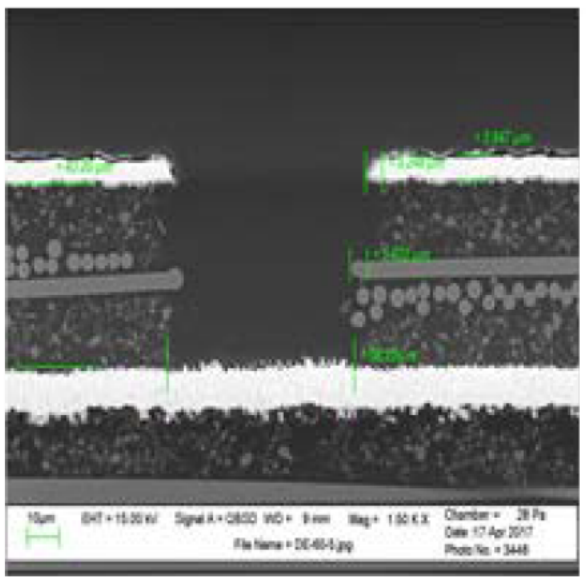


Optimizing laser via formation required to minimize voiding

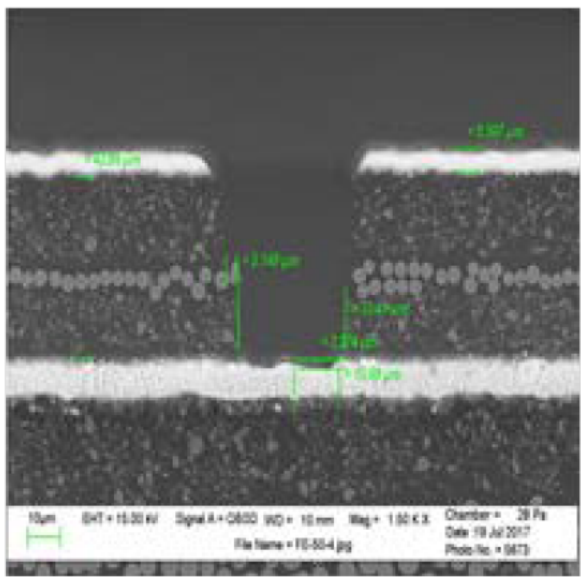
Via Drilling Technology Comparison



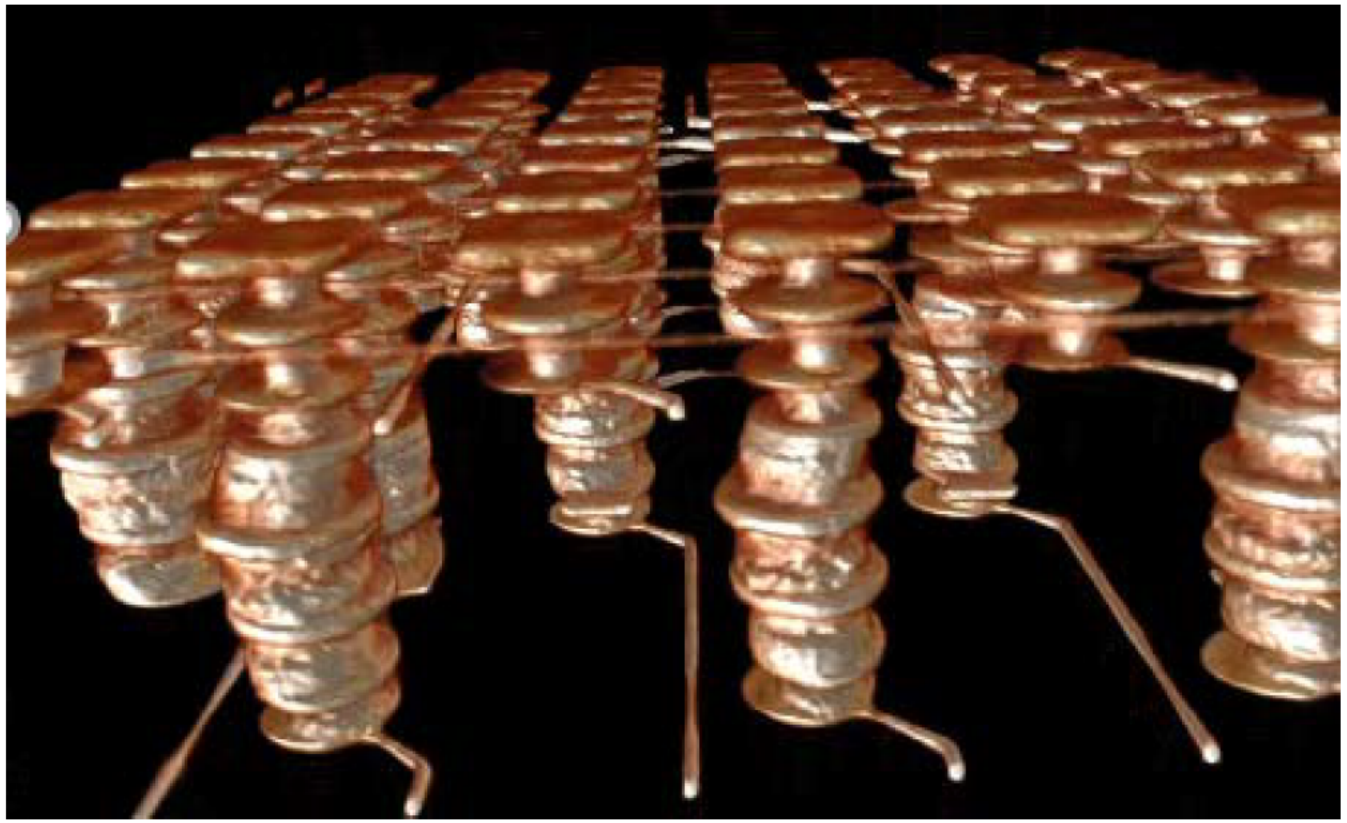
CO_2



UV + CO_2

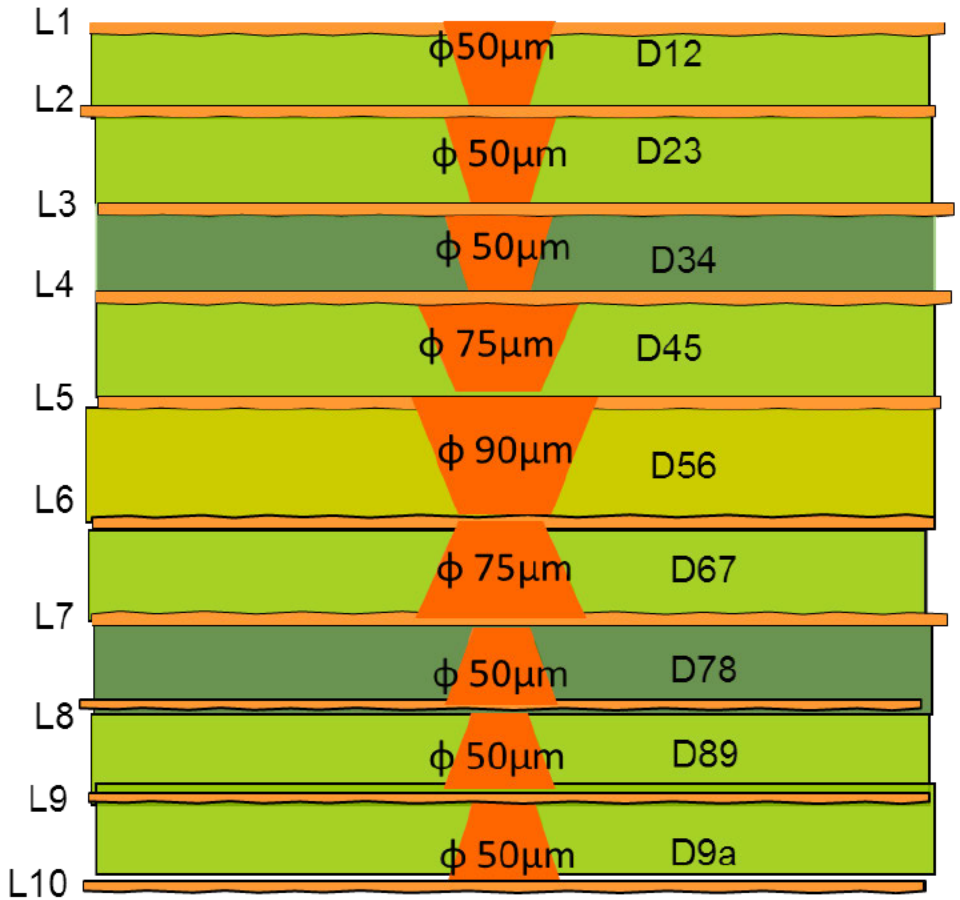


Picosecond Green



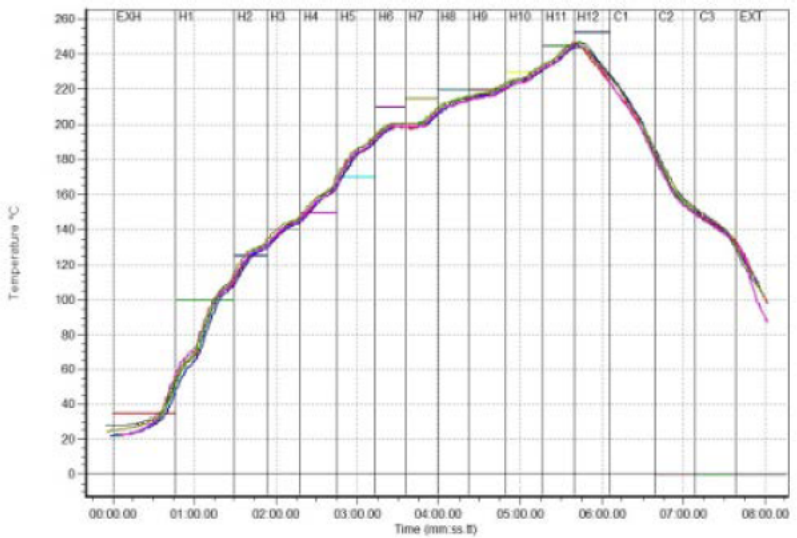
- 3D µCT scan

Test Vehicle Stack-up



- Layers with via diameters of 50 um are produced with substrate-like materials (T_g of ~270°C, Z-axis α_1 values of 10-15 ppm/°C).
- All other layers are made with conventional HDI materials (T_g of ~170°C, Z-axis α_1 values of 40 ppm/°C, α_2 values of 200 ppm/°C above T_g).

Reliability Test Conditions:



Reflow profile

- LLTS condition - 5X reflow cycles (preconditioning) + 1000 cycles (-55°C / 125 °C, 5 / 5 min dwell time, 15 sec transition)
- Resistance is checked every 100 cycles, and changes greater than 10% are considered a failure.
- 60 Coupons per test.
- Air-to-air condition - 5X reflow cycles (preconditioning) + 1000 cycles (-55°C / 125 °C, 10 / 10 min dwell time)

Reliability Results

Laminate	Pitch (µm)	Reflow	Air-to-Air Cycling	Liquid-to-Liquid Cycling
HDI / IC Substrate Material Hybrid	200, 250, 300	Passed 10 cycles	Passed 1000 cycles	Passed 1000 cycles

Conclusion

- We have reduced via, trace, and pad sizes to deliver a 200 µm-pitch BGA.
- Trace size reduced with an MSAP process
- Via size reduced with improved laser via formation, and materials with lower z-axis expansion.
- The finer pitch allows removal of BGA substrate to reduce the interconnect footprint in X, Y, and Z dimensions.
- The 200 µm-pitch interconnect solution passes 10X solder reflow and 1000 cycles of air-to-air and liquid-to-liquid thermal cycling.

Thank you!

Questions & Answers