SURVIVING 3K THERMAL CYCLES WITH VARIABLE VOID LEVELS (-40°C TO 125°C)

Rafael Padilla*, Derek Daily, TokuroYamaki, Tomoyasu Yoshikawa and Masato Shimamura
Senju Comtek Corporation
Santa Clara, CA, USA (*former-Senju)

Hayato Hiwatashi, Hiroaki Iseki and Tomohiro Yamagame
Senju Metal Industry Co., Ltd.
Tokyo, Japan
hhiwatashi@senju.com

ABSTRACT
Electronics manufacturers are searching for new lead-free solders that can improve upon SAC305 voiding performance and that exceed the current thermal cycle performance of this solder in harsh environments, all the while being processed at or near current typical SAC305 peak temperatures.

This paper compares -40ºC to 125ºC, thermal cycle test (TCT) results of boards built with SAC305 and a new SAC347+Bi/Sb/Ni/Co solder paste, which were assembled to intentionally contain three levels of voiding, ranging from 0% to 0.5%, 5% to 20% and higher than 20%, in order to not only observe variation in TCT performance but find any correlation between voiding levels of up to 30% and the corresponding thermal cycle reliability of the solder joint.

INTRODUCTION
The majority of the electronics industry has widely accepted the SAC305 (96.5Sn-3.0Ag-0.5Cu) alloy, not only due to processing temperature (i.e. 221ºC liquidus point), but also for SAC305's capability to provide similar or better thermal cycle test (TCT)reliability results than SnPb solders, within TCT temperature ranges of up to 85ºC. This is the defacto benchmark method used to determine the theoretical maximum temperature of products that are considered low to mid-level reliability (i.e. mobile phone products, appliance products, general consumer electronics, etc…).

However, there are various electronics environments where SnPb solders may continue to outperform SAC305, specifically in elevated operation temperature settings like those found in under-the- hood automotive applications. Such applications are usually thermal cycle tested up to 125ºC (or even up to 150ºC).

In view of the increasing requirements related to critical to function applications, such as those found in the automobile, medical or infrastructure industries, new lead-free solders are being developed in order to meet the higher temperature cycle environments.

This study compares harsh environment (i.e. -40ºC/125ºC) thermal cycle reliability test results for printed circuit boards that contain QFNs, DPAKs and chip components, assembled with three designated void levels (all below 35% by X-Ray area), using the standard lead-free Tin-Silver-Copper (SAC) solder paste alloy Sn-3.0%Ag-0.5%Cu (SAC305), and a SAC alloy (Sn-3.4%Ag-0.7%Cu+Bi/Sb which includes the presence of dopant elements i.e. Ni and Co), by three methods; electrically checking the QFN component I/Os for any changes in resistance (i.e. complete cracks) during thermal cycling, cross-sectional (CS) analysis after thermal cycling and shear strength comparisons after thermal cycling, in order to investigate any differences and/or correlations between these two alloys, their void levels and their corresponding thermal cycle performance.

Simply stated, the purpose of this study is to investigate the difference in alloy performance as well as any correlation between voiding and solder joint thermal cycle reliability for QFNs, DPAKs and Chip Resistors.

As works have reviewed the effect of voiding on the reliability of solder joints in area-array components while using higher reliability focused Pb-Free alloys [2]; including void review within BGAs (ball grid arrays) and their corresponding thermal cycle reliability [1]; this work will focus on QFN and chip resistor components reliability up to 3,000 cycles, with some exploration of DPAK under body joint integrity.

Key words: Pb-Free (Lead Free), SnPb (Tin Lead), TCT (Thermal Cycle Test), SAC347+Bi/Sb/Ni/Co (Sn3.4%Ag0.7%Cu3.2%Bi3.0%Sb+Ni/Co), SAC305 (96.5%Sn3.0%Ag0.5%Cu), QFN (Quad Flat No-Lead Package), DPAK (Discrete Package), I/O (Input Output), BGA (Ball Grid Array), and CS (Cross Section).

DOE (DESIGN OF EXPERIMENT)

For the DOE, two solder paste alloys were selected for testing, along with two different paste flux chemistries, in an effort to obtain a variation in voiding levels between each DOE group.

In total, four pastes were chosen for testing and six DOE legs were to be tested, as can be seen in Figure 1.

	REFLOW ENVIRONMENT	
	VACUUM REFLOW	AIR
SAC305 NO-CLEAN (ROL0)	<0 5% VOID LEVEL	5~20% VOID LEVEL
SAC305 NO-CLEAN (ROL1)	-	25~35% VOID LEVEL
SAC347+ NO-CLEAN (ROL0)	<0 5% VOID LEVEL	5~20% VOID LEVEL
SAC347+ NO-CLEAN (ROL1)	-	25~35% VOID LEVEL

Figure 1: Four pastes tested with a total of 6 DOE legs, 4 air reflow legs and 2 vacuum reflow legs, used in order to obtain 3 levels of voiding (below 0.5%, between 5-20%, and around 30% +/-5%)

One SAC305, Type 4 powder, Halogen Free (ROL0), No-Clean paste; a SAC305, Type 4 powder, halogenated (ROL1), No-Clean paste, a SAC347+Bi/Sb/Ni/Co, Type 4 powder, Halogen Free (ROL0), No-Clean paste and a SAC347+Bi/Sb/Ni/Co, Type 4 powder, Halogenated (ROL1), No-Clean paste were chosen for testing. For the DOE, two test vehicle boards were selected with two types of components per board.

The first Test Vehicle board (TV-1),an FR-4, 6 Cu layer, single sided, Cu-OSP, NSMD (non-solder mask defined), test vehicle board with dimensions of 105mm X 105mm X 1.5mm was used (Fig. 2).

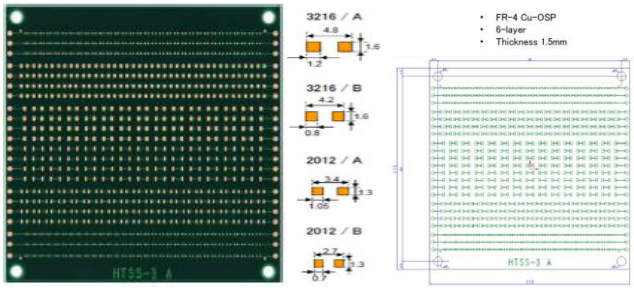


Figure 2 Top Side Picture of Test Vehicle 1 (bare board), which is 105mm X 105mm X 1.5mm thick, FR4, 6 Cu layer, NSMD (non-solder mask defined), circuit board.

TV-1 board layout contains 80, 2012-Chip Resistors and 56, 3216-Chip Resistors. 48 total boards were assembled (meaning 3,840 2012-Chip Resistors and 2,688 3216-Chip Resistors in total).
Two Cu OSP pad geometries and distances were used for each chip component, as can also be seen in Figure 2.

The 3216-Resistors (metric) are 3.2mm in length, 1.6mm in width, and 0.55mm in height. The pad geometries used for the 3216-Resistors (metric) were A:1.6mm X 1.2mm, with 4.8mm distance apart from both ends, and B:1.6mm X 0.8mm with 4.2mm distance apart from both ends. The 2012-Resistors (metric) are 2.0mm in length, 1.2mm in width, and 0.45mm in height. The pad geometries used for the 2012-Resistors (metric) were A:1.3mm X 1.05mm, with 3.4mm distance apart from both ends, and B:1.3mm X 0.7mm, with 2.7mm distance apart from both ends.

The second Test Vehicle board (TV-2), an FR-4,6Cu layer, single sided, Cu-OSP, NSMD (non-solder mask defined), test vehicle board with dimensions of 105mm X 105mm X 1.2mm was used (Fig 3).

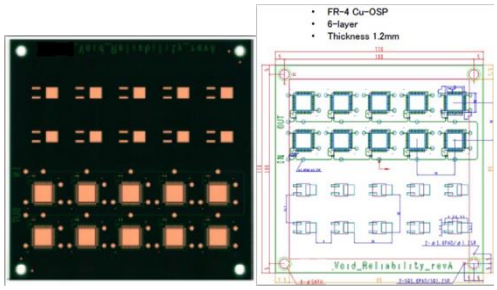


Figure 3 Top Side Picture of Test Vehicle 2 (bare board), which is 105mm X 105mm X 1.2mm thick, FR4, 6 Cu layer, NSMD (non-solder mask defined), circuit board, along with corresponding daisy-chain layout.

The TV-2 board layout contains 10 QFNs and 10 DPAKs, as illustrated in Figure 4.

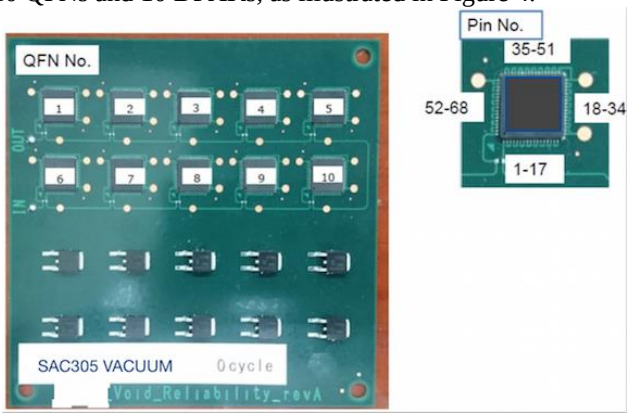


Figure 4 Example of QFN/DPAK circuit board daisy chain and pin numbers for the QFN inputs/outputs (I/Os).

68 total TV-2 boards where assembled (meaning 680 QFN and DPAK components in total).

It is also important to note, that the QFNs on the Test Vehicle-2 boards are powered by a daisy chain with ground pads and a chip resistor per QFN component, so significant cracks in the I/Os can be detected via electrical resistance changes, so even if the resistor cracks there is still a step/incremental difference between QFN components.

An example of how this is detected is illustrated below in Figure 5.

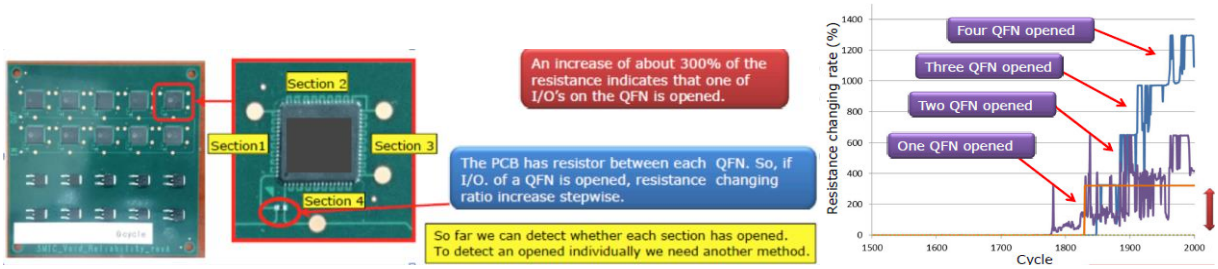


Figure 5 Example of QFN/DPAK circuit board daisy chain, used to detect cracks in the QFN I/Os via electrical resistance changes, with example of expected value changes and how they correlate to cracking in the I/Os.

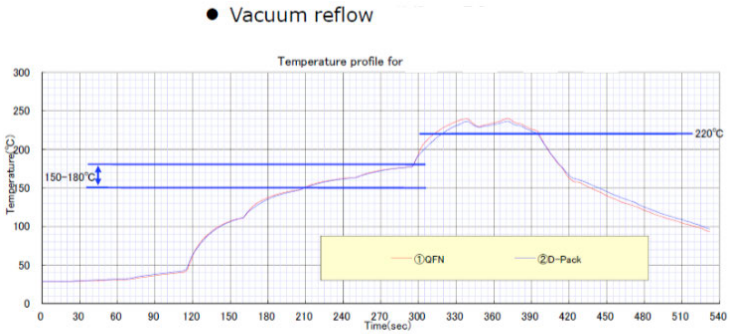
Two different bottom terminated components (QFN and DPAK) were assembled to TV-2; 10QFNs per board, which are 10mm X 10mm, and 10 Power Transistor Discrete Packages (DPAKs) per board all on the same board.

All 3 DOE legs per paste alloy were assembled with similar reflow profiles, meaning a peak temperature within +/- 5ºC of each other, the only major difference was either reflow environment or solder paste flux chemistry used (which was done to create 3 different levels of voiding while minimizing any difference in the process variables). The reflow profiles used can be seen in Figure 6-8, and cross sections confirming similar intermetallic compound growth at the interfaces of the solder joints before TCT can be seen in Figure 33.

		1Zone	2Zone	3Zone	4Zone	5Zone	6Zone	7Zone	8Zone	9Zone	10Zone
Setting [℃]	Upeer	100	135	165	170	175	180	185	235	265	250
	Lower	100	135	165	170	175	180	185	235	265	250

	①	②	
Soak Time(sec) (150 ～ 180)	80	78	
RF time(sec) (220 ℃以上)	42	41	⊿t
Peak Temp.	241.6	239.0	2.6

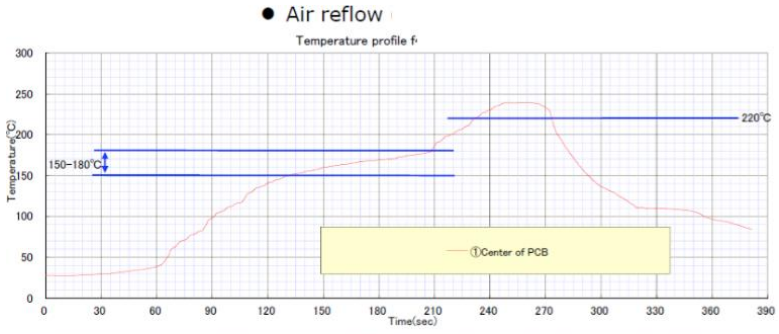
Figure 6 Air reflow thermal couple readout (i.e. reflow profile) that was attached to one solder joint of each component (QFN and DPAK) on the TV-2 circuit board.



		1Zone	2Zone	3Zone	4Zone	5Zone	6Zone
Setting [℃]	Upeer	120	155	170	180	260	-
	Lower	120	155	170	185	260	300

	①	②	
Soak Time (150 ～ 180)	88	88	
RF time(sec) (220 ℃以上)	84	76	⊿t
Peak Temp.	240.2	236.7	3.5

Figure 7 Vacuum reflow thermal couple readout (i.e. reflow profile) that was attached to one solder joint of each component (QFN and DPAK) on the TV-2 circuit board. The same profile was used for TV-1 vacuum reflow.



		1Zone	2Zone	3Zone	4Zone	5Zone	6Zone	7Zone	8Zone	9Zone	10Zone
Setting [℃]	Upeer	100	135	165	170	175	180	185	235	265	250
	Lower	100	135	165	170	175	180	185	235	265	250

	①		
Soak Time(sec) (150 ～ 180)	77		
RF time(sec) (220 ℃以上)	42	⊿t	
Peak Temp.	239.2	2.6	

Figure 8 Air reflow thermo-couple readout (i.e. reflow profile) that was attached to the center solder joint of one chip component on the TV-1 circuit board

As can be seen from the DSC graph in Figure 9, SAC305 and SAC347+Bi/Sb/Ni/Co alloys have similar liquidus temperatures.

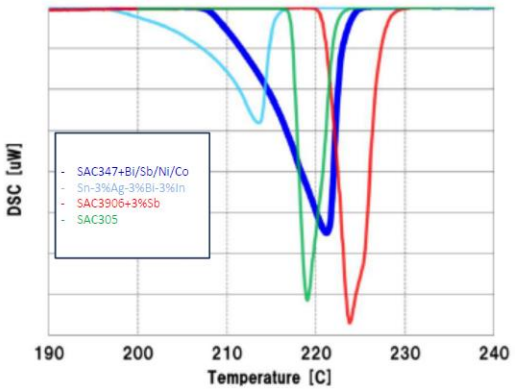


Figure 9 DSC chart of SAC305 and SAC347+Bi/Sb/Ni/Co alloys.

Each DOE leg was assembled using the same SMT (Surface Mount Technology) printer settings and pick-and-place equipment settings.

The production printer used in the DOE is a commonly found printer in various electronics factories, as well as the production pick and place equipment. The settings used can be seen in Figure 10.

【Printing condition】

Machine	
Speed	30mm/sec
Stencil Thickness	0.12mm
Squeegee	Metal/Angle 60deg
Pressure	0.20N/mm
Removal speed	5.0mm/s
Snap off	On contact

Figure 10 Production SMT (Surface Mount Technology) printer settings used during the DOE testing.

The assembly procedures are also considered standard. We printed a test board (to confirm alignment), performed a stencil under wipe cleaning, printed a fresh board, mounted the components, reflowed the boards, x-rayed the boards, then saved the void measurement data using the production X-Ray machine. The reflow ovens used during the test were both from the company. One oven was a standard convection reflow oven, the other was a vacuum reflow oven. Figure 11 provides an example of the ovens used.

Figure 11 Production convection air reflow oven (left) and production vacuum reflow oven (right) used for the DOE.

X-Ray images were acquired from each component using a production X-Ray machine and void ratio was determined by calculating the area of the void in comparison to the land (examples provided in Figure 12 - 15).

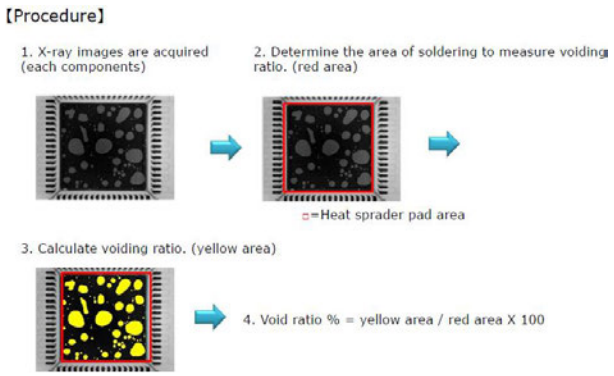


Figure 12 Examples of how the production X-Ray equipment calculated void area ratio under a QFN.

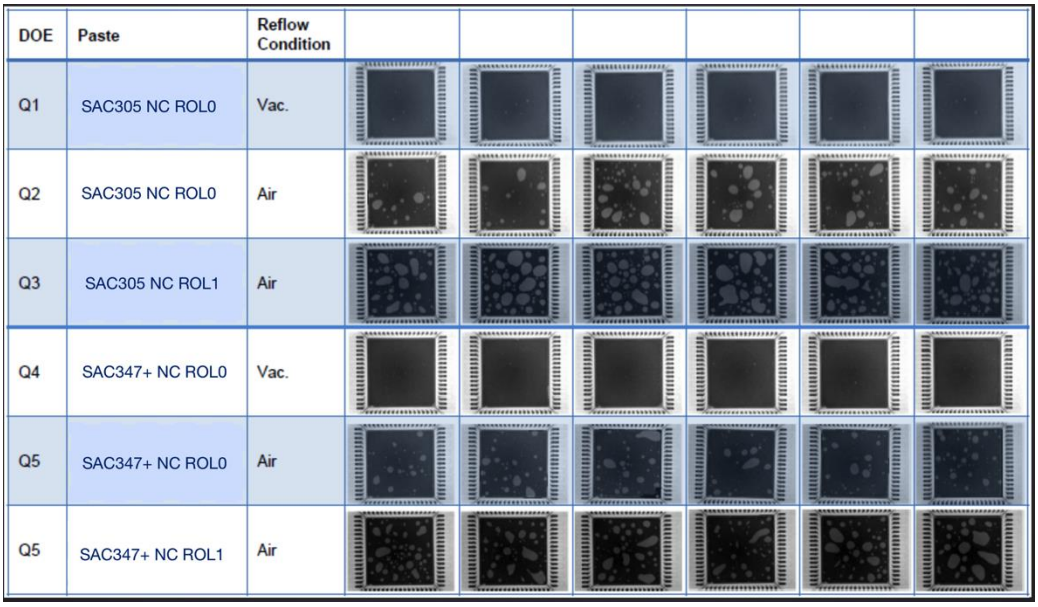


Figure 13 Examples of x-ray void images from the QFN components in varying reflow environments

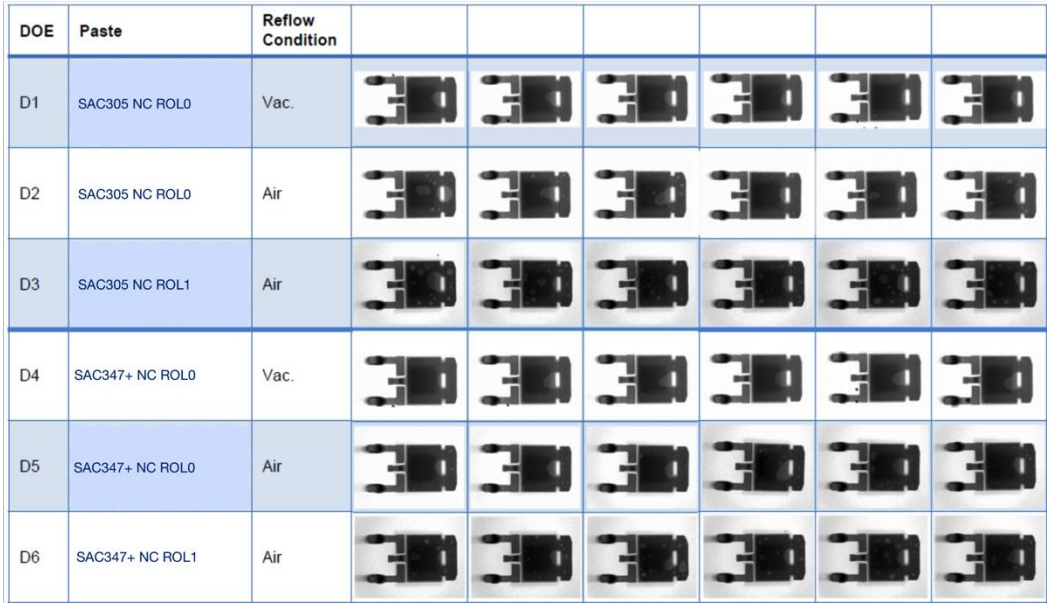


Figure 14 Examples of x-ray void images from the DPAK components in varying reflow environments.

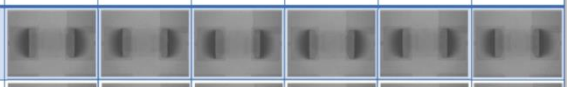
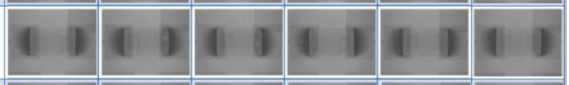
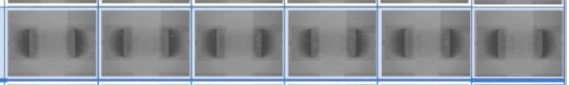
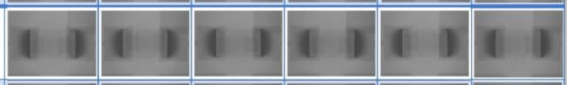
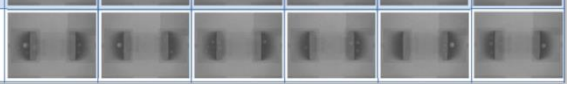
DOE	Paste	Reflow Condition						
C1-3	SAC305 NC ROL0	Vac.						
C2-3	SAC305 NC ROL0	Air						
C3-3	SAC305 NC ROL1	Air						
C4-3	SAC347 NC ROL0	Vac.						
C5-3	SAC347 NC ROL0	Air						
C6-3	SAC347+ NC ROL1	Air						

Figure 15 Examples of x-ray void images from the chip components in varying reflow environments

As seen in Figure 16, by using 2 reflow environments (convection air and vacuum reflow) we were able to obtain 10 boards each with 3 levels of voiding for the QFN and DPAK components.

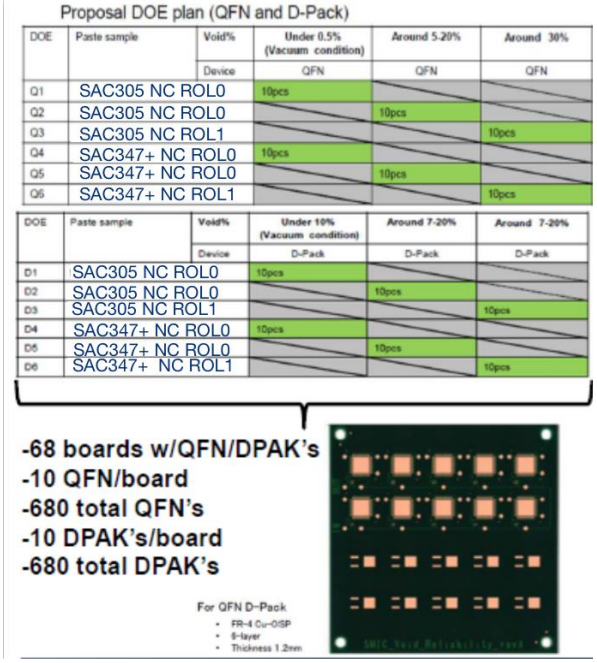


Figure 16 DOE test matrix for QFNs and DPAKs, showing 3 levels of voiding (<0.5%, between 5-20%, and around 30% +/-5%), for each paste leg.

Unfortunately, voiding under the chip components (TV-1) could not be varied enough to create 3 different levels of voiding, so the TV-1 DOE legs with chip components were used only to compare the difference in shear strength after thermal cycling between the two alloys tested.

Figure 17 shows the DOE test matrix for the chip components.

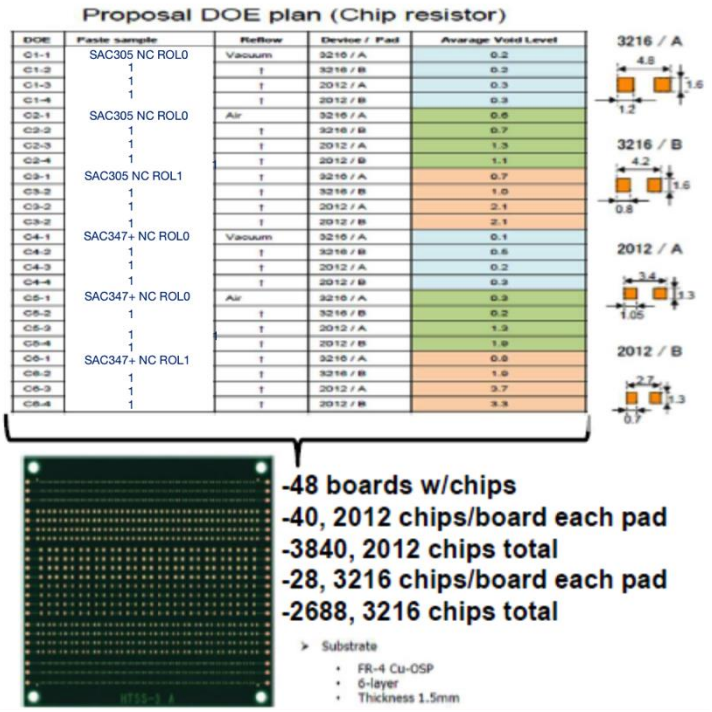


Figure 17 Chip component DOE test matrix, for alloy comparison testing, showing average level of voiding for all legs is below 3%, regardless of reflow environment or pad geometry tested

After the boards were assembled they were placed into a production thermal cycling chamber and thermal cycled between -40ºC and 125ºC with 30min dwell per cycle and 5-minute dwell at ambient.

Figure 18 provides an example of the thermal cycle chamber profile.

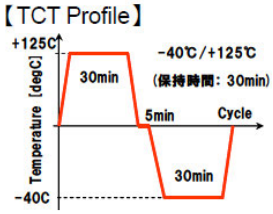
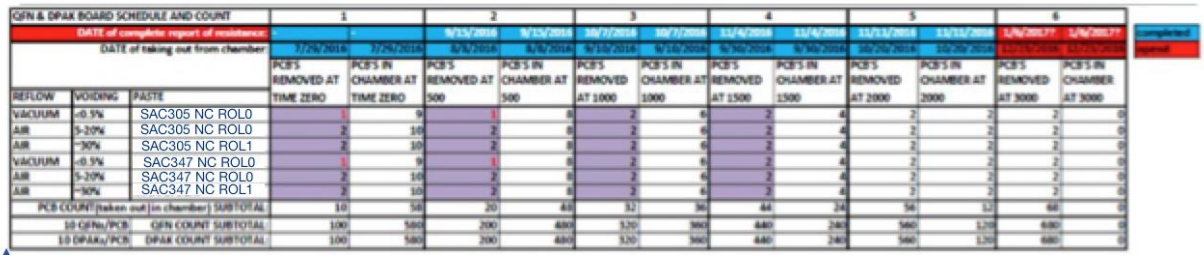
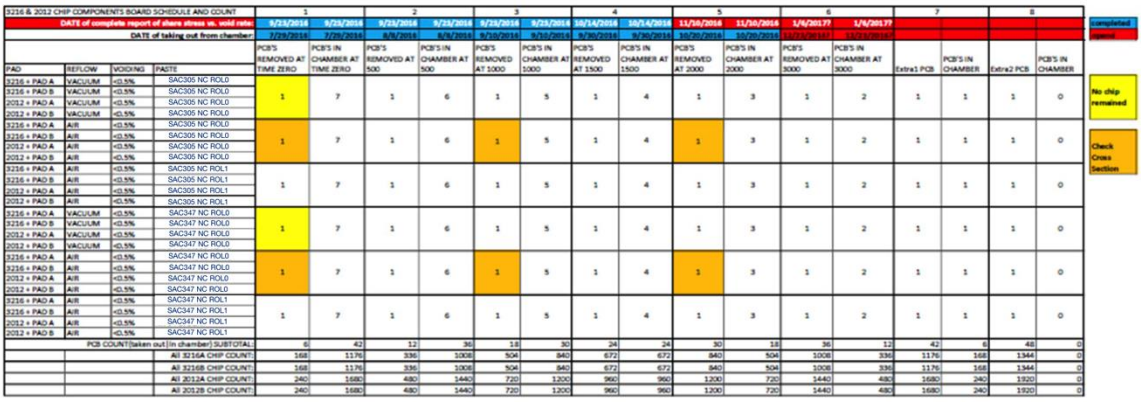


Figure 18 Thermal cycle profile of -40ºC to 125ºC with 30min dwell per cycle and 5min dwell at ambient, which was used during the testing.

Figure 19 depicts the schedule of when boards were pulled out of the chamber for testing (i.e. after 500, 1000, 1500, 2000 and 3000 cycles) as well as how many boards remained in the chamber until completion.





3216 & 2012 CHIP COMPONENTS BOARD SCHEDULE AND COUNT				1		2		3		4		5		6		7		8		
DATE of complete report of shore stress vs. void rate:				9/23/2014	9/24/2014	9/23/2014	9/23/2014	9/23/2014	9/23/2014	10/14/2014	10/14/2014	11/30/2014	11/30/2014	1/6/20177	1/6/20177					completed
DATE of taking out from chamber:				7/24/2215	7/25/2015	8/9/2015	8/9/2015	8/19/2215	8/19/2015	9/30/2215	9/30/2015	10/20/2015	10/20/2015	12/23/20141	12/23/20141					missed
PAD	REFLOW	VOIDING	PASTE	PCB'S REMOVED AT TIME ZERO	PCB'S IN CHAMBER AT TIME ZERO	PCB'S REMOVED AT 500	PCB'S IN CHAMBER AT 500	PCB'S REMOVED AT 1000	PCB'S IN CHAMBER AT 1000	PCB'S REMOVED AT 1500	PCB'S IN CHAMBER AT 1500	PCB'S REMOVED AT 2000	PCB'S IN CHAMBER AT 2000	PCB'S REMOVED AT 3000	PCB'S IN CHAMBER AT 3000	Extra1 PCB	PCB'S IN CHAMBER	Extra2 PCB	PCB'S IN CHAMBER	
3216 + PAD A	VACUUM	<0.5%	SAC305 NC ROL0	1	7	1	6	1	5	1	4	1	3	1	2	1	1	1	0	No chip remained
3216 + PAD B	VACUUM	<0.5%	SAC305 NC ROL0																	
2012 + PAD A	VACUUM	<0.5%	SAC305 NC ROL0																	
2012 + PAD B	VACUUM	<0.5%	SAC305 NC ROL0																	
3216 + PAD A	AIR	<0.5%	SAC305 NC ROL0	1	7	1	6	1	5	1	4	1	3	1	2	1	1	1	0	Check Cross Section
3216 + PAD B	AIR	<0.5%	SAC305 NC ROL0																	
2012 + PAD A	AIR	<0.5%	SAC305 NC ROL0																	
2012 + PAD B	AIR	<0.5%	SAC305 NC ROL0																	
3216 + PAD A	AIR	<0.5%	SAC305 NC ROL1	1	7	1	6	1	5	1	4	1	3	1	2	1	1	1	0	
3216 + PAD B	AIR	<0.5%	SAC305 NC ROL1																	
2012 + PAD A	AIR	<0.5%	SAC305 NC ROL1																	
2012 + PAD B	AIR	<0.5%	SAC305 NC ROL1																	
3216 + PAD A	VACUUM	<0.5%	SAC347 NC ROL0	1	7	1	6	1	5	1	4	1	3	1	2	1	1	1	0	
3216 + PAD B	VACUUM	<0.5%	SAC347 NC ROL0																	
2012 + PAD A	VACUUM	<0.5%	SAC347 NC ROL0																	
2012 + PAD B	VACUUM	<0.5%	SAC347 NC ROL0																	
3216 + PAD A	AIR	<0.5%	SAC347 NC ROL0	1	7	1	6	1	5	1	4	1	3	1	2	1	1	1	0	
3216 + PAD B	AIR	<0.5%	SAC347 NC ROL0																	
2012 + PAD A	AIR	<0.5%	SAC347 NC ROL0																	
2012 + PAD B	AIR	<0.5%	SAC347 NC ROL0																	
3216 + PAD A	AIR	<0.5%	SAC347 NC ROL1	1	7	1	6	1	5	1	4	1	3	1	2	1	1	1	0	
3216 + PAD B	AIR	<0.5%	SAC347 NC ROL1																	
2012 + PAD A	AIR	<0.5%	SAC347 NC ROL1																	
2012 + PAD B	AIR	<0.5%	SAC347 NC ROL1																	
PCB COUNT(taken out/in chamber) SUBTOTAL:				6	42	12	36	18	30	24	24	30	18	36	12	42	6	48	0	
All 3216A CHIP COUNT:				168	1176	336	1008	504	840	672	672	840	504	1008	336	1176	168	1344	0	
All 3216B CHIP COUNT:				168	1176	336	1008	504	840	672	672	840	504	1008	336	1176	168	1344	0	
All 2012A CHIP COUNT:				240	1680	480	1440	720	1200	960	960	1200	720	1440	480	1680	240	1920	0	
All 2012B CHIP COUNT:				240	1680	480	1440	720	1200	960	960	1200	720	1440	480	1680	240	1920	0	

Figure 19 TCT schedule showing when the boards where removed from the chamber and how many remain throughout the testing. The thermal cycle test duration was around 5 months.

CHIP COMPONENT DOE RESULTS (3000 CYCLES)

One board after every 500, 1000, 1500, 2000 and 3000 cycles was removed from the chamber for solder joint shear strength testing. The shear speed setting used for the test was 6.0mm/min. The results for each thermal cycle evaluated can be seen in Figures 20 and 21.

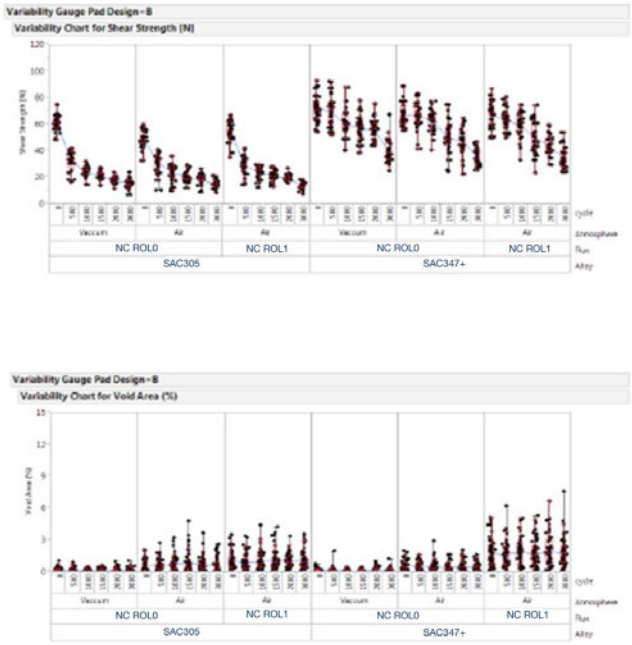


Figure 20: 3216-Chip Resistor "B" (metric) results for initial shear strength, and shear strength after 500, 1000, 1500, 2000 and 3000 thermal cycles, as well as the level of voiding for each chip tested (all below 10% voiding).

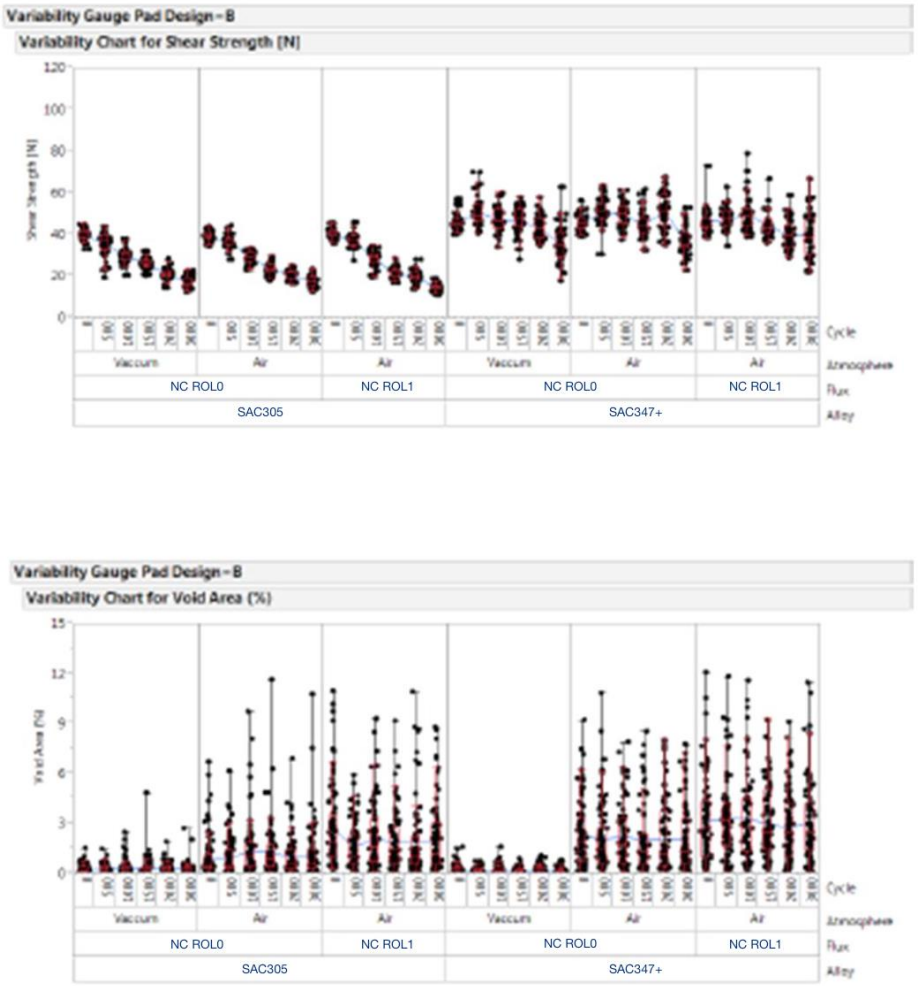


Figure 21: 2012-Chip Resistor (metric) results for initial shear strength, and shear strength after 500, 1000, 1500, 2000 and 3000 thermal cycles, as well as the level of voiding for each chip tested (all below 12% voiding).

The results indicate a significant increase in initial and final shear strength before and after thermal cycling is observed for the SAC347+Bi/Sb/Ni/Co paste alloy when compared to the base SAC305 alloy results.

For example, after completion of the entire 3,000 cycles, the 3216-Resistors (metric) with the pad A geometries, assembled with SAC347+Bi/Sb/Ni/Co paste, had at minimum over 30 Newton of shear strength remaining with an average of 45 Newton of shear strength. Whereas the boards assembled with SAC305 paste fell below 30 Newton of shear strength only after 500 cycles, and carried an average shear strength of between 10-20 Newton after 3000 cycles.

As seen in Figure 22, through cross sectional analysis, it was confirmed that after 3000 cycles the chip resistors crack length and crack rate was shortened by using SAC347+Bi/Sb/Ni/Co paste, compared to SAC305.

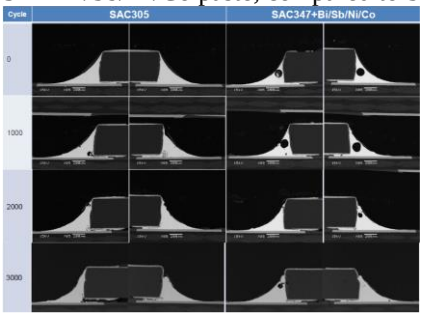


Figure 22: 3216-Chip Resistor cross sectional analysis for initial and 500, 1000, 1500, 2000 and 3000 thermal cycles.

QFN DOE RESULTS (3000 CYCLES)

After 1500 cycles of testing, although we can see some noise in the resistance values (which was later confirmed to be related to where the cable harness was resting in the chamber), there were no large deviations in the electrical resistance detected from any of the boards QFN I/Os in the chamber, regardless of the alloy or void level in the component (they all follow the same electrical performance trends) so we randomly selected boards to remove for CS analysis.

This means, theoretically, up to 1500 thermal cycles, for all of the DOE legs, there are no large cracks occurring in the QFN solder joint I/Os which would cause a significant change in the electrical resistance (i.e. above 300%). However prior to 2000 cycles, we begin to detect large spikes in the electrical resistance with all the SAC305 boards. Figure 23, for example, clearly shows the results for six SAC305 boards pulled from the chamber after 2000 cycles. Resistance spikes are first detected in the SAC305, No-Clean (ROL0) boards with medium level voiding (5-20%) at 1770 thermal cycles.

Shortly thereafter a spike was detected in the SAC305 boards with 25-35% voiding at 1830 thermal cycles, and then almost immediately after that the SAC305 vacuum reflowed boards begin spiking at 1848 thermal cycles.

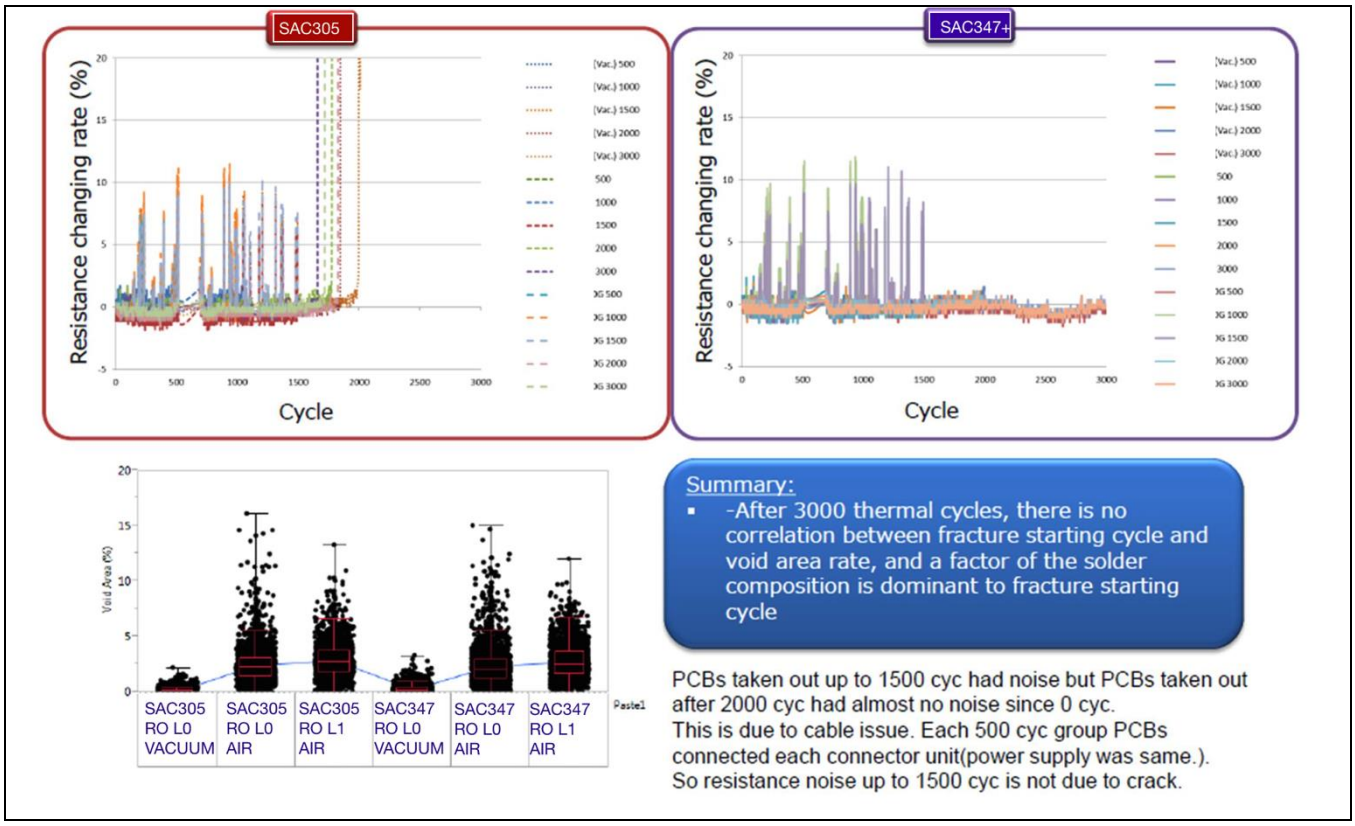


Figure 23 Electrical resistance results for the 6 SAC305 boards, and 6 SAC347+Bi/Sb/Ni/Co boards pulled from the chamber after 2000 thermal cycles.

As illustrated in Figure 24, CS analysis of I/Os 1-17 of the QFNs confirmed fully cracked joints (i.e. over 50% of the solder joint axis) does not occur with the SAC305 boards in any of the QFN I/Os until around or slightly after 1500 cycles are reached.

However, we do see the beginning of cracks appearing after 500 cycles with all the SAC305 convection air reflowed boards, but not until 1000 cycles with SAC305 vacuum reflowed boards, nonetheless fully open joints (>50%) of the QFN I/Os, regardless of reflow environment or initial void level, are all occurring around the same time (in between 1500-2000 thermal cycles).

Figure 24 Example of QFN I/O row 1-17, CS analysis results of the SAC305, No-Clean (ROL0) convection air reflowed boards.

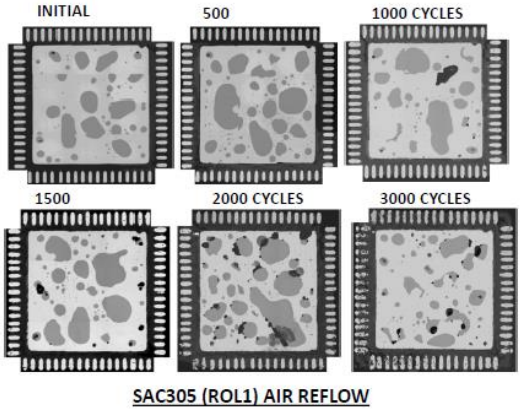


Figure 25 Selected QFN input-output and center pad, top-side view, CS analysis results of the SAC305, No-Clean (ROL1) convection air reflowed boards.

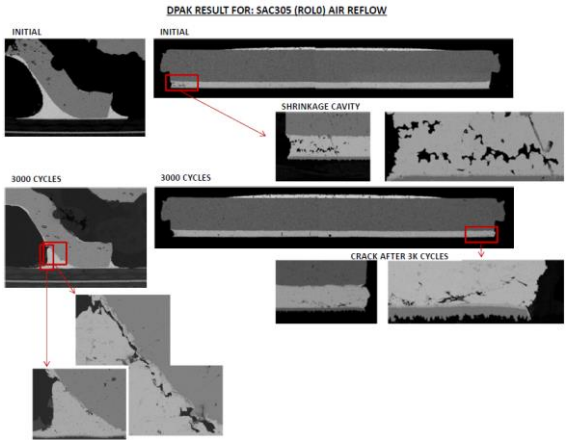


Figure 26 DPAK, side-view CS analysis of the SAC305, No-Clean (ROL0) convection air reflowed boards.

When reviewing the event detection results for the QFN I/Os after 2000 thermal cycles, as illustrated in Figure 27, in combination with the CS analysis results for all the boards removed from the chamber (Figures 24 – 26), we can see *no direct correlation between void percentage levels and thermal cycle reliability.*

Solder Paste	Atmosphere	QFN No.	QFN Lead No.			
			1-17	18-34	35-51	52-68
SAC305 ROLO	Vacuum	1	-	Open	Open	Open
		2	-	Open	Open	Open
		3	Open	Open	-	-
		4	-	-	-	-
		5	-	-	Open	-
		6	-	Open	Open	Open
		7	-	-	Open	-
		8	-	Open		-
		9	-	Open	Open	-
		10	-	Open	Open	-
SAC305 ROLO	Air	1	-	-	Open	-
		2	-	-	-	-
		3	-	Open	Open	-
		4	-	Open	Open	-
		5	-	Open	Open	Open
		6	-	Open	Open	-
		7	-	Open	Open	Open
		8	-	Open	-	-
		9	Open	Open	-	-
		10	Open	Open	Open	-
SAC305 ROL1	Air	1	-	-	Open	Open
		2	-	Open	Open	-
		3	-	Open	Open	-
		4	Open	Open	Open	-
		5	Open	Open	Open	-
		6	Open	Open	Open	-
		7	Open	Open	Open	-
		8	Open	Open	Open	Open
		9	Open	Open	Open	-
		10	-	Open	Open	-

18 OPENS

17 OPENS

27 OPENS

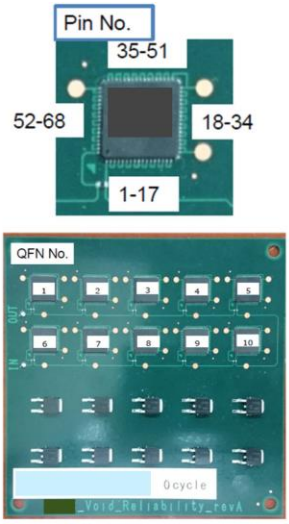


Figure 27 After 2000 cycles, electrical resistance spikes were detected in all SAC305 boards, with the SAC305 vacuum reflowed boards having the most events of 7, compared to the SAC305 boards which were reflowed in air, and had below 2 events.

As the testing progressed, the chamber detected resistance changes in all the boards built with SAC305 paste prior to reaching 2000 cycles, but no boards built with SAC347+Bi/Sb/Ni/Co paste detected a change in resistance. As no SAC347+Bi/Sb/Ni/Co boards exhibited spikes in electrical resistance, boards were randomly selected for CS analysis at each thermal cycle interval (i.e. initial, 500, 1000, 1500, 2000, 3000 thermal cycles).

As illustrated in Figures 28 through 31, CS analysis confirmed no significant cracking beyond 50% as having occurred up to 3000 cycles for the SAC347+Bi/Sb/Ni/Co.

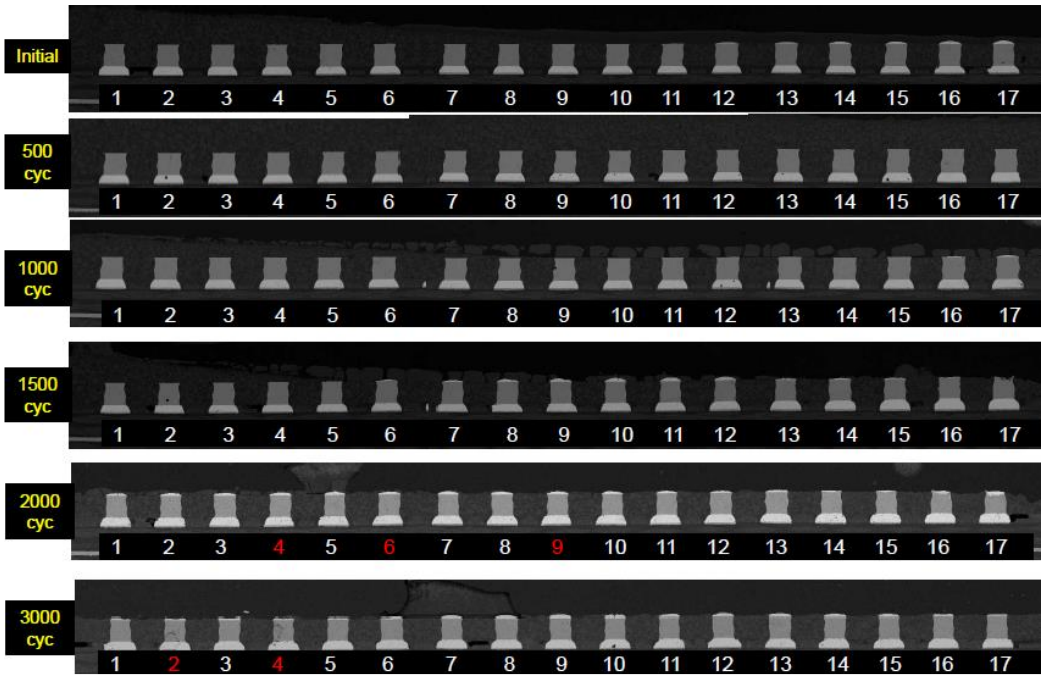


Figure 28 QFN input-output, CS analysis results of the SAC347+Bi/Sb/Ni/Co, No-Clean (ROL0) vacuum reflowed boards.

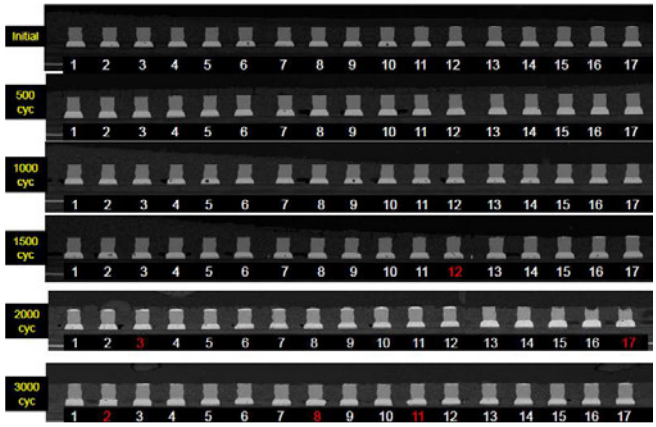


Figure 29 SAC347+Bi/Sb/Ni/Co, No-Clean (ROL0) convection air reflowed boards.

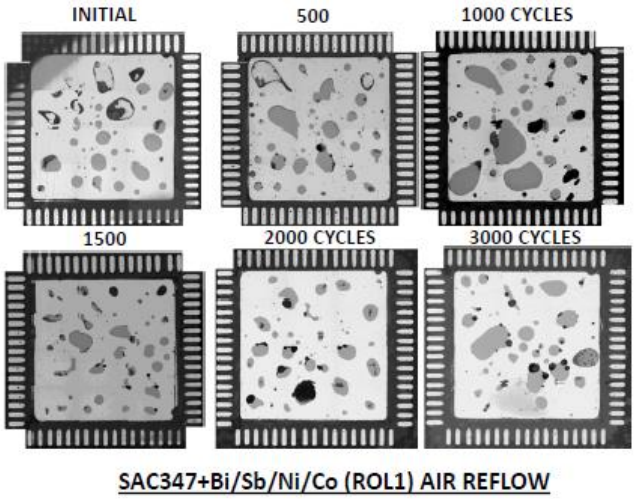


Figure 30 Selected QFN input-output and center pad, top-side view, CS analysis results of the SAC347+Bi/Sb/Ni/Co No-Clean (ROL1) convection air reflowed boards.

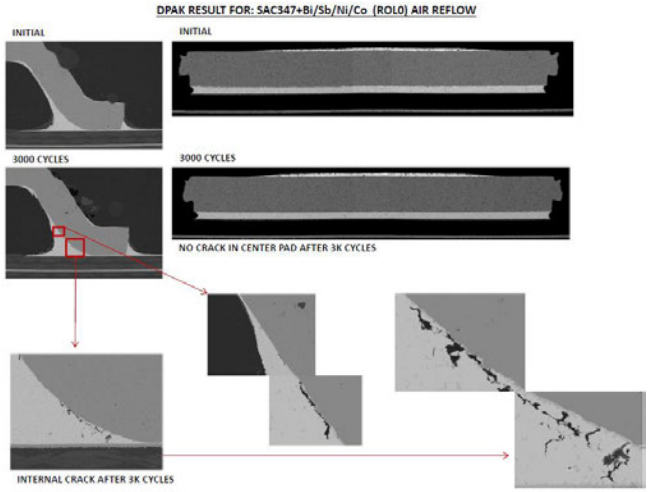


Figure 31 DPAK, side-view CS analysis of the SAC347+Bi/Sb/Ni/Co, No-Clean (ROL0) convection air reflowed boards.

Combining the event detection results with the CS analysis results of the QFN I/O rows 1-17, as we can see in Figure 32, there appears to be no meaningful correlation between voiding and thermal cycle reliability.

CS ANALYSIS AND EVENT DETECTION COMBINED

	SAC305						SAC347+Bi/Sb/Ni/Co					
	CS ANALYSIS (I/O'S 1-17 OF QFN)			EVENT DETECTION (ROWS)			CS ANALYSIS (I/O'S 1-17 OF QFN)			EVENT DETECTION (ROWS)		
TEMP CYCLE	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)
INITIAL	0/17	0/17	0/17	0	0	0	0/17	0/17	0/17	0	0	0
500	0/17	1/17	7/17	0	0	0	0/17	0/17	0/17	0	0	0
1000	04/17	3/17	10/17	0	0	0	0/17	0/17	4/17	0	0	0
1500	06/17 [1]	4/17 [2]	5/17 [1]	0	0	0	0/17	1/17	1/17	0	0	0
2000	08/17 [0]	13/17 [2]	11/17 [4]	7	2	1	3/17	2/17	3/17	0	0	0
3000	15/17 [5]	16/17 [5]	16/17 [5]	-	-	-	2/17 [0]	3/17 [0]	5/17 [0]	0	0	0

TCT: -40 ~ 125 Degree Celsius, 30min dwell

Figure 32 Chart showing the combined results from the CS analysis of the QFN I/O rows 1-17 and the event detection results for every board in the chamber. Yellow indicates the initiation of a crack, while orange signifies a crack over 25%, and red means a complete crack.

When reviewing the DOE results, it is difficult to make any true correlation with regards to voiding and thermal cycle reliability. Differences within each assembly were statistically insignificant and CS analysis of the intermetallic compounds (IMC) formed between the SAC305 alloy and SAC347+Bi/Sb/Ni/Co, which can be seen in Figure 33, show that the initial IMC layer began at similar thicknesses for both alloys.

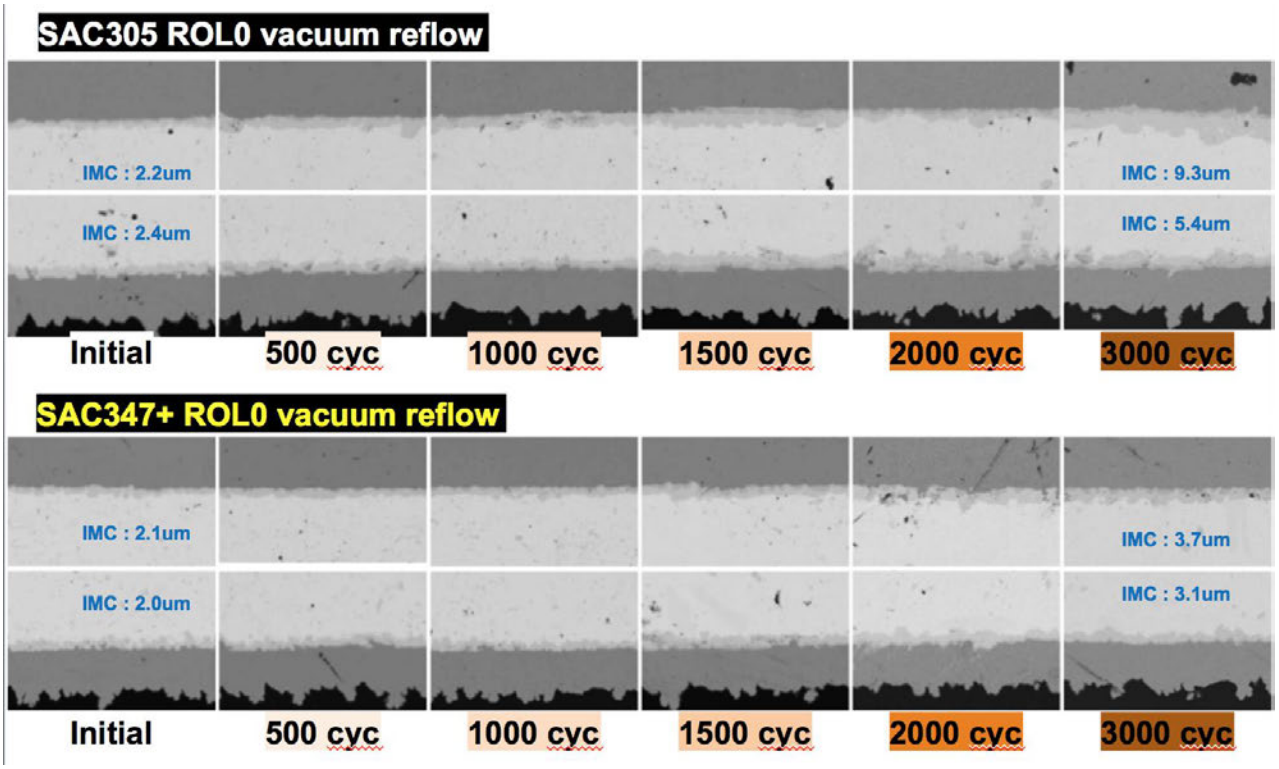


Figure 33 Comparison between initial, 500, 1000, 1500, 2000 and 3000 thermal cycles CS analysis images showing IMC thickness of the QFN I/Os from row 1-17.

However, after 3000 thermal cycles it is clear that the IMC thicknesses of the SAC305 solder joints are growing at a faster rate than those of SAC347+Bi/Sb/Ni/Co alloy. As seen in Figure 34, when one compares the IMC structures after 3000 cycles of the SAC305 and SAC347+Bi/Sb/Ni/Co alloy, the SAC305 alloy not only has a larger IMC thickness, but a greater amount of Cu3Sn intermetallic formed in comparison to the solder joint with SAC347+Bi/Sb/Ni/Co paste, making the SAC305 solder joint more susceptible to cracking.

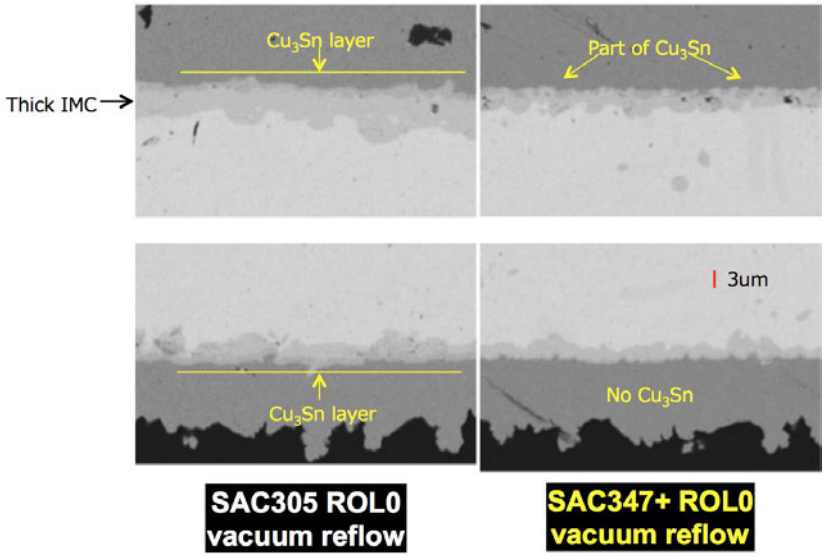


Figure 34 Comparison of IMC structure between SAC305 and SAC347+Bi/Sb/Ni/Co after 3,000 thermal cycles from -40ºC to 125ºC.

CONCLUSIONS

In conclusion, this study found no significant resistance changes detected up to 3,000 thermal cycles with SAC347+Bi/Sb/Ni/Co for the QFN portion of this study. Furthermore, cross section analysis confirmed no or minimal cracking (under 25%) after 3000 thermal cycles for both chip resistors and DPAK when processed with the SAC347+ alloy. This finding was also consistent with the lack of electrical resistance changes detected during the test.

A significant increase in initial and final shear strength before, during and after thermal cycling is observed for both chip resistors on both pad designs, when using SAC347+Bi/Sb/Ni/Co compared to SAC305.

Changes in electrical resistance were detected before 2,000 thermal cycles with SAC305 and cross section images for the QFN and chip components confirmed that large cracks were consistent with the observed electrical resistance changes during TCT in SAC305 for QFNs.

Lastly, and most importantly, this study found no direct correlation between voiding (below 35% for visual DPAK reviewed and below 25% in the QFN and chip components) and thermal cycle solder joint mechanical or electrical reliability. However one point is obvious, the SAC347+Bi/Sb/Ni/Co outperforms SAC305 in thermal cycling from -40ºC to 125ºC and is a good candidate for Lead-free products being used in harsh environments.

ACKNOWLEDGEMENTS

The authors would like to thank each of the package suppliers, contract manufacturers, and equipment manufacturers who were involved in supporting this study. They would also like to acknowledge the support of Continental Automotive Systems Inc. in particular Mark Fulcher, and Dr. Stan Rak.

REFERENCES

[1]David Hillman, Dave Adams, Tim Pearson, Brad Williams, Brittany Petrick, and Ross Wilcoxon, Rockwell Collins, “The Last Will and Testament of the BGA Void”. SMTA International 2011, September 21, 2011.
[2] Richard Coyle, Richard Parker, Dave Hillman, Joe Smetana et al., “A Collaborative Industrial Consortia Program for Characterizing Thermal Fatigue Reliability of Third Generation Pb-Free Alloys”. SMTA International 2016, September 25, 2016.

APEX EXPO IPC 2018
SUCCEED AT THE VELOCITY OF TECHNOLOGY

SURVIVING 3K THERMAL CYCLES WITH VARIABLE VOID LEVELS (-40°C TO 125°C)

Rafael Padilla*, Derek Daily, Tokuro Yamaki, Tomoyasu Yoshikawa and Masato Shimamura
Senju Comtek Corporation Santa Clara, CA, USA (*formerly- Senju)
Hayato Hiwatashi, Hiroaki Iseki and Tomohiro Yamagame
Senju Metal Industry Co., Ltd. Tokyo, Japan

Outline

- Background
- Design of Experiment (DoE)
- Void Measurement / Issue
- Chip Component Results
- QFN Component Results
- DPAK Observations
- Cross Section and SEM (IMC) Observation
- Conclusions

As the drive to improve solder joint reliability and widen the process window continues…

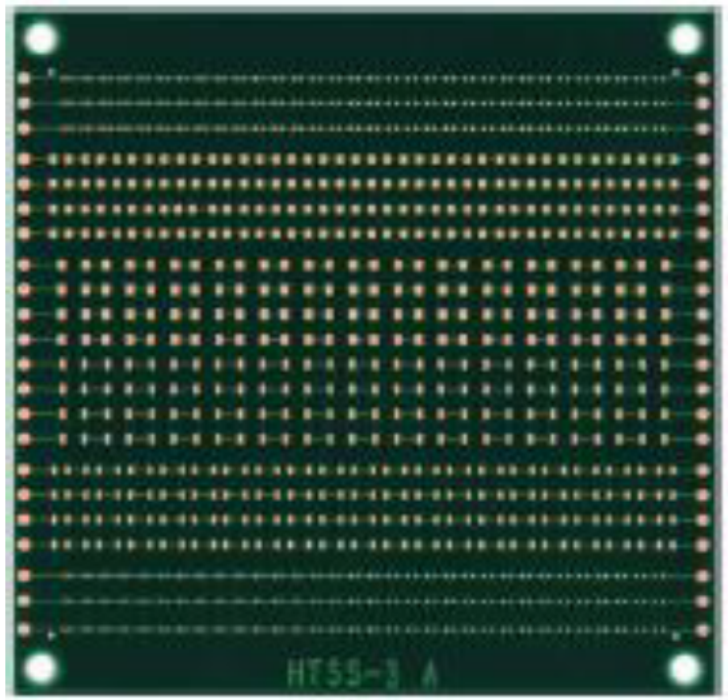
An investigation into the potential correlation between void percentage levels and solder joint reliability for both the Base SAC305 Alloy and an Improved SAC347+ Alloy, having greater Resistance to Thermal Cycle Failure, is summarized.

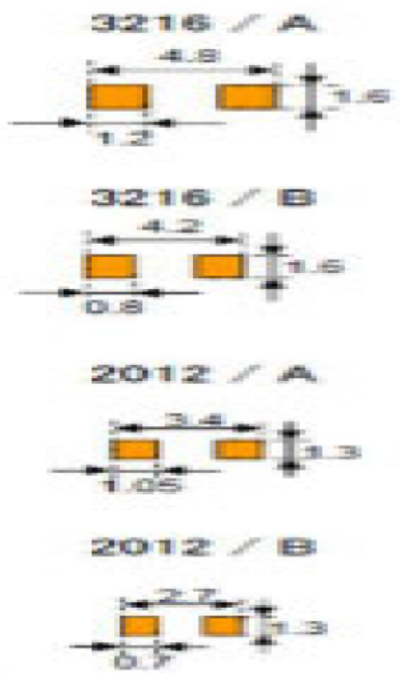
Design of Experiment Concept

- A Design of Experiment (DoE) was proposed to selectively generate various percentages of void levels under chip components, QFNs and DPAK type components and to monitor relative solder joint reliability.
- Parts were to be measured for void area (%)
- Parts were to be monitored for electrical resistance under thermal cycle stress.
- Post TCT observation to review crack growth.
- Post TCT mechanical shear strength testing was to be performed.

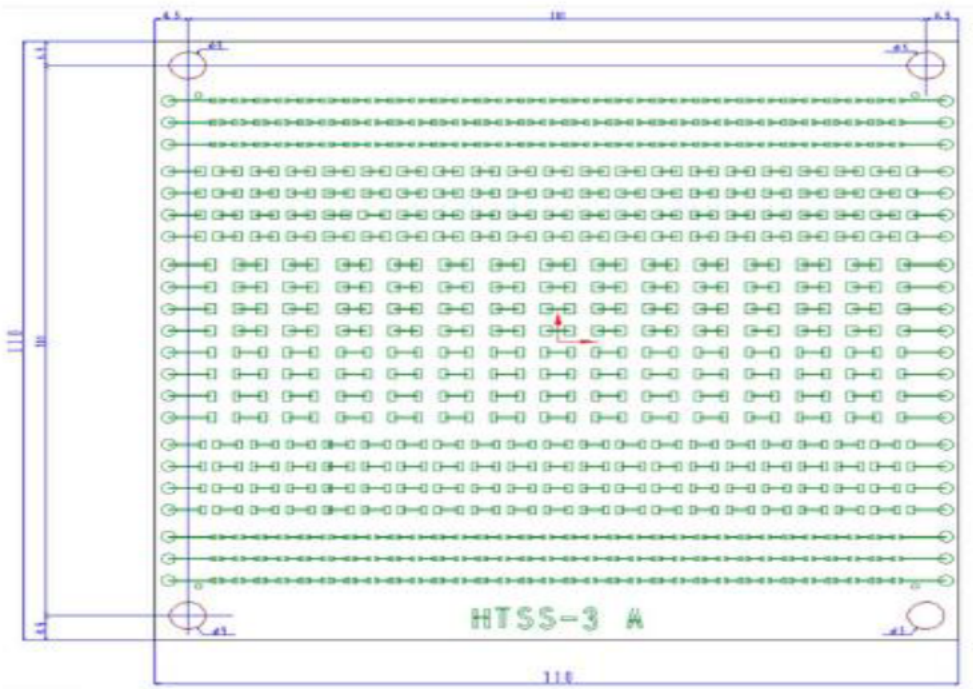
Test Vehicle #1 (Chip Components)

- **Bare board: 105mm X 105mm X 1.5mm thick, FR4, 6Cu layer, NSMD (non-solder mask defined), circuit board**
- 80, 2012-Chip Resistors and 56, 3216-Chip Resistors each PCB
- 48 PCB were assembled



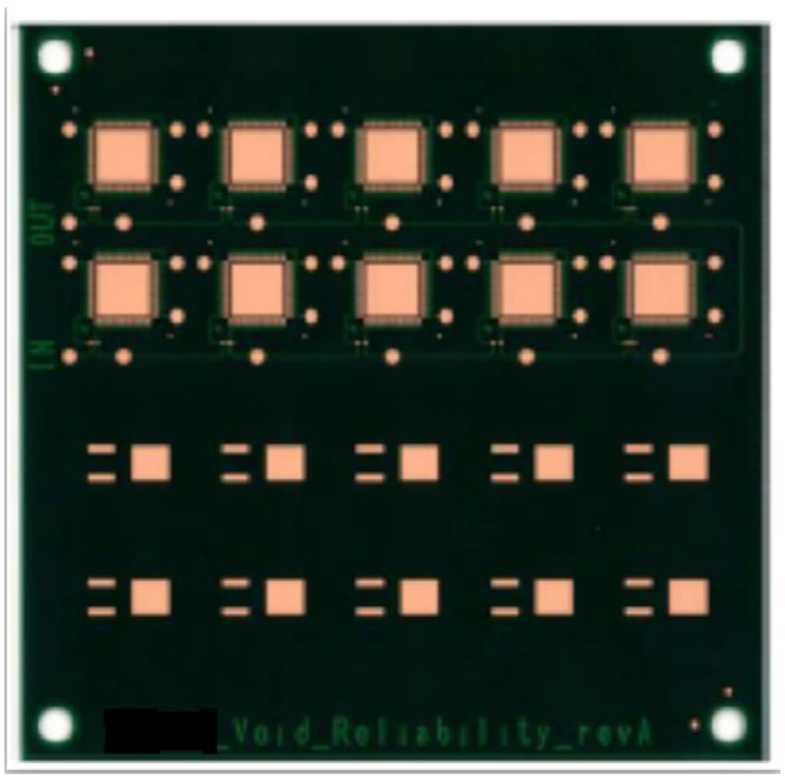


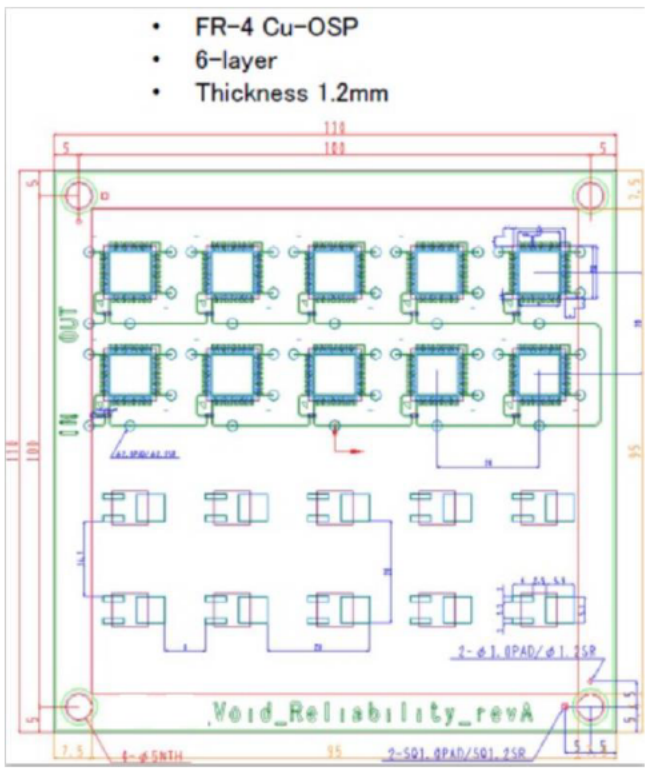
- FR-4 Cu-OSP
- 6-layer
- Thickness 1.5mm



Test Vehicle #2 (QFN/DPAK)

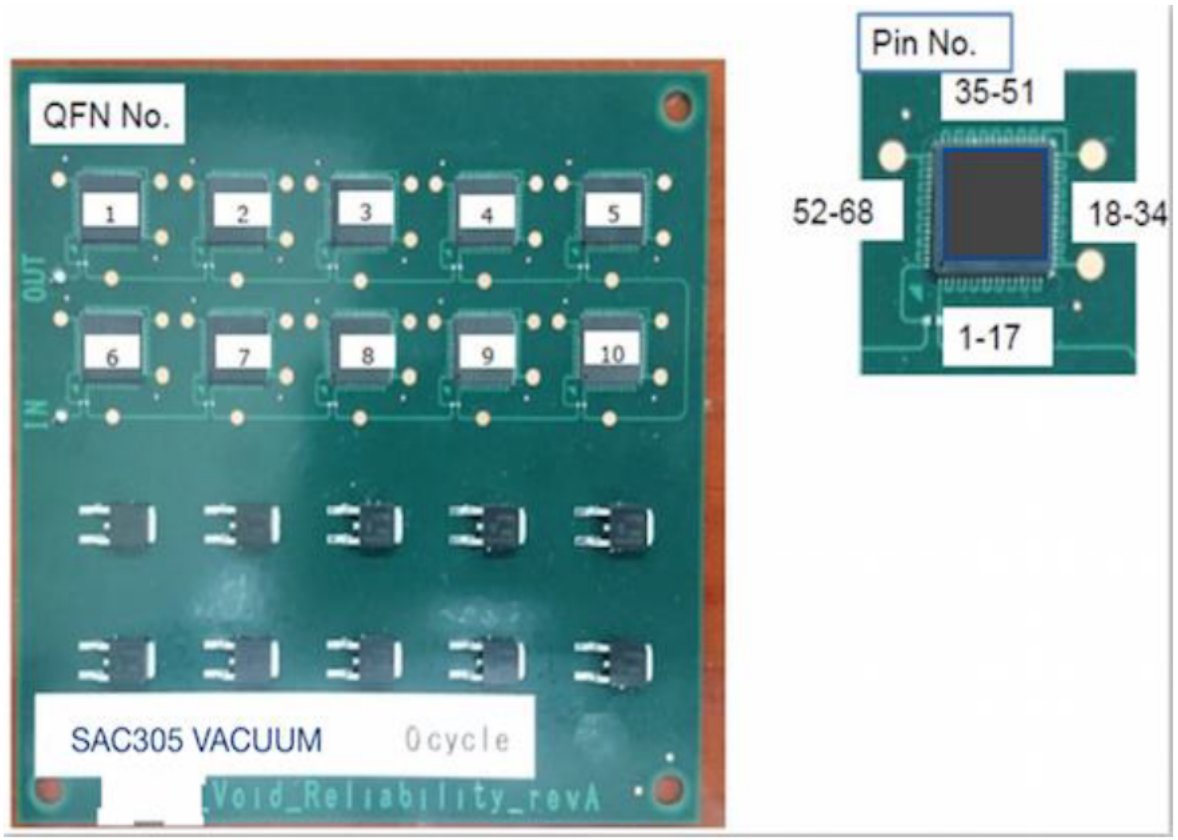
- **Bare board: 105mm X 105mm X 1.2mm thick, FR4, 6 Cu layer, NSMD (non-solder mask defined), circuit board, along with corresponding daisy-chain layout**
- 10 QFNs and 10 DPAKs and 68 total TV-2 boards where assembled (680 parts)





Test Vehicle #2 (QFN/DPAK) Detail

- Daisy chain with ground pads and a chip resistor per each QFN component, significant cracks in the I/Os can be detected via electrical resistance changes.
- If the resistor cracks there is still a step/incremental difference between QFN components.

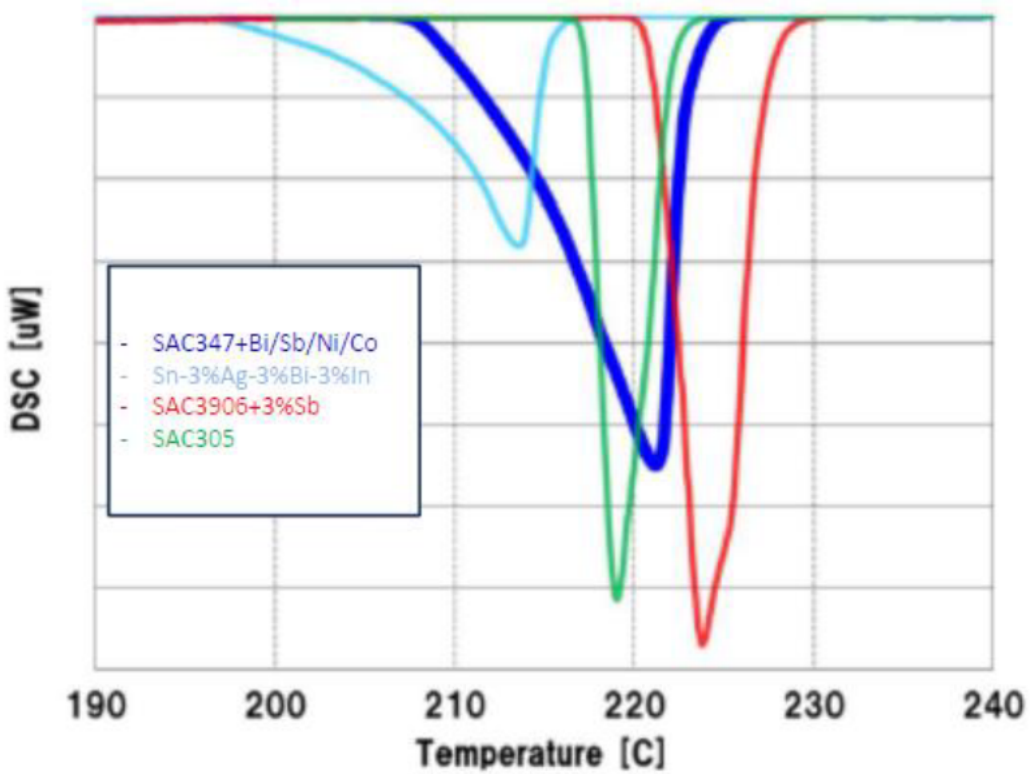


Solder Paste Selection and Reflow Variation

- **SAC305 Alloy, No-Clean ROL0 Flux**
- **SAC305 Alloy, No-Clean ROL1 Flux**
- **SAC347+ Alloy, No-Clean ROL0 Flux**
- **SAC347+ Alloy, No-Clean ROL1 Flux**
- The ROL1 flux paste is a legacy material, with known good performance, considered to have relatively *higher voiding* than the newer ROL0 flux.
- Reflow environments were chosen to intentionally reduce or increase the expected void areas.

SAC347+ Higher Reliability Alloy Approach

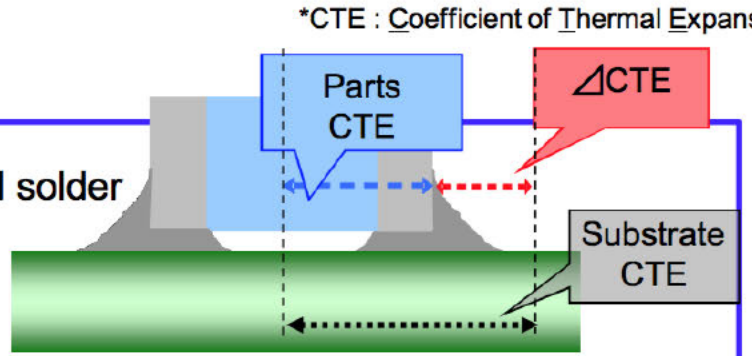
- A combination of elemental additions within the SAC347+ alloy are designed to improve upon joint strength performance after more strenuous TCT conditions.
- Solid Solution Strengthening & Precipitation
- Goal: Maintain current process; improve shear strength and other items post TCT

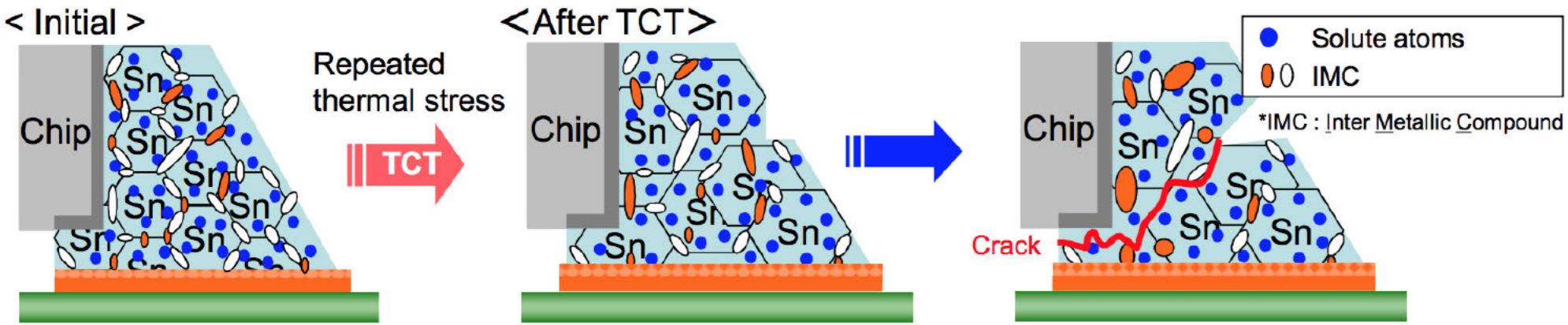


1-2. Purpose and problem to be solved

Task of solder material for automotive

Thermal stress by the difference in CTE of the substrate, parts and solder affects to solder repeatedly, then the crack occur into the solder.
Performance required for the solder material is increased,
The solder material having high joint reliability is required.





Structure after soldering

Structure	State
Sn grain	Fine
IMC	Distributed at the Sn grain boundaries. Ag3Sn network is formed.

Structure after TCT

Structure	State
Sn grain	Coarsening
IMC	Disappearance of Ag3Sn network.
Joint	Deformation

Structure after crack has occurred

Structure	State
Sn grain	Crack has occurred.
IMC	Disappearance of Ag3Sn network.
Joint	Crack has occurred in the low-strength area.

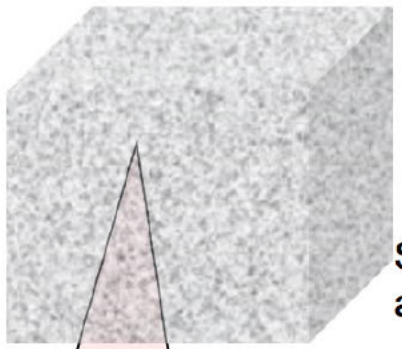
Purpose The development of solder alloy to restrain a crack due to control solder microstructure and improvement of mechanical strength.

2-1. Improvement of mechanical strength by the precipitation and the solid solution

- Precipitation of IMC : Because IMC is very hard, strength of joint is improved.
- Solid solution : The transfer of the crystal lattice is controlled by the existence of a different atom.

Solid solution strengthening

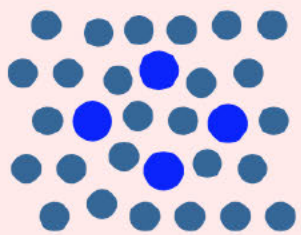
The strength improvement by solid solution in Sn.
(Sb / Bi / In / etc…)



Solid atoms
Sn atom

Solute atoms are distributed at the atomic level.

Extended to the atomic level



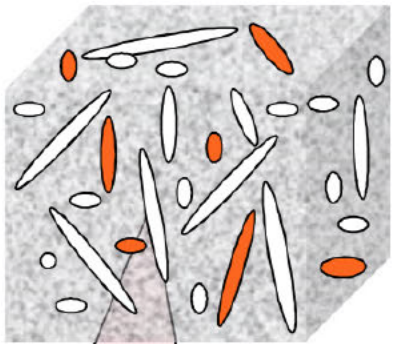
Solid solution state

The transformation of the crystal lattice is controlled by the existence of a different atom.

The absence of a solid solution

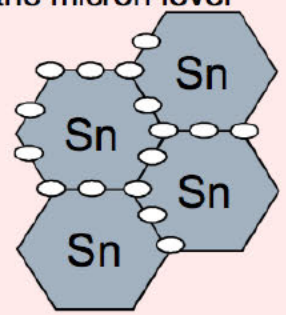
Precipitation strengthening

The strength improvement by IMC generation.
(Cu_6Sn_5 / Ag_3Sn / etc…)



Sn phase
IMC

Extended to the micron level



The transformation is controlled by distribution of IMC at the grain boundary.

Mechanical strength is improved by using solid solution and precipitation at the same time.

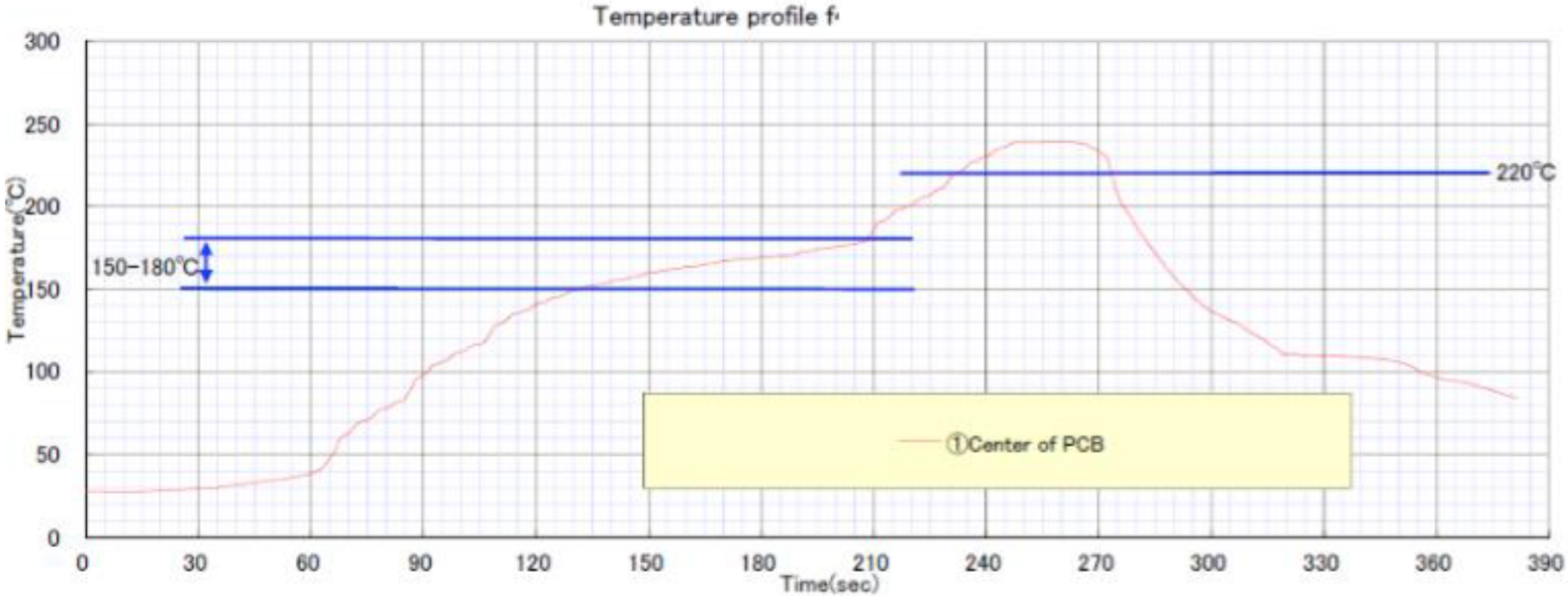
Processing Conditions

- Air Reflow Environments for Chip Component and QFN/DPAK were aligned.
- Vacuum Reflow for QFN/DPAK
- TARGET: **Low Void (<0.5%), Medium (5~20%), High Void (<35%)**
- Basic Print Process Followed

【Printing condition】

Machine	
Speed	30mm/sec
Stencil Thickness	0.12mm
Squeegee	Metal/Angle 60deg
Pressure	0.20N/mm
Removal speed	5.0mm/s
Snap off	On contact

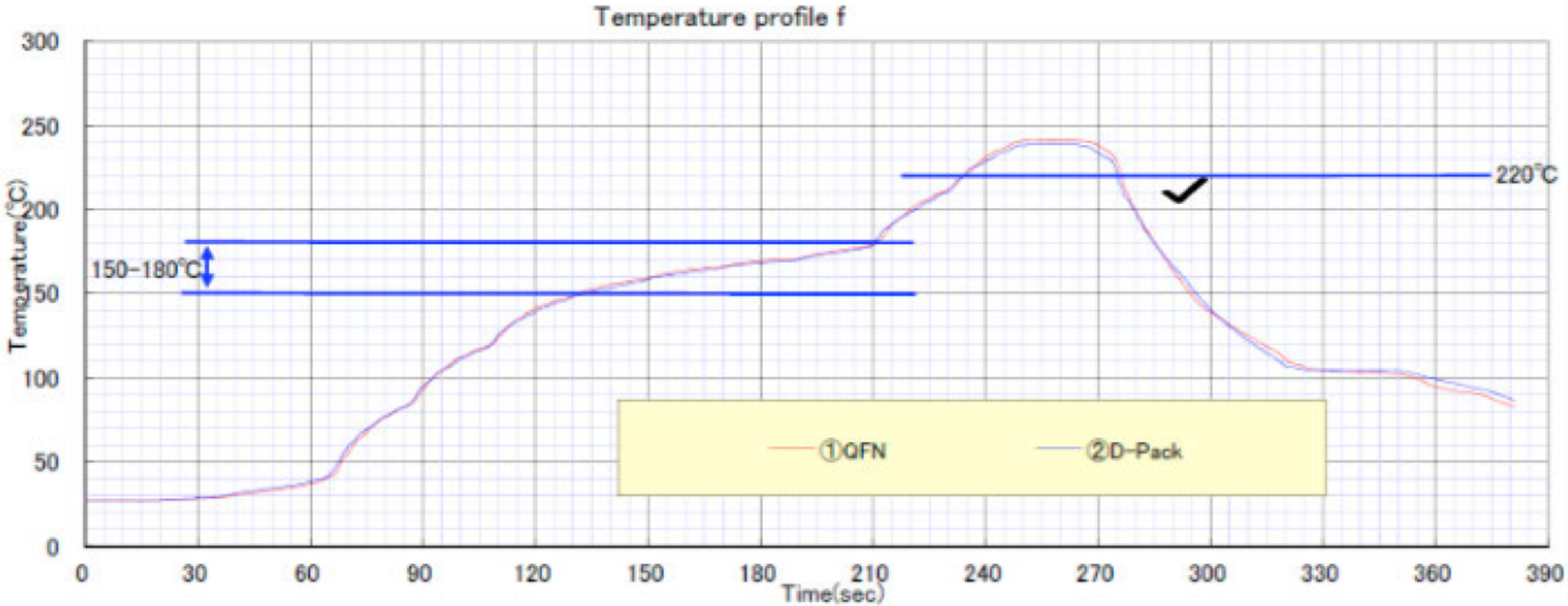
● Air reflow



		1Zone	2Zone	3Zone	4Zone	5Zone	6Zone	7Zone	8Zone	9Zone	10Zone
Setting [℃]	Upeer	100	135	165	170	175	180	185	235	265	250
	Lower	100	135	165	170	175	180	185	235	265	250

	①	
Soak Time(sec) （ 150 ～ 180 ）	77	
RF time(sec) （ 220 ℃以上 ）	42	⊿t
Peak Temp.	239.2	2.6

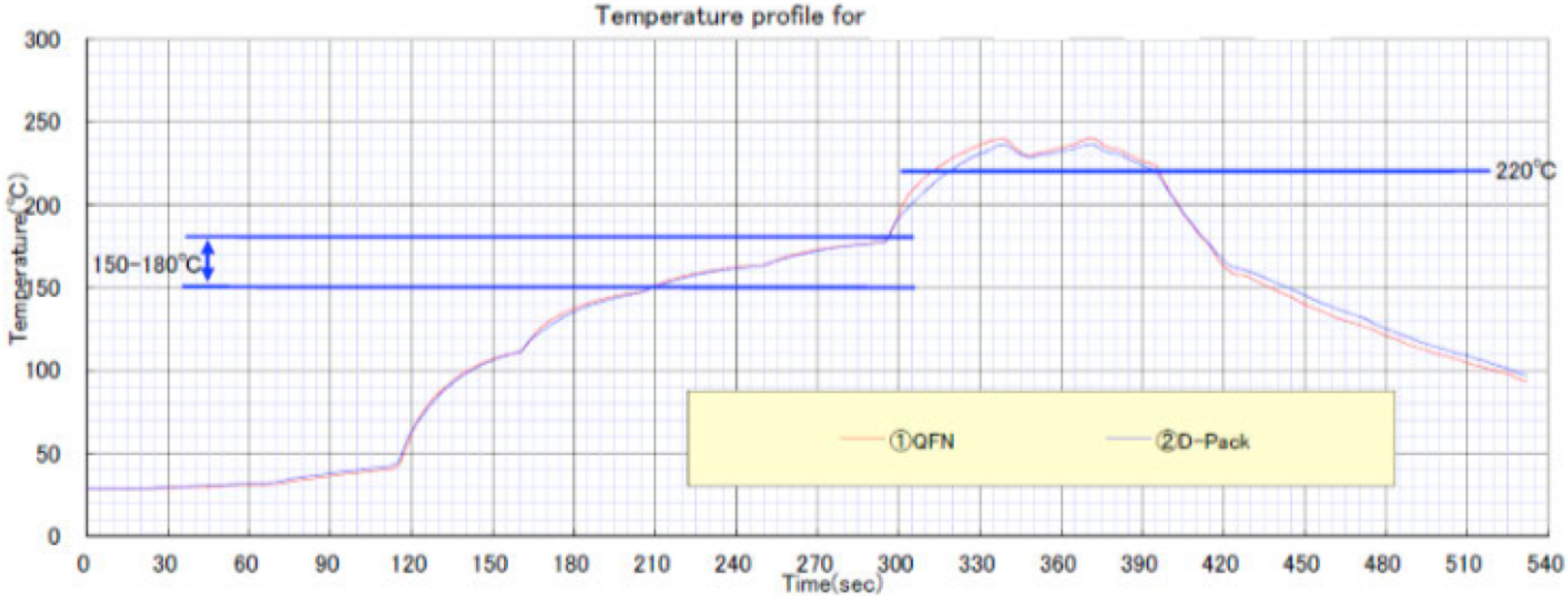
● Air reflow



		1Zone	2Zone	3Zone	4Zone	5Zone	6Zone	7Zone	8Zone	9Zone	10Zone
Setting [℃]	Upeer	100	135	165	170	175	180	185	235	265	250
	Lower	100	135	165	170	175	180	185	235	265	250

	①	②	
Soak Time(sec) （ 150 ～ 180 ）	80	78	
RF time(sec) （ 220 ℃以上 ）	42	41	⊿t
Peak Temp.	241.6	239.0	2.6

● Vacuum reflow



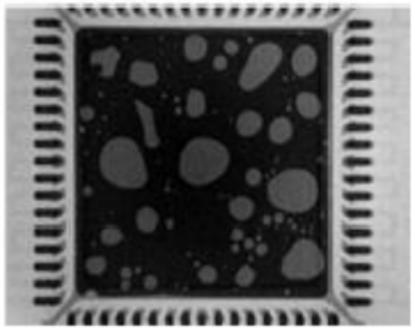
		1Zone	2Zone	3Zone	4Zone	5Zone	6Zone
Setting [℃]	Upeer	120	155	170	180	260	-
	Lower	120	155	170	185	260	300

	①	②	
Soak Time (150 ～ 180)	88	88	
RF time(sec) (220 ℃以上)	84	76	⊿t
Peak Temp.	240.2	236.7	3.5

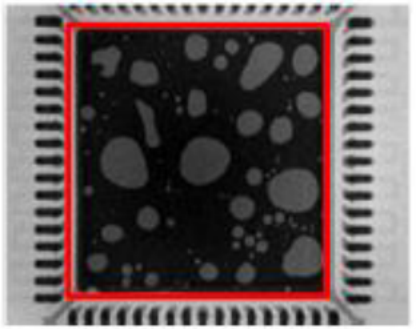
Void Measurement

【Procedure】

1. X-ray images are acquired (each components)

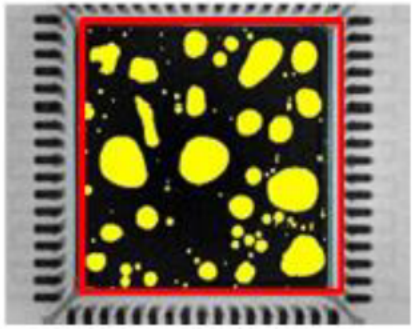


2. Determine the area of soldering to measure voiding ratio. (red area)



□=Heat sprader pad area

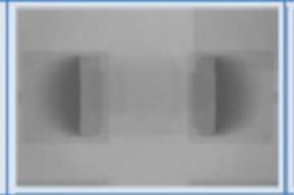
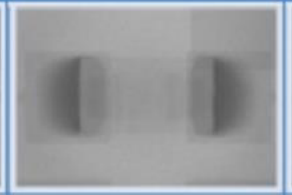
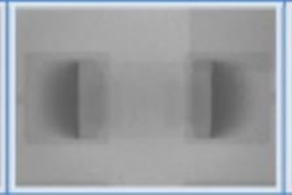
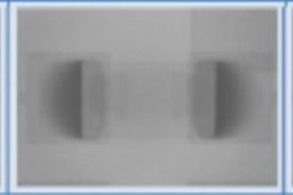
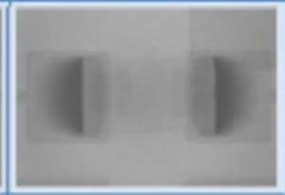
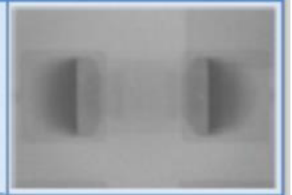
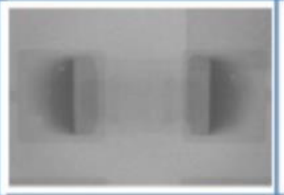
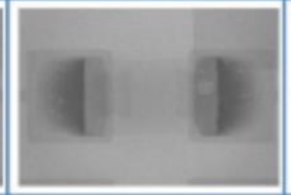
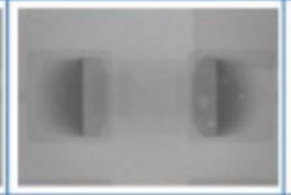
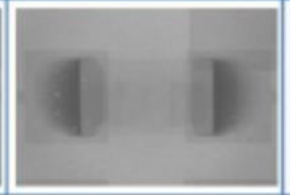
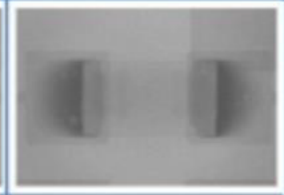
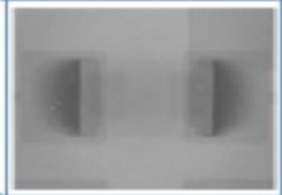
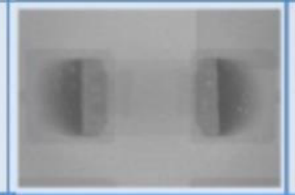
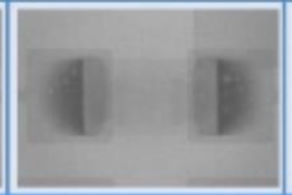
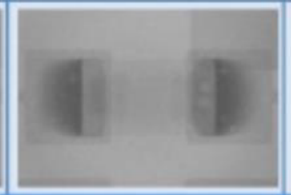
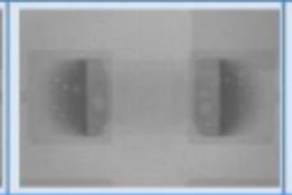
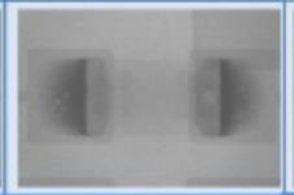
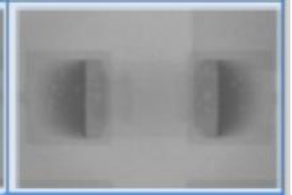
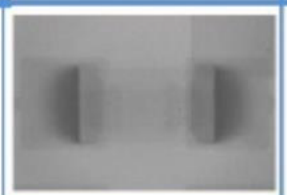
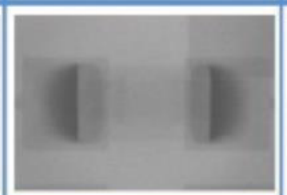
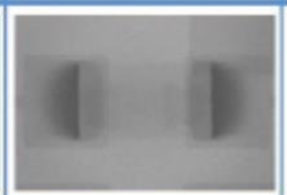
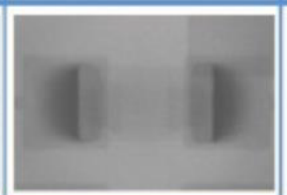
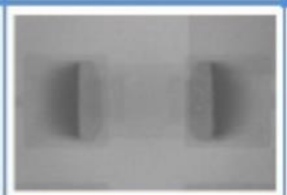
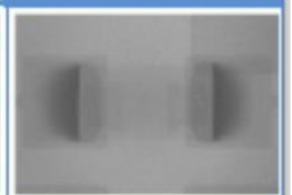
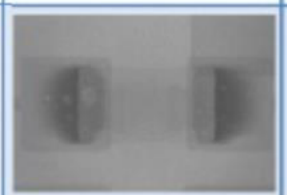
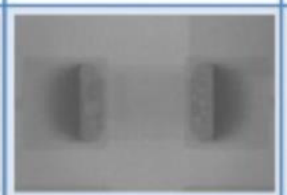
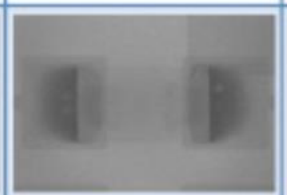
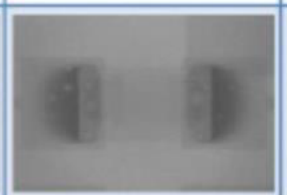
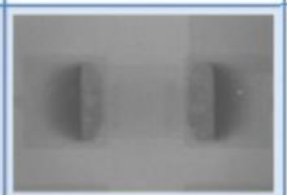
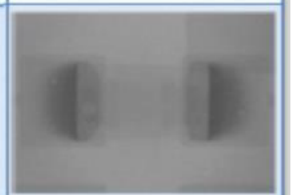
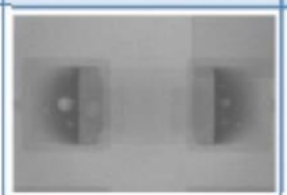
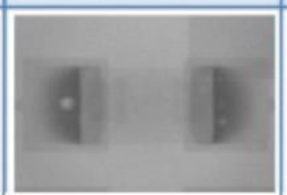
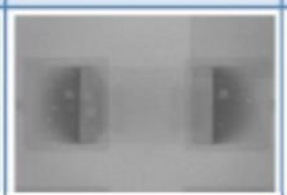
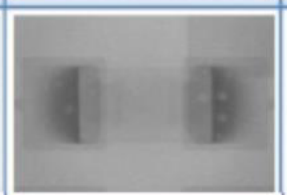
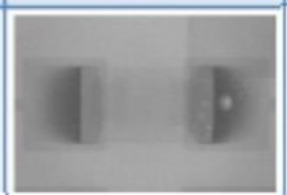
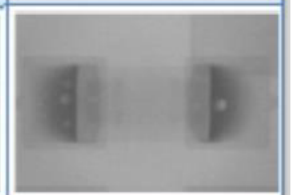
3. Calculate voiding ratio. (yellow area)



4. Void ratio % = yellow area / red area X 100

Chip Resistor: Voiding

- The research laboratory was unable to secure a more poorly performing competitive paste product and therefore all results were relatively low in voiding.
- Even without use of vacuum reflow, most components saw voiding in the range of 2~5%. All void areas were below 15%.
- This did not meet the DoE target of having three (3) discernable void levels.
- Nevertheless, it was decided to continue with shear testing of TV #1 post TCT.
- Components were removed via shear every 500 cycles in order to compare force values after TCT.

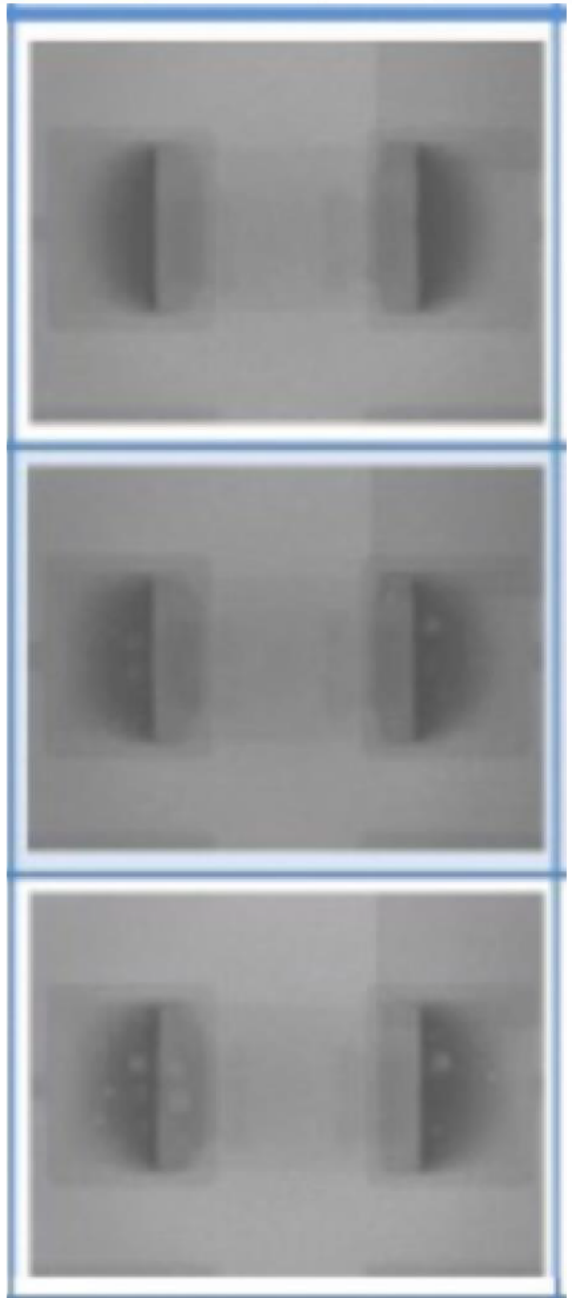
DOE	Paste	Reflow Condition						
C1-3	SAC305 NC ROL0	Vac.						
C2-3	SAC305 NC ROL0	Air						
C3-3	SAC305 NC ROL1	Air						
C4-3	SAC347 NC ROL0	Vac.						
C5-3	SAC347 NC ROL0	Air						
C6-3	SAC347+ NC ROL1	Air						

Typical view of Chip Components

SAC347+ ROL0: Vacuum

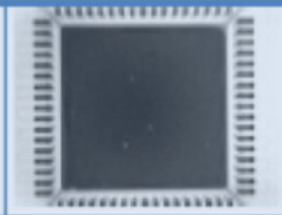
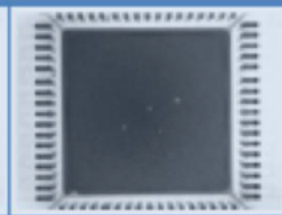
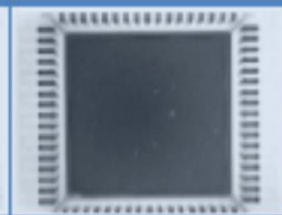
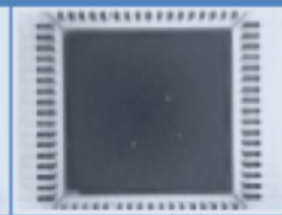
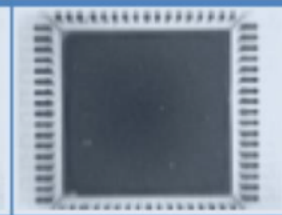
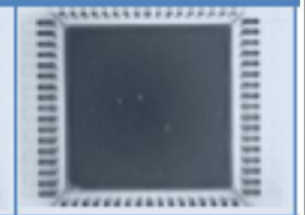
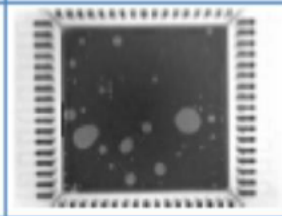
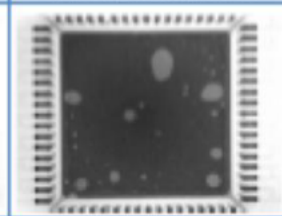
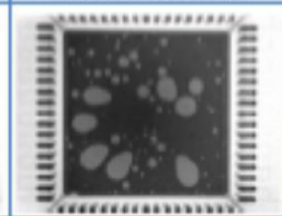
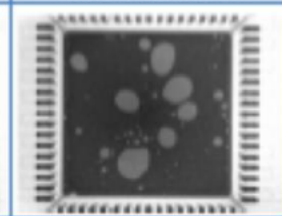
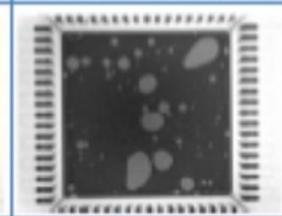
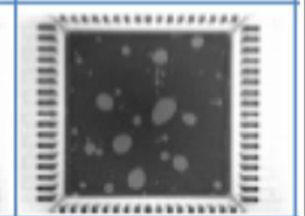
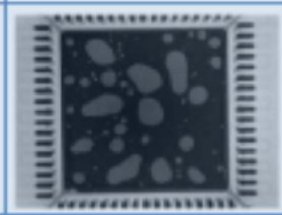
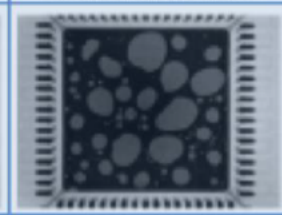
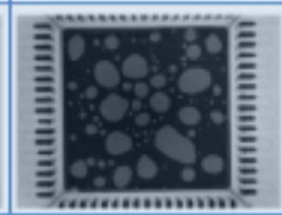
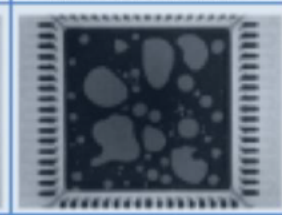
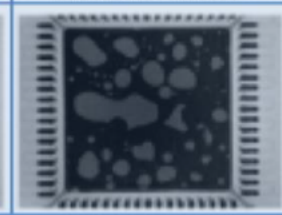
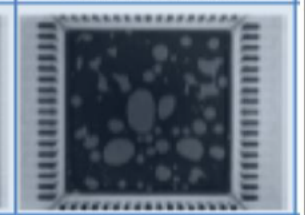
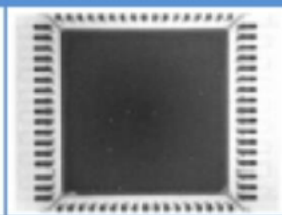
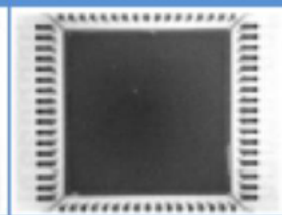
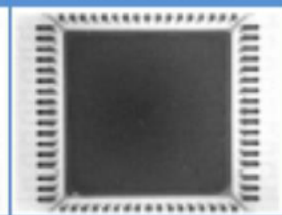
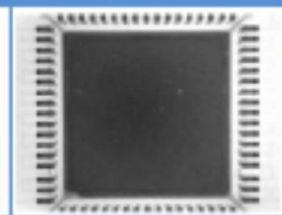
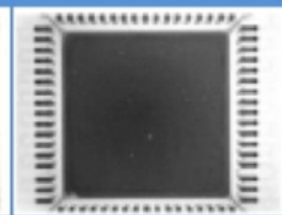
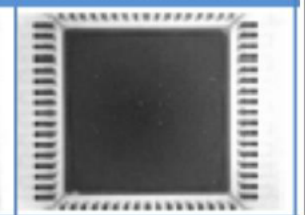
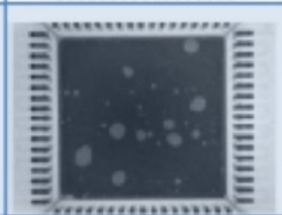
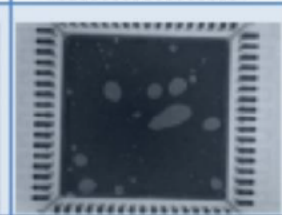
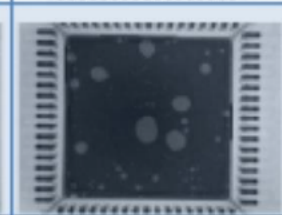
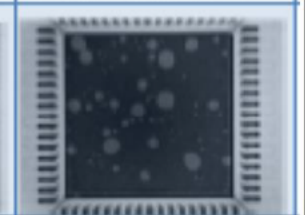
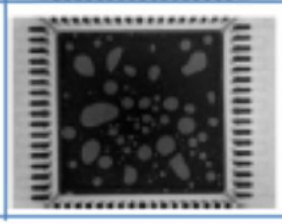
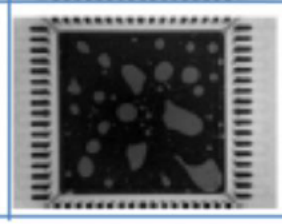
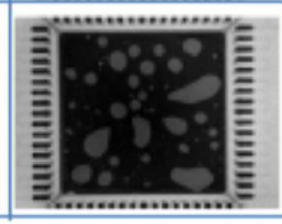
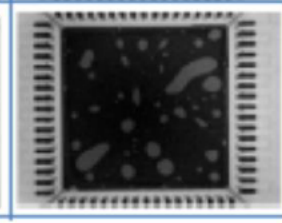
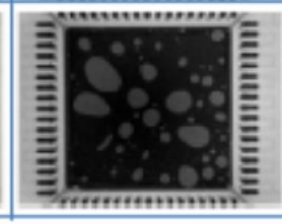
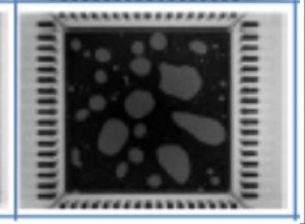
SAC347+ ROL0: Air

SAC347+ ROL1: Air



QFN Void Observation

- Here we could see a greater variation in the void levels between the paste materials and the reflow processing.
- Voids levels were measured and Low, Medium and High level void ratios were acknowledged.
- The Resistance values were to be collected in situ for TV #2 with QFNs and DPAK components placed on board.

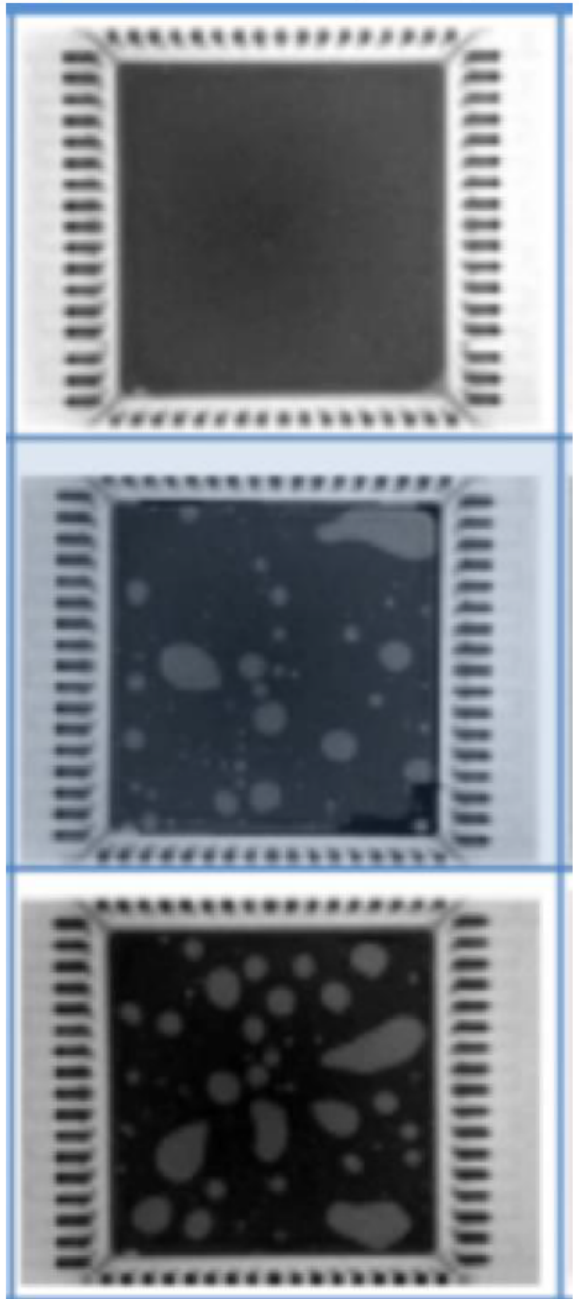
DOE	Paste	Reflow Condition						
Q1	SAC305 NC ROL0	Vac.						
Q2	SAC305 NC ROL0	Air						
Q3	SAC305 NC ROL1	Air						
Q4	SAC347+ NC ROL0	Vac.						
Q5	SAC347+ NC ROL0	Air						
Q5	SAC347+ NC ROL1	Air						

Typical view of QFN Components (Top to bottom…)

SAC347+ ROL0: Vacuum

SAC347+ ROL0: Air

SAC347+ ROL1: Air

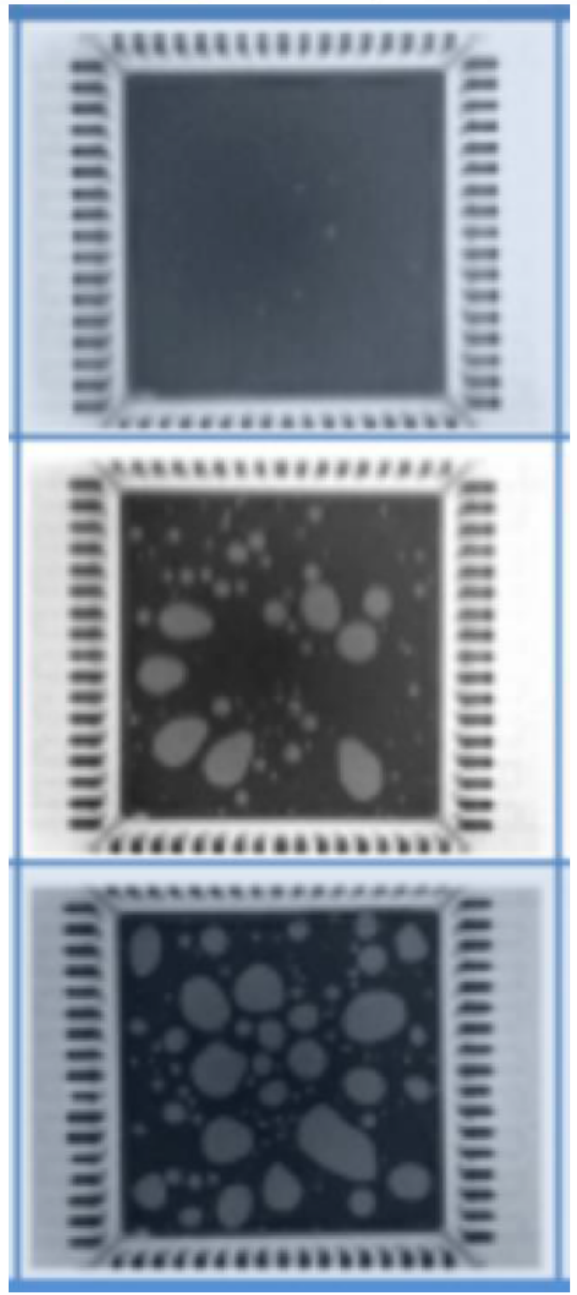


Typical view of QFN Components

SAC305 ROL0: Vacuum

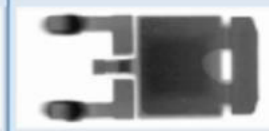
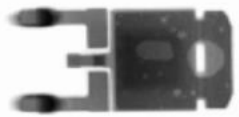
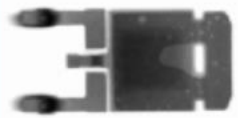
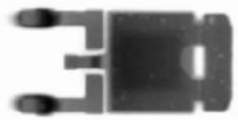
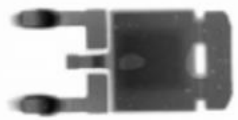
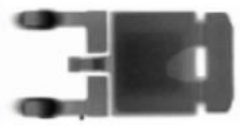
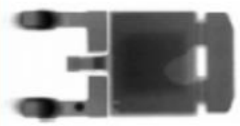
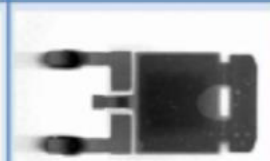
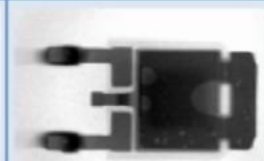
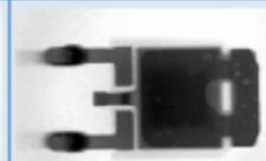
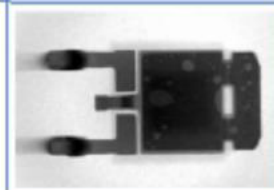
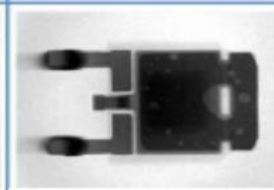
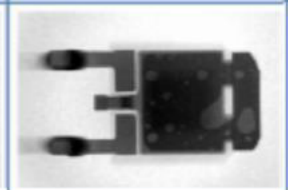
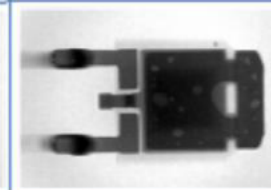
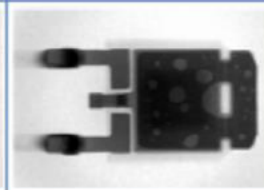
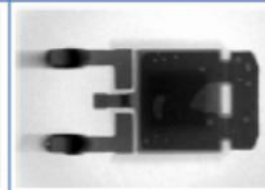
SAC305 ROL0: Air

SAC305 ROL1: Air



DPAK Void Observations

- The DPAK components often exhibited a higher level of voiding than the QFN and up to 35%.
- The components were to be cross sectioned for failure analysis prior to and after TCT chamber runs with the combined QFN / DPAK PCB
- Test Vehicle #2

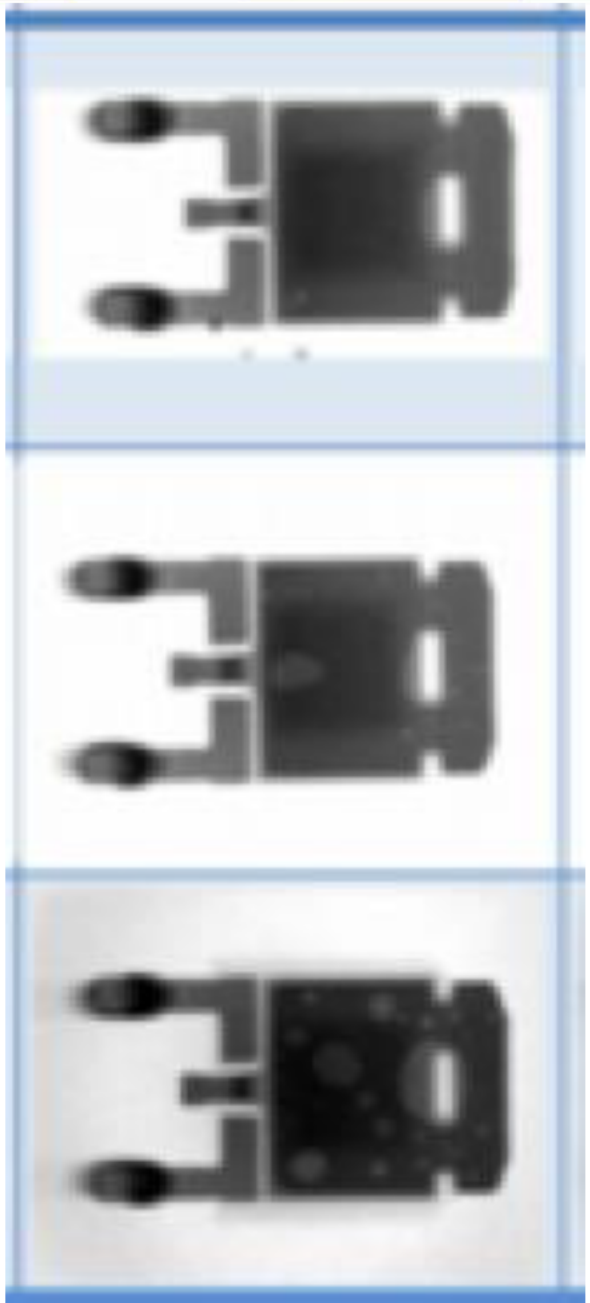
DOE	Paste	Reflow Condition						
D1	SAC305 NC ROL0	Vac.						
D2	SAC305 NC ROL0	Air						
D3	SAC305 NC ROL1	Air						
D4	SAC347+ NC ROL0	Vac.						
D5	SAC347+ NC ROL0	Air						
D6	SAC347+ NC ROL1	Air						

Typical view of DPAK Components

SAC305 ROL0: Vacuum

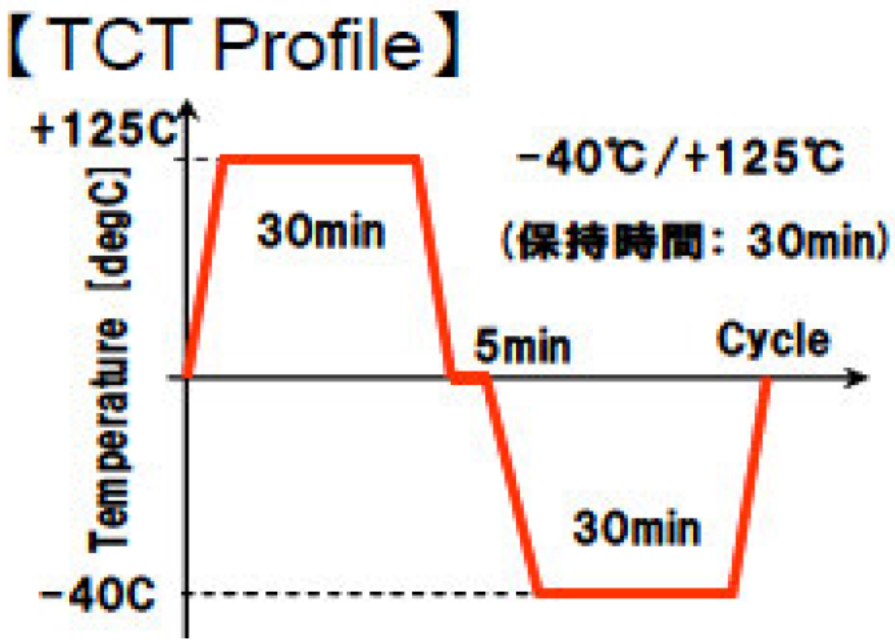
SAC305 ROL0: Air

SAC305 ROL1: Air



Thermal Cycle Test Condition

- The Assembled TVs were to be subjected to a -40C/+125C TCT
- 30min dwell
- 5min ramps
- TVs are to be reviewed for initial characteristics (void, IMC) and observed throughout the test each 500 cycles up until 3,000 completed cycles.

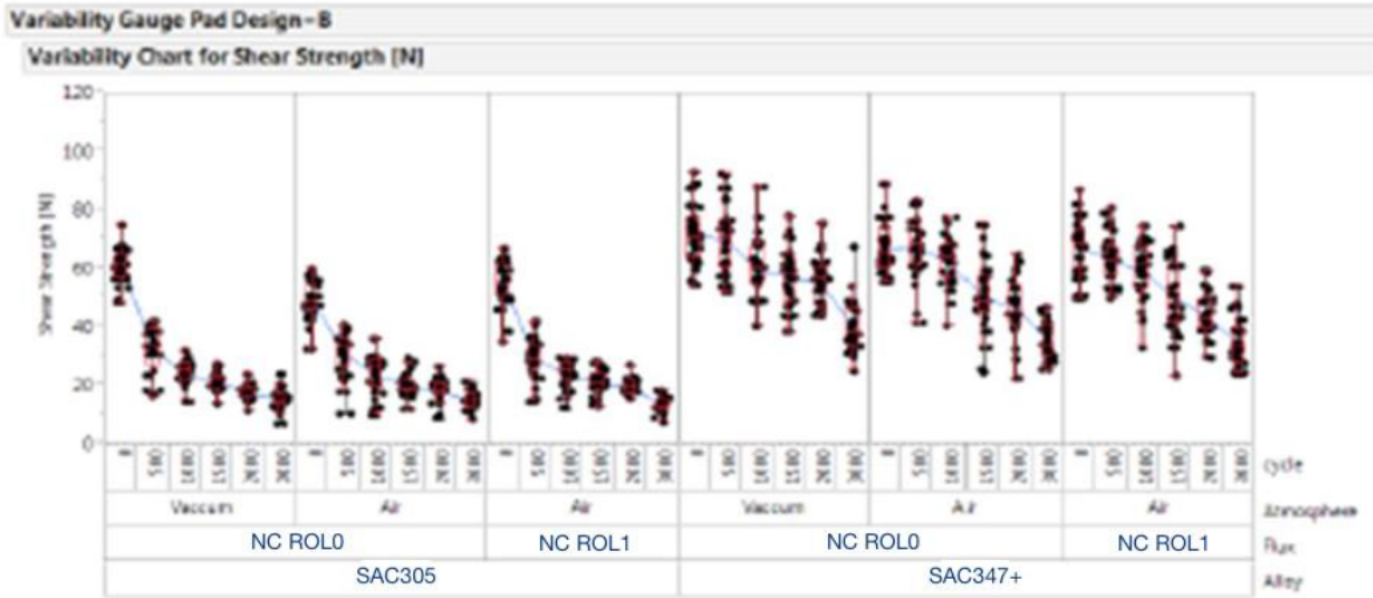


Chip Resistor: Shear Test Results

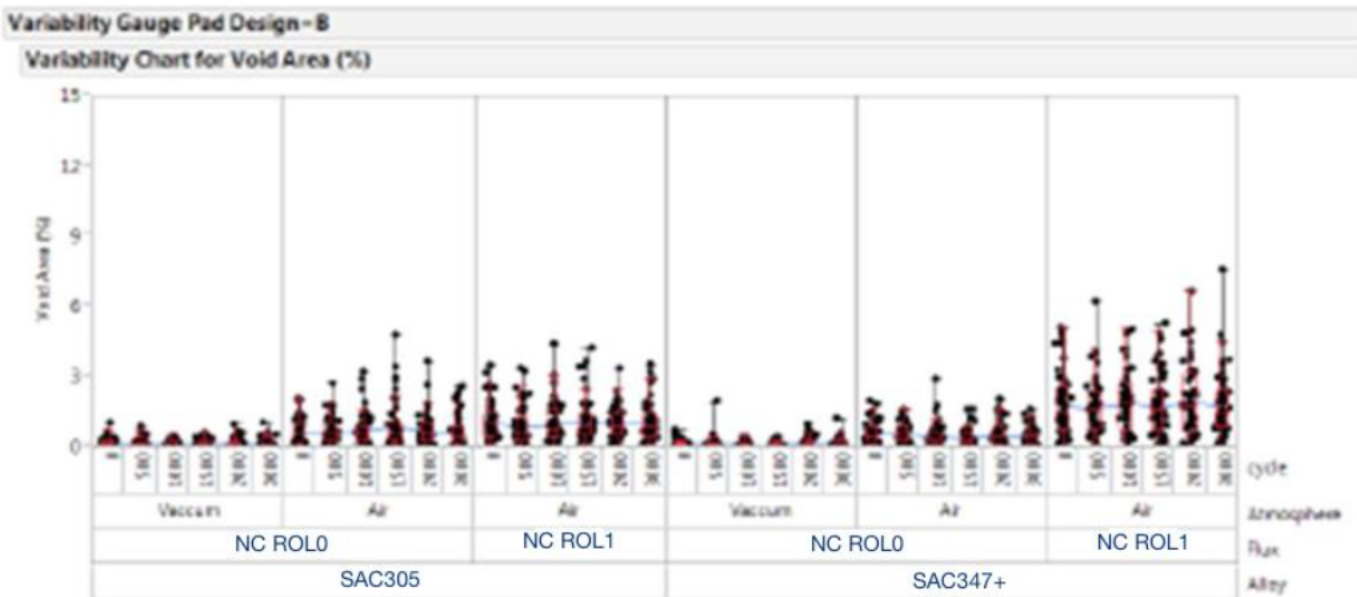
- Again, although the variation in void levels was not ideal to meet the targeted Low, Medium and High void levels, we could measure some variation due to materials and process.
- Shear Speed: 6mm/sec.

3216 Shear Results

- Upper Chart: Shear Values (N)
- Lower Chart: Void Area



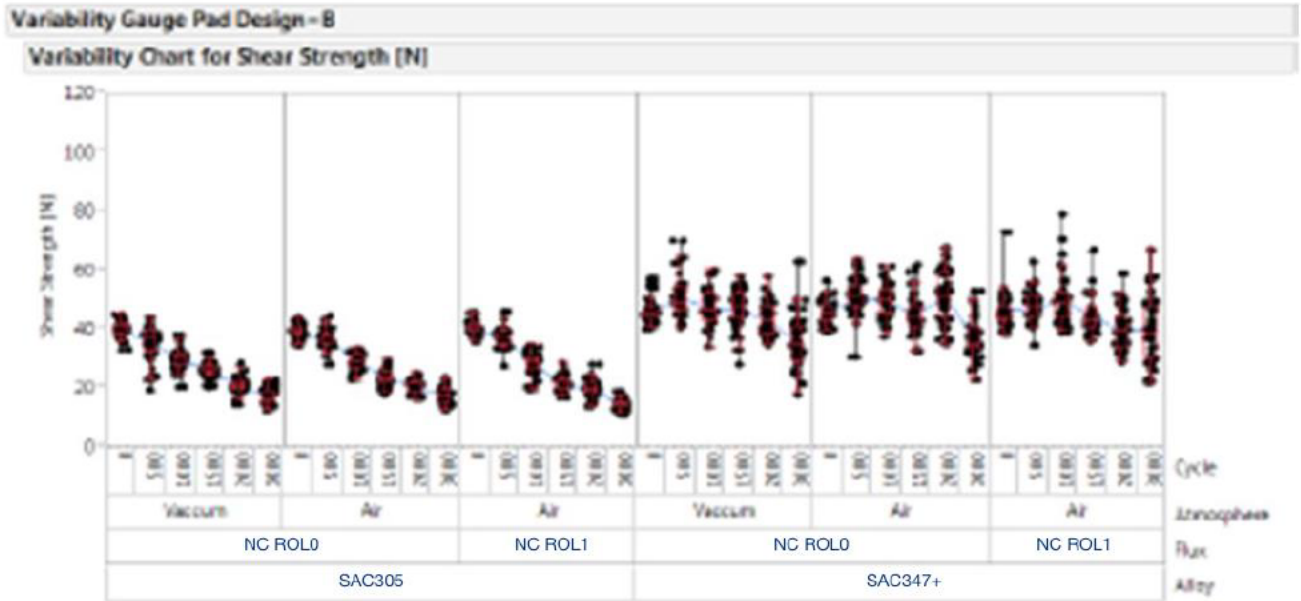
- NOTES:
  - *SAC347+ initial values much greater than SAC305*
  - *Regardless of void level, SAC347+ with similar result and consistently higher value versus SAC305 post 3000 cycles.*

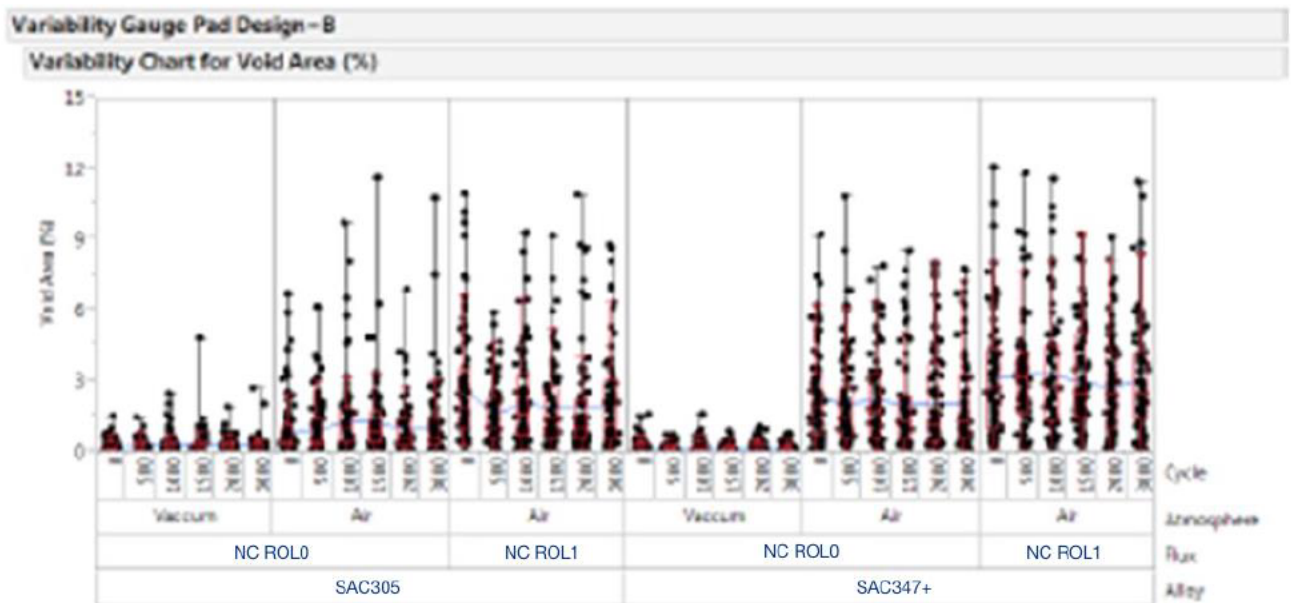


2012 Shear Results

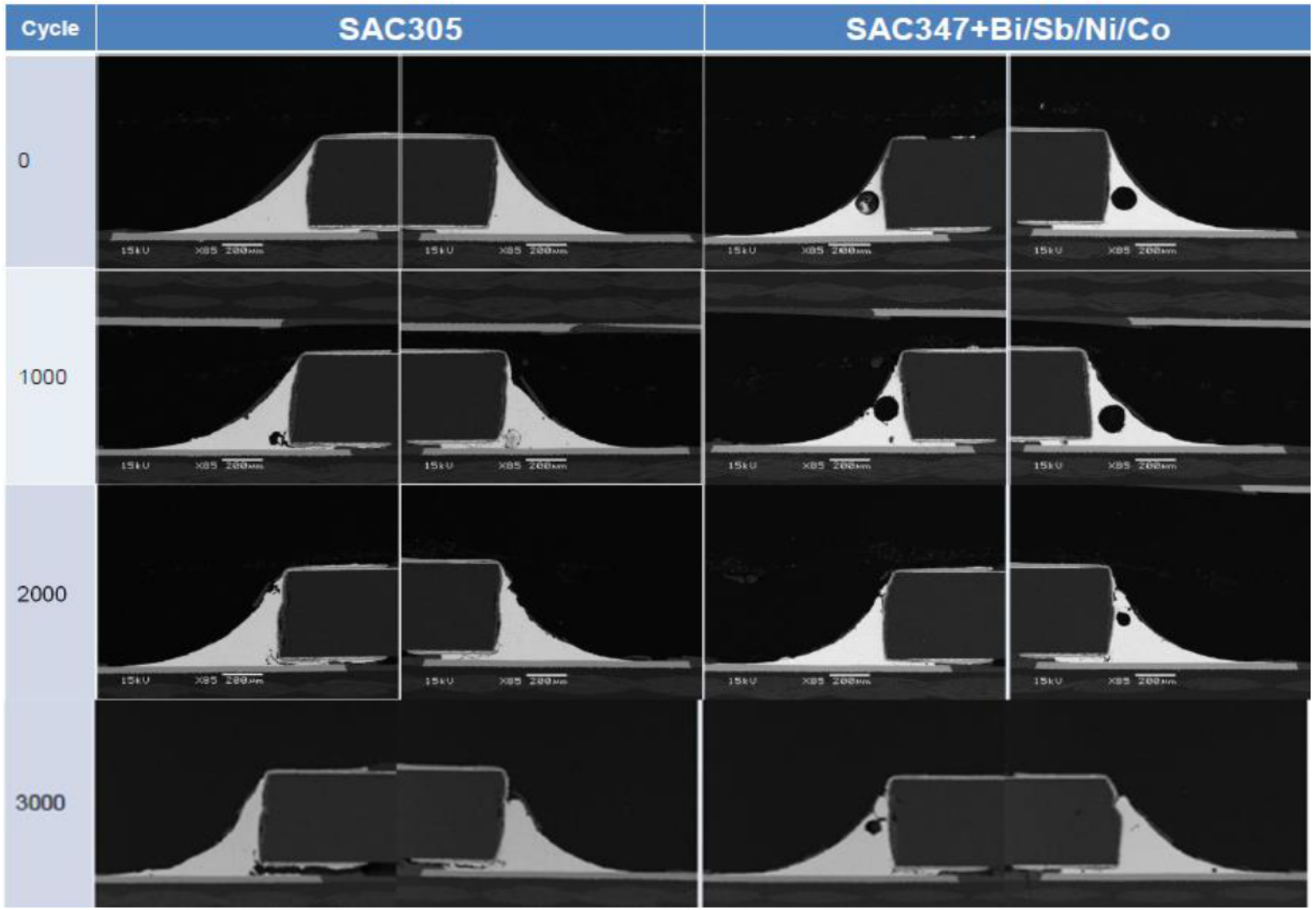
- Upper Chart: Shear Values (N)
- Lower Chart: Void Area

- NOTES:
  - *Greater void variation from 3216 results.*
  - *But LESSER variation in shear force readings from initial through 3000 cycles.*





Chip Resistor Representative X-Ray

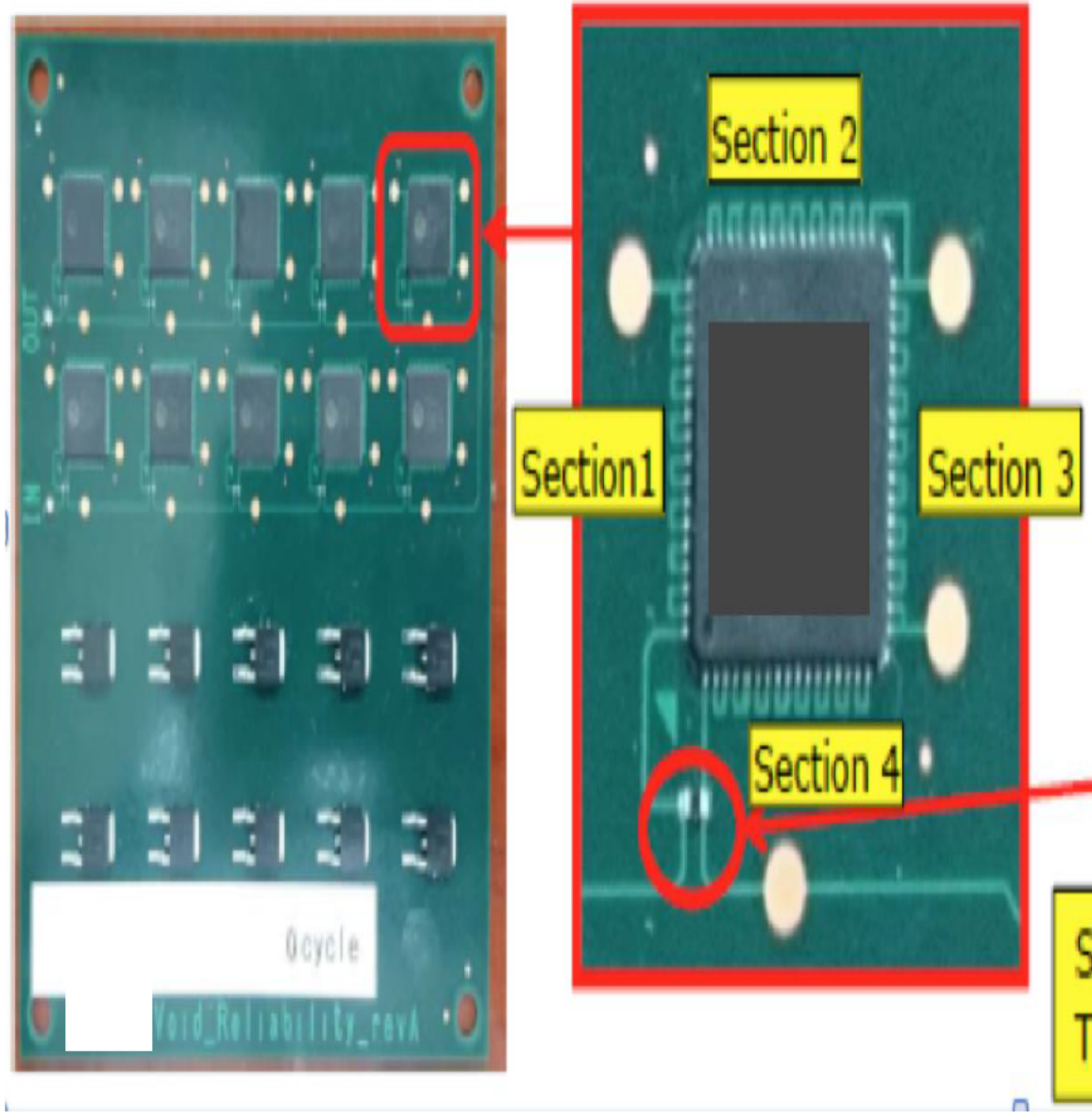


- Left Side: SAC305
- Right Side: SAC347+
- NOTES:
  - *Top: T0*

    Bottom: T3000
  - *SAC347 larger voiding*
  - *But as TCT progresses, the crack propagates throughout the SAC305 underside and termination.*
  - *SAC347+ crack growth is limited.*
  - *This is typical of other joints observed.*

Test Vehicle #2 (QFN/DPAK) Resistance

- QFNs are connected via daisy chain and resistance is measured.
- Should a section or side of the QFN leads suffer a failure, the resistance measured will increase by a factor of ~3X.
- Individual lead failure detection is not possible with this process.
- DPAK are also mounted for the purpose of relative voiding and crack propagation comparisons.



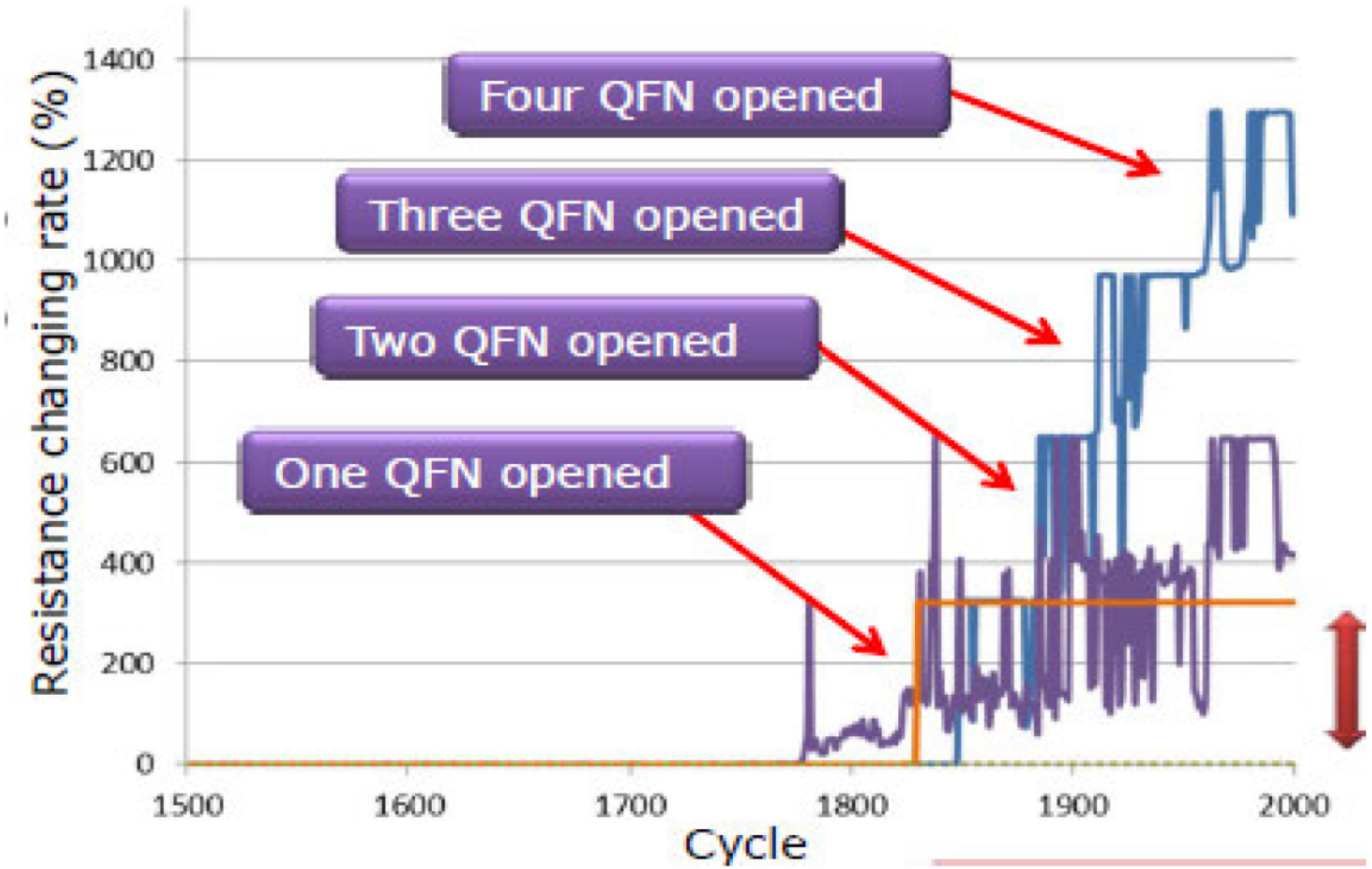
An increase of about 300% of the resistance indicates that one of I/O's on the QFN is opened.

The PCB has resistor between each QFN. So, if I/O. of a QFN is opened, resistance changing ratio increase stepwise.

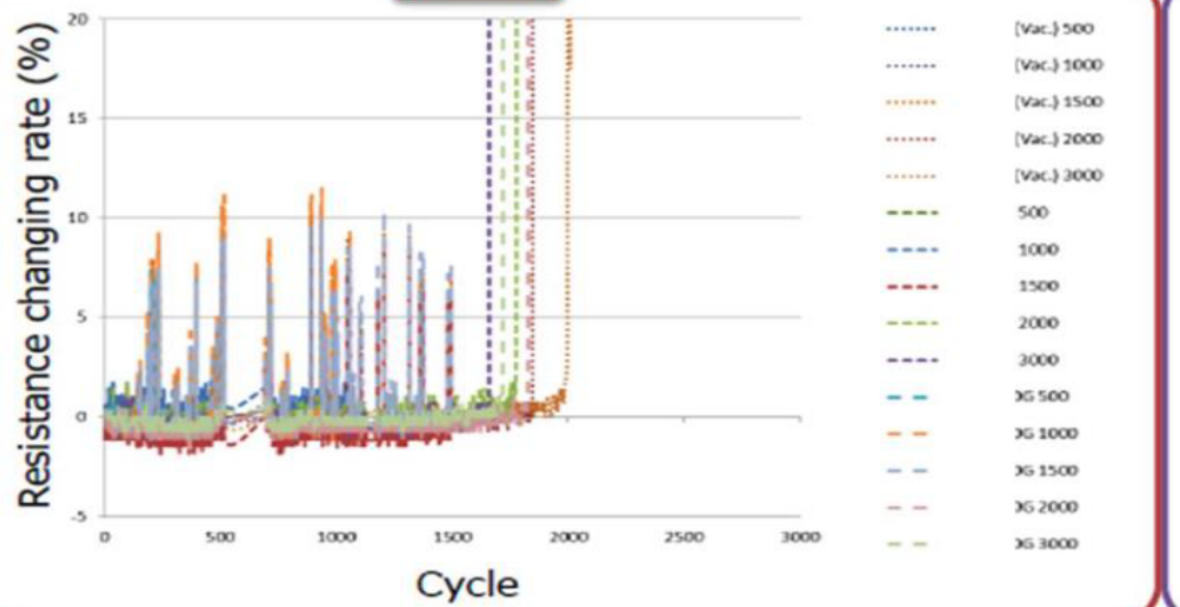
So far we can detect whether each section has opened.
To detect an opened individually we need another method.

Resistance Detection Example

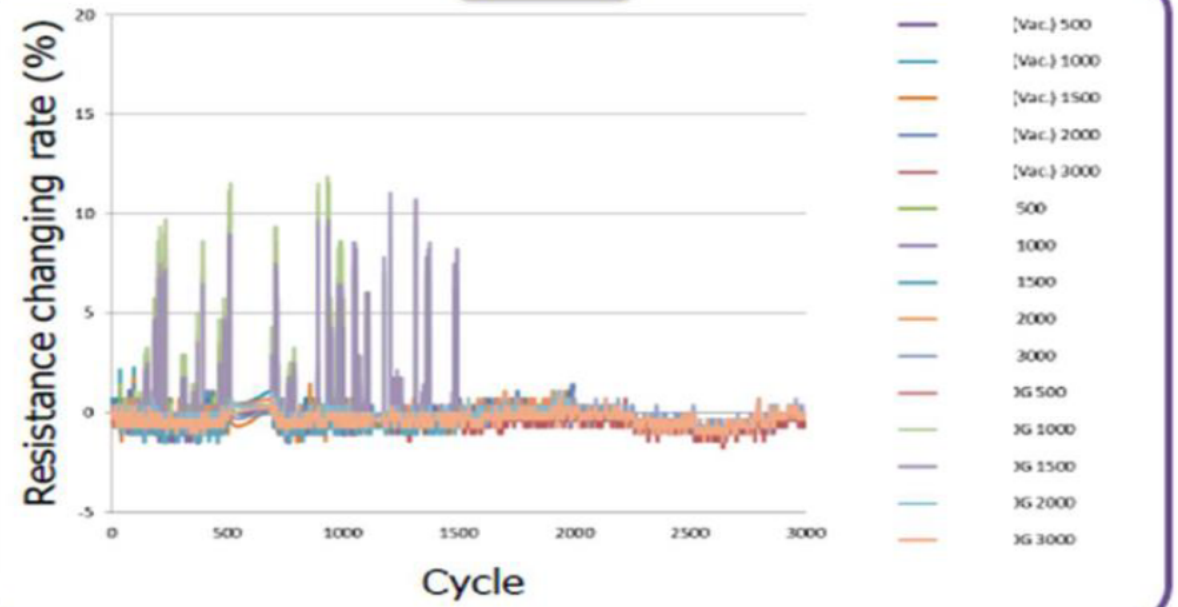
- Can observe a failure of a QFN section (“side”) as the resistance changes significantly.
- After approximately 1850 cycles, the resistance peak increased ~300%.
- A similar increase is observed almost at 1900 cycles, 1920, 1960 and so on…

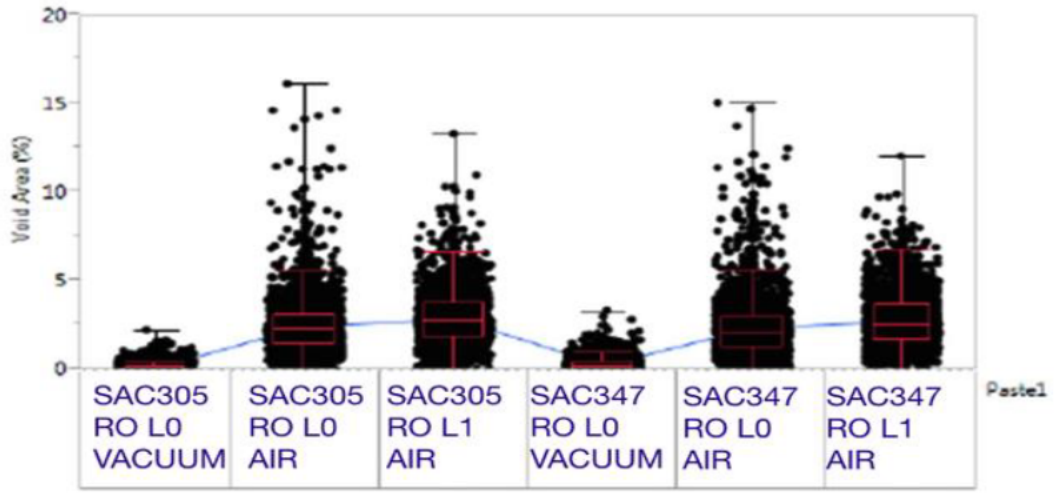


SAC305



SAC347+





Summary:

- -After 3000 thermal cycles, there is no correlation between fracture starting cycle and void area rate, and a factor of the solder composition is dominant to fracture starting cycle

PCBs taken out up to 1500 cyc had noise but PCBs taken out after 2000 cyc had almost no noise since 0 cyc.
This is due to cable issue. Each 500 cyc group PCBs connected each connector unit(power supply was same.).
So resistance noise up to 1500 cyc is not due to crack.

QFN Resistance Results Summary

- An issue with noise was found due to harness cable positioning within the chamber prior to 1500 cycles.
- However, no resistance changes (“step up”) were detected prior to nearly1800 cycles.
- At this point, the SAC305 QFN began to fail, with the Medium Void level (~15-25%) components failing first.
- Regardless of process condition, and regardless of Low to High voids content, all SAC305 QFNs are failing within a very narrow and similar timeframe.

Cross Section (CS) and Observations

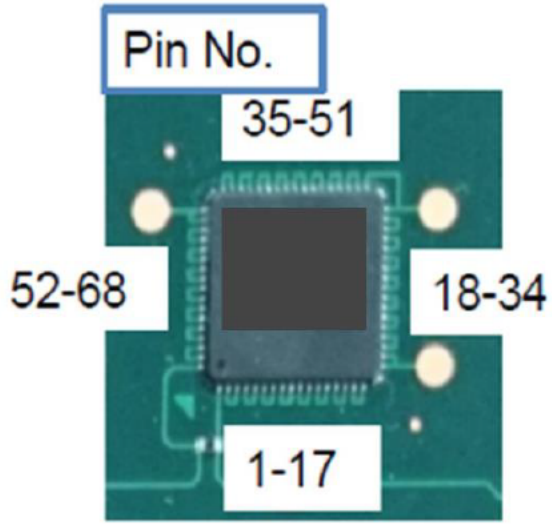
- After the Resistance Test results were found, QFN and DPAK components were reviewed via cross-sectioning and SEM.
- The spreadsheet on the next page shows how a section would be detected for failure via resistance values and this side of the QFN would then be inspected via cross section.
- For SAC305 this allowed CS targeting of rows which failed prior to 2000 cycles.
- For SAC347+, with no failures, rows of QFNs were randomly selected for FA.
- Examples for those CS FA are shown on the next slides.

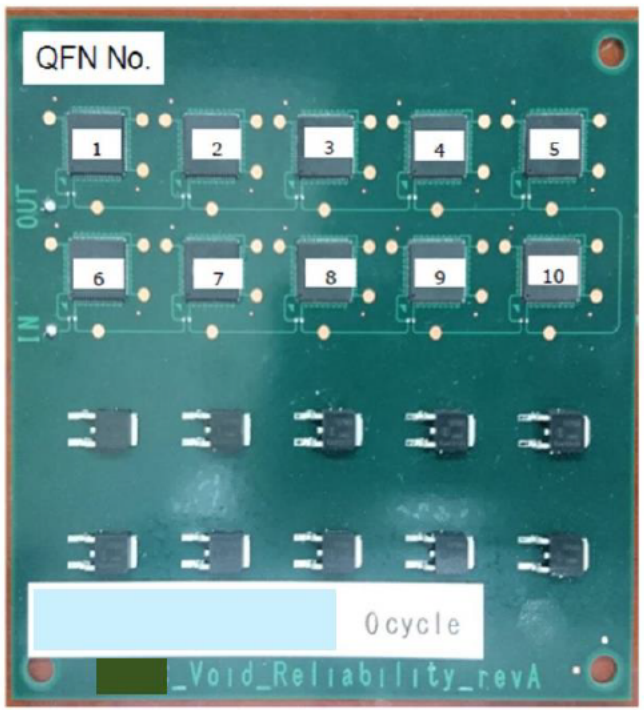
Solder Paste	Atmosphere	QFN No.	QFN Lead No.			
			1-17	18-34	35-51	52-68
SAC305 ROLO	Vacuum	1	-	Open	Open	Open
		2	-	Open	Open	Open
		3	Open	Open	-	-
		4	-	-	-	-
		5	-	-	Open	-
		6	-	Open	Open	Open
		7	-	-	Open	-
		8	-	Open		-
		9	-	Open	Open	-
		10	-	Open	Open	-
SAC305 ROLO	Air	1	-	-	Open	-
		2	-	-	-	-
		3	-	Open	Open	-
		4	-	Open	Open	-
		5	-	Open	Open	Open
		6	-	Open	Open	-
		7	-	Open	Open	Open
		8	-	Open	-	-
		9	Open	Open	-	-
		10	Open	Open	Open	-
SAC305 ROL1	Air	1	-	-	Open	Open
		2	-	Open	Open	-
		3	-	Open	Open	-
		4	Open	Open	Open	-
		5	Open	Open	Open	-
		6	Open	Open	Open	-
		7	Open	Open	Open	-
		8	Open	Open	Open	Open
		9	Open	Open	Open	-
		10	-	Open	Open	-

18 OPENS

17 OPENS

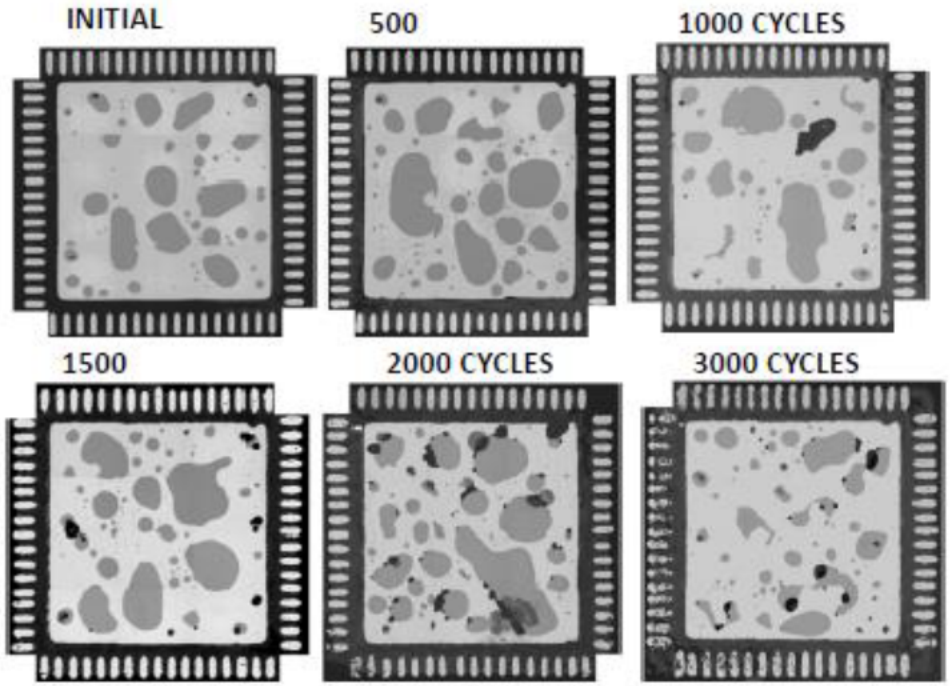
27 OPENS



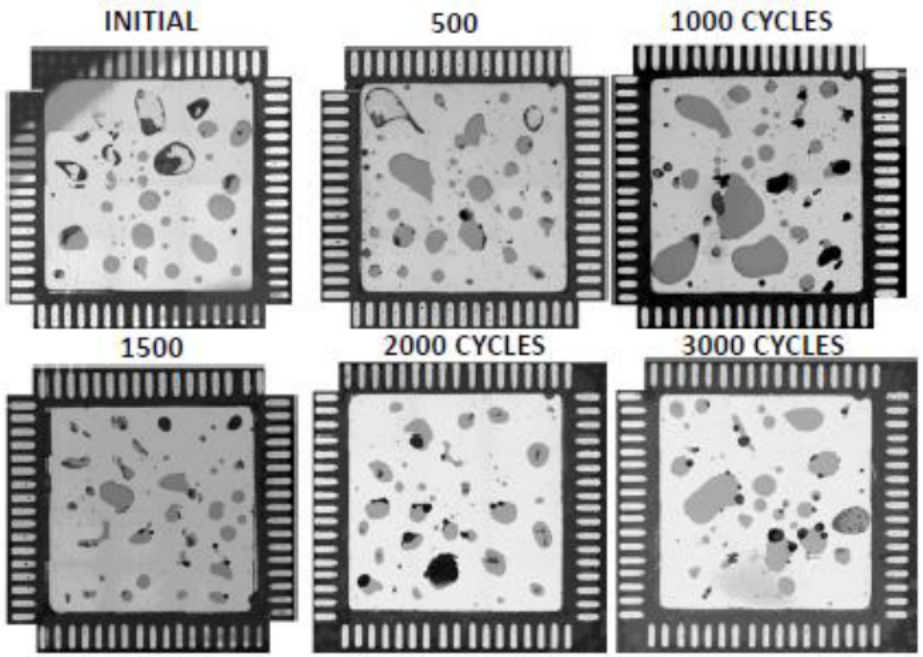


Example of FA

- Here QFN rows are analyzed for crack initiation and length.
- In this case, a SAC305 with relatively lower voiding had still a significant number of failures.
- CS could find significant (yellow) and major (red) cracks.



SAC305 (ROL1) AIR REFLOW

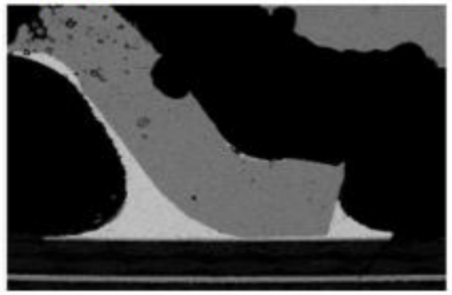


SAC347+Bi/Sb/Ni/Co (ROL1) AIR REFLOW

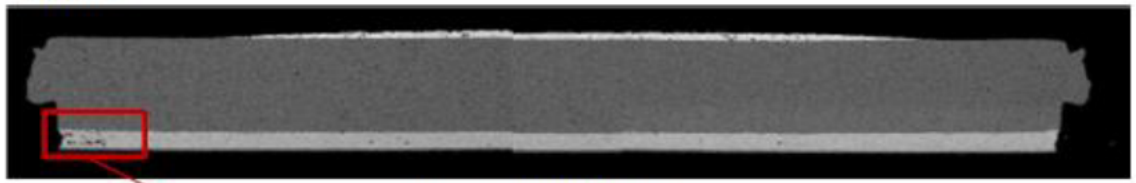
- QFN components with SAC305 on Left and SAC347+ on Right.
- Similar void occurrences for this test.

DPAK RESULT FOR: SAC305 (ROL0) AIR REFLOW

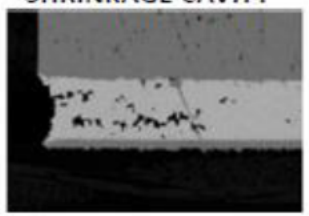
INITIAL

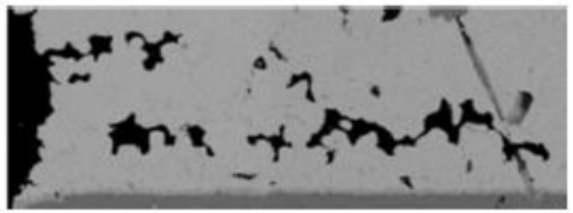


INITIAL

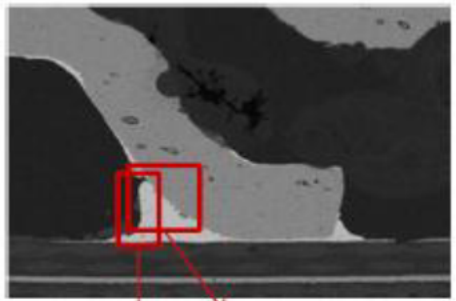


SHRINKAGE CAVITY

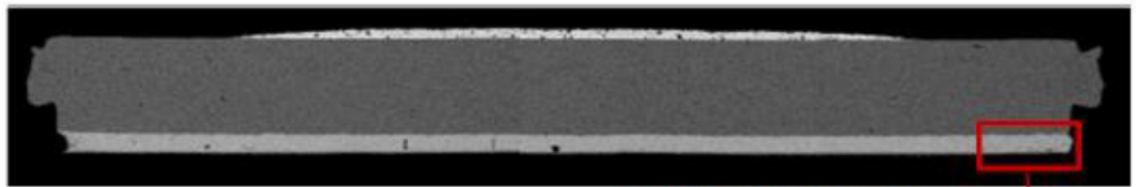




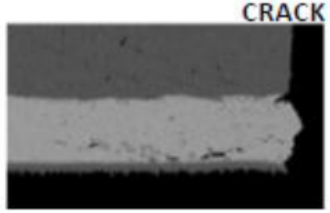
3000 CYCLES

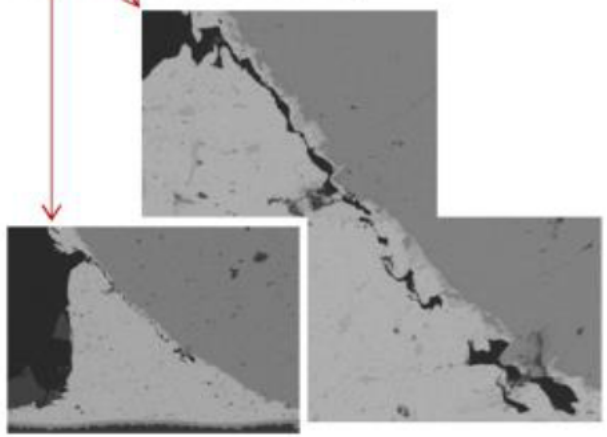


3000 CYCLES



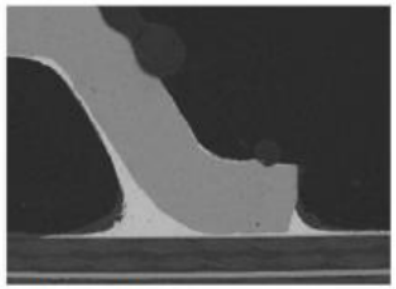
CRACK AFTER 3K CYCLES



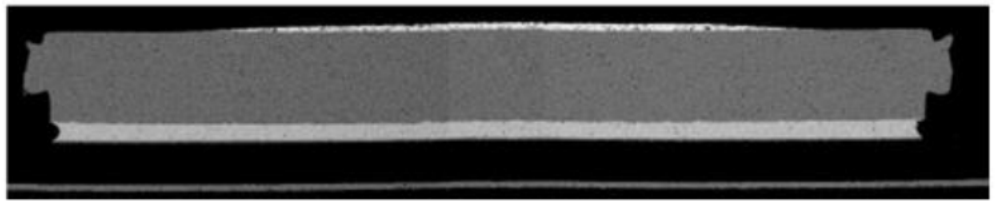


DPAK RESULT FOR: SAC347+Bi/Sb/Ni/Co (ROL0) AIR REFLOW

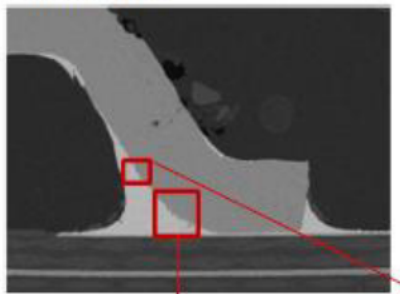
INITIAL



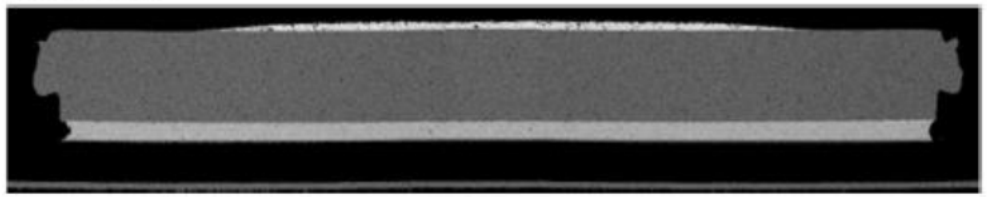
INITIAL



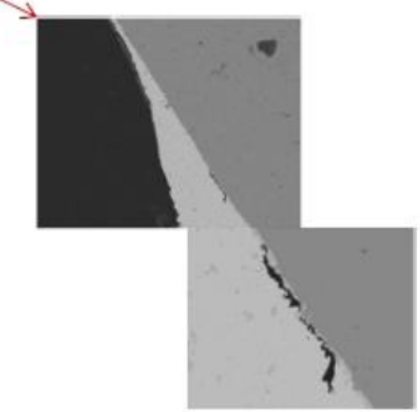
3000 CYCLES

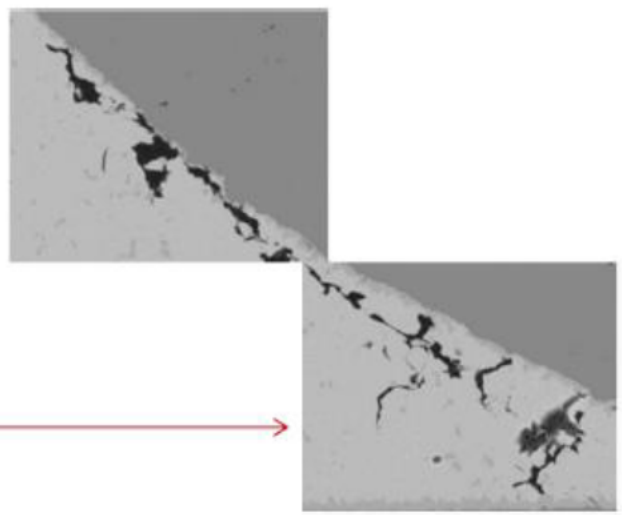


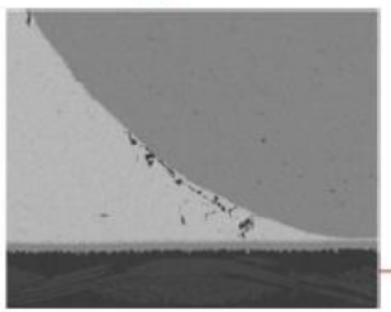
3000 CYCLES



NO CRACK IN CENTER PAD AFTER 3K CYCLES







INTERNAL CRACK AFTER 3K CYCLES

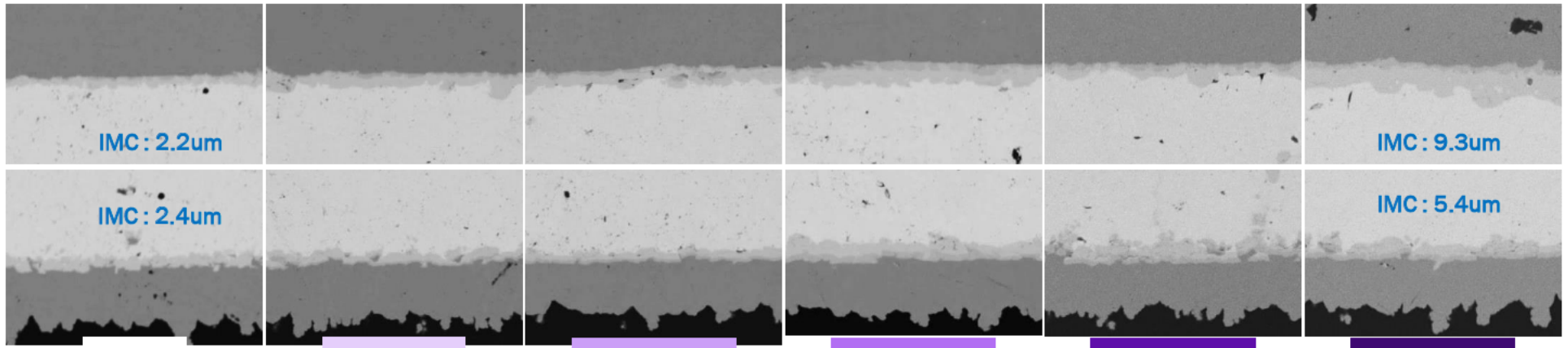
No direct failure relationship with void level, SAC347+ performing better regardless of void %.

CS ANALYSIS AND EVENT DETECTION COMBINED

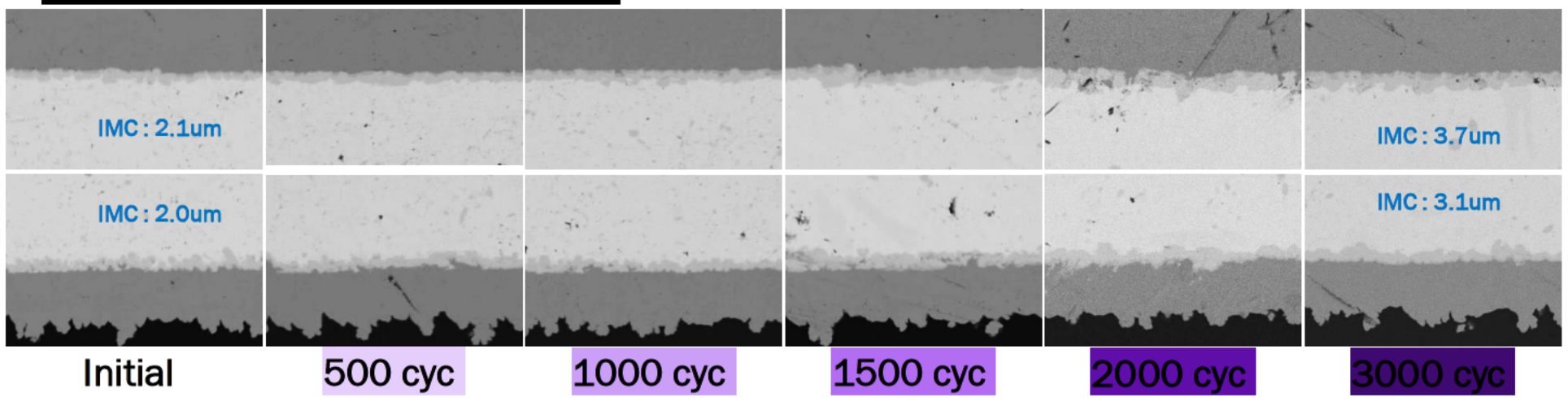
	SAC305						SAC347+Bi/Sb/Ni/Co					
	CS ANALYSIS (I/O'S 1-17 OF QFN)			EVENT DETECTION (ROWS)			CS ANALYSIS (I/O'S 1-17 OF QFN)			EVENT DETECTION (ROWS)		
TEMP CYCLE	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)	ROL0 VACUUM (<0.5% void)	ROL0 AIR (5-20% void)	ROL1 AIR (25-25% void)
INITIAL	0/17	0/17	0/17	0	0	0	0/17	0/17	0/17	0	0	0
500	0/17	1/17	7/17	0	0	0	0/17	0/17	0/17	0	0	0
1000	04/17	3/17	10/17	0	0	0	0/17	0/17	4/17	0	0	0
1500	06/17 [1]	4/17 [2]	5/17 [1]	0	0	0	0/17	1/17	1/17	0	0	0
2000	08/17 [0]	13/17 [2]	11/17 [4]	7	2	1	3/17	2/17	3/17	0	0	0
3000	15/17 [5]	16/17 [5]	16/17 [5]	-	-	-	2/17 [0]	3/17 [0]	5/17 [0]	0	0	0

TCT: -40 ~ 125 Degree Celsius, 30min dwell

SAC305 ROLO vacuum reflow

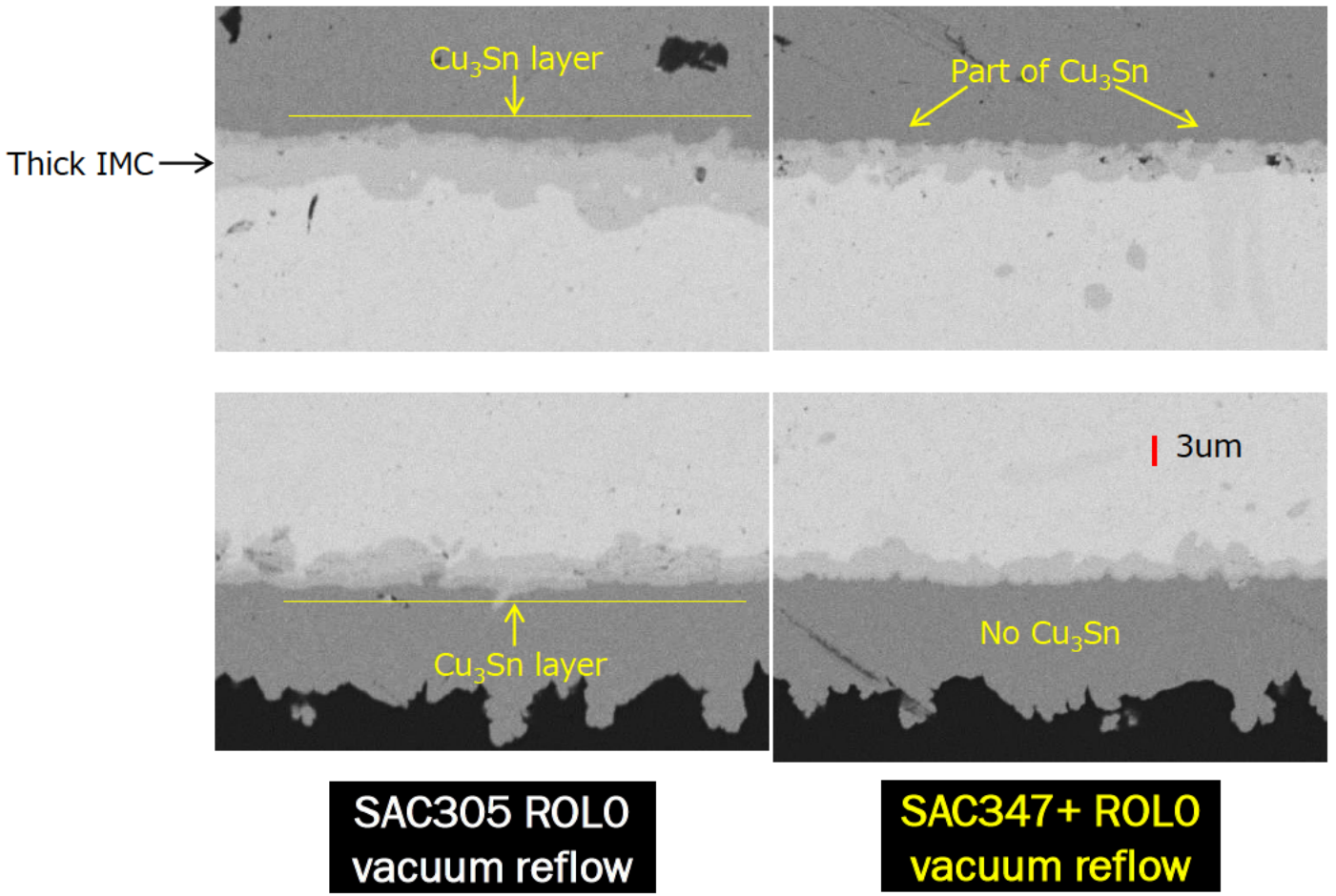


SAC347+ ROLO vacuum reflow



SAC305 IMC growth is faster than SAC347+. Especially Cu_3Sn growth is clear in SAC305

IMC thickness closeup w/ Cu3Sn growth for SAC305



Conclusions

- Testing was performed in order to compare void level content and any relationship to reliability for the SAC305 and the SAC347+ Bi/Sb/Ni/Co alloys.
- For chip components, the void level delta was not significant enough in order to draw a clear conclusion. A clear shear strength benefit was confirmed for the SAC347+ post -40/+125 degC TCT after 3,000 cycles.
- A QFN resistance measurement method to detect operation failures for regions (“sides”) of QFNs during stress testing was developed.
- QFN soldered with SAC305 alloy had failures prior to 2,000 cycles, while SAC347+ fractures were not observed prior to 3,000+ cycles.
- Test results could not find a clear relationship between lower, medium and higher levels of voids and the failure modes targeted via resistance or shear testing.
- Future work to potentially include thermal resistance value measurement, as they may relate to void content and alloy composition.

Acknowledgements

- The authors thank Continental Automotive Deer Park members, including Dr. Stan Rak and Mark Fulcher for material and consultative support.
- Thank you!