Equivalent Capacitance Approach to Obtain Effective Roughness Dielectric Parameters for Copper Foils

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Abstract
Effective Roughness Dielectric (ERD) is a homogeneous lossy dielectric layer of certain thickness with effective (averaged) dielectric parameters. The ERD layer is used to model copper foil roughness in printed circuit board (PCB) interconnects by being placed on a smooth conductor surface to substitute an inhomogeneous transition layer between a conductor and laminate substrate dielectric. This work derives the ERD parameters based on the understanding that there is a gradual variation of concentration of metallic inclusions in the transition layer between the dielectric and foil. The gradual variation can be structured as thin layers that are obtained using the equivalent capacitance approach. The concentration profile is extracted from scanning electron microscopy (SEM) or high-resolution optical microscopy. As the concentration of metallic particles increases along the axis normal to the laminate dielectric and foil boundary, two regions can be discerned: an insulating (pre-percolation) region and a conducting (percolation) region. The rates of increase in effective loss (or corresponding conductivity) in these two regions differ significantly. The proposed model of equivalent capacitance with gradient dielectric is applied to STD, VLP, and HVLP foils. The frequency-dependent dielectric parameters of the homogenized ERD are calculated from the equivalent capacitance. The results are validated using 3D numerical electromagnetic simulations. There are two types of numerical models: with homogeneous ERD parameters, as well as layered. Both models show excellent agreement with measurements.

Introduction
Printed circuit boards (PCBs) used in high-speed digital design are known to have a substantial level of copper foil roughness which compromises signal integrity (SI) and may also cause electromagnetic compatibility (EMC) problems. Therefore, knowledge of the correct parameters of laminate PCB dielectrics refined from any copper foil roughness impact and the proper foil roughness characterization are important constituents of modeling high-speed digital electronics designs, see, *e.g.*, **[1]-[3]** and references therein.

The Effective Roughness Dielectric (ERD)concept was introduced in **[4]-[6]**. ERD is a homogeneous lossy dielectric layer of certain thickness T_r with effective (averaged) dielectric constant DK_r and dissipation factor DF_r. ERD is placed on a smooth conductor surface to substitute an inhomogeneous transition layer between a conductor and laminate substrate dielectric. While the concept is simple, it is physically illuminating, meaningful, and powerful. It has been successfully applied to model conductor (copper foil) roughness in printed circuit boards for signal integrity (SI) and electromagnetic interference (EMI) purposes when designing high-speed digital electronics devices **[7]**, **[8]**. The ERD model has been implemented and tested in a number of numerical electromagnetic modeling tools, see,*e.g.*,**[9], [10]**, **[11], [12]**.

In our previous publications **[6]**, **[13]**, **[14]**, the ERD "design curves", determining the ranges of the DK_r and DF_r parameters for different types of PCB copper foils, were developed. The methodology of generating these "design curves "is based on the following procedures:

- Stripline S-parameter Sweep (S3) technique to measure S-parameters of single-ended comparatively long (~40 cm, or 16 inches) striplines with TRL calibration to remove connector effects **[15], [16]**;
- Scanning Electron Microscopy (SEM) or high-resolution optical microscopy of cross-sections of PCB samples with signal traces and the proper quantification of surface roughness profile parameters **[17]-[19]**;
- Differential Extrapolation Roughness Measurement (DERM) technique **[20]-[22]**; and
- 2D-FEM and/or 3D FIT numerical modeling that allow for accurately fitting the measured S-parameters of the striplines and extract the data for DK_r and $DF_r$of the roughness layers **[4]**,**[6]**, **[13], [14]**. This fitting may include an optimization procedure, *e.g.*, a genetic algorithm, to minimize the discrepancy between the modeled and measured S-parameters.

The "design curves" in the abovementioned papers were generated using SEM and/or optical microscopy to quantify foil roughness. Any designer can use these "design curves" and does not necessarily need to cut a PCB and prepare samples of the lines cross-sections for microscopic inspection. It is sufficient to know which type of foil is used in the PCB under test – this may be standard (STD) foil, VLP (very low profile), RTF (reverse-treated foil), or HVLP (hyper-very low profile)/

SVLP (super-very low profile) foil. Each foil type (group) has some ranges of DK_r, DF_r, and T_r values, and a designer may take average values DK_r, DF_r, and T_r within these ranges for the reasonable estimation of the data which then could be used in modeling of the PCB designs.

Although the "design curves" were developed using fitting between the experimental data and modeling results, it is always desirable to have an analytical model. In this work, the DK_r and DF_r parameters are derived based on the understanding that the transition layer between the dielectric and foil contains gradual variation of concentration of metallic inclusions: from zero concentration in laminate dielectric through some percolation limit to 100% at the smooth copper foil level. The equivalent material parameters of this layered structure can be obtained using equivalent capacitance approach. In the equivalent capacitor the dielectric properties vary gradually according to the concentration profile of metallic particles in the roughness layer. The concentration profile can be obtained from SEM or high-resolution optical microscopy. As concentration of metallic particles increases along the axis normal to the laminate dielectric and foil boundary, two regions can be determined: insulating (pre-percolation) and conducting (percolation). Rates of increase of effective loss (or effective conductivity) in these two regions significantly differ. The proposed model of equivalent capacitance with gradient dielectric has been applied to STD and VLP foils, and the results are validated using 3D numerical electromagnetic simulations.

Description of Equivalent Capacitance Model

A roughness profile on a PCB conductor surface can be tested using optical or SEM microscopy, or a surface profiler. The average contents (volume concentration) of metallic particles in the roughness layer varies as a function of the coordinate z normal to the surface. It can be approximated by an exponential function

$$v_{incl}(z) = a \times \exp(K_1 z), \tag{1}$$

where a and K_1 are the fitting parameters.

Two separate regions of effective roughness dielectric can be considered:

Region I: $0<z<T_p$, where the concentration of metallic inclusions is below the percolation threshold, *i.e.*, where the mixture remains in the dielectric phase; this is the region adjacent to the dielectric matrix of the PCB. Herein, T_p is the distance within the layer at which percolation is reached.

Region II: $T_p<z<T$, where the concentration of metallic inclusions is higher than the percolation threshold; this is the region adjacent to the smooth foil level and is conducting. Herein, T is the entire thickness of ERD layer. It includes

$$T = T_p + \Delta T, \tag{2}$$

where ΔT is the thickness of the region above the percolation.

The concentration v_p, at which percolation will occur for the metallic particles in the roughness dielectric layer, can be obtained empirically, *i.e.*, estimated from the microscopy pictures, or from the profiler data. By solving the equation

$$v_p = a \times \exp(K_1 T_p) \tag{3}$$

with respect to T_p, one can get the height of the dielectric phase of ERD.

First, let us consider the region $0<z<T_p$. This is the dielectric layer with relative permittivity varying according to the profile function (1) from the matrix dielectric properties ε_m (at z=0) to the final pre-percolation value ε_p (at $z=T_p$). Since dielectric function varies with z as

$$\varepsilon(z) = \varepsilon_m v_{incl}(z), \tag{4}$$

The effective permittivity of such a layer can be calculated through the equivalent partial layered capacitor consisting of series connection of sublayer capacitors. The capacitance of the resultant capacitor with variable properties of the dielectric is

$$C = C_0 d / \int_0^d dz/(1+\varepsilon(z)), \tag{5}$$

Where C_0 is the capacitance of the corresponding air-filled rectangular parallel-plate capacitor of thickness d.Herein, $d = T_p$.

The effective dielectric properties of such dielectric layer can be easily derived from (5) as

$$\varepsilon_d = T_p / \int_0^{T_p} dz/(\varepsilon_m(1 + v_{incl}(z))). \quad (6)$$

This permittivity is complex,

$$\varepsilon_d = \varepsilon_d{}' - j\varepsilon_d{}'. \quad (7)$$

If the imaginary part is represented through the equivalent conductivity, the corresponding equivalent conductivity is

$$\sigma_d = -\omega\varepsilon_0\varepsilon_d{}'. \quad (8)$$

This conductivity will not be high, because it is coming from a lossy effective roughness dielectric in the dielectric phase. Its value ison the order of 10^{-2} S, which is similar to a comparatively lossy dielectric.

However, in Region II, the conductivity increases exponentially towards smooth copper level until it reaches the conductivity of the pure copper used on a PCB. Therefore,

$$\sigma_p = \sigma_d \times e^{K_2 T}, \quad (9)$$

where K_2 is the exponent parameter for conductivity after percolation, and it can be solved from the equation, when σ_p reaches the level at the beginning of percolation, *e.g.*, $\sigma_p = 0.01\,\sigma_{Cu}$. Percolation threshold is assumed to be 25% of volume concentration of metallic inclusions in the epoxy-resin fiber-filled dielectric matrix. As a reminder, *T* is the entire thickness of the ERD layer.

Then the conductivity profile function with respect to the coordinate *z* will be

$$\sigma(z) = \sigma_d \times e^{K_2 z}. \quad (10)$$

The dielectric profile function in the second conducting layer will be defined as

$$\varepsilon_p(z) = \varepsilon_d + \frac{\sigma_d}{j\omega\varepsilon_0} \times e^{K_2 z}. \quad (11)$$

The effective permittivity of the two lossy dielectric layers is calculated through the equivalent capacitor containing two capacitors in series. Both capacitors have gradient fillers. The filler of the first layer is in the non-conducting dielectric phase, and the other is close to percolation, *i.e.*, conducting phase.

$$\varepsilon_{eff} = T/(\int_0^{T_p} dz/(\varepsilon_m(1 + v_{incl}(z)) + \int_{T_p}^{T} dz/(\varepsilon_p(1 + v_{incl}(z))))). \quad (12)$$

From (12), separating real and imaginary parts, the following ERD parameters can be calculated: $DK_r = \varepsilon_{eff}{}'$ and $DF_r = \tan\delta_{eff} = \varepsilon_{eff}{}''/\varepsilon_{eff}{}'$.

Metal Inclusion Profiles in Different Foils

Cross-sectional microscopic (SEM or optical) analysis is used to characterize roughness profile of the foil. For this purpose, typically a signal trace is cut perpendicular to the direction of the electromagnetic wave propagation. The procedure of image processing is described in detail in **[17]-[19]**. An example of a binary (black-and-white) image of the trace cross-section of VLP foil on PPO Blend substrate is shown in **Figure 1**. The bottom ("foil", or "matte") side of this foil is rougher that the

top ("oxide", or "drum") side.

Figure 1 – Binary Image of the Cross-section of the Signal Trace of Black Oxide VLP Foil on PPO Blend Substrate

The surface roughness profile can be extracted and then quantified using digital image processing based on the analysis of pixels**[16]**. The average peak-to-valley magnitude of the roughness profile corresponding to the bottom of **Figure 1**is shown in **Figure 2**.

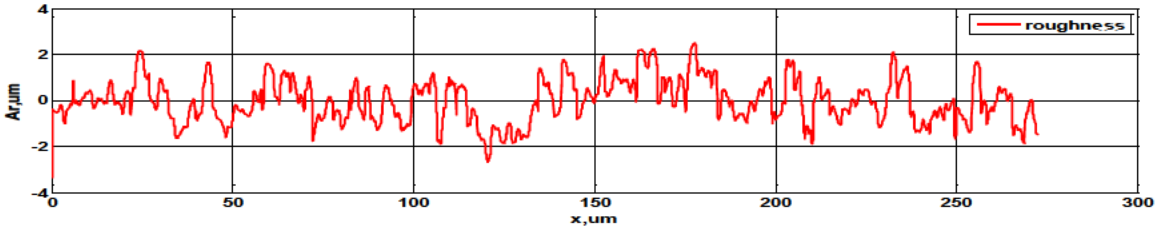


Figure 2 – An Example of Foil Roughness Profile Extracted from the Bottom Side of the Binary Image

Foil surface roughness has the stochastic nature, therefore, along with peak-to-valley values, it can be characterized it in terms of the probability density function (PDF) and autocorrelation function (ACR). Corresponding PDF and ACR curves for VLP foil type are presented in **Figure 3**. The PDF shows that copper foil surface roughness has normal (Gaussian) distribution, and from ACR it is clearly seen that the roughness is uncorrelated and does not contain any periodicity.

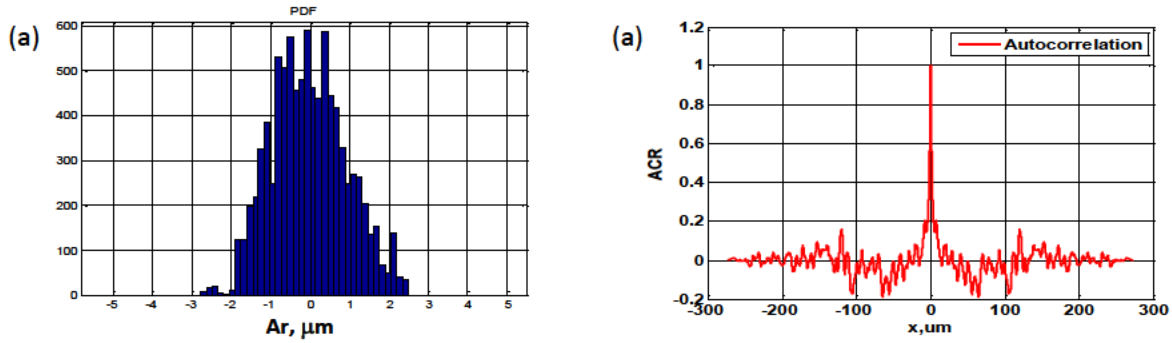


Figure 3 – Probability Density Function Histogram (a) and Autocorrelation Function (b) Corresponding to Roughness Profile in Figure 2

In many cases (though not always),surface roughness is isotropic, *i.e.*, the PDF is invariant with respect to any direction of the wave propagation. Since the parameters of PDF can be obtained from the profile, the roughness 3D profile can be reconstructed for the future investigation using, for example, Gaussian filter, or any other low-pass filter widely used in digital image processing. The parameters of this filter should be adjusted to get the best correlation with the measured roughness profile **[23]**.

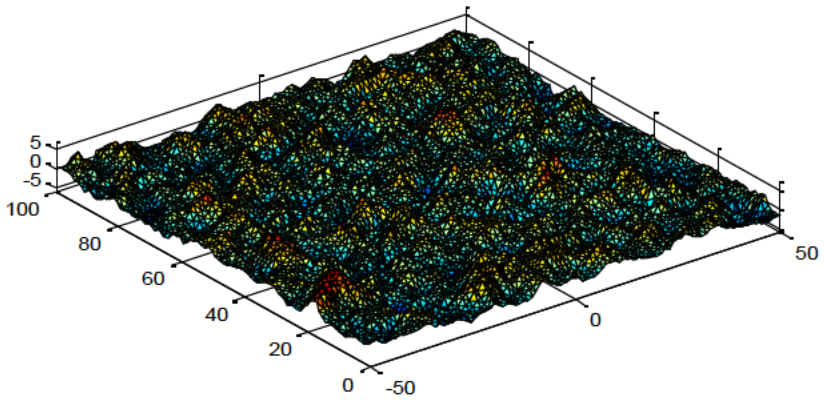


Figure 4 –3D Roughness Profile Surface Generated Using PDF and Gaussian Filter

The PDF and ACR of the generated 3D roughness profile shown in **Figure 4** agree well with those shown in **Figure 3**. The 3D generated roughness profiles are useful for roughness quantification, *e.g.*, as in **[19]**, **[22]**, including ERD "design curves" **[6]**, as well as for metallic concentration variation study needed for equivalent capacitance approach.

Applying the same image processing technique as for the roughness magnitude extraction, but performing summation for each column of pixels, one can get the volume concentration of metallic inclusions in the transition between pure dielectric to pure metal. **Figure 5** shows the function $v_{incl}(z)$for different types of foils. It is seen that 0% concentration corresponds to dielectric matrix, while 100% to smooth copper. The transitions are comparatively smooth – the left-hand front corresponds to the "foil" side, and the right-hand side to the "oxide" side. The smoother the conductor side, the more abrupt the metallic concentration slope is.

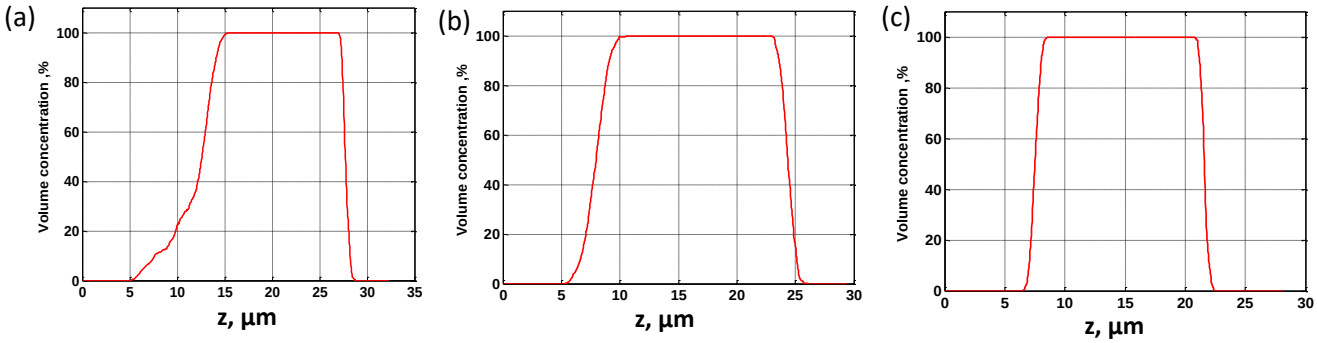
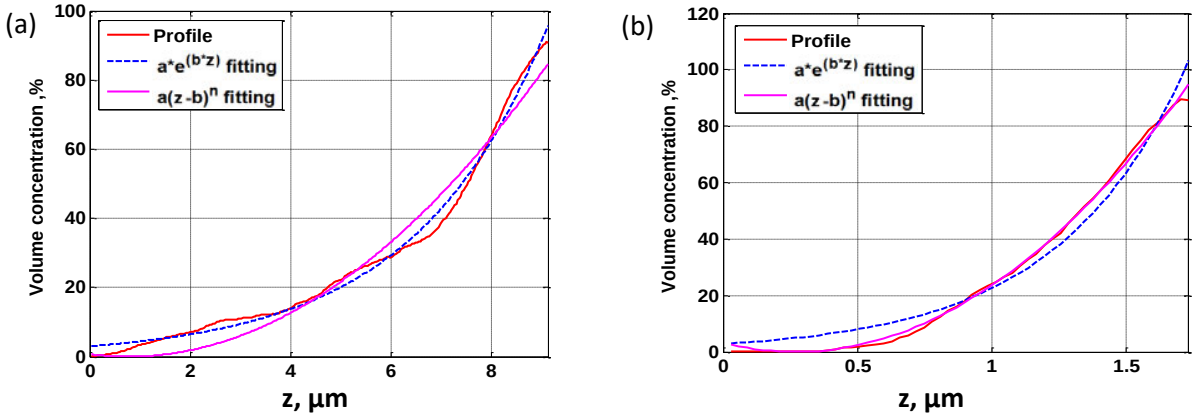


Figure 5 – Volume Concentration of Metallic Inclusions in Black Oxide STD(a), VLP(b), and HVLP (c)Foil on PPO Blend Substrate

The profiles on the "foil" and "oxide" sides can be fitted using exponential or polynomial functions as is shown in **Figures 6-8**.For simplicity of calculating integrals analytically in (5), (6), and (12), the exponential approximationae^{bz}will be further used. Note that the parameter *b* herein is the same as K_1 in (1). The approximation data for a number of studied samples of black-oxide foils on PPO Blend substrates are presented in **Table 1**. The parameter δrms herein is the root-mean-square error



at the approximation.

Figure 6 – Approximation of Volume Concentration of Metallic Inclusions as a Function of Distance from the Smooth Conductor: "Foil" Side (a) and "Oxide" Side (b) on STD Foil

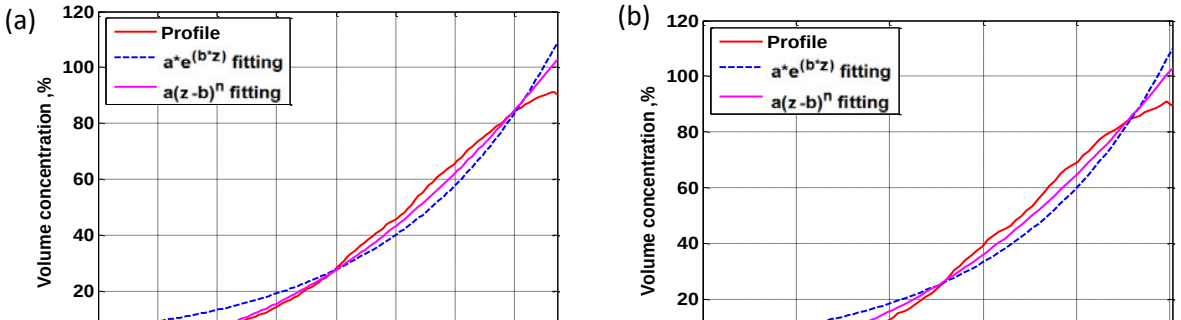


Figure 7– Approximation of Volume Concentration of Metallic Inclusions as a Function of Distance from the Smooth Conductor: "Foil" Side (a) and "Oxide" Side (b) on VLP Foil

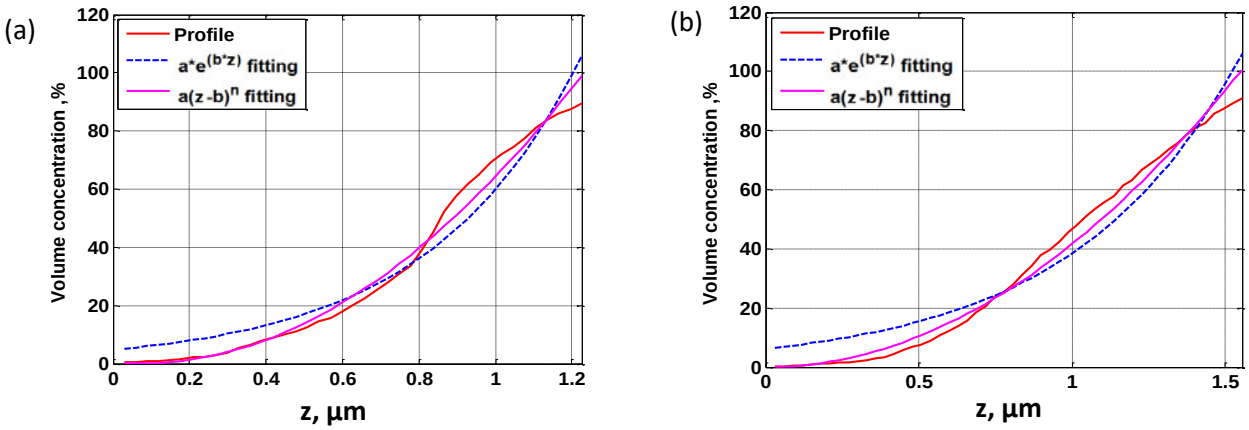


Figure 8 – Approximation of Volume Concentration of Metallic Inclusions as a Function of Distance from the Smooth Conductor: "Foil" Side (a) and "Oxide" Side (b) on HVLP Foil

Table 1. Exponential Approximation of Profile Functions on "Foil" and "Oxide" Sides of Copper Foils

Foil type / Model		$f(z) = ae^{b \cdot z}$ Coefficients (with 95% confidence bounds):
STD	"Foil" side	*a*= 3.03 (2.91, 3.15), *b*= 0.3787 (0.3737, 0.3837), δrms=2.0962
	"Oxide" side	*a*= 2.829 (2.233, 3.425), *b*= 2.075 (1.937, 2.213), δrms= 4.9168
VLP	"Foil" side	*a*= 5.991 (5.253, 6.73), *b*= 0.7479 (0.7103, 0.7855), δrms=6.1539
	"Oxide" side	*a*= 5.665 (4.518, 6.812), *b*= 1.18 (1.086, 1.275), δrms= 8.0289
HVLP	"Foil" side	*a*= 5.537 (3.922, 7.152), *b*= 2.182 (1.936, 2.428), δrms =8.4887
	"Oxide" side	*a*= 6.193 (4.762, 7.624), *b*= 1.827 (1.653, 2.001), δrms = 7.3620

Calculation of ERD Parameters Using the Proposed Analytical Model

The proposed equivalent capacitance model was applied to calculate the ERD parameters of the three types of foils as in **Table 1**. **Figures 9-11** show the calculated frequency dependences for DK_r and DF_r of the corresponding ERD layers.The thicknesses of the layers are also determined from the metallic concentration profiles. Note that in the previous publications**[4]**, **[6]**, **[13]**, **[14]**, the ERD parameters were independent of frequency. However, the new analytical model shows that there is frequency dependence. The ERD parameters for the STD foil on its "foil" and "oxide" sides differ significantly because the "foil" side is much rougher than the "oxide" side. The corresponding differences for the sides on the VLP and HVLP foils do not differ that much, though they are not equal. Though the extracted ERD parameters for the VLP foil herein are close to those of the HVLP, the thicknesses of the layers to be modeled differ: the HVLP layers are thinner than VLP. Note that the calculated ERD results are not the same as reported in **[10]**, because the test samples studied herein are different from those in **[13]**. In the present study, the roughness parameters of HVLP and VLP samples are not much different, while in **[13]** the VLP and HVLP foils are quite distinct.

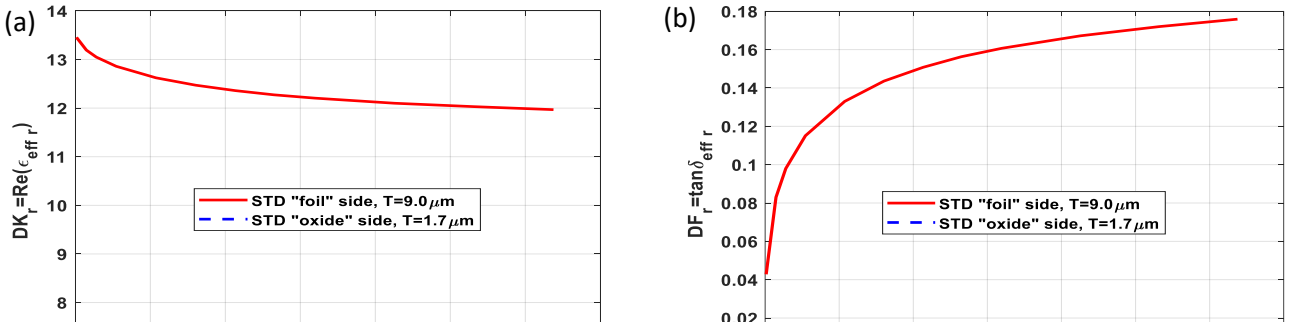


Figure 9 – Effective Roughness Dielectric Parameters as Functions of Frequency for STD Foil: DK_r (a) and DF_r (b)

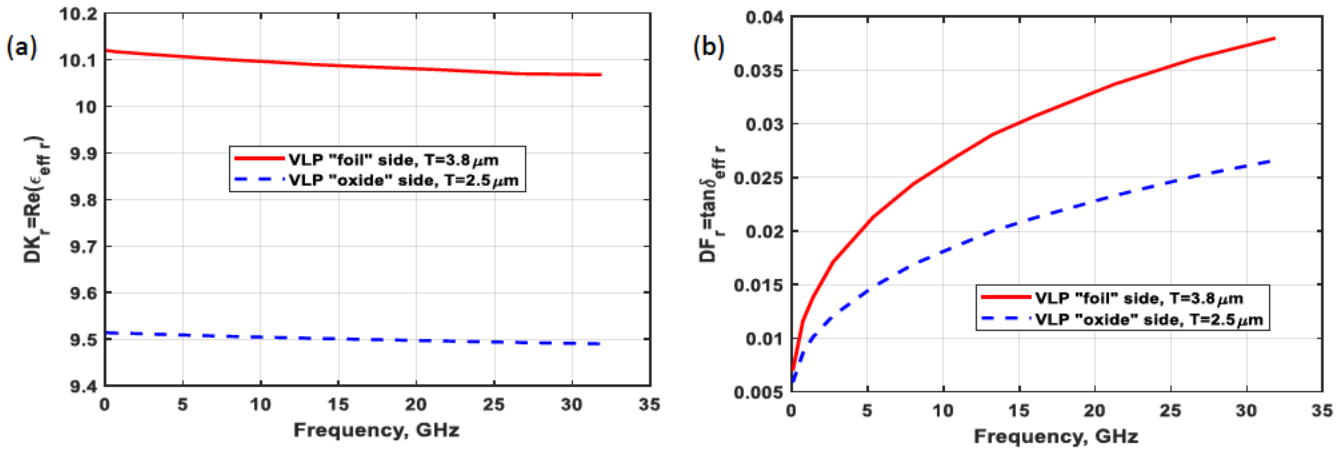


Figure 10 – Effective Roughness Dielectric Parameters as Functions of Frequency for VLP Foil: DK_r (a) and DF_r (b)

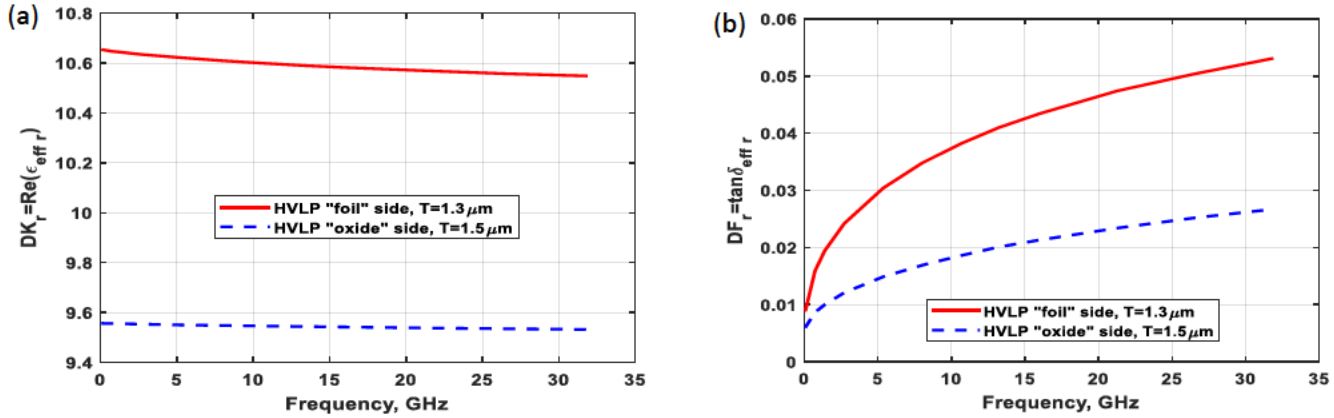


Figure 11 – Effective Roughness Dielectric Parameters as Functions of Frequency for HVLP Foil: DK_r (a) and DF_r (b)

Numerical Simulations Based on Analytically Calculated ERD

The measured insertion loss $|S_{21}|$, dB and time delay τ on a transmission line, *i.e.*, a single-ended stripline, increase as conductor roughness magnitude increases, and hence, the values DK_r and DF_r of the corresponding ERD layers increase. This is illustrated by **Figure 12.**

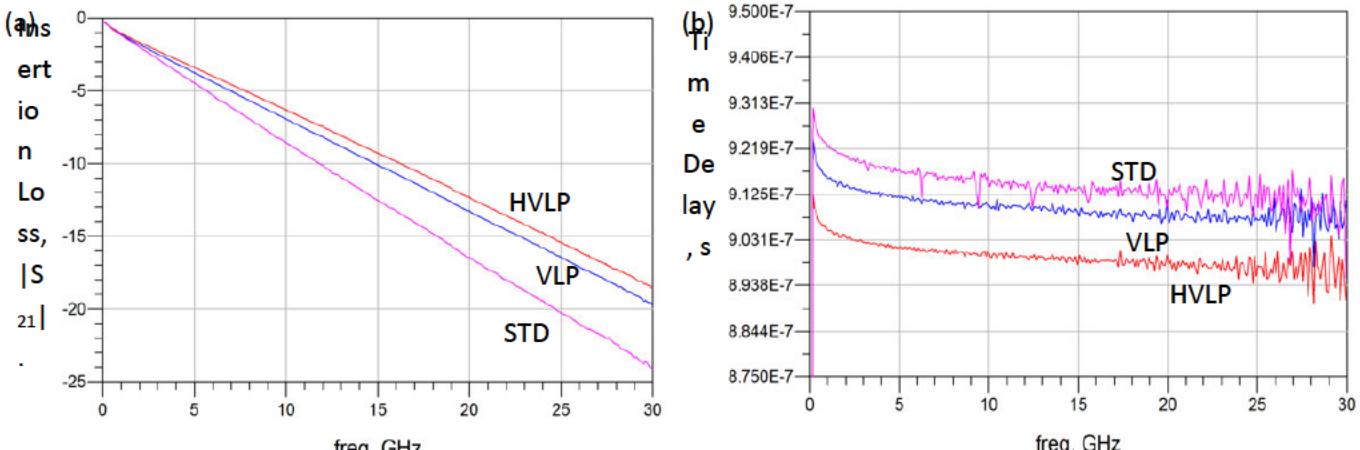


Figure 12 – Insertion Loss (a) and Time Delay (b) on 16-inch Stripline with PPO Blend Dielectric and Different Foil Types

The delay time increase as conductor roughness increases is the direct consequence of the capacitive (dielectric) nature of the ERD. Since phase progression in a TEM transmission line of the length *l*and with the homogeneous dielectric filling $\varepsilon_r$is **[24]**

$$\varphi = \beta l = 2\pi f l\sqrt{\mu_0\varepsilon_0}\sqrt{\varepsilon_r}, \tag{13}$$

the corresponding time delay is calculated as

$$\tau = \frac{\partial\varphi}{\partial f} = \frac{2\pi l}{c}\sqrt{\varepsilon_r}. \tag{14}$$

The corresponding insertion loss on the line is approximately

$$|S_{21}|, dB = -8.686\alpha l, \tag{15}$$

where the total loss constant α for the TEM mode on the line is comprised of the conductor and dielectric loss parts**[24]**,

$$\alpha = \alpha_C + \alpha_D, \tag{16}$$

and

$$\alpha_D = \frac{\omega}{c} tan\delta\sqrt{\varepsilon_r}. \tag{17}$$

Note that hereinε_r is the dielectric constant (real part of permittivity) of the effective dielectric inside the transmission line, which includes both the substrate dielectric matrix and ERD.

Model Setup for Numerical Simulations

Similar to the previous studies **[13],** the stripline simulation numerical electromagnetic model has been created. It includes the dielectric matrix material characterization of the substrate dielectric obtained through the extrapolation DERM technique as in **[20]**, **[22]**,and thin layer-like objects representing conductor surface roughness as the ERD: above the trace ("foil" side) and below the trace ("oxide" side). The corresponding ERD layers are also placed on the reference (ground/return) planes. **Figure 13** shows a cross-sectional view of the numerical model setup. The line length of the stripline structure was 391.414 mm (15.4 inches); stripline traces were 17.5 µm thick (0.5-oz copper) and 340 µm (13.5 mil) wide. The impedance of the single-ended line was 50 Ohms. Cross-sectional dimensions for all the three test lines were identical, except for the foil roughness.

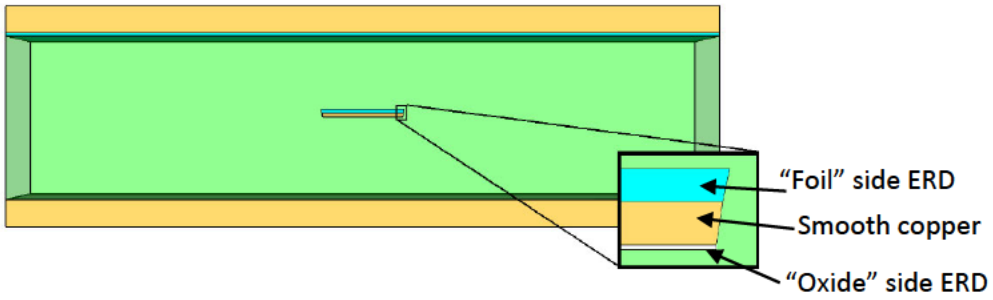


Figure 13 – Numerical Model Setup

Numerical Simulations Results with Homogenized Frequency-dependent ERD.

The models were simulated using the Finite Integral Technique (FIT), a time domain solver**[9]**. Time domain solvers are suited to capturing phase results across wide frequency bands. A mesh size in the models was about 2 million cells. The waveguide ports were used for excitation. The measured and modeled data are shown in **Figures 14-16**. The dielectric parameters of the homogeneous ERD layers in these models are as shown in **Figures 9-11**. The agreement of the modeled and measured results for all the three test scenarios with STD, VLP, and HVLP foils validate the proposed analytical approach.

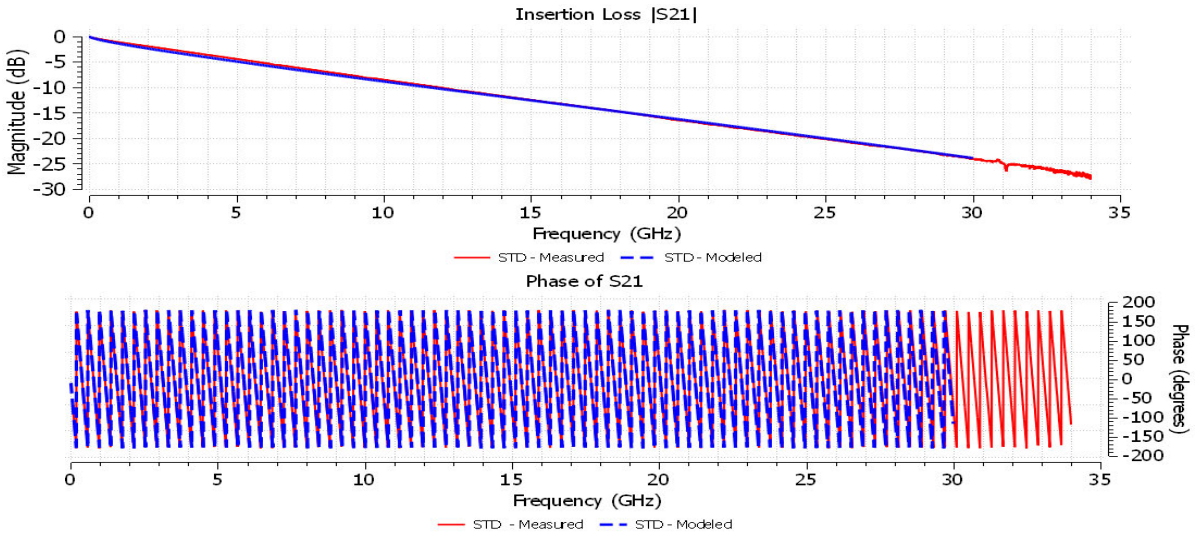


Figure 14 – Measured and Modeled S_{21}Results for a Stripline Structure with STD Foil

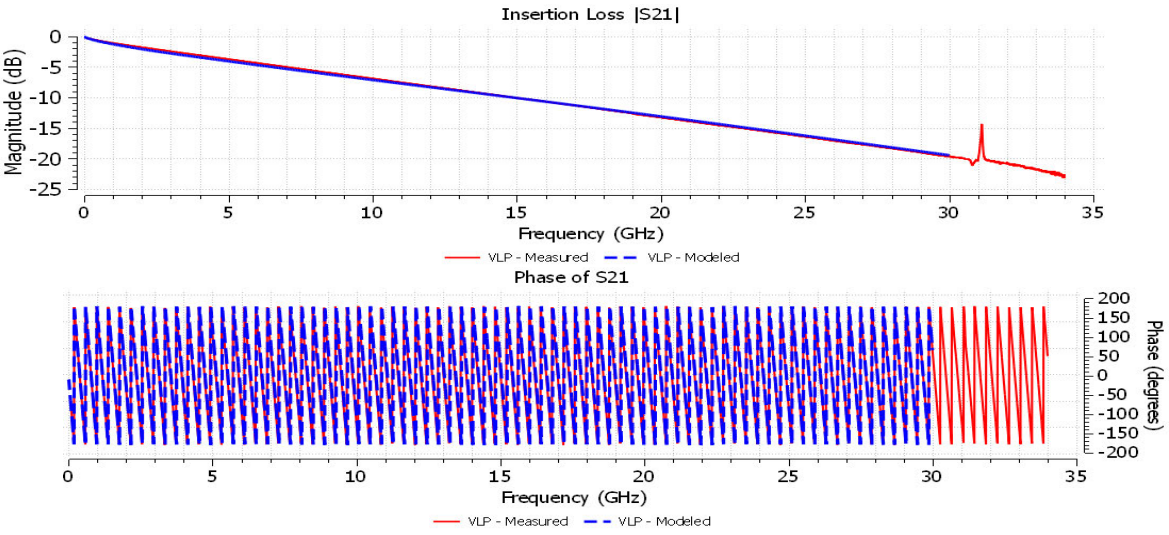


Figure 15 – Measured and Modeled S_{21}Results for a Stripline Structure with VLP Foil

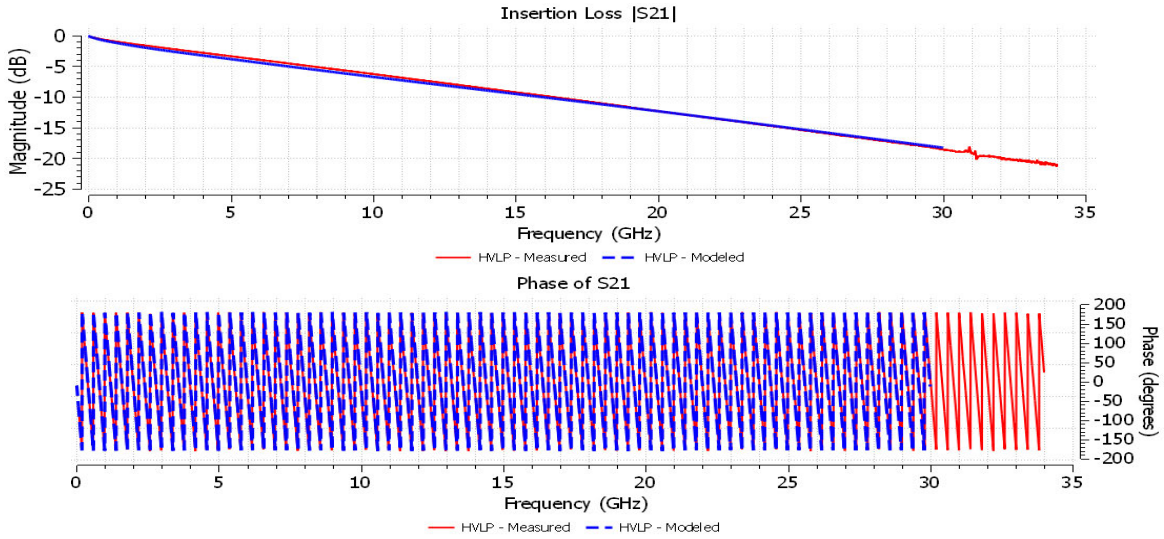


Figure 16 – Measured and Modeled S_{21}Results for a Stripline Structure with HVLP Foil

Numerical Model of Layered ERD Structure

Another way of roughness dielectric numerical modeling was also tested. The"layered" model was set up in the same way as the other models with the only one difference. The foil layer is specified differently from the previous models with homogeneous ERD parameters. In the "layered" model for the STD foil, the roughness dielectric properties are split into three parts: the top 1/3rdpart (close to metal) has DK_r = 16, the middle 1/3rdpart has DK_r= 12, and bottom 1/3rdpart (next to matrix) has DK_r =8. In this case, each layer is very thin, adding significant mesh count and therefore increasing simulation time.

However, herein, when space mapping for the "layered" model is applied, the object is not split into three separate layers/objects with homogeneous dielectric constants, but the object material properties change depending on the position within the object according to the specified "space map". Note that a "space map" based model does not introduce a new kind of material, but is used to define, for a normal (or anisotropic) material, a generic spatial distribution. This allows for modeling complicated and arbitrary materials. In this work, the ERD itself is specified this way within the matrix material.

In **Figure 17**, the measured phase is compared to the modeled using "space map" of the ERD layer. The tested cases are the dielectric constants of all three ERD sublayers having first DK_r=12; then all of them having DK_r =16; and finally, the "layered "roughness dielectric "space map" object with three different DK_r values defined consequently. Loss tangent DF_r=0.17 in all the layers. Phase results are chosen for comparison because they are the most sensitive to the model parameters choice. As **Figure 17**shows, there is an excellent agreement between the measured and the layered model results. From **Table 2**, the difference between these two results is indeed small (within a few degrees) when compared to the overall phase.

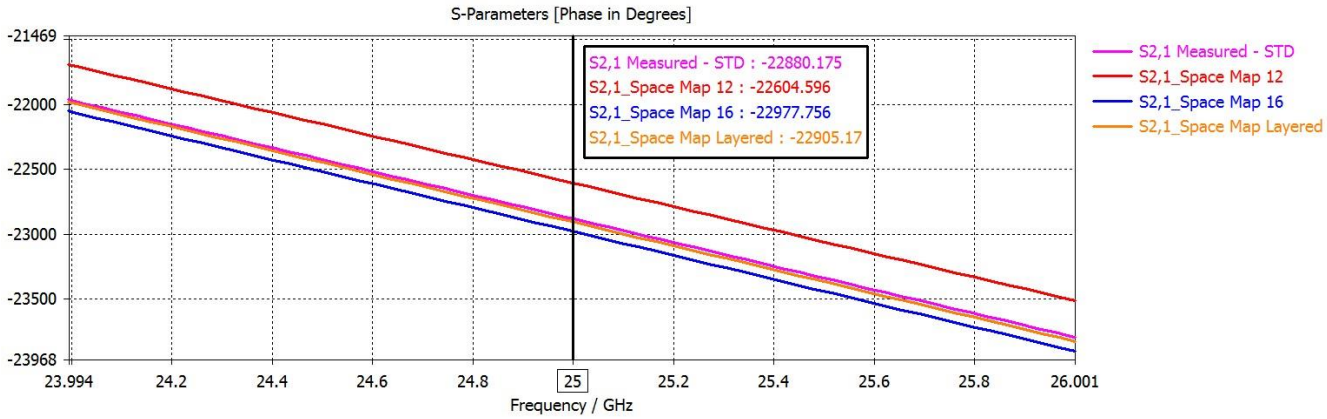


Figure 17 – The Phase of Measured and Modeled Structures Over a Narrow Frequency Band of ~24-26GHz: ERD withDKr=12, with DKr=16, and with Space Map Layered Structure

Table 2. Phase of Analytical and Layered ERD Model at a Number of Frequencies

Discrete Frequencies	Phase, degrees (modeled with DK_r=12)	Phase, degrees (modeled with DK_r=16)	Phase, degrees (modeled as layered)	Phase, degrees (measured)
f=7 GHz	-6334.4757	-6442.2698	-6426.1821	-6436.3764
Difference as compared to measured	101.9007	-5.8934	10.1943	0
f=15 GHz	-13563.894	-13790.774	-13752.316	-13753.362
Difference as compared to measured	189.468	-38.46	1.046	0
f=20 GHz	-18080.365	-18380.305	-18325.425	-18318.775
Difference as compared to measured	238.41	-61.53	-6.65	0
f=25 GHz	-22604.596	-22977.756	-22905.17	-22880.175
Difference as compared to measured	275.579	-97.581	-24.995	0
f=30GHz	-27127.231	-27573.701	-27482.865	-27435.057
Difference as compared to measured	307.826	-138.644	-47.808	0
f=34GHz	-30755.643	-31262.769	-31156.153	-31078.478
Difference as compared to measured	322.835	-184.291	-77.675	0

Conclusions

In this work, an analytical model to calculate effective roughness dielectric (ERD) parameters for conductor surface roughness of a PCB foil is presented. Based on the microscopic analysis of the roughness profile, a concentration dependence of metallic inclusions in the transition between the ambient dielectric matrix and copperis obtained. Using such a concentration dependence, the equivalent capacitance associated with the roughness layer is calculated analytically. Then the parameters of the effective roughness dielectric are extracted from this equivalent capacitance. The ERD parameters obtained from the analytical model are frequency dependent unlike in the previous works; therefore, they describe the high-frequency behavior (at data rates of a few dozen Gbps) of PCB interconnects more accurately than the frequency-independent models. The proposed model is applied to three stripline test scenarios with three different types of foils - STD, VLP, and HVLP, and is validated by an excellent agreement between the full-wave FIT numerical modeling and measurements. Two types of numerical models are obtained: using homogeneous effective roughness dielectric and using space mapping when modeling a "layered" ERD. The "layered" ERD provides the closest to the measured result when S_{21}phases are compared.

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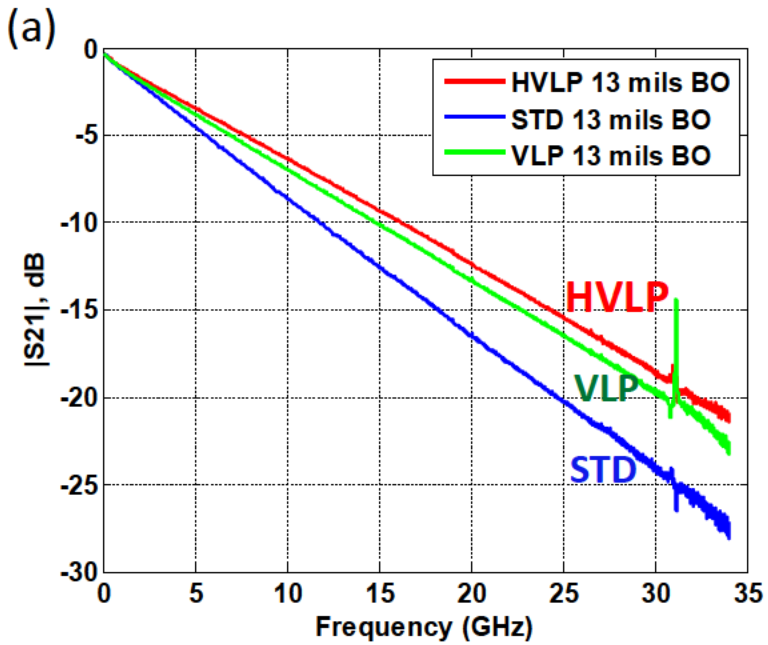
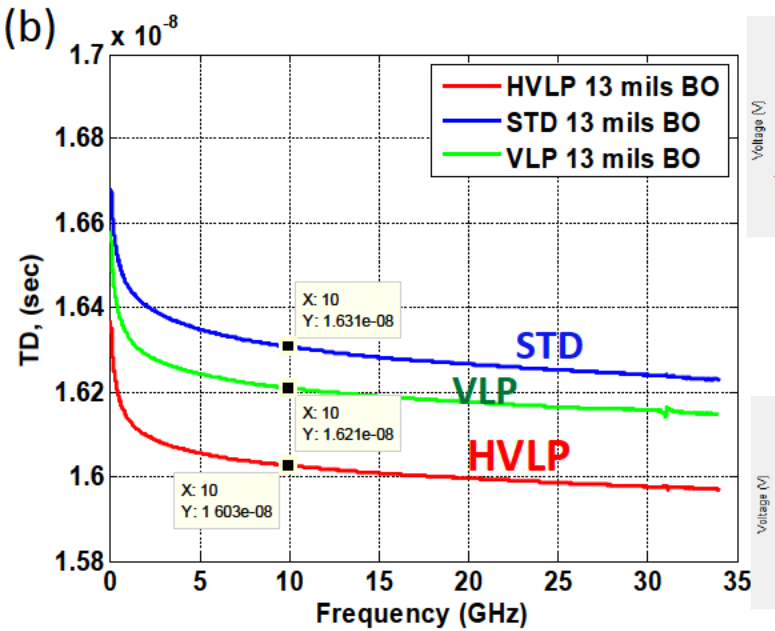
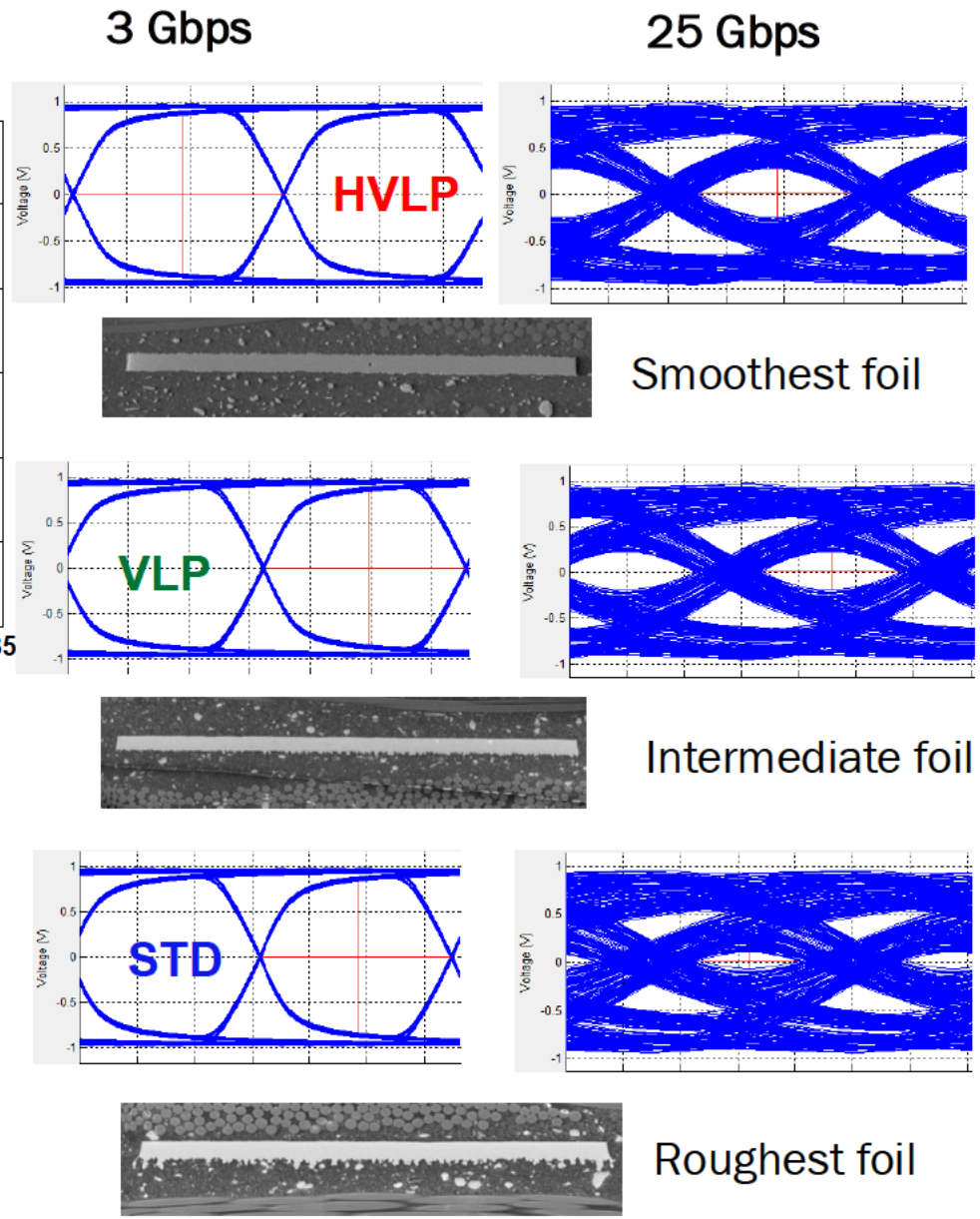
Equivalent Capacitance Approach to Obtain Effective Roughness Dielectric Parameters for Copper Foils

Marina Koledintseva(Oracle, USA)
&
Tracey Vincent (CST of America)

Introduction and Motivation





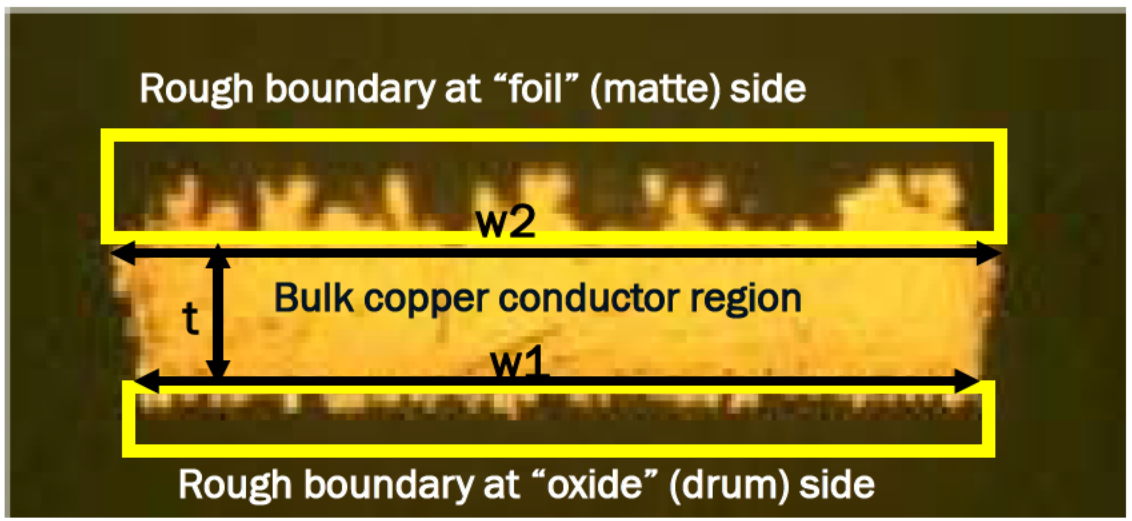


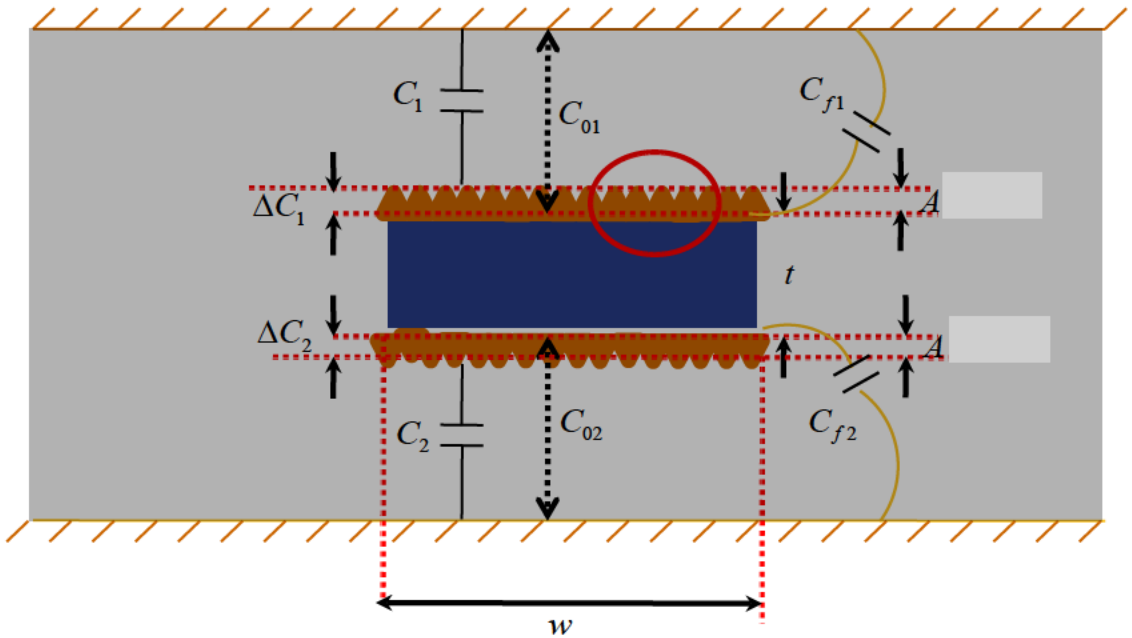
- Copper foil roughness affects SI by increasing loss and time delay on PCB interconnects and causes eye diagram closure, especially as frequencies go up.
- Copper foil roughness may affect EMC as well by increasing mode conversion in imbalanced differential lines.
- Adequate modeling of roughness is important. Analytical mode is desirable.

Capacitive Effect of Copper Roughness

- Per-unit-length C and G parameters increase with roughness.
- Slope of insertion loss as a function of frequency linearly increases with roughness.
- Group delay increases with roughness.

Similar behavior of roughness as a lossy dielectric!

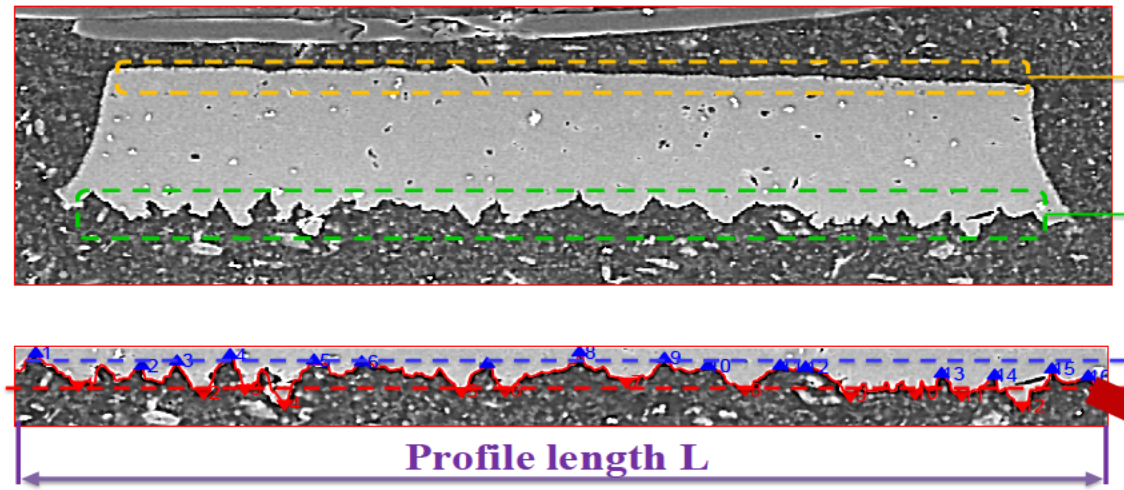




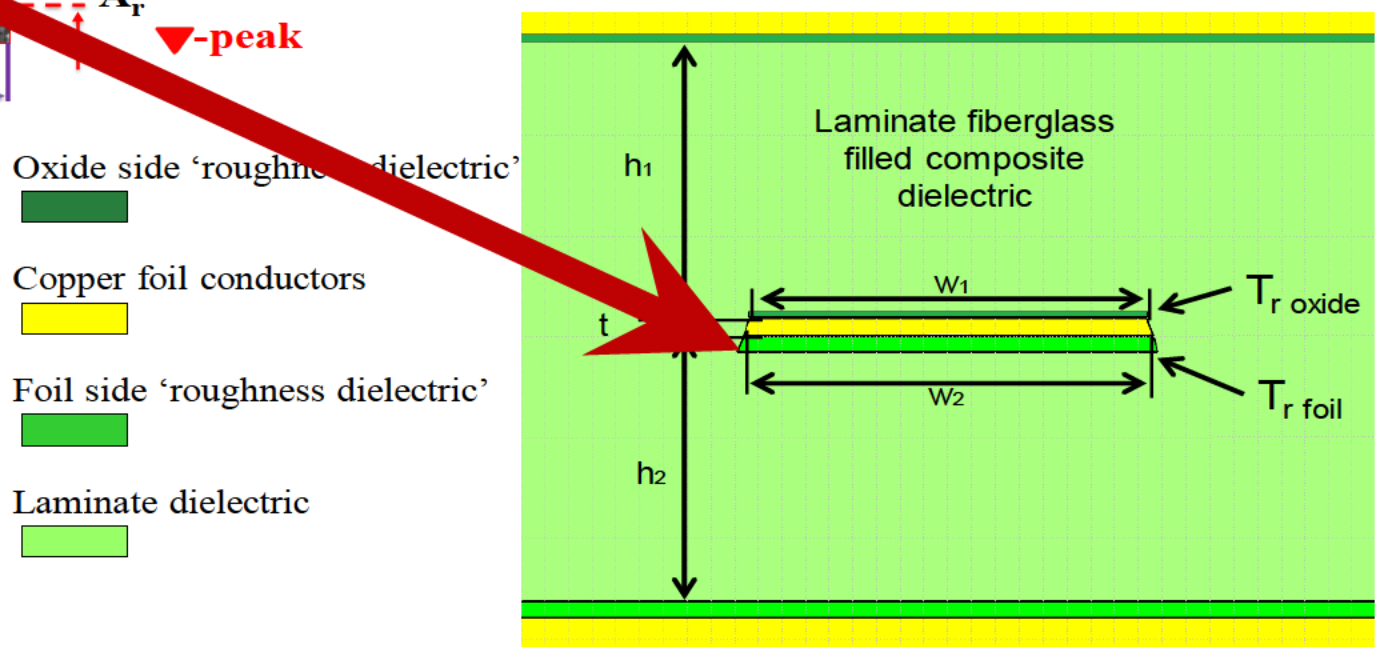
Metallic inclusions in the composite roughness layer are not as conductive as copper!

=> All these factors suggest that copper foil roughness may be substituted by a homogeneous layer of Effective Roughness Dielectric (ERD)

Effective Roughness Dielectric Approach



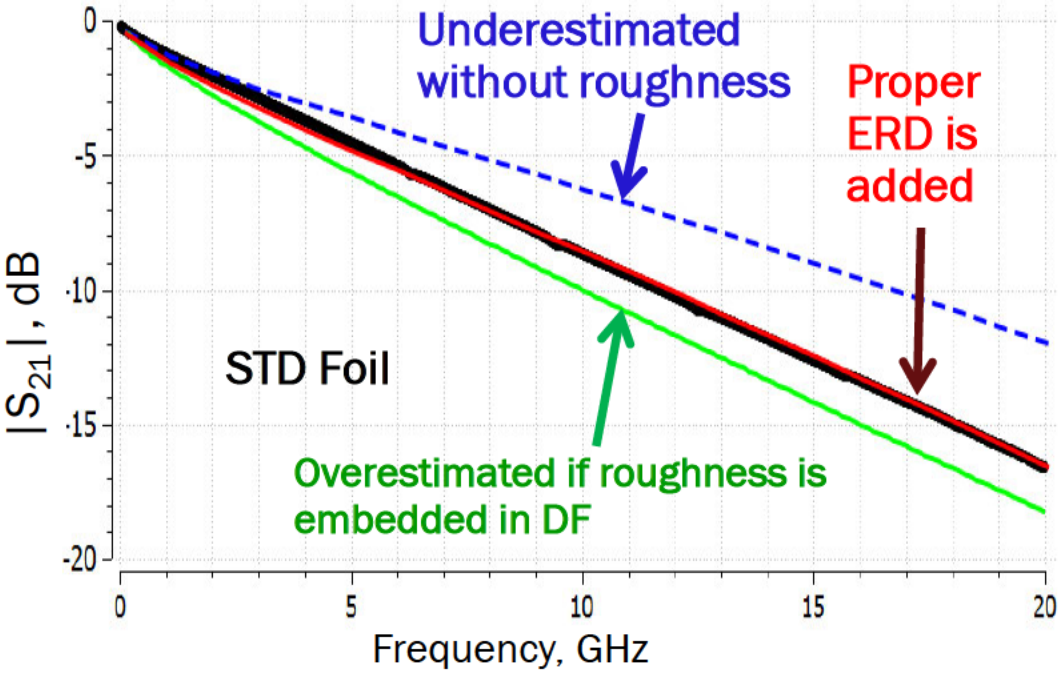
The idea is to substitute inhomogeneous transition layer between copper and dielectric by flat homogeneous layer of effective roughness dielectric (ERD)

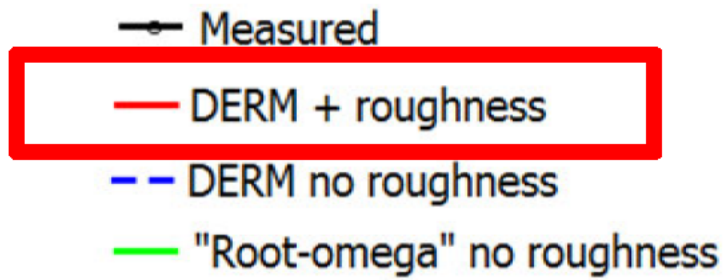


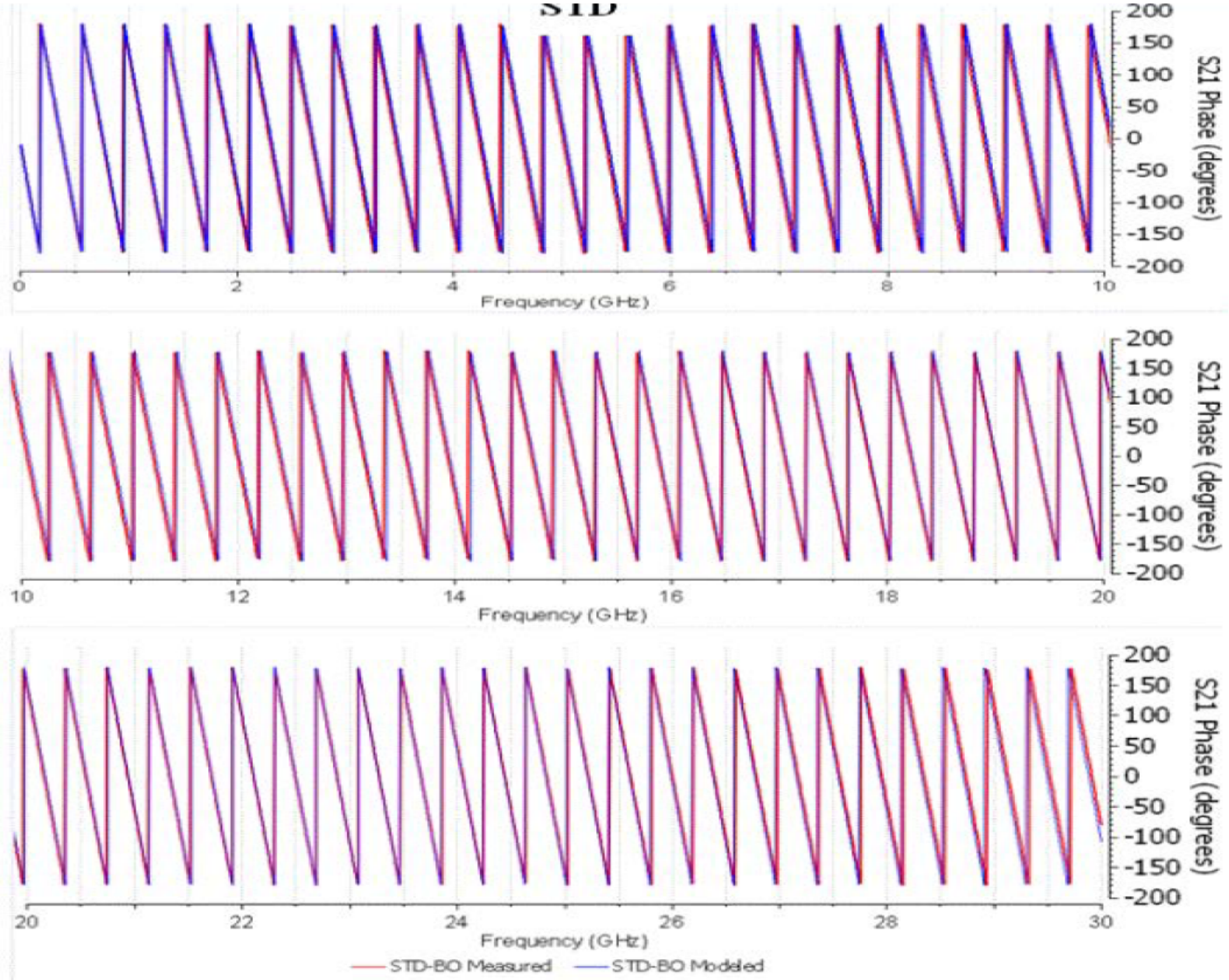
Initial Publication/Reference on ERD: *M.Y. Koledintseva, A. Razmadze, A. Gafarov, S. De, S. Hinaga, and J.L. Drewniak, "PCB conductor surface roughness as a layer with effective material parameters", IEEE Symp. Electromag. Compat., Pittsburg, PA, 2012, pp. 138- 142.*

- Laminate dielectric parameters are extracted from DERM2 (for both α and β).
- Heights of ERD $T_{r\ oxide}$ and $T_{r\ foil}$ are taken as $2A_{r\ oxide}$ and $2A_{r\ foil}$, respectively.

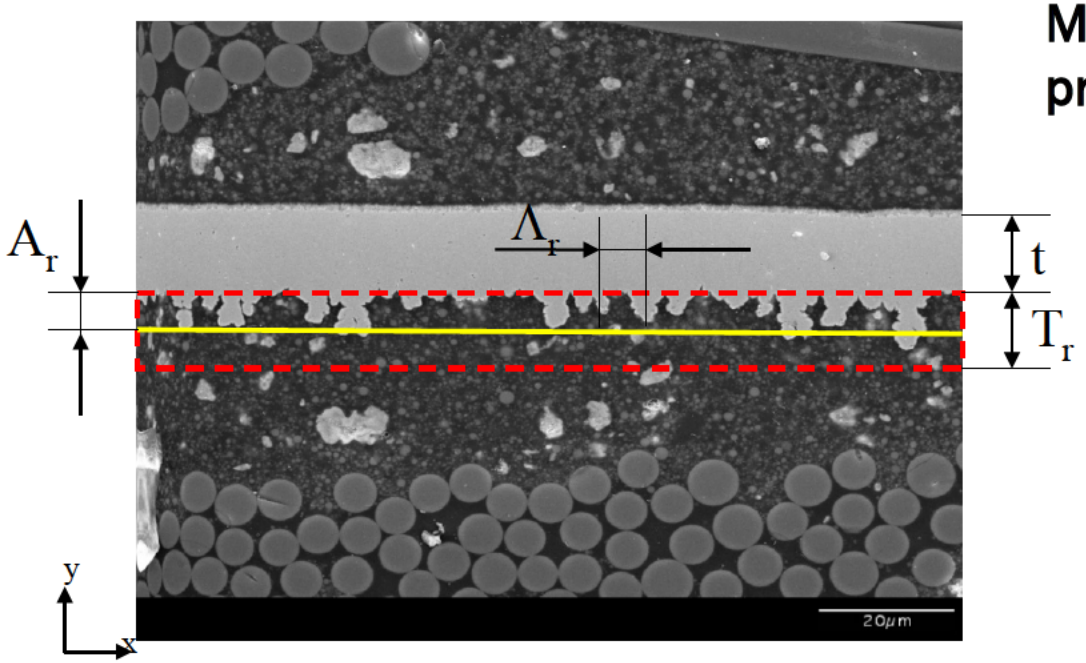
Using ERD Layers in Fitting Both Magnitude and Phase of S21







Maxwell Garnett Mixing Rule to Obtain ERD Parameters



MG theory allows for obtaining homogeneous material EM properties of inhomogeneous materials – composites:

$$\varepsilon_{eff,y} = \varepsilon_{matrix}\left(1 + v_{incl}\frac{\varepsilon_{incl} - \varepsilon_{matrix}}{\varepsilon_{matrix} + (1 - v_{incl})N_y(\varepsilon_{incl} - \varepsilon_{matrix})}\right)$$

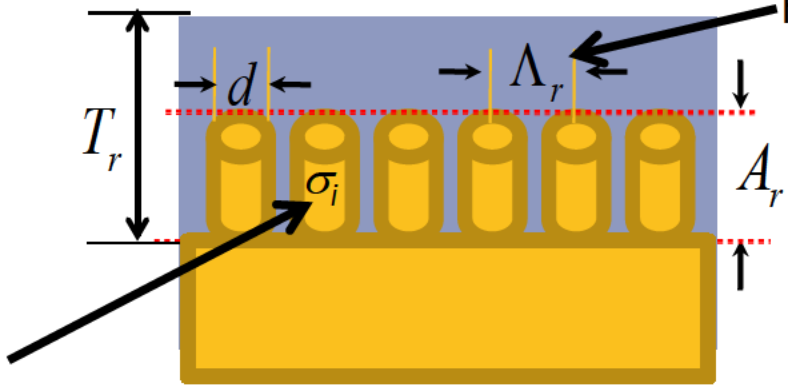
$N_y = \frac{1}{a^2}\ln(a)$ Depolarization factor of cylindrical inclusions

$a = A_r/d$ Aspect ratio of cylindrical inclusions

$$\varepsilon_{incl} = \varepsilon_i - \frac{j\sigma_i}{\omega\varepsilon_0} \qquad \varepsilon_{matrix} = \varepsilon'_m - j\varepsilon''_m.$$

Thickness of "roughness dielectric"

Intrinsic conductivity of metallic inclusions



Roughness quasi-period

Average peak-to-valley roughness amplitude

Problems: periodicity, cylinders are aligned and do not touch each other, conductivity is unknown

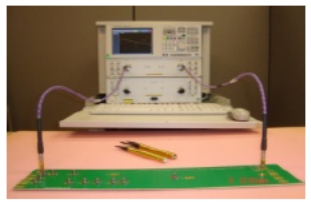
Optimization Approach to Extract ERD Parameters

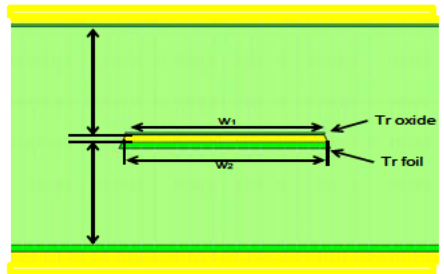
Measurements of S-parameters

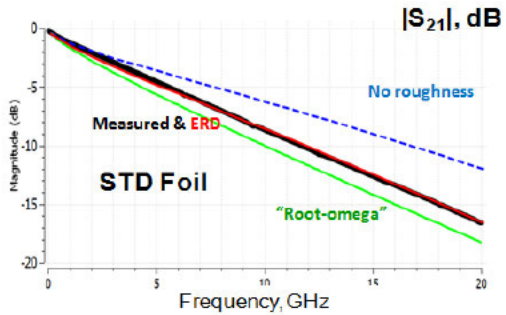
Extraction of true DK and DF of PCB dielectric *(DERM)*

2D-FEM Model

$\varepsilon_{rough} = \varepsilon'_{rough} - j\,\varepsilon''_{rough}$







Criteria for acceptable agreement of measured and modeled S_{21} (both IL & phase)

Satisfied

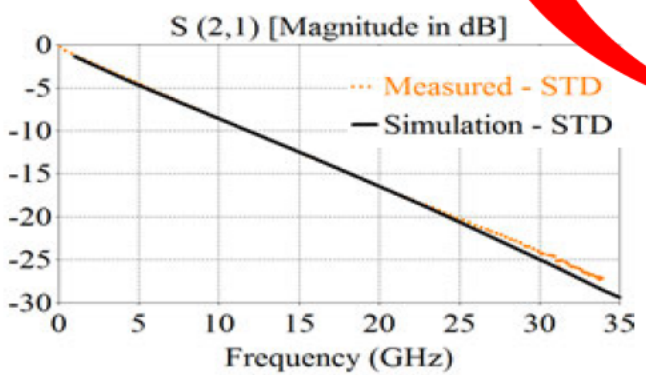
Extracted ERD

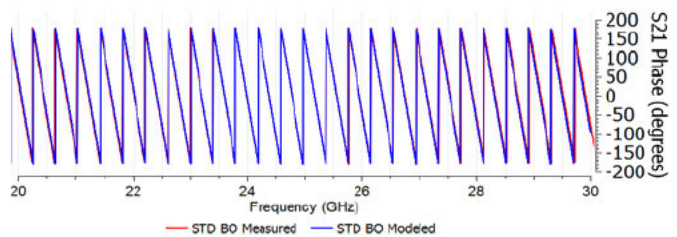
$\varepsilon_{rough} = \varepsilon'_{rough} - j\,\varepsilon''_{rough}$

Validation by full-wave simulation

Not satisfied

Correction



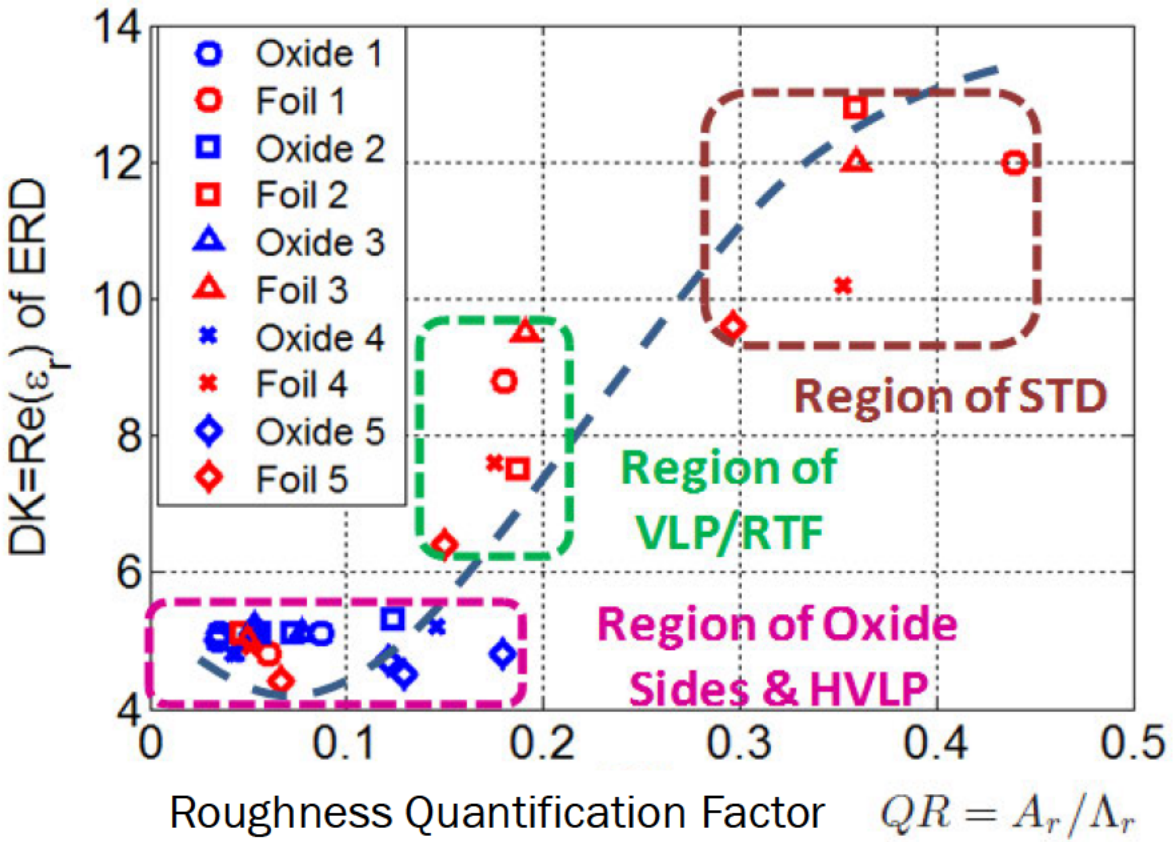


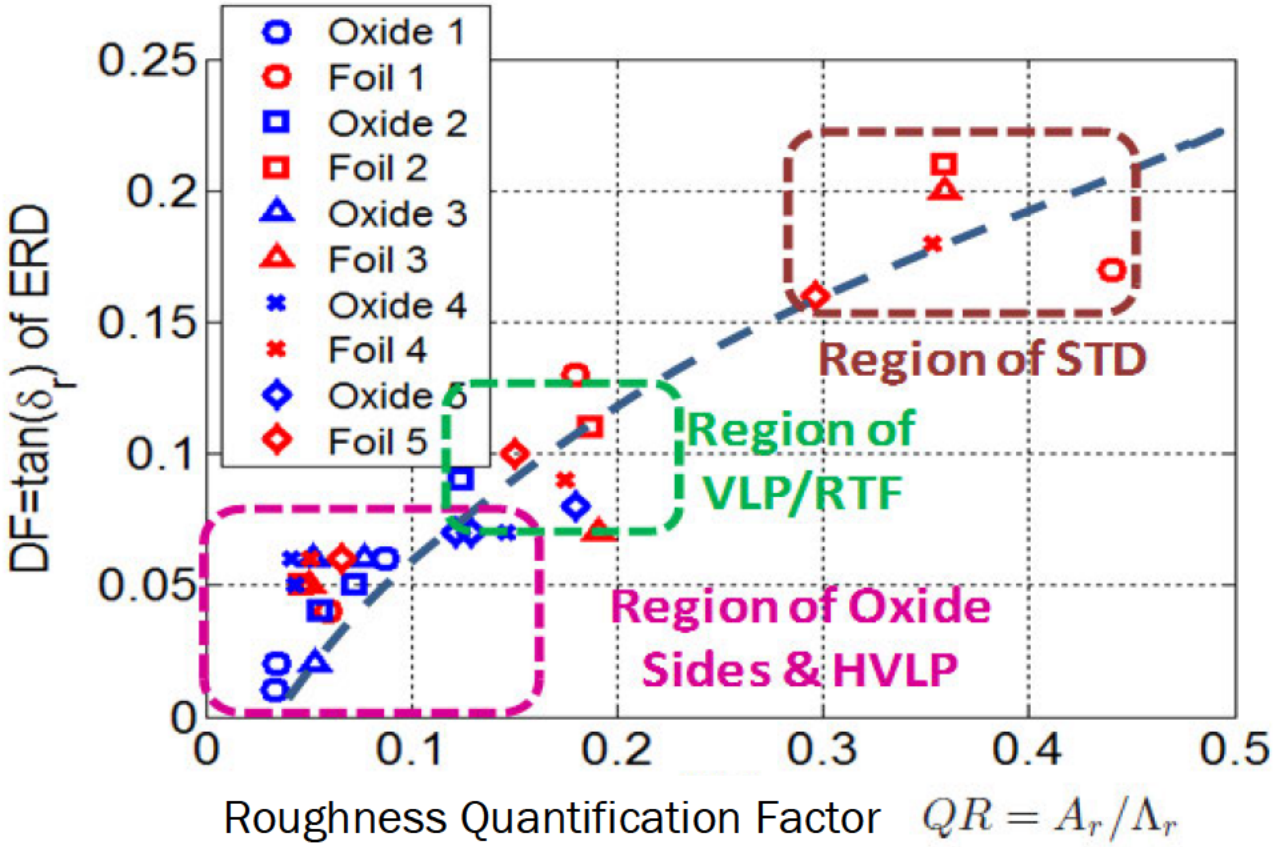
Optimization procedure uses numerical modeling in the loop for fitting S-parameters until measured and modeled results agree within some criteria.

M.Y. Koledintseva, T. Vincent, A. Ciccomancini Scogna, and S. Hinaga, "Method of effective roughness dielectric in a PCB: measurement and full-wave simulation verification", IEEE Trans. Electromag. Compat., vol. 57, no. 4, Aug. 2015, pp. 807-814

ERD "Design Curves": Independent of Frequency DK and DF

Sets 1,2,3 – **13mil** traces, Sets 4, 5 – **7 mil** traces

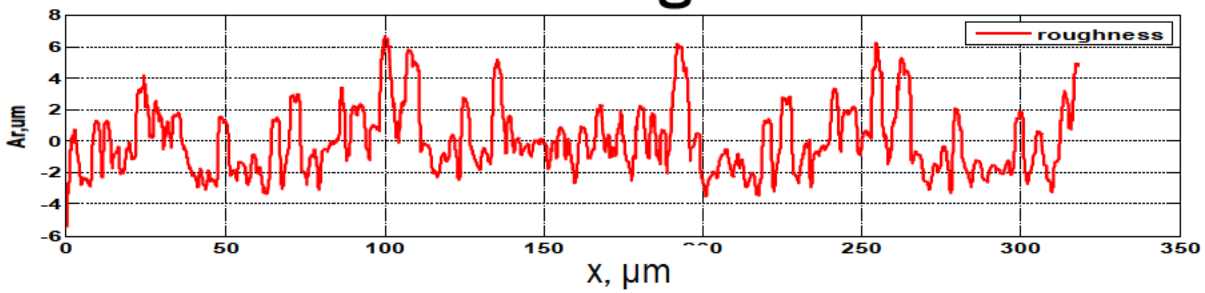




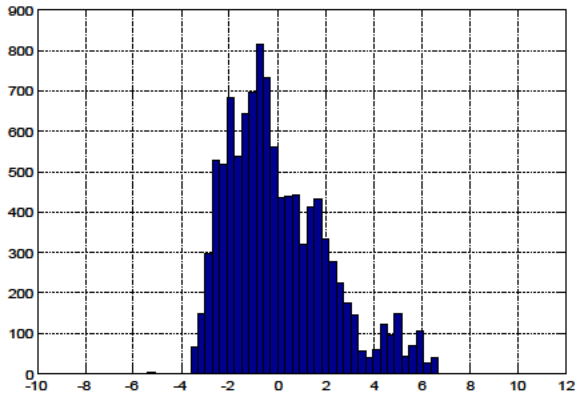
M.Y. Koledintseva, T. Vincent, A. Ciccomancini Scogna, and S. Hinaga, "Method of effective roughness dielectric in a PCB: measurement and full-wave simulation verification", IEEE Trans. Electromag. Compat., vol. 57, no. 4, Aug. 2015, pp. 807-814

Roughness Probability Density and Autocorrelation Functions

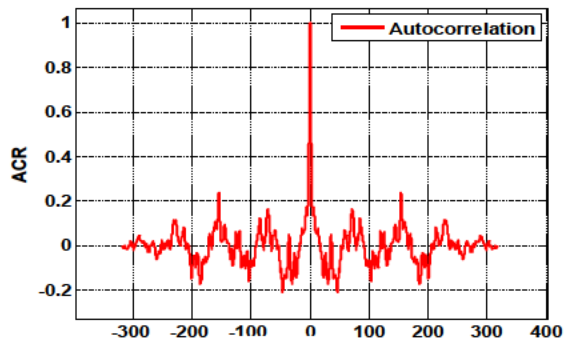
STD "Foil" Side Roughness Profile

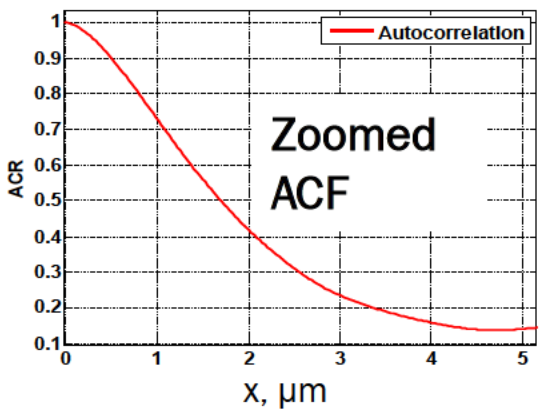


PDF (pixels)



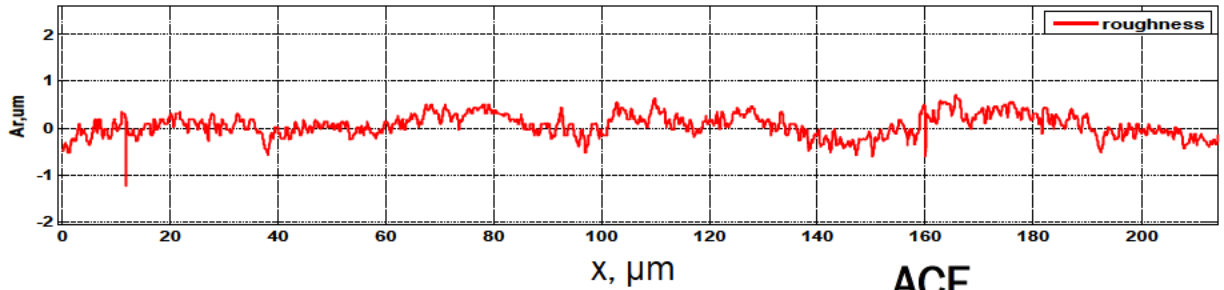
ACF



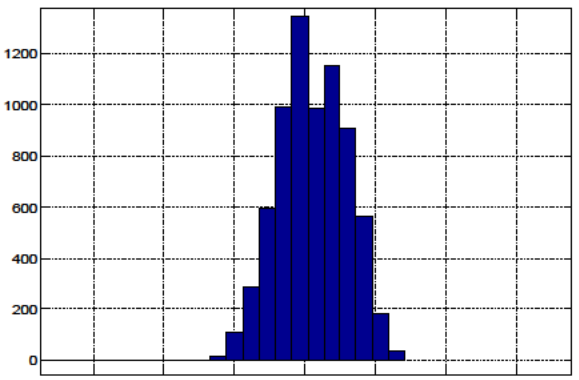


PDF determines average peak-to-valley roughness amplitude A_r values.

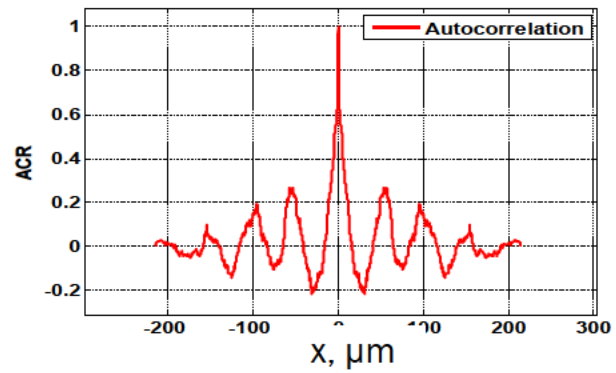
STD "Oxide" Side Roughness Profile

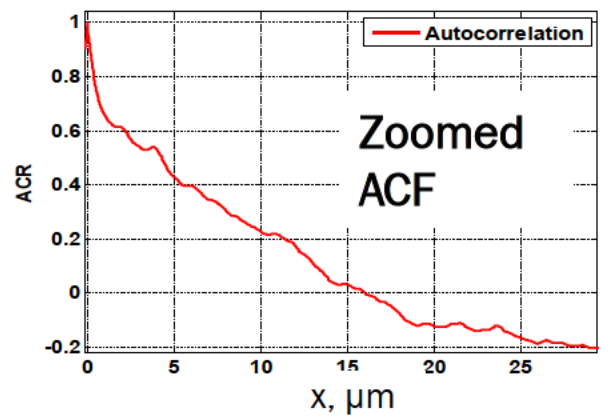


PDF (pixels)



ACF

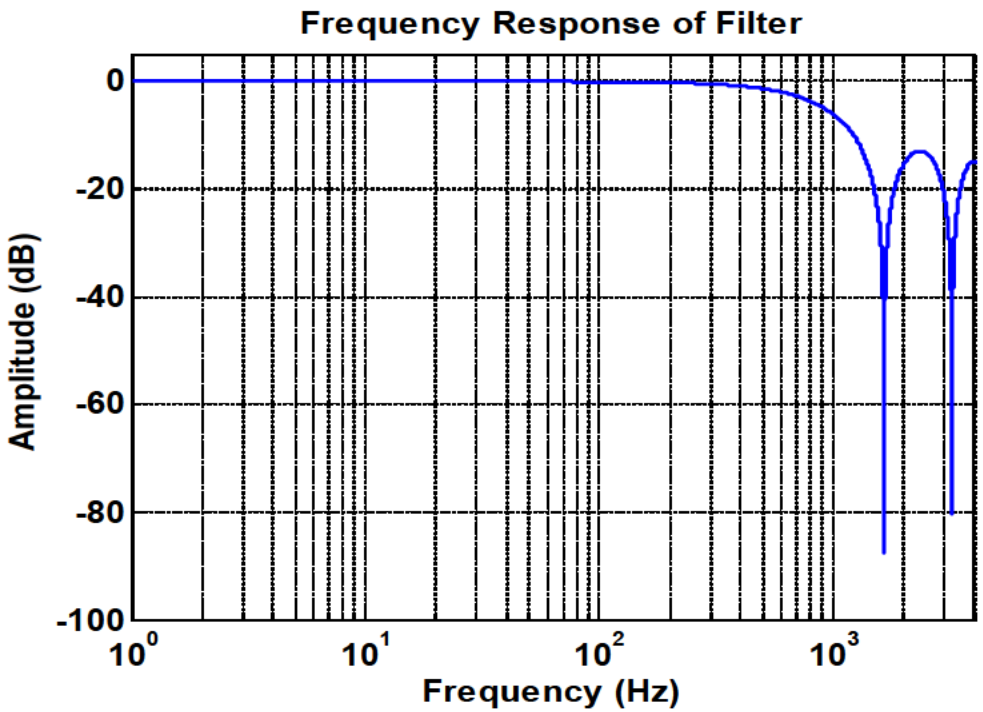




ACF determines quasiperiod Λ_r values. Hence PDF and ACF determine roughness quantification factor QR.

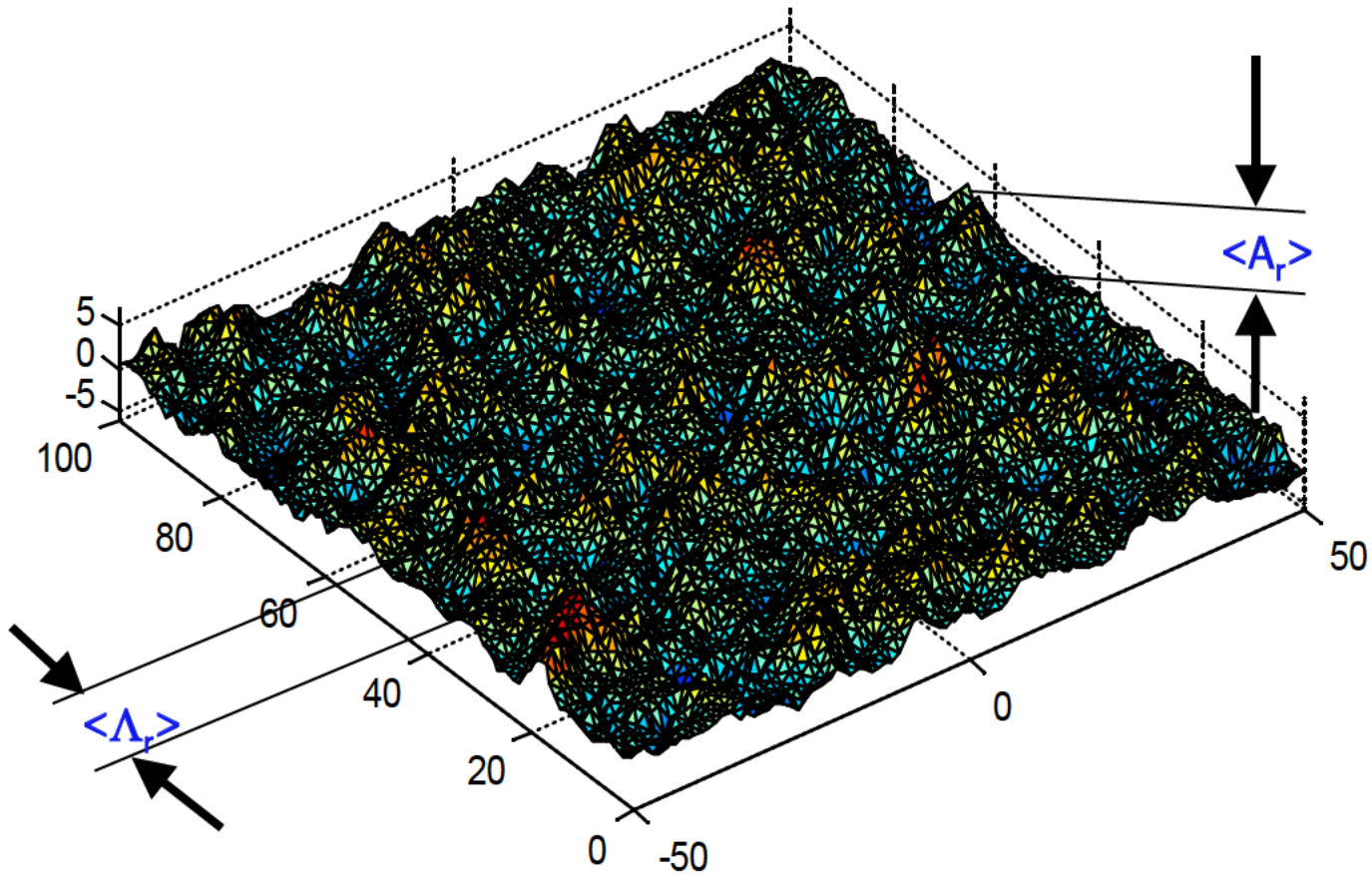
Generation of 3D Roughness Profile Surface

Gaussian finite impulse response digital filter



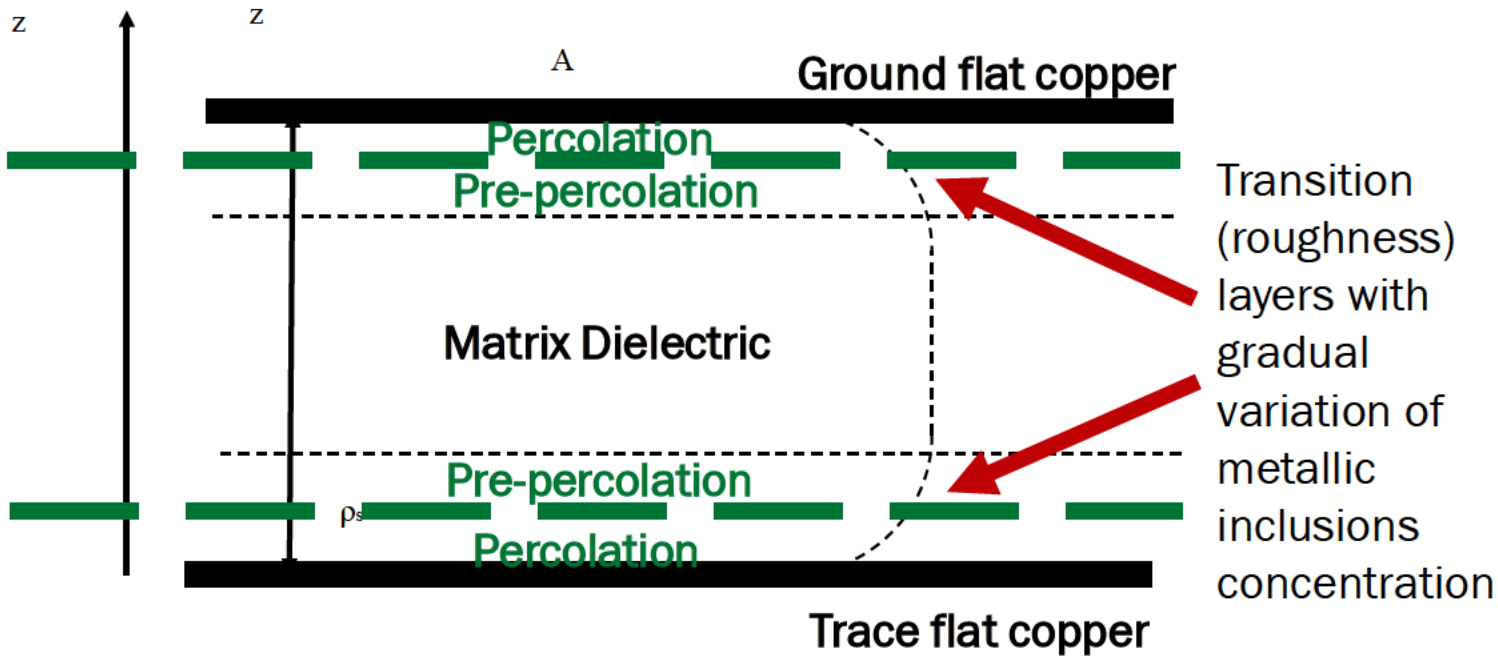
O.Y. Kashurkin, Measurements and simulation of conductor-related loss of PCB transmission lines, M.S.E.E. Thesis, Missouri S&T, 2016

Artificially Generated Roughness Profile from PDF, ACR, and Gaussian finite impulse response digital filter



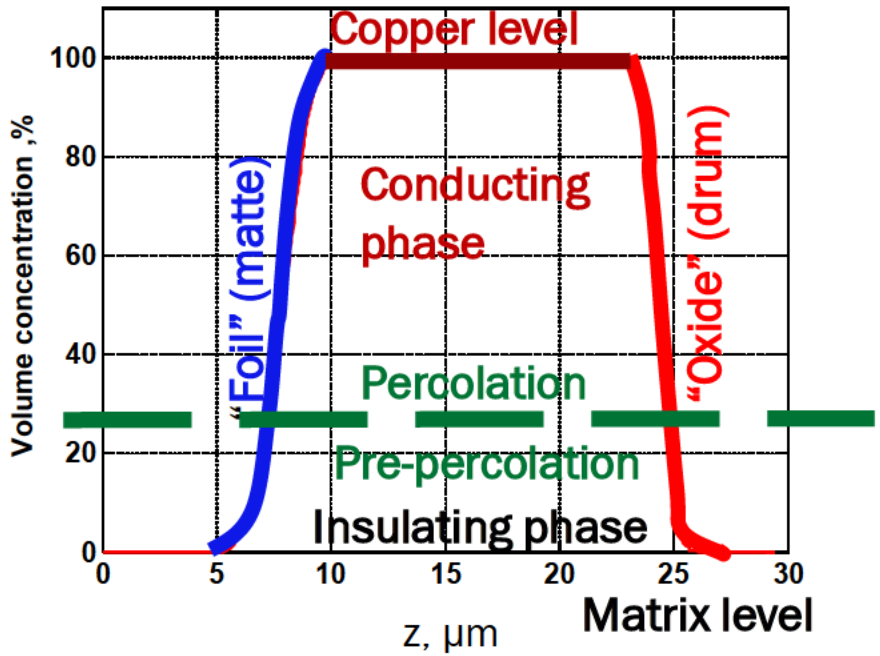
Such a profile reproduces actual surface roughness and is convenient for roughness quantification and modeling

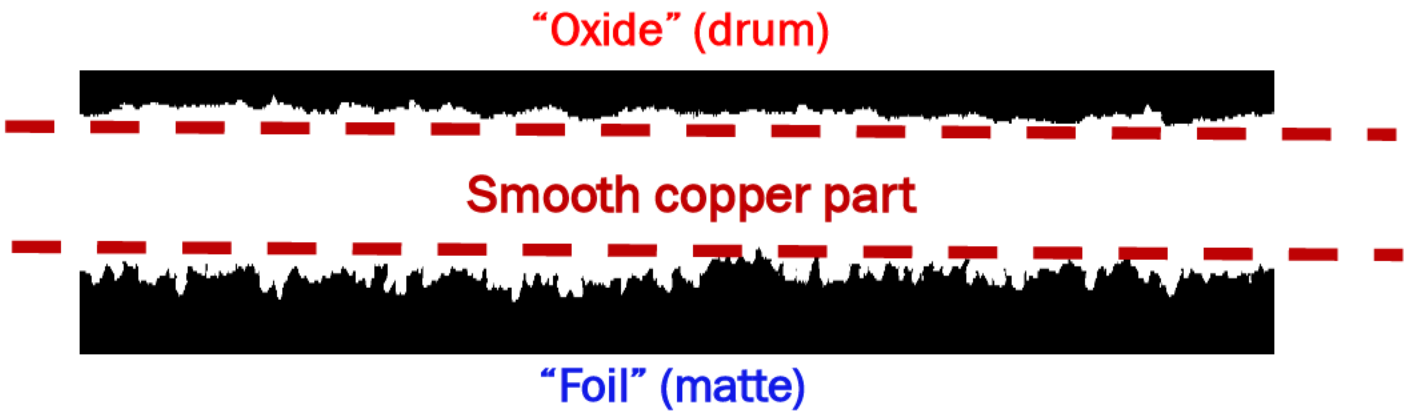
Equivalent Capacitance Model Construction



Transition (roughness) layers with gradual variation of metallic inclusions concentration

Concentration Profile





Percolation is the concentration at which insulating phase turns to conducting phase, herein for copper/epoxy resin ~ 25%.

Transition (roughness) layer will be modeled as a capacitor with variable dielectric properties following the concentration profile

Equivalent Capacitance Model

$v_{incl}(z) = a \times \exp(K_1 z)$ Concentration profile of pre-percolation region

$T = T_p + \Delta T$ Roughness layer thickness, Tp is pre-percolation thickness

$v_p = a \times \exp(K_1 T_p)$ Percolation threshold, K_1 is the exponent parameter

$\varepsilon(z) = \varepsilon_m v_{incl}(z)$ Variable dielectric profile in the transition (roughness) layer

Effective permittivity calculated from both pre-percolation and percolation parts

$$\varepsilon_{eff} = T/\left(\int_0^{T_p} dz/\left(\varepsilon_m\left(1+v_{incl}(z)\right)\right) + \int_{T_p}^{T} dz/\left(\varepsilon_p(1+v_{incl}(z))\right)\right)$$

$DK_r = \varepsilon_{eff}'$ and $DF_r = \tan\delta_{eff} = \varepsilon_{eff}''/\varepsilon_{eff}'$.

Region I - Pre-percolation (Insulating)

$C = C_0\, d \Big/ \int_0^d dz/(1+\varepsilon(z))$ Capacitance of the pre-percolation layer; C_0 is for the corresponding air-filled capacitor

$\varepsilon_d = T_p \Big/ \int_0^{T_p} dz/(\varepsilon_m(1+v_{incl}(z)))$ Effective dielectric properties inside pre-percolation layer

$\sigma_d = -\square\ {}_0\varepsilon_d''$ Effective conductivity inside pre-percolation layer

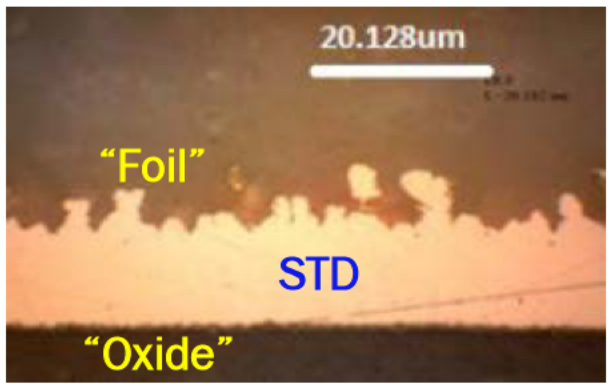
Region II- Percolation (Conducting)

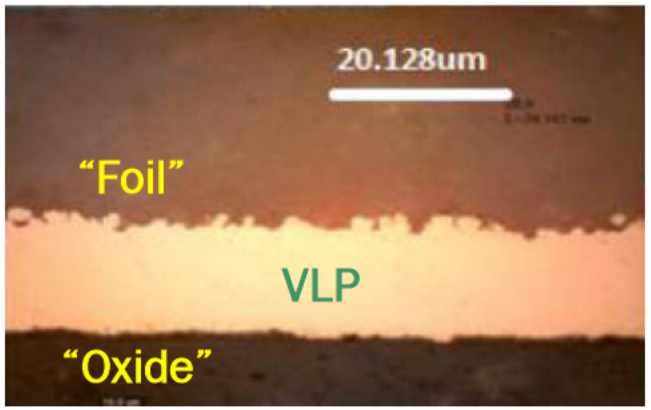
$\sigma(z) = \sigma_d \times e^{K_2 z}$ Conductivity profile in the percolation phase

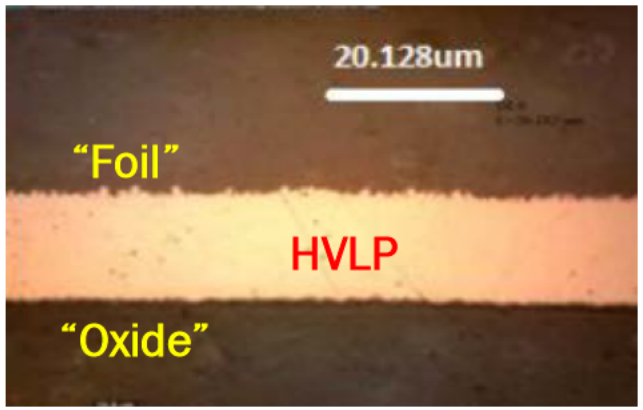
$\sigma_p = \sigma_d \times e^{K_2 T} = 0.01\sigma_{CU}$ Conductivity in percolation phase, K_2 is the exponent parameter

$\varepsilon_p(z) = \varepsilon_d + \frac{\sigma_d}{j\omega\varepsilon_0} \times e^{K_2 z}$ Dielectric profile in percolation phase

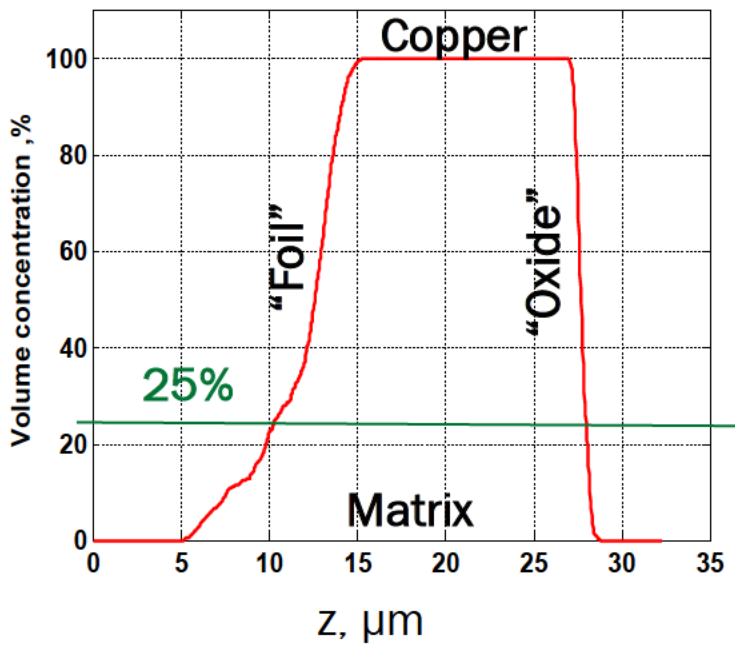
Volume Concentration of Metallic Inclusions in Roughness Profiles of Different Foils



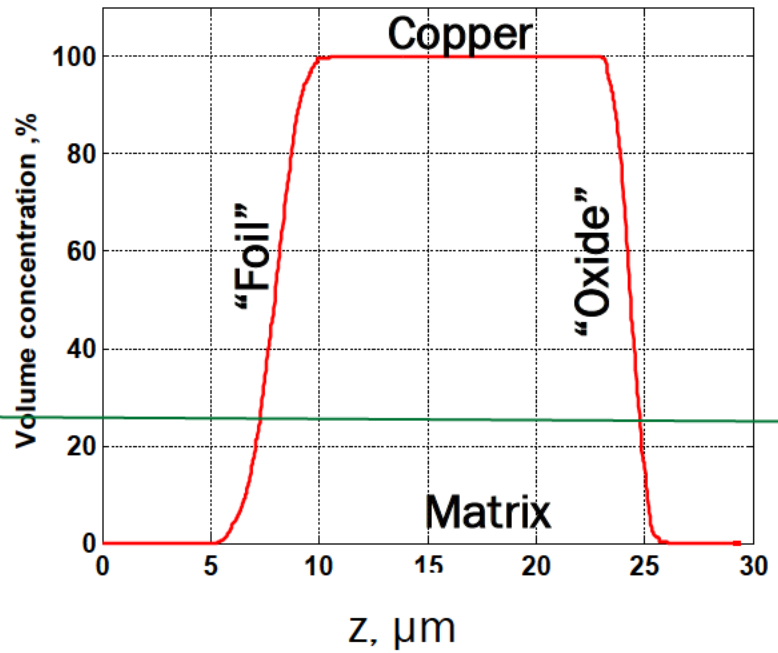




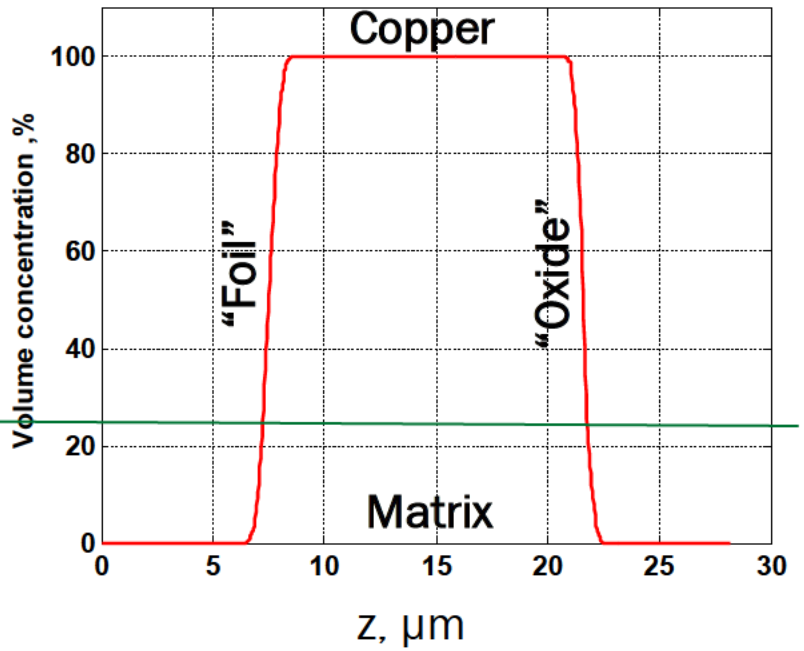
(a)



(b)

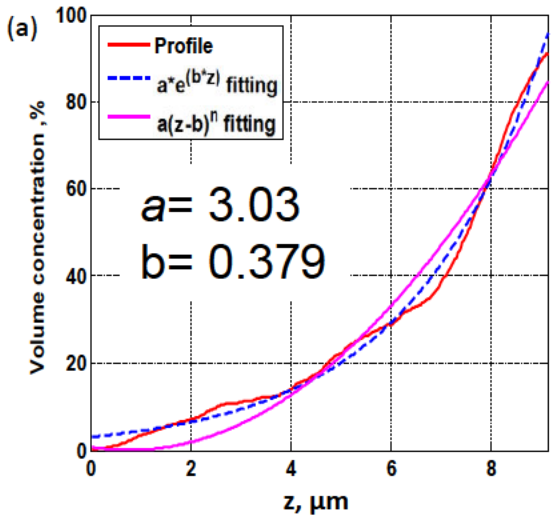


(c)

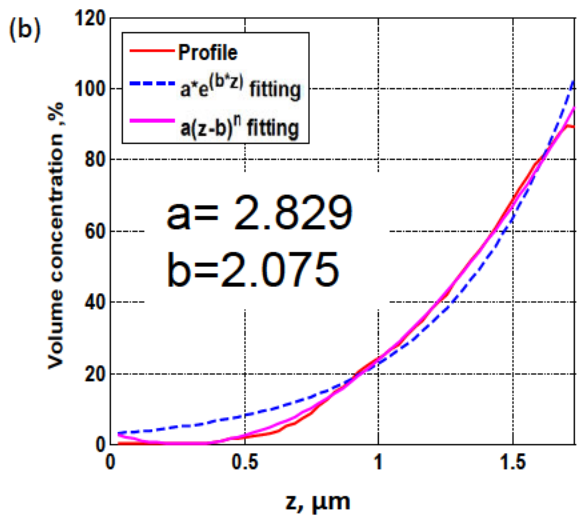


Volume Concentration of Metallic Inclusions in Roughness Layer

STD "Foil" side

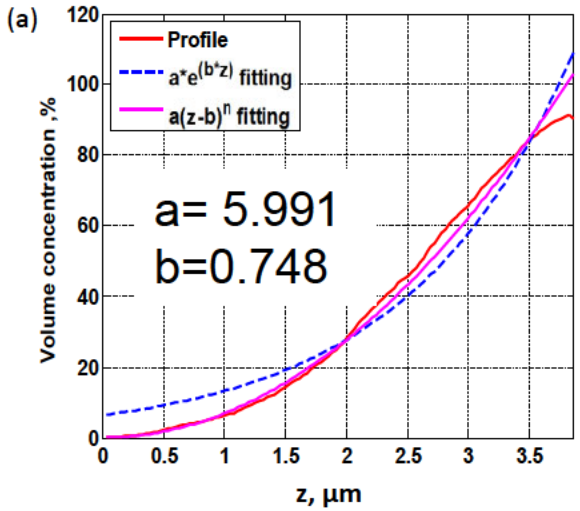


STD "Oxide" side

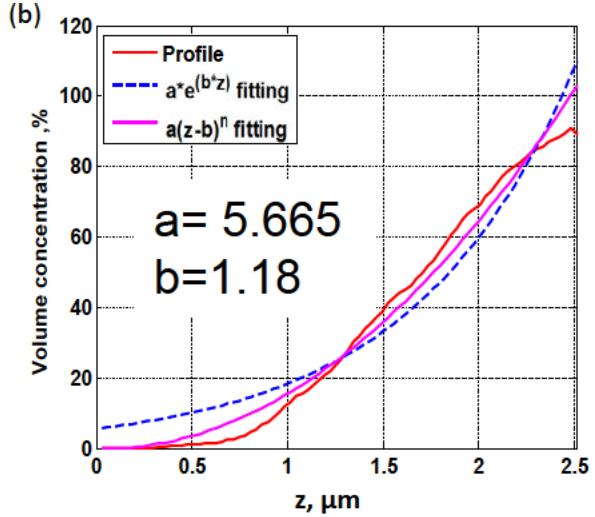


Fitting parameters (*a*, *b*) are extracted from these profiles for each type of tested foils (STD, VLP, HVLP), on both "foil" and "oxide" sides.
Herein, fitting parameters are given for exponential fitting.
Then they are used in the equivalent capacitance model.

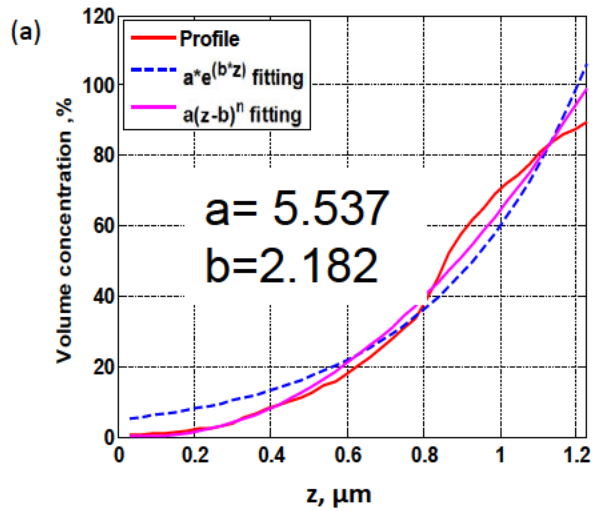
VLP "Foil" side



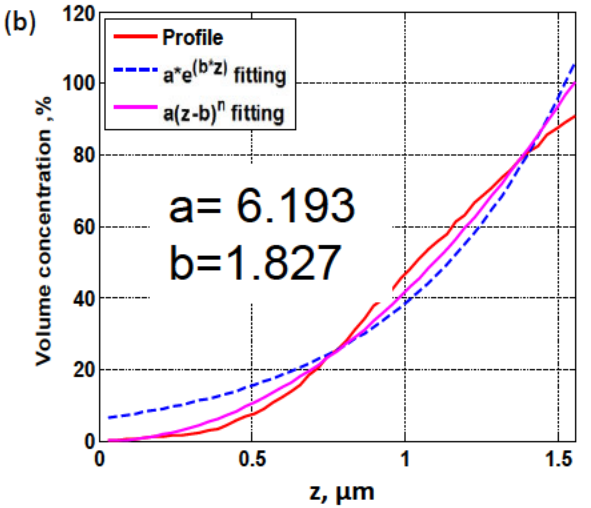
VLP "Oxide" side



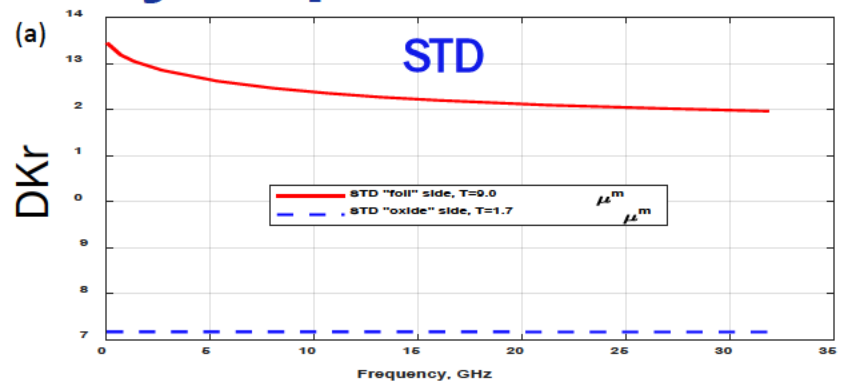
HVLP "Foil" side

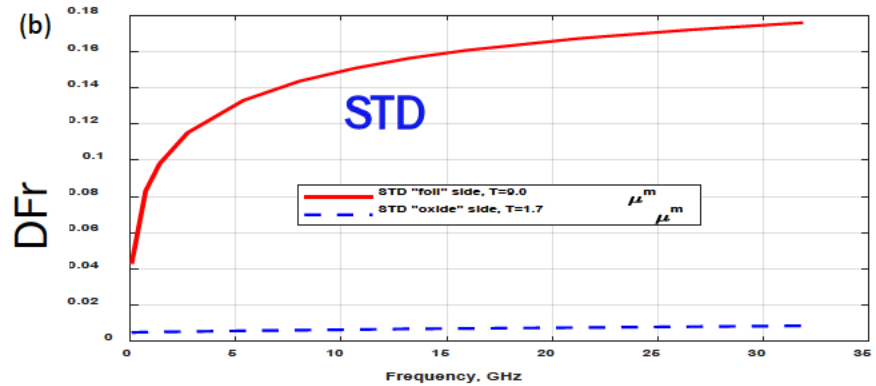


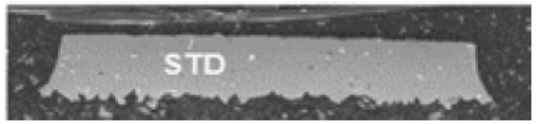
HVLP "Oxide" side

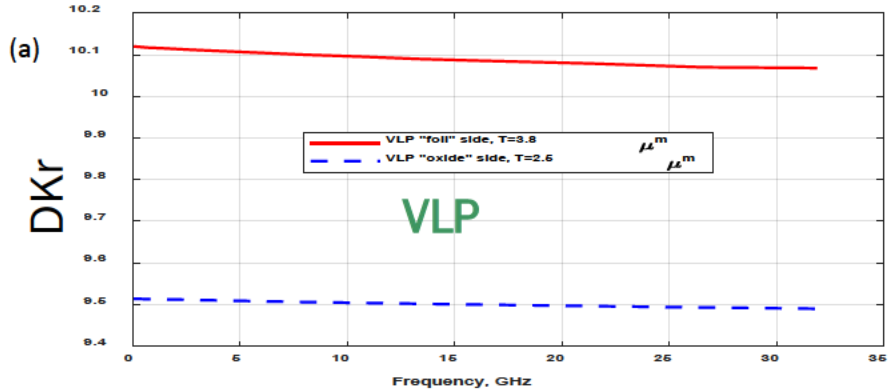


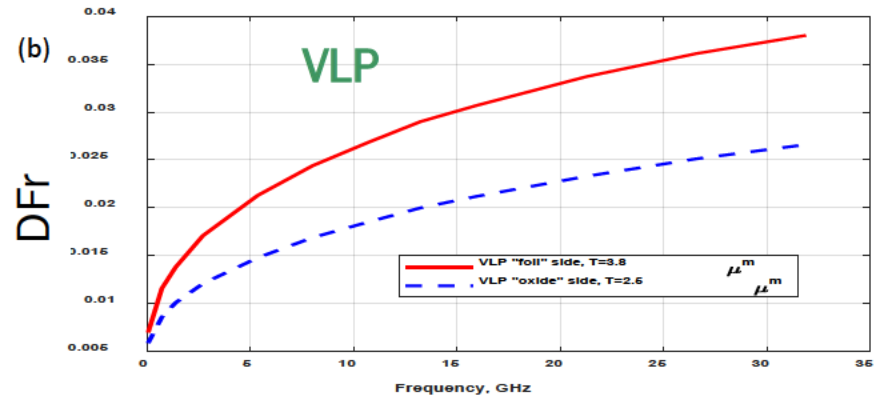
Frequency-dependent ERD Parameters of Foils

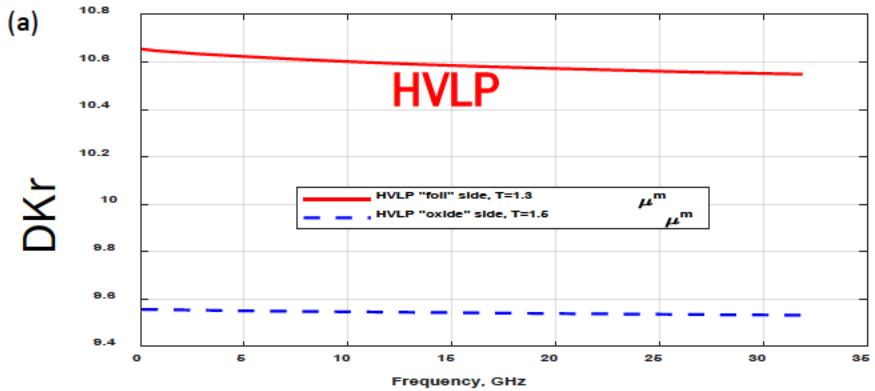


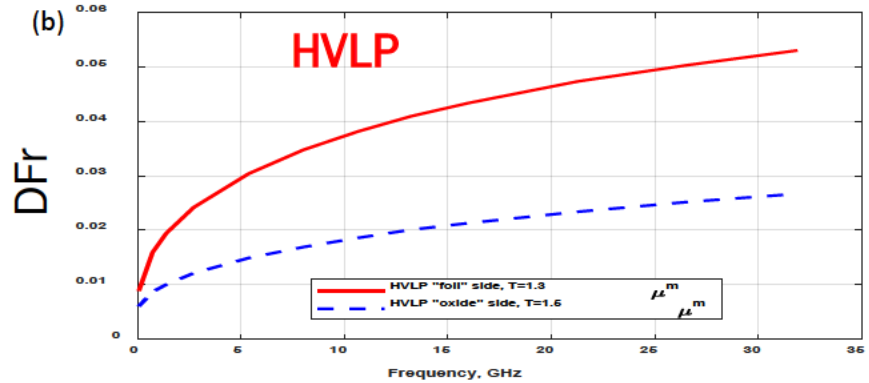




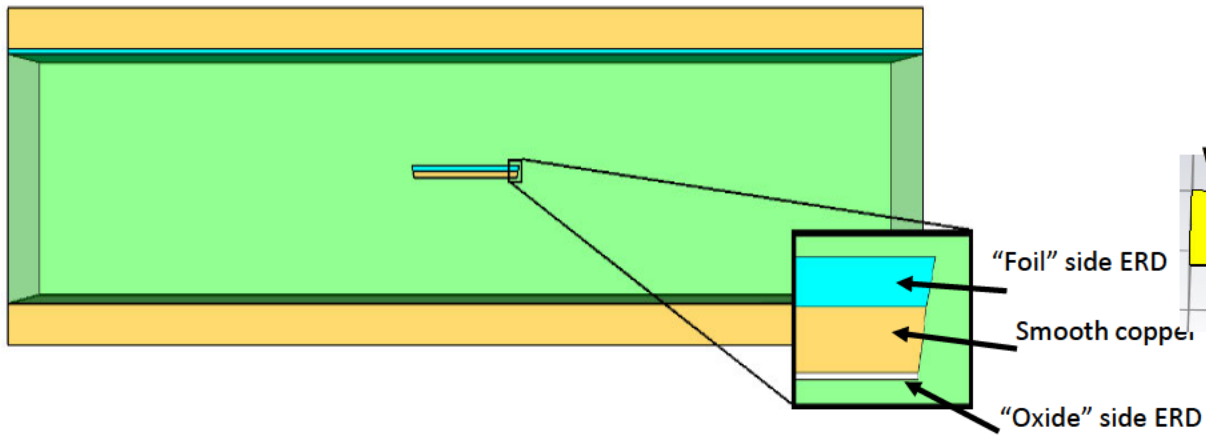




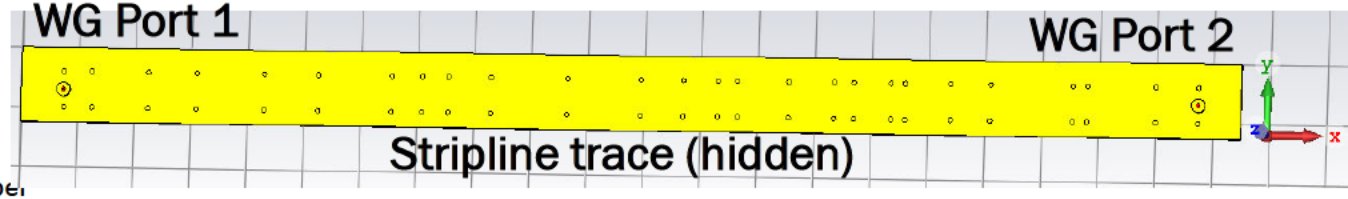




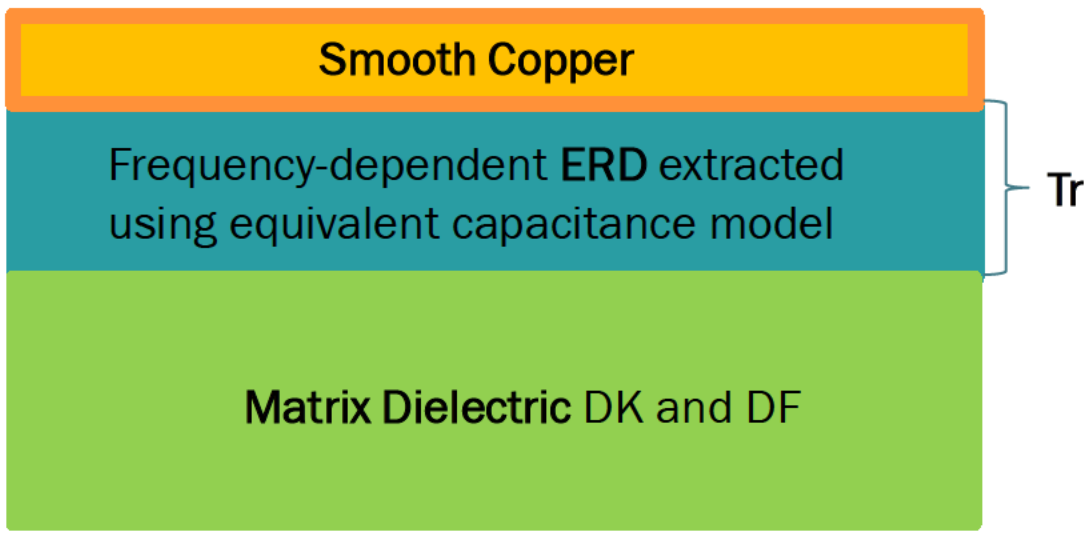
3D Numerical Model Setup



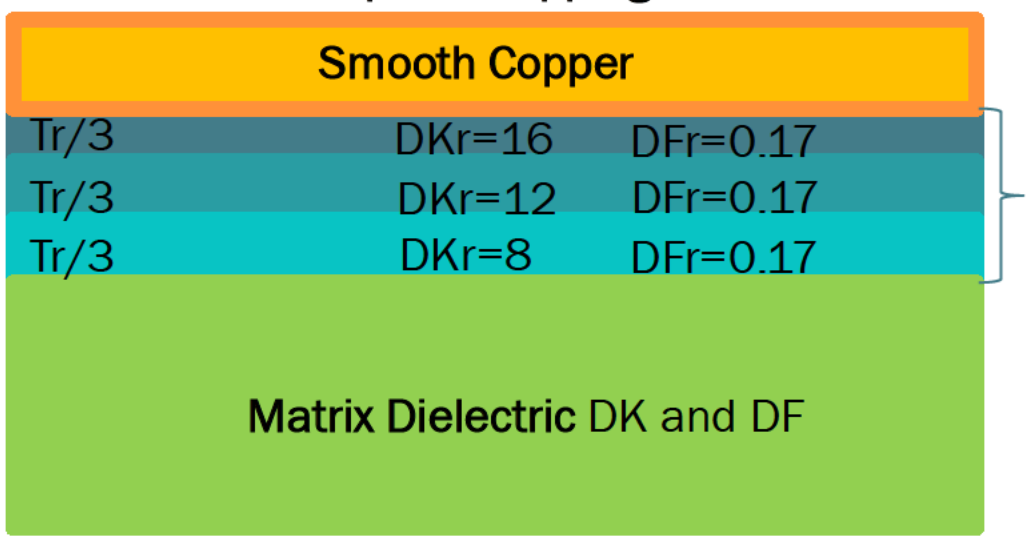
Time-domain FIT solver is used for 3D full-wave electromagnetic simulations



Roughness Model 1: Homogenized ERD layer modeled

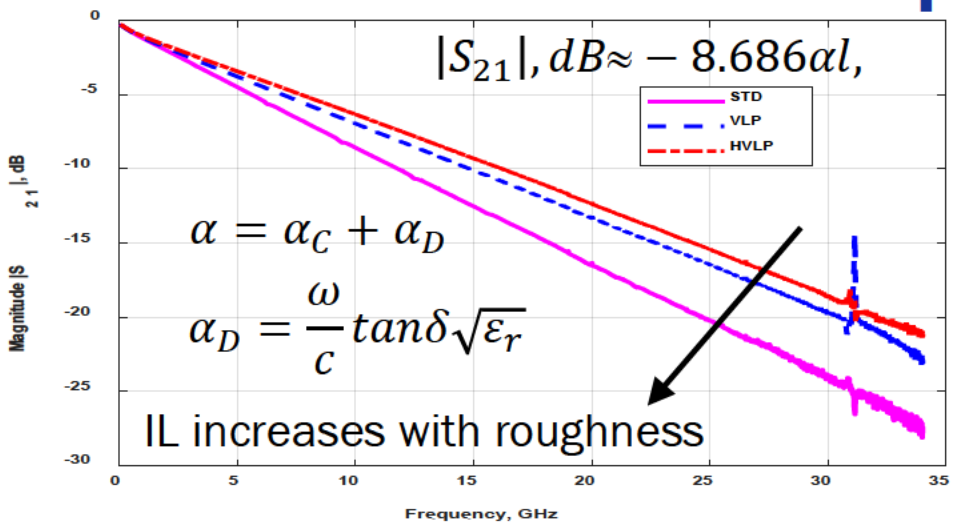


Roughness Model 2: Layered structure modeled using space mapping

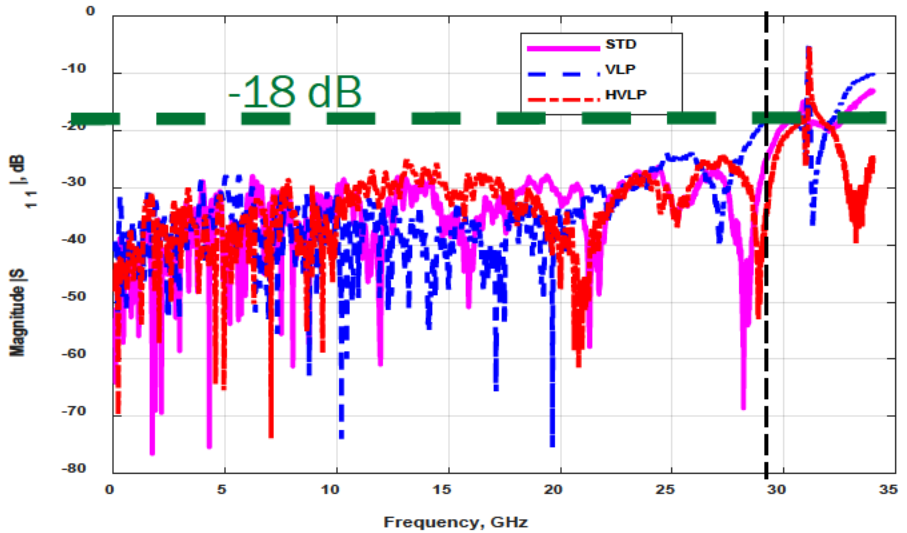


These DKr and DFr are for STD only

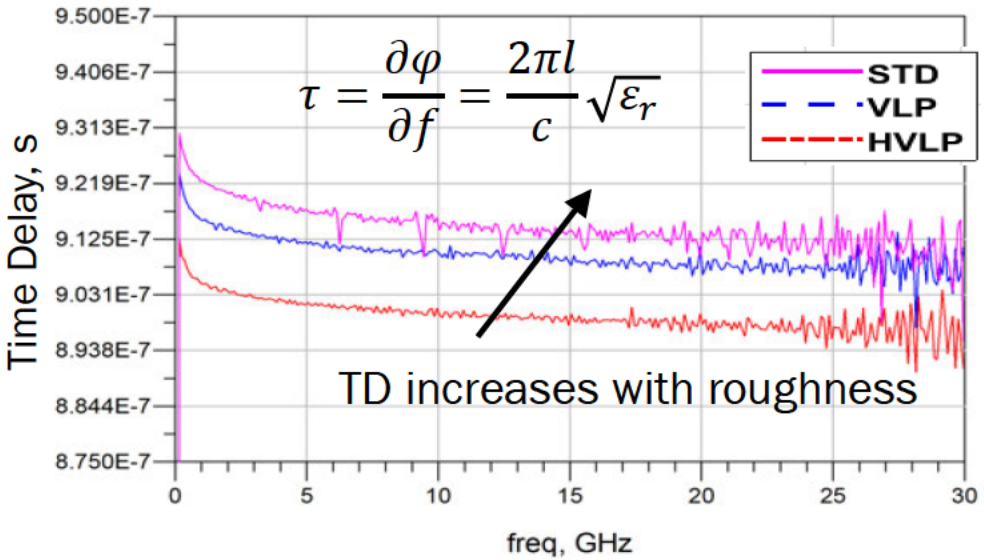
Model Validation Using S-parameter Sweep Stripline (S3) Measurement Technique



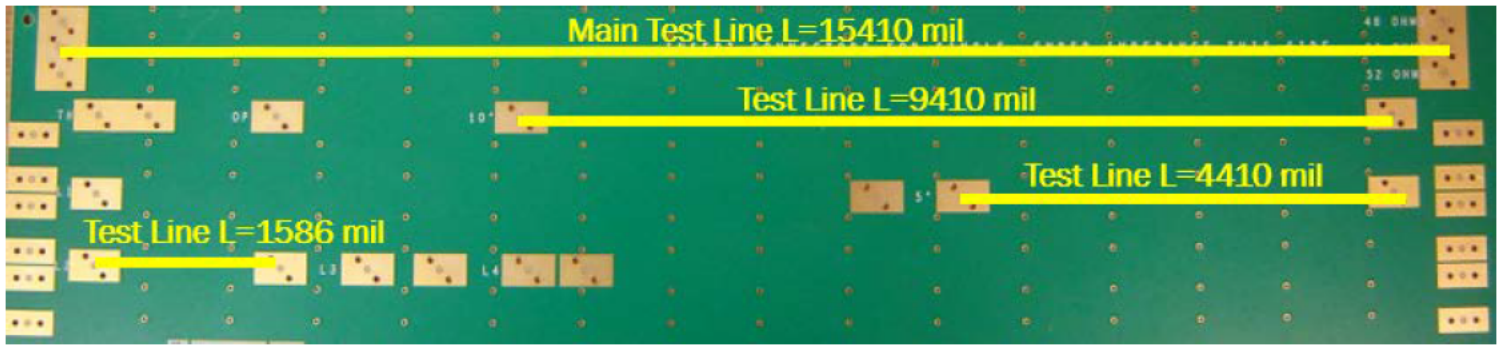
ε_r includes both matrix dielectric and ERD



RL level in S3 must be below -18 dB for errors in extracting DK < 1% and in DF < 5%.

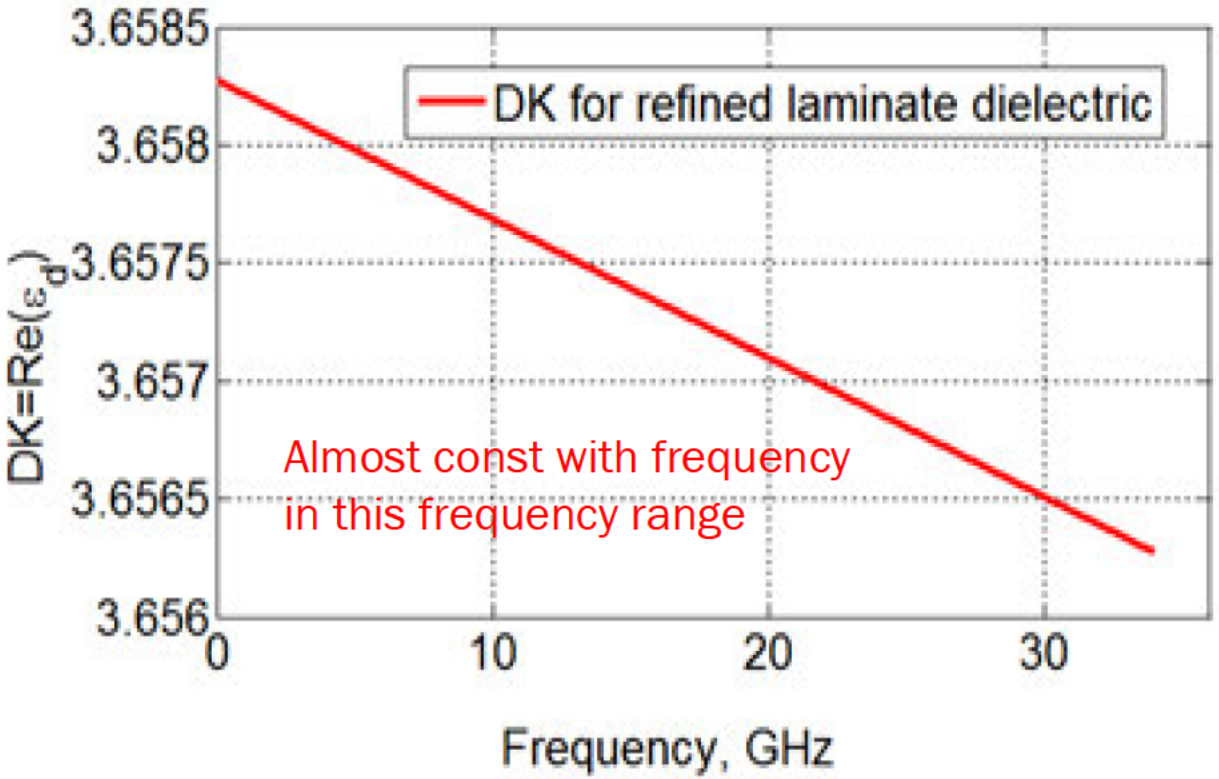


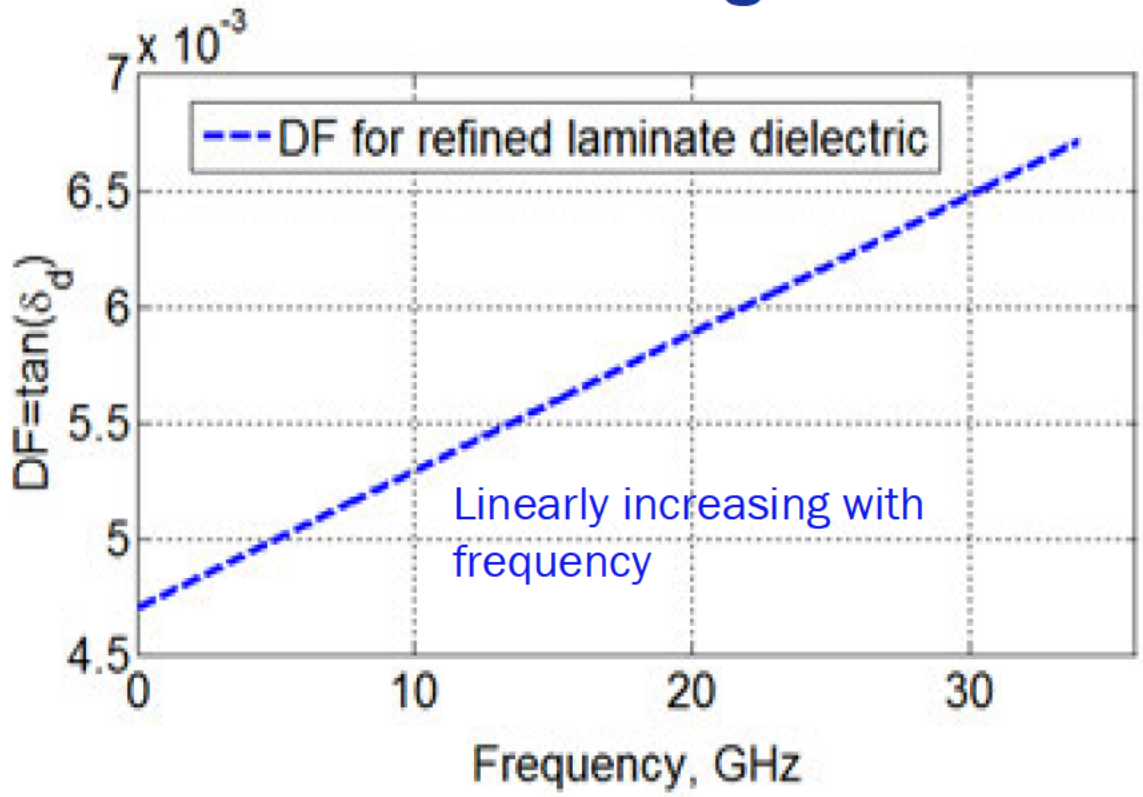
Test Board with Striplines



Other lines are used for TRL calibration to remove port/connector effects

PCB Laminate Dielectric Properties Used in Modeling



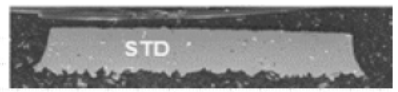


Pure (refined from copper roughness) DK and DF parameters of PPO Blend extracted using Differential Extrapolation Roughness Measurement (DERM) technique:

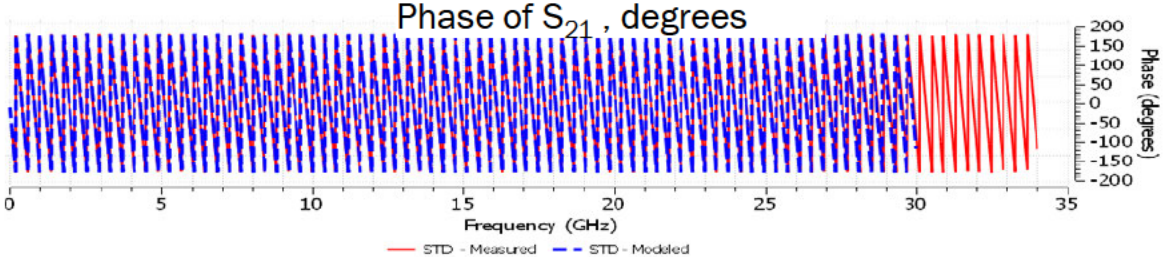
M.Y. Koledintseva, A.V. Rakov, A.I. Koledintsev, J.L. Drewniak, and S. Hinaga, "Improved experiment-based technique to characterize dielectric properties of printed circuit boards", IEEE Trans. Electromag. Compat., vol. 56, no. 6, 2014, pp. 1559-1566.

Results of Numerical Modeling and Measurements

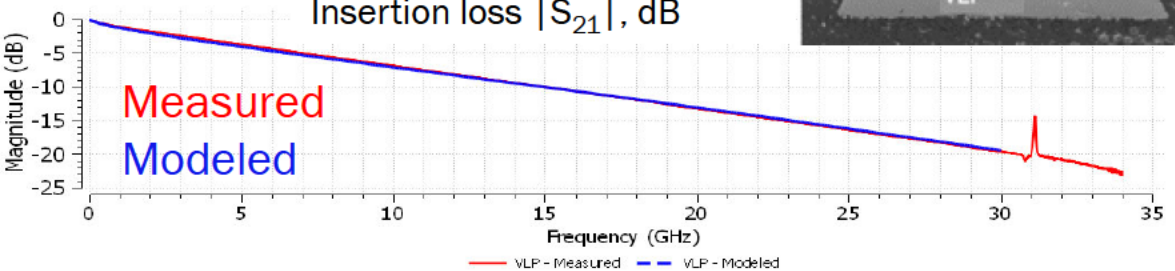
Insertion loss $|S_{21}|$, dB



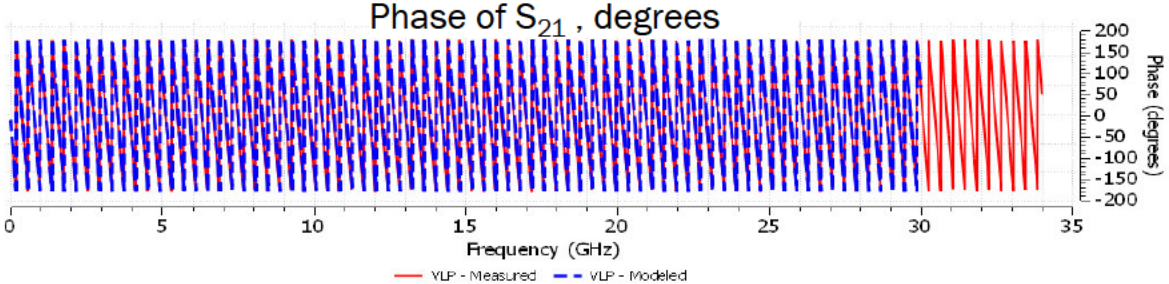
Phase of S_{21}, degrees



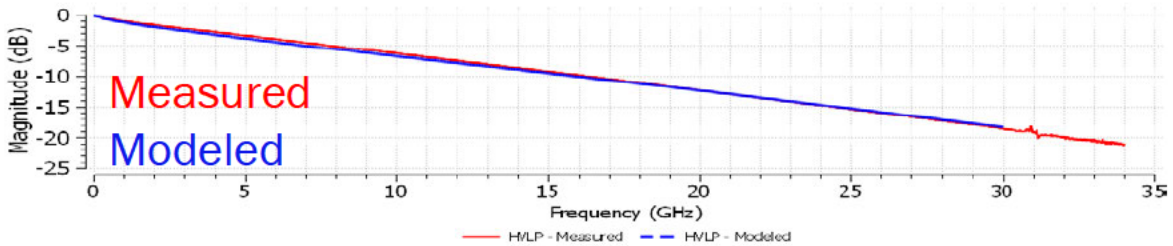
Insertion loss $|S_{21}|$, dB



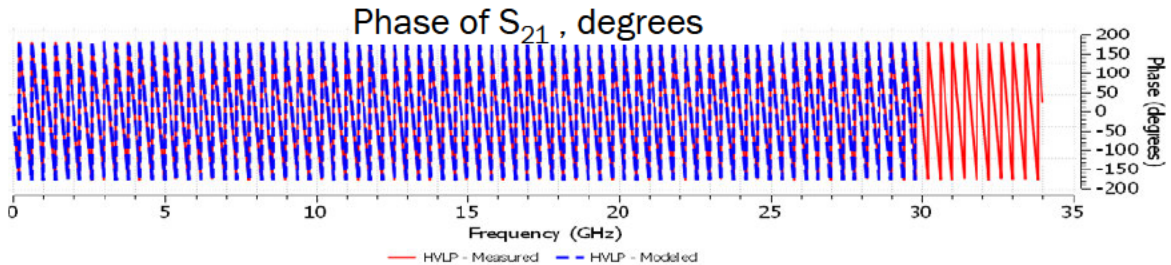
Phase of S_{21}, degrees



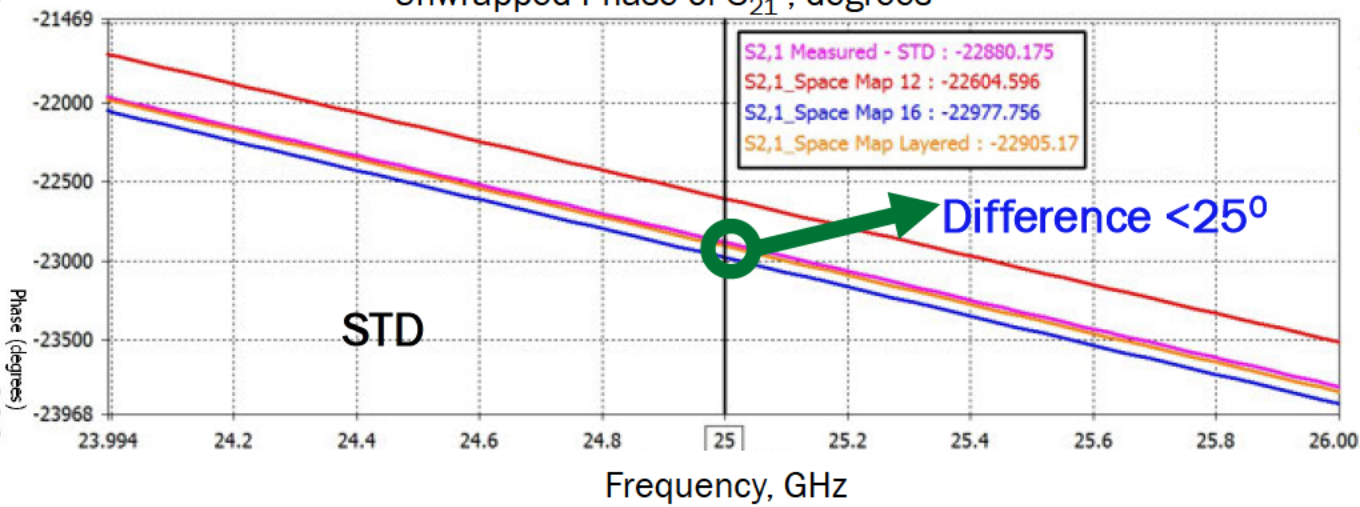
Insertion loss $|S_{21}|$, dB



Phase of S_{21}, degrees



Unwrapped Phase of S_{21}, degrees



Conclusions

- An analytical model to calculate effective roughness dielectric (ERD) parameters for conductor surface roughness of a PCB foil is presented.
- Using concentration dependence of metallic inclusions in the roughness transition layer between matrix dielectric and smooth copper, the equivalent capacitance is calculated analytically. Percolation threshold is taken into account to subdivide the layer into two series capacitances.
- The ERD parameters DK_r and DF_r are extracted from the equivalent capacitance.
- The ERD parameters for STD, VLP, and HVLP foils at their “foil” and “oxide” sides are calculated.
- The ERD parameters are frequency-dependent unlike in the previous publications.
- The extracted ERD parameters are used in full-wave 3D numerical electromagnetic models of single-ended striplines.
- Two methods of modeling ERD are proposed – with homogenized ERD parameters and with space mapping.
- The measured by S3 technique and numerically modeled results, both magnitudes and phases of S_{21} for the stripline structures, show excellent agreement over the frequency range up to ~ 30 GHz.

THANK YOU!

Questions?

marina.koledintseva@oracle.com