# Development of a High Temperature Protective Coating to Enable Organic Printed Circuit Boards to Operate at Higher Temperatures

Martin Wickham, Vimal Gopee, Adam Lewis and Christine Thorogood
National Physical Laboratory, Teddington, UK

**Abstract**
Reliable operation of electronics at higher temperatures requires a combination of performance improvements in components, interconnects and substrates. Ceramic based substrate options can be costly, heavy and prone to mechanical damage. Printed circuit board (PCB) options are restricted to lower working temperatures of the organic resins and degradation of their conductive tracks. A collaborative research programme between project partners has successfully developed innovative materials specifically designed to offer protection to organic PCBs and interconnects allowing them to operate at higher temperatures or for longer durations. Currently, the operation of electronic assemblies at higher temperatures is limited by the ability of copper clad PCBs to maintain circuit integrity. The project has developed a coating material which when applied to printed circuit assemblies (PCAs) makes them more suitable for operating at temperatures above 200ºC. This paper summarises the work undertaken by the authors to develop and better understand the performance enhancements produced by these materials. The project brought together a materials supplier, an end-user and a research technology organisation to jointly develop, test and implement the solution based on silicone coating materials. This paper focuses on the testing and materials evaluation undertaken to determine the long-term performance of these alternative materials in harsh environments. Details of the electrical performance of component and PCB interconnects between the substrates and components during the test regimes are given as well as the degradation mechanisms experienced in unprotected PCAs. The manufacturing process is outlined including details of the test vehicles utilised. Details of the test methodology used and comparable results for coated and uncoated systems will be given. The results show a significant improvement of mean-time-before-failure (MTBF) for coated PCAs and PCBs compared to uncoated samples. The primary performance improvement is shown to be reduction in the oxidation rate of copper in both the inner and outer layers of copper tracking in the multilayer structures.

**Introduction**
Many applications are now emerging for systems where elevated temperatures, pressures and aggressive media are involved. Aerospace, engine management systems, oil and gas resources, automotive and power management for hybrid/electric vehicles are some applications. These industries have tough specifications that command sustainable, high value solutions and also maintain a strong UK manufacturing presence. As a result of emission legislation (e.g. $CO_2$ emissions) and the drive for improvements in efficiency, the market for these applications is growing rapidly. As electronics move ever closer to the source of combustion (engines) or drill heads (down hole applications), normal lead-free solders (melting at ~220ºC) and organic FR4 PCBs (<140ºC) become unsuitable due to the ambient temperatures exceeding operating limits. Traditionally these high-reliability applications have had to use high cost alumina technologies. Alumina substrates are hard to machine, and use gold, silver or palladium conductor inks interleaved with dielectric material requiring successive firing at high temperatures (600ºC). The result is very reliable and stable but very high cost in terms of monetarily outlay (high tooling costs) and energy use. Through-hole component assembly and through-substrate vias are also difficult to produce with ceramic technology.

Using polymeric based systems at temperatures above 175ºC can be problematic. Whilst several substrates with decomposition temperatures (the temperature at which a 5% weight loss occurs by thermal gravimetric analysis (TGA) (Reference 3)) above 400°C and/or T288 (measures time to delamination at 288°C (Reference 4)) times of greater than 60 mins (References 1,2), these figures make no account for the performance of the copper (Cu) cladding. Previous work by the authors to develop a high temperature solder alternative (Reference 5) showed that the weak link in the system was the electroless nickel immersion gold (ENIG) finished Cu tracking connecting the components. Figure 1 shows track failures generated after 6,500 hours aging at 250ºC. Here the Cu track has oxidised causing embrittlement and subsequent fracture resulting in electrical failures.

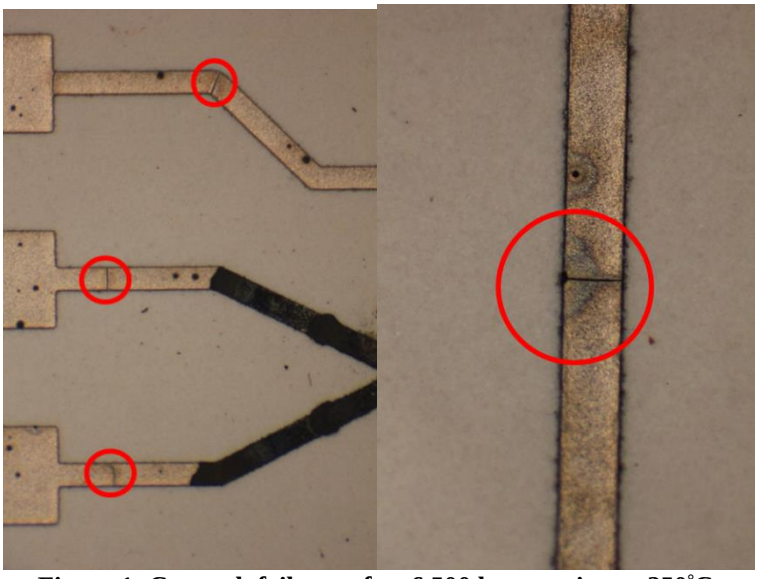


**Figure 1: Cu track failures after 6,500 hours aging at 250˚C.**

Figure 2 shows energy dispersive x-ray spectroscopy (EDAX) scans of cross-sections of similar samples before and after 3000 hours at 250 ˚C. Increased oxygen content can be seen in the aged sample.

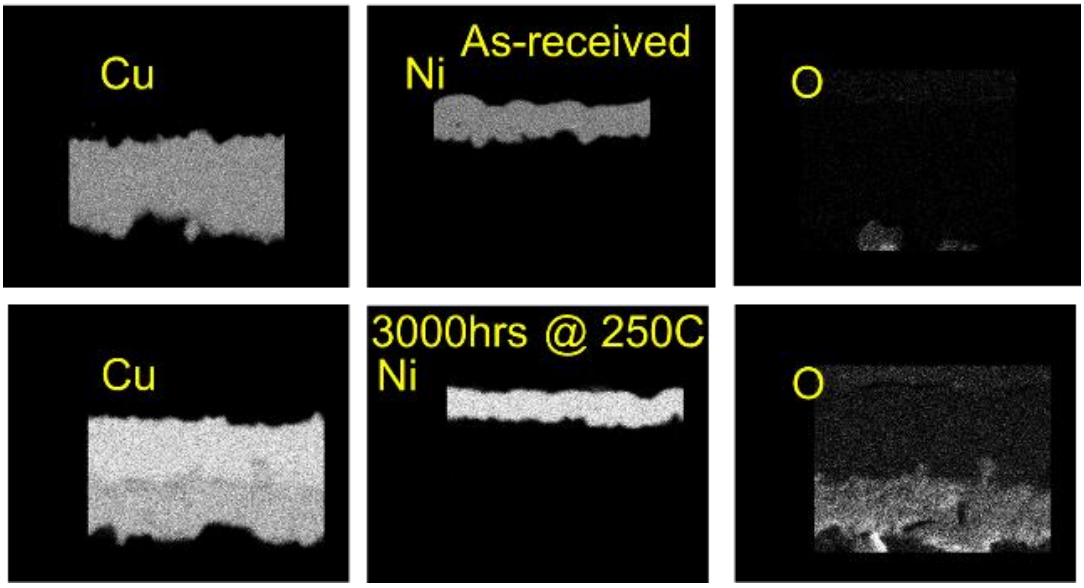



**Figure 2: EDAX scans showing increased oxygen content after ageing at 250 °C for 3000 hours.**

The Cu failures occurred earlier and with higher frequency in samples soldered using high melting point solder. This is shown in Figure 3 where the failure rates of high temperature conductive adhesives (designated D2 and D5) manufactured by curing the adhesives at 250 ˚C are compared with the soldered samples (HMP) manufactured above the melting point of the solder (~300˚C). Full pad refers to solder paste, or adhesive printed over the full area of a normal 1206 component pad or land. For half pad samples the adhesive was only printed on the inner half of the pad or land (i.e. underneath the component). The increased temperatures of HMP reflow have caused the extra degradation of the PCB and subsequent higher failure rate of the samples (Reference 5).

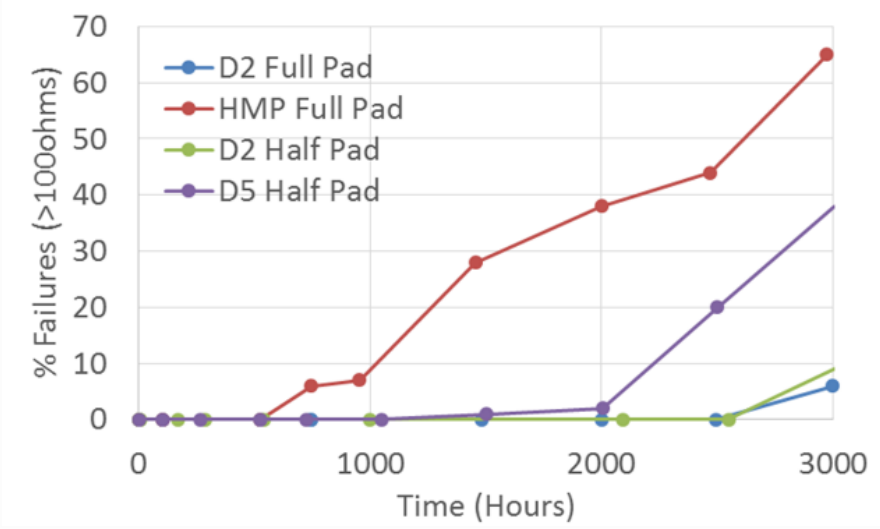



**Figure 3: Relative performance of conductive adhesive (D2 and D5) samples versus high temperature soldered (HMP) samples**

The premature failures of the Cu tracking on the test vehicles led the authors to consider using high temperature organic coatings to inhibit oxide formation.

**Phase 1: Initial Trials of Coatings**

Trials of specially formulated coatings were conducted on glass-reinforced polyimide substrate samples with surface tracks with an ENIG finish on Cu. The samples were dip coated with two coatings (designated D2 and D3) and cured at 250 °C for 30 minutes. Control samples were left uncoated. The samples were then aged for up to 425 hours at 250 °C. Examples were micro-sectioned at 0, 257 and 425 hours of aging. Optical images can be seen in Figure 4. The development of the Cu can clearly be seen as the darker area on the underside (lower) of the track. The outer (upper) surface of the Cu was protected from oxygen ingress by the ENIG surface finish. Thus the rate of oxide formation is controlled by the rate that oxygen can permeate through the underlying substrate. The coated samples showed reduced oxidation compared to the unprotected samples with the slowest rate being exhibited by the D3 samples. This material was therefore chosen for further evaluation for the remainder of the project.

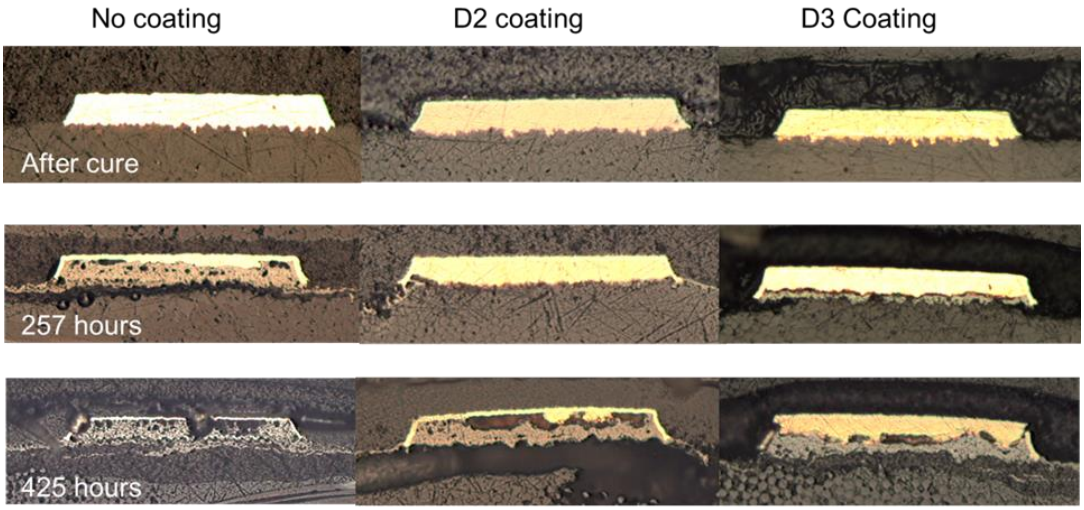



**Figure 4: Micro-sections of ENIG coated copper tracks after 0, 257 and 425 hours of ageing at 250 ˚C.**

**Phase 2: Performance assessment of coated multilayer test vehicles**

To determine the performance benefits of the high temperature coating, a four-layer PCB test vehicle was designed. A schematic of the PCB and main features of the design can be seen in Figure 5. The design consisted of 4 measurement circuits (designated R1 to R4) of decreasing feature size. The main features of each circuit were as follows:

R1: Vias = 5Xmm Ø, Tracks = 8Ymm
R2: Vias = 2.5Xmm Ø, Tracks = 4Ymm
R3: Vias = 1.5Xmm Ø, Tracks = 2Ymm
R4: Vias = Xmm Ø. Tracks = Ymm

Each measurement circuit consisted of four daisy chains connected in series. These circuits consisted of:

Upper chain: Outer layers and through vias
Upper middle chain: Inner layers and through vias
Lower middle chain: Outer/inner layers and µvias
Lower chain: Outer/inner layers and larger µvias

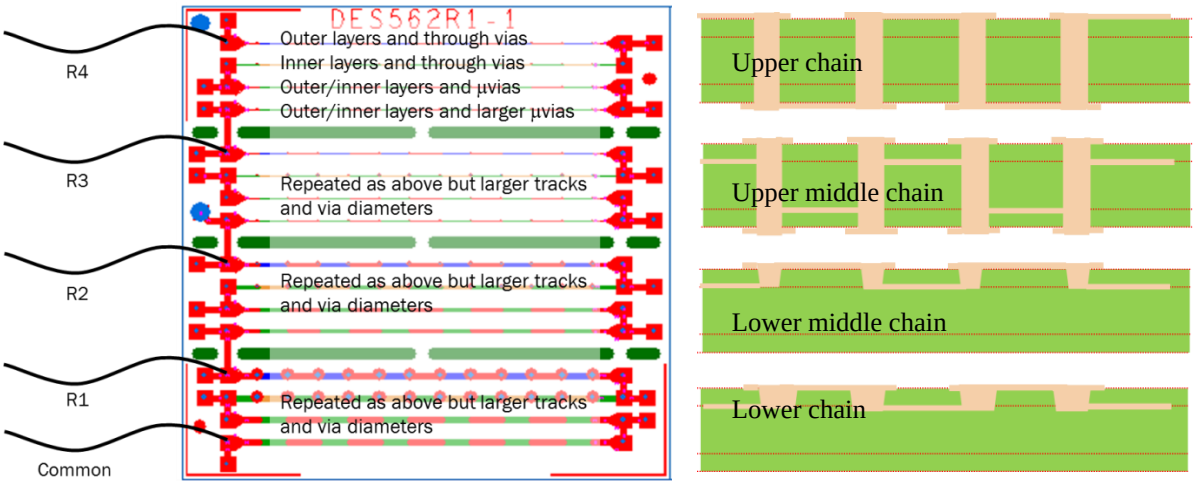



**Figure 5: Schematic of the daisy-chained test vehicle (upper left) with details (upper right) of feature types in each circuit.**

Test vehicles were fabricated in a glass-reinforced polyimide laminate system (designated PI) and a high Tg (~260 °C) glass-reinforced epoxy system (designated EP). Thermally resistant wires were soldered to the PCBs using a high Pb content solder to allow continuous monitoring. Control samples were left uncoated. To coat the coated samples, they were dip coated with the D3 coating and cured at 250˚C for 30 mins. This method ensured complete coating of the entire PCB. A resist version of the coating was developed which was screen-printed onto the upper(Resist) and upper and lower surfaces(Resist1) of the PCB with annular ring clearances around vias and uncoated edges. The test vehicles were subjected to isothermal ageing at 250˚C for up to 3500 hours. The electrical resistance of each of the four measurement chains was logged every minute using a switching system and digital resistance meter using 2-probe resistance measurements.

**Results:**

Figure 6showsthe failures for each measurement chain as a function of time for the polyimide samples. The failure criteria was a chain resistance of greater than 10 ohms. As the feature size increases (R4 < R3 < R2 < R1), it can be seen that the hours to failure increase corresponding, due to the increased volume of Cu requiring oxidation before failure occurred. Figure 7 shows some typical micro-sections of the polyimide substrates after ageing. The thinner inner layer can be seen to be almost totally consumed by oxide, with the upper surface of the outer layer again protected by the PCB surface finish. The coated samples (in orange) performed better than both the resist and uncoated samples, extending the typical time to failure by greater than 50% compared to the resist coated examples, indicating that complete encapsulation of the test vehicle was required to achieve the best performance.

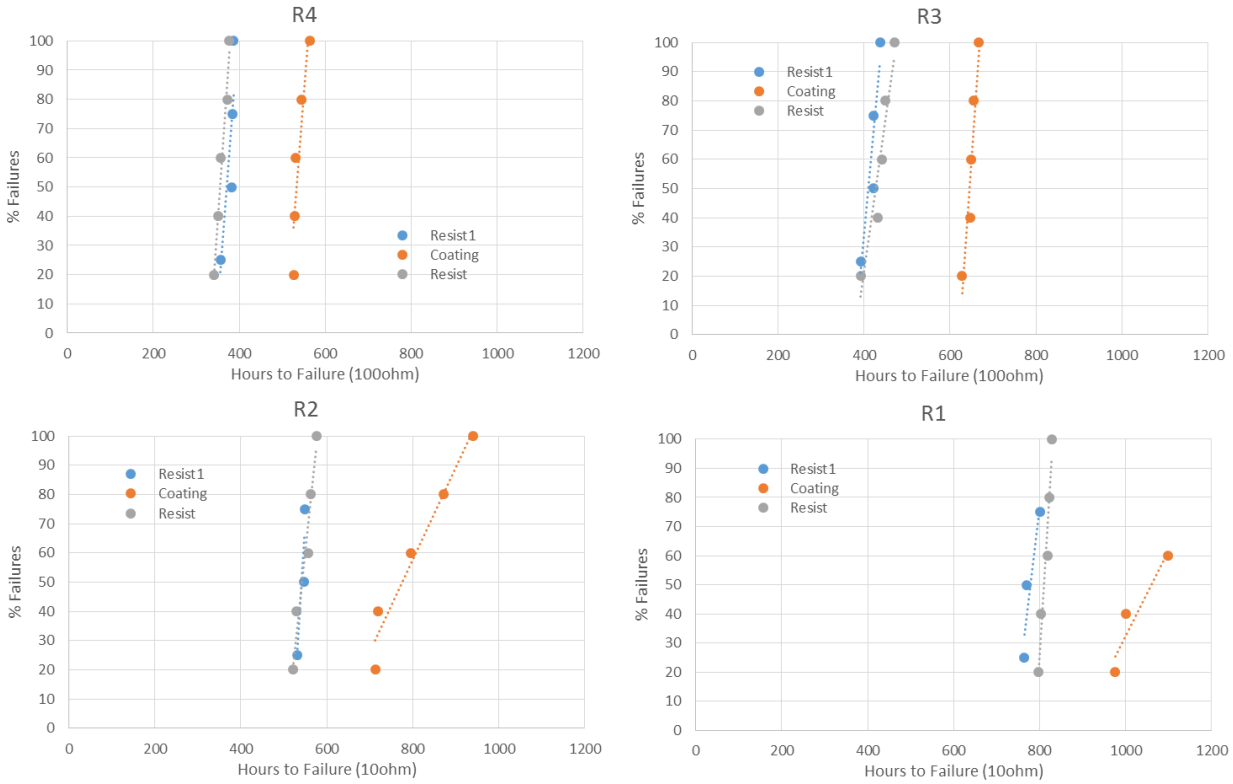



**Figure 6 : Time to failure for the four circuits of different feature sizes (R4 < R3 < R2 < R1) for polyimide substrates**

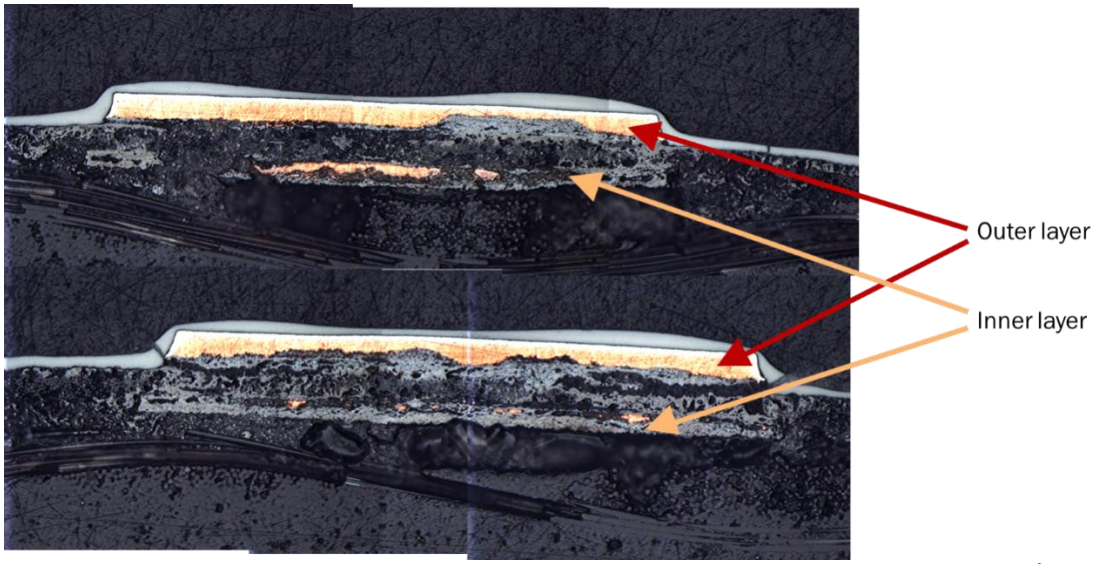



**Figure 7 : Typical micro-sections of polyimide substrates after ageing (1100 hours at 250˚C).**

For the high Tg epoxy substrates the resist was only applied to one surface of the substrate. Figure 8 shows the failures for each measurement chain as a function of time for the high Tg epoxy samples. The failure criteria was again a chain resistance of greater than 10 ohms. After 3500 hours of testing at 250 °C, the coated examples exhibited no failures, indicating an improvement in performance of at least 100% compared to uncoated substrates. As the feature size increased (R4 < R3 < R2 < R1), it can be seen that the hours to failure increase correspondingly for the uncoated substrates, due to the increased volume of Cu requiring oxidation before failure occurred. The failures in the resist coated samples is largely independent of feature size. Figure 9 shows the failure analysis of high Tg epoxy substrates after 3500 hours at250 °C (uncoated above, resist coated below) showing relative abundance of outer and inner layer failures. The only failures on the resist coated substrates

were immediately adjacent to the connection points for the soldered wires. These failures may occur earlier than the other features on the substrates as they were subjected to increased thermal stress as a result of the hand soldering of the wires used for connecting to the constant monitoring setup.

Figure 10 shows a comparison of failures rates for high Tg epoxy and polyimide substrates for the R1 feature size. This indicates that the high Tg epoxy system substrates showed improved performance compared to the polyimide substrates.

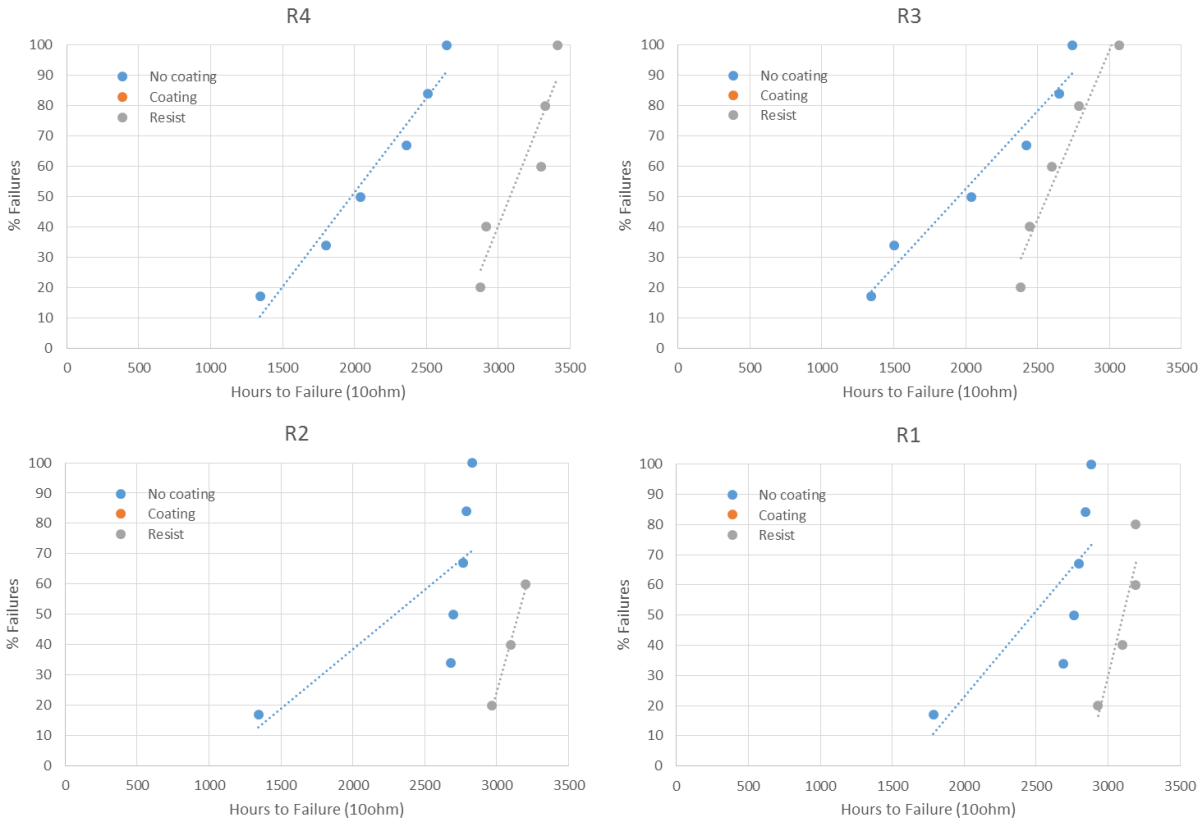
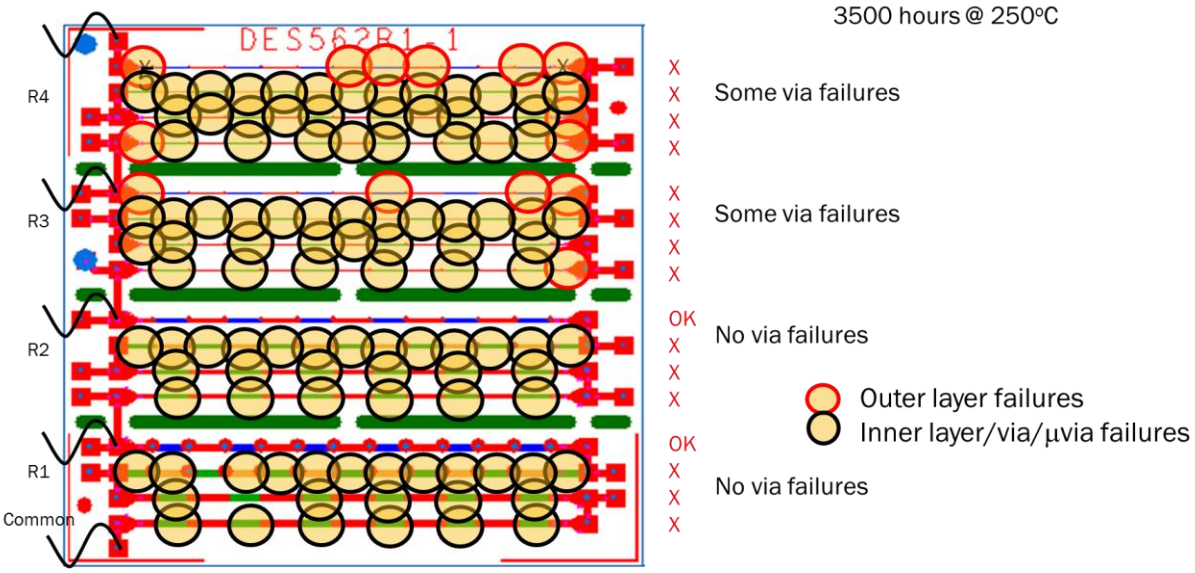



**Figure 8: Time to failure for the four circuits of different feature sizes (R4 < R3 < R2 < R1) for high Tg epoxy substrates.**



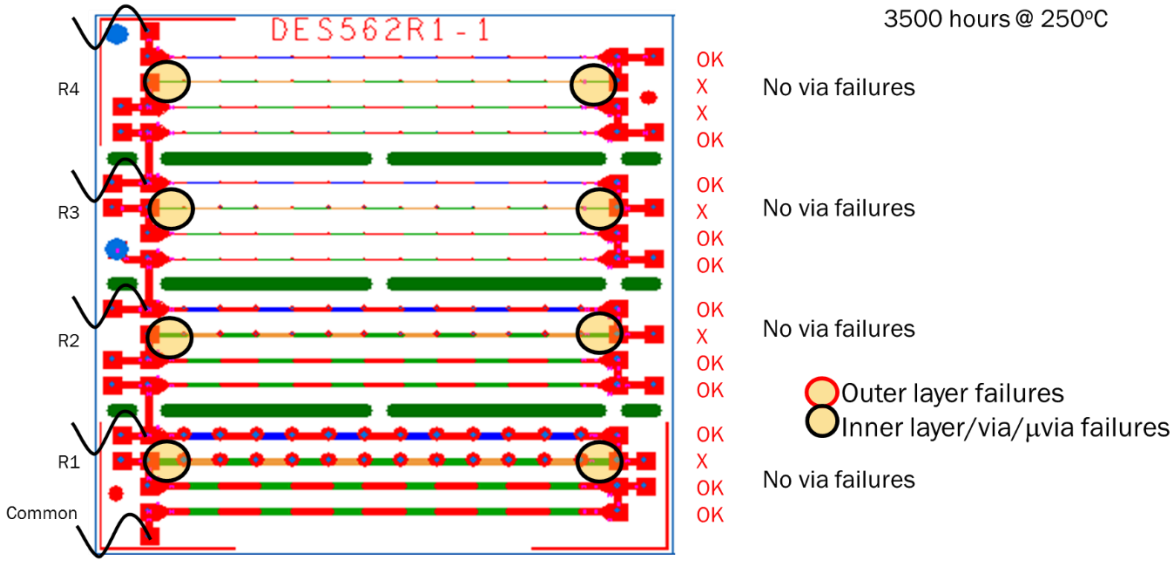



**Figure 9 : Failure analysis of high Tg epoxy substrates after 3500 hours at 250 °C (uncoated above, resist coated below) showing relative abundance of outer and inner layer failures.**

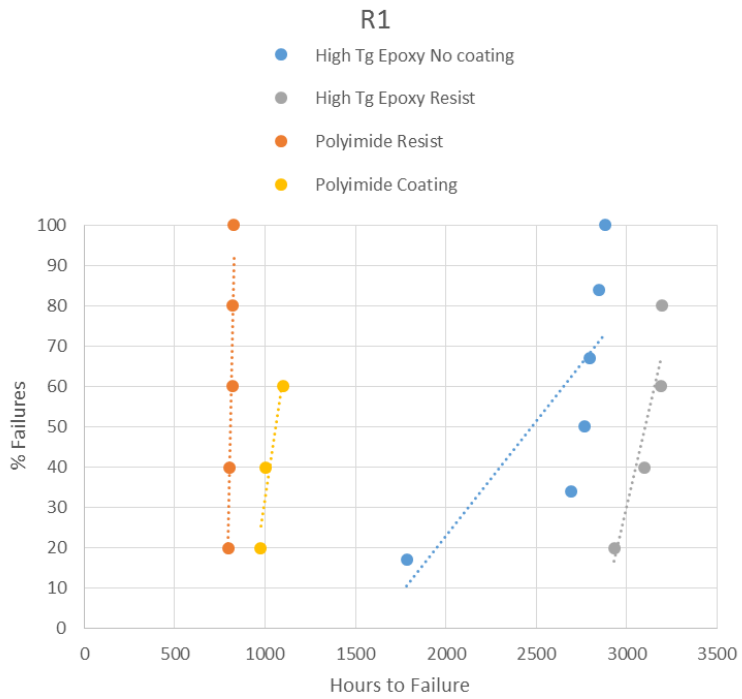



**Figure 10 : Comparison of failures rates for high Tg epoxy and polyimide substrates for R1 feature size.**

## Conclusions

This evaluation of substrate materials has shown that by careful choice of material and the use of innovative coating materials, the ability to survive isothermal ageing at 250 °C can be significantly improved. The polyimide system evaluated here showed significant resistance increases after approximately 800 hours at 250 °C for larger PCB feature sizes. By using an alternative high Tg epoxy substrate and an innovative coating material, the performance of the system has been improved to better than 3500 hours at 250 °C even for its smallest feature sizes. With the coating an improvement of at least 100% in lifetime has been shown.

**Acknowledgements**

The authors wish to acknowledge our partners in the project whose participation made the work possible; Piers Tremlett of Microsemi, and Robin Pittson and Laura Statton of Gwent Electronic Materials. We also wish to acknowledge the support of the UK Department for Business, Energy & Industrial Strategy, the National Measurement Office and Innovate UK.

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4. IPC-TM-650 2.4.24.1 Time to Delamination (TMA Method)
5. Martin Wickham, Kate Clayton, Ana Robador, Chris Hunt, Robin Pittson, Laura Statton, Tina Brown, Fiona Lambert, and Tracy Wotherspoon; Development of a High Temperature Interconnect Solution as an Alternative to High Lead or Gold Content Solders: HiTEC, May 2016, pp. 196-206.

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martin.wickham@npl.co.uk

# Issues in operating at higher temperatures

- Components
  - *SOI, SiC, passives now increasingly available*
- Packaging
  - *Non-ceramic options still a challenge*
  - *Low-cost and better CTE match to potential substrate options*
- *Interconnect*
- *Substrates*

# Available Solder Alloys for 200ºC+ operation

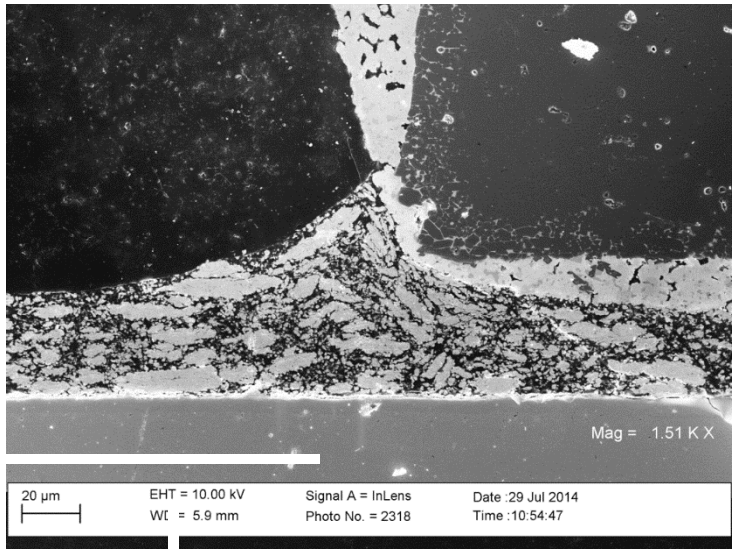
- Whilst high temperature Pb-containing alloys are ROHS exempt, RoHS2 has a more dynamic approach to exemptions, creating an automatic expiration if exemptions are not renewed by requests from industry
- Alloys with sufficient headroom are limited
- Alloys with sufficient headroom and do not contain Pb are very limited
  - *SnSb (solidus 232-235ºC)*
  - *AuSn (280ºC eutectic)*

| Asc / Dsc Liquidus oC | Temperature | Solidus oC | Asc / Dsc Largest Element (% by mass) 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|---|
| 227 | | 215 | 98.5 Sn | 1 Ag | 0.5 Cu | |
| 220 | | 217 | 95.5 Sn | 3.8 Ag | 0.7 Cu | |
| 225 | | 217 | 95.5 Sn | 4 Ag | 0.5 Cu | |
| 225 | | 217 | 96.2 Sn | 2.5 Ag | 0.8 Cu | 0.5 Sb |
| 220 | | 217 | 95.5 Sn | 3.9 Ag | 0.6 Cu | |
| 220 | | 217 | 96.5 Sn | 3 Ag | 0.5 Cu | |
| 221 | E | 221 | 96.5 Sn | 3.5 Ag | | |
| 226 | | 221 | 97.5 Sn | 2.5 Ag | | |
| 240 | | 221 | 95 Sn | 5 Ag | | |
| 295 | | 221 | 90 Sn | 10 Ag | | |
| 238 | | 232 | 97 Sn | 3 Sb | | |
| 240 | | 235 | 95 Sn | 5 Sb | | |
| 247 | | 237 | 83 Pb | 10 Sb | 5 Sn | 2 Ag |
| 285 | | 239 | 92 Pb | 5 Sn | 3 Sb | |
| 260 | | 240 | 75 Pb | 25 In | | |
| 255 | | 245 | 85 Pb | 10 Sb | 5 Sn | |
| 260 | | 252 | 90 Pb | 10 Sb | | |
| 295 | | 252 | 95 Pb | 5 Sb | | |
| 275 | | 260 | 81 Pb | 19 In | | |
| 290 | | 267 | 88 Pb | 10 Sn | 2 Ag | |
| 302 | | 275 | 90 Pb | 10 Sn | | |
| 302 | | 275 | 89.5 Pb | 10.5 Sn | | |
| 280 | E | 280 | 80 Au | 20 Sn | | |
| 296 | | 287 | 92.5 Pb | 5 Sn | 2.5 Ag | |
| 310 | | 290 | 90 Pb | 5 In | 5 Ag | |
| 304 | | 299 | 95.5 Pb | 2.5 Ag | 2 Sn | |
| 313 | | 300 | 95 Pb | 5 In | | |
| 310 | | 300 | 92.5 Pb | 5 In | 2.5 Ag | |
| 320 | | 300 | 98 Pb | 2 Sb | | |
| 303 | E | 303 | 97.5 Pb | 2.5 Ag | | |
| 365 | | 304 | 94.5 Pb | 5.5 Ag | | |
| 364 | | 305 | 95 Pb | 5 Ag | | |
| 312 | | 308 | 95 Pb | 5 Sn | | |
| 309 | E | 309 | 97.5 Pb | 1.5 Ag | 1 Sn | |
| 235 | MP | | 99 Sn | 1 Sb | | |
| 292 | MP | | 90 Pb | 5 Ag | 5 Sn | |

Reference 1

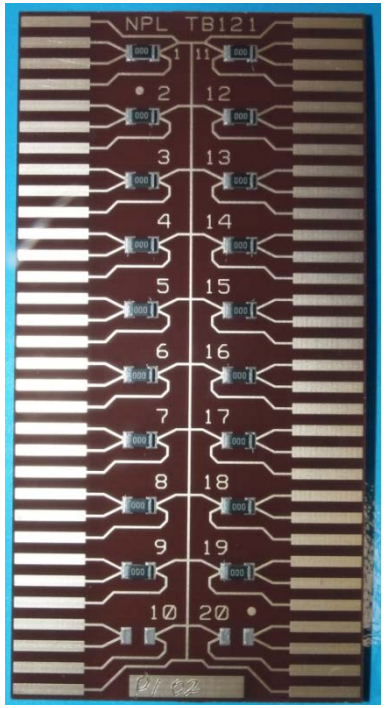
# Ongoing High Temp Interconnect Research

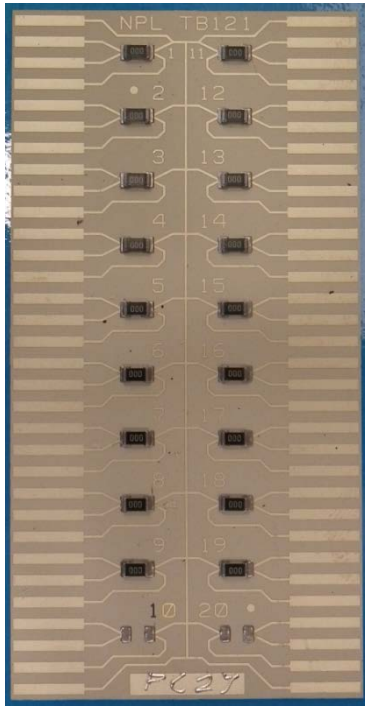
- High temperature conductive adhesives project (Reference 2)
  - *Comparison with HMP solder*
- On-going projects
  - *High temperature protective coatings (Reference 3)*
  - *Additive manufacture of high temperature substrates (Reference 4)*

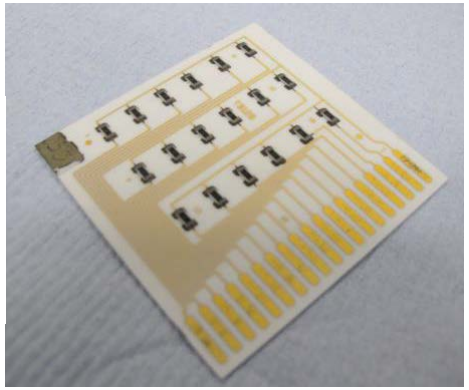


# High temperature conductive adhesives project

- 18 R1206 jumpers on polyimide/glass, high temp. PCB (Reference 5) (or ceramic substrates
- Immersion Au (PCB) or thick film Au (ceramic)
- Silicone/Ag adhesives D2 and D5, and HMP solder
- Stencil print
  - *75$\mu$m laser cut s/s*
  - *Print/print, aperture 100% or 50% of pad*
  - *Auto-placement*
  - *Batch oven cure 35 mins at 250$^{o}$C*
  - *HMP (PbSnAg) – Reflow at 325$^{o}$C (peak)*
- Components
  - *PtAg terminations (not Sn)*
  - *1 ohm*

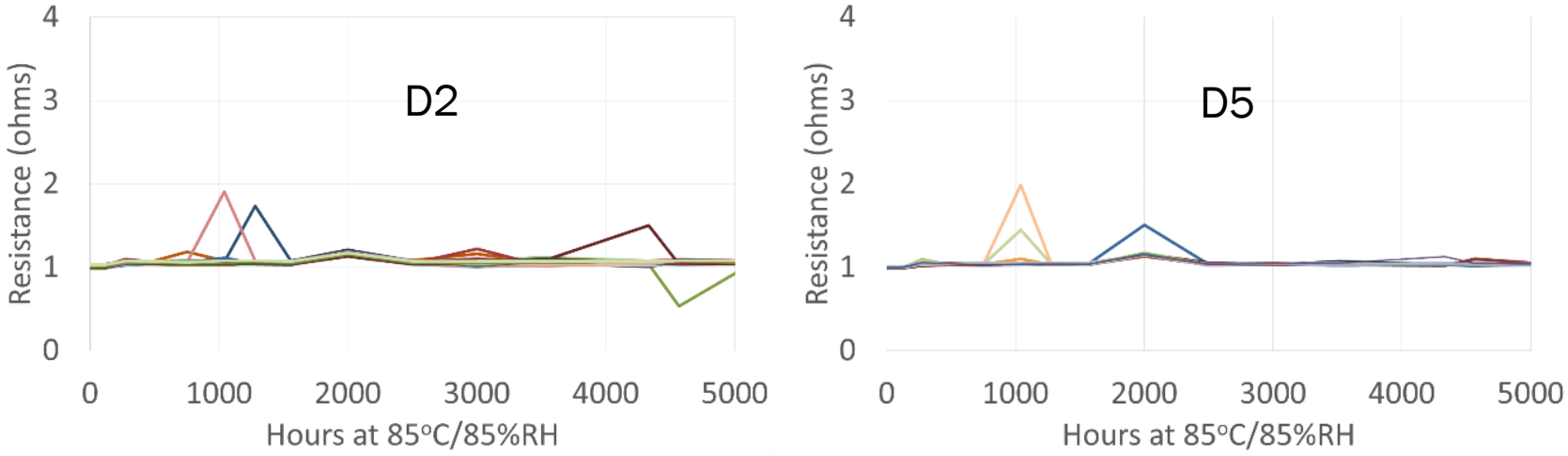


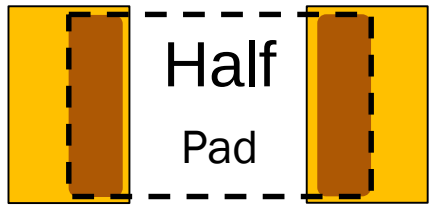
# Damp Heat Testing

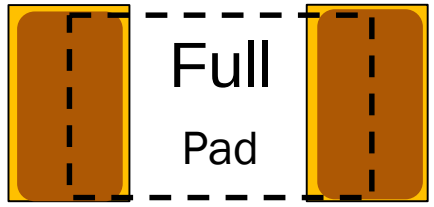
- 5000 hours testing completed at 85°C/85%RH
- Silicone based conductive adhesives
- PtAg terminated components



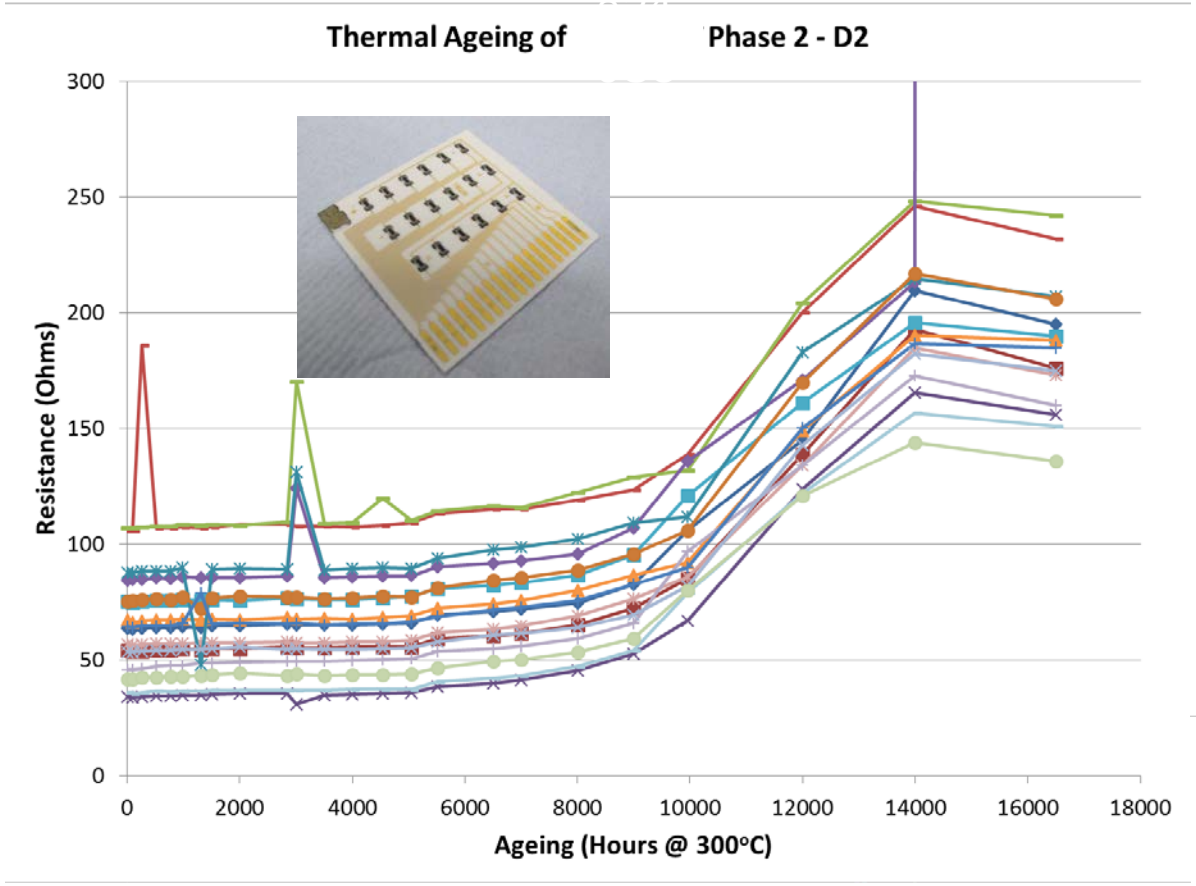
# Thermal Cycling – Constant monitoring

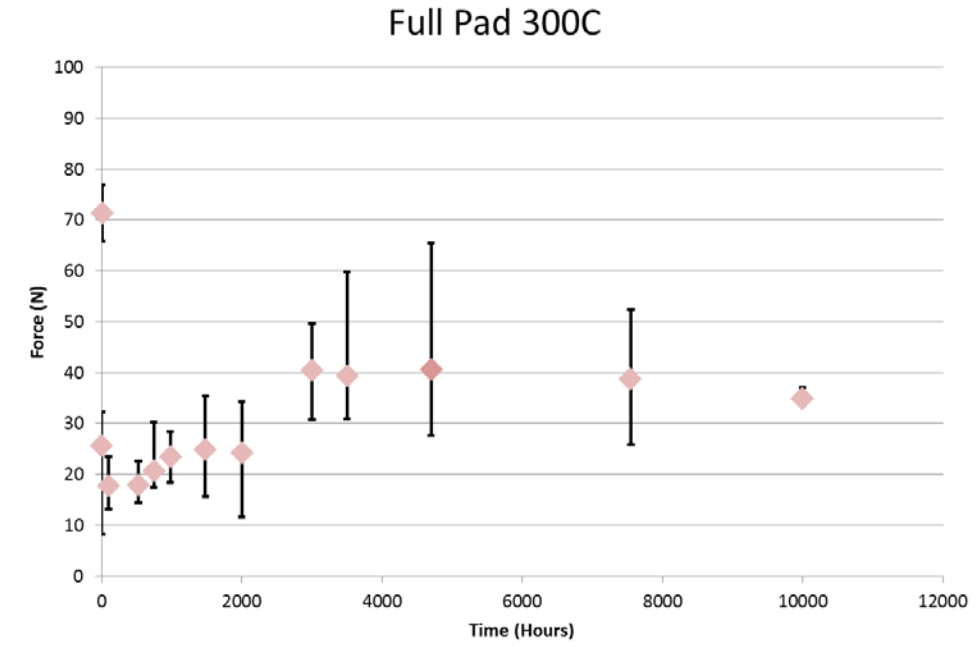
- 3000 cycles completed - *-55°C to 125°C*
  - *D1*
    - *Half pad – No failures*
    - *Full pad – No failures*
  - *D5*
    - *Half pad – No failures*
  - *SAg1*
    - *Half pad – No failures*
  - *SAg2*
    - *Half pad – No failures*
  - *HMP*
    - *Full pad - 10% failures (mostly within first few hundred cycles)*



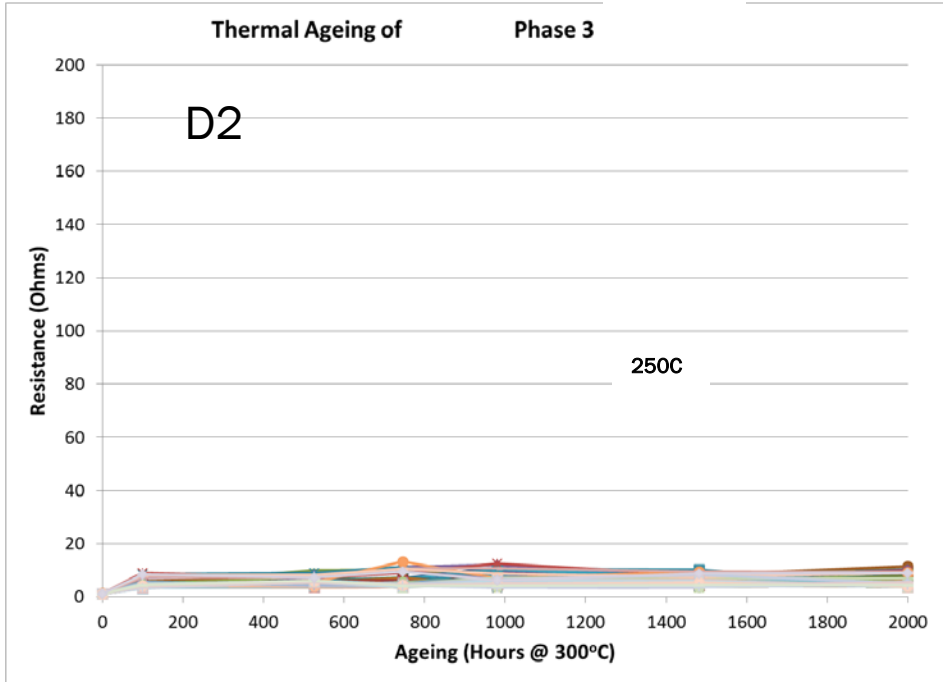



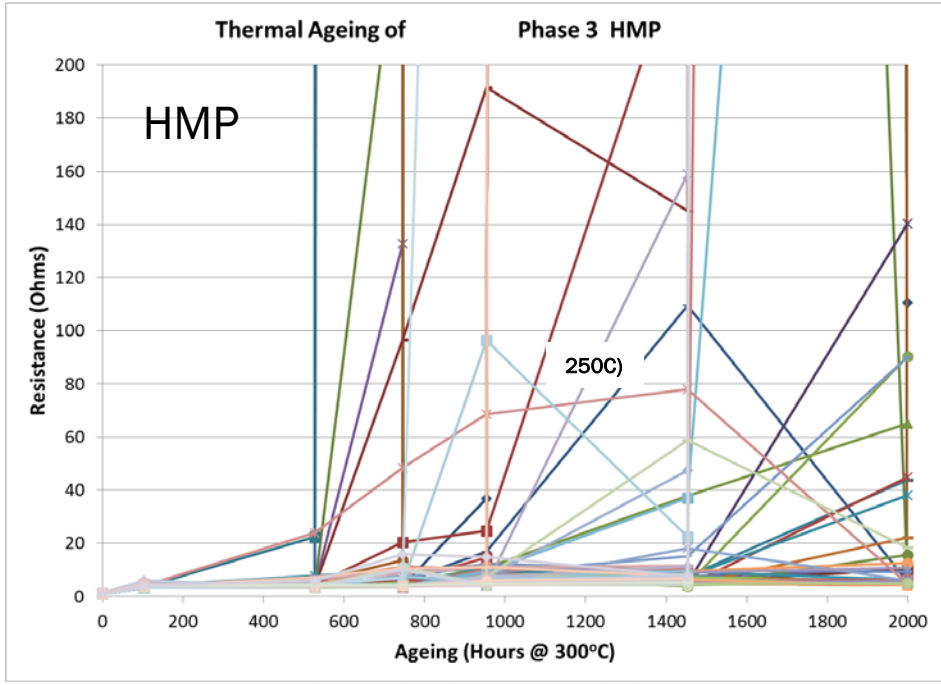
# Isothermal Ageing at 300°C



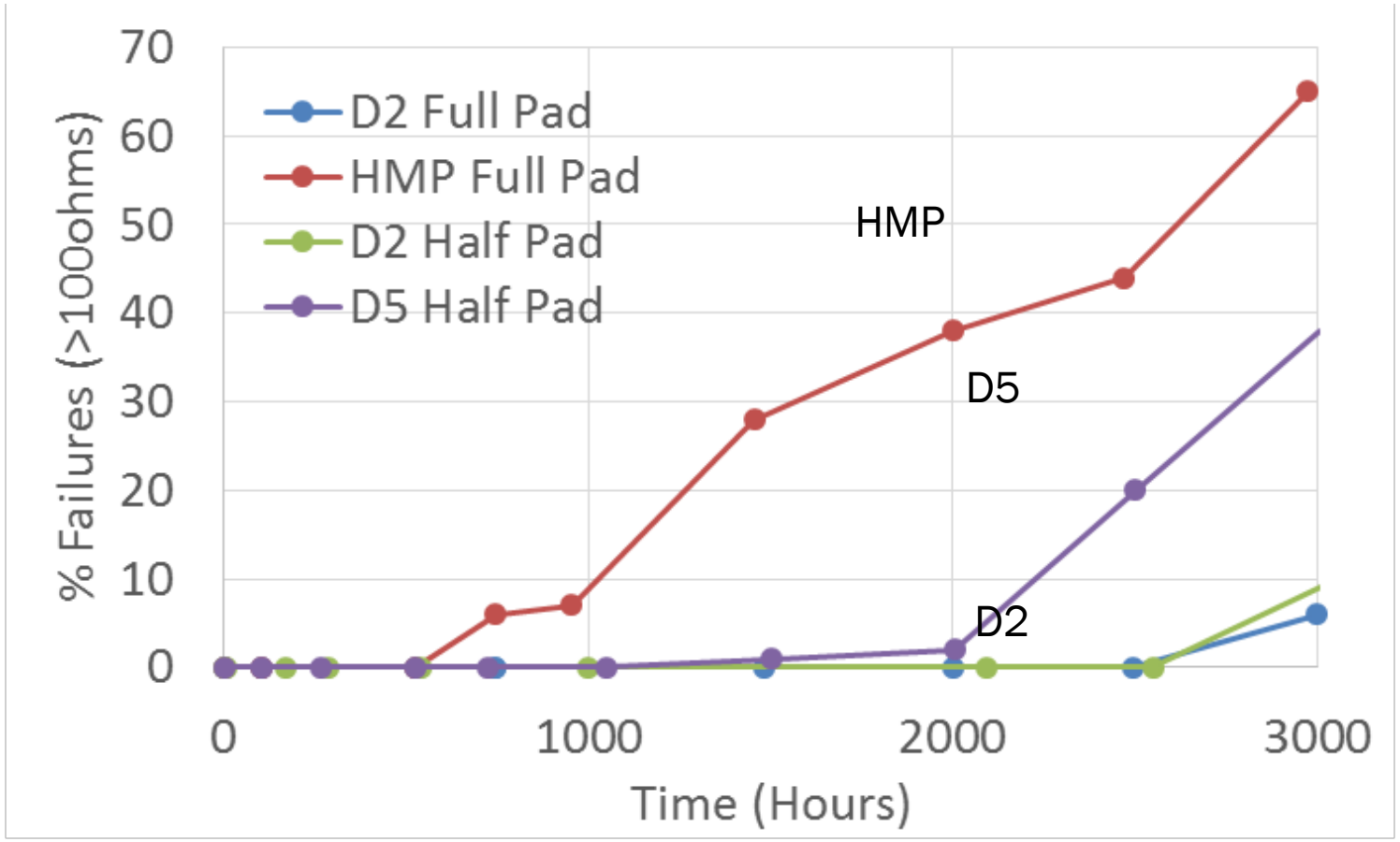



# Comparison Thermal Ageing @ 250ºC

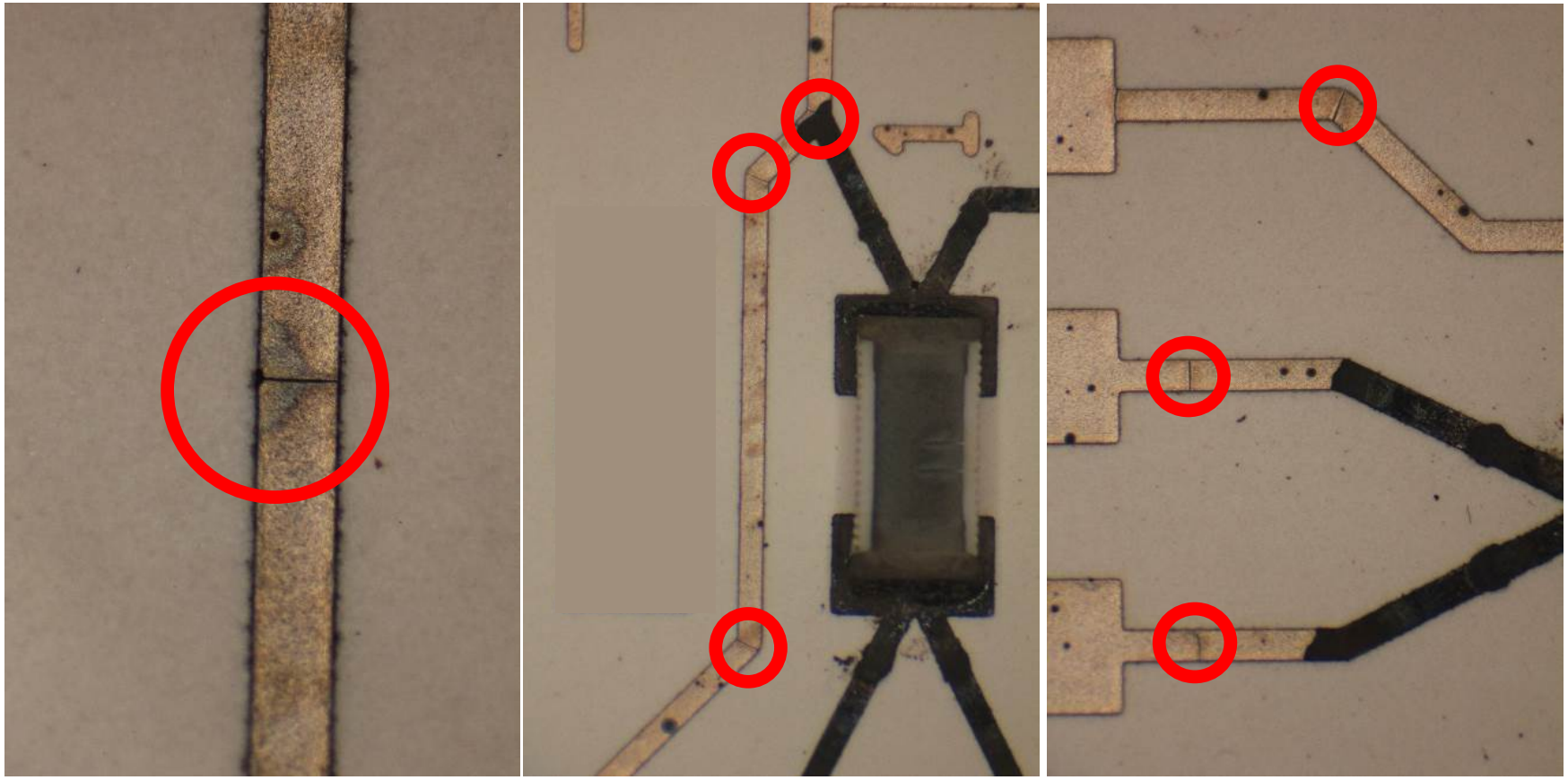


# Comparison of ageing at 250ºC

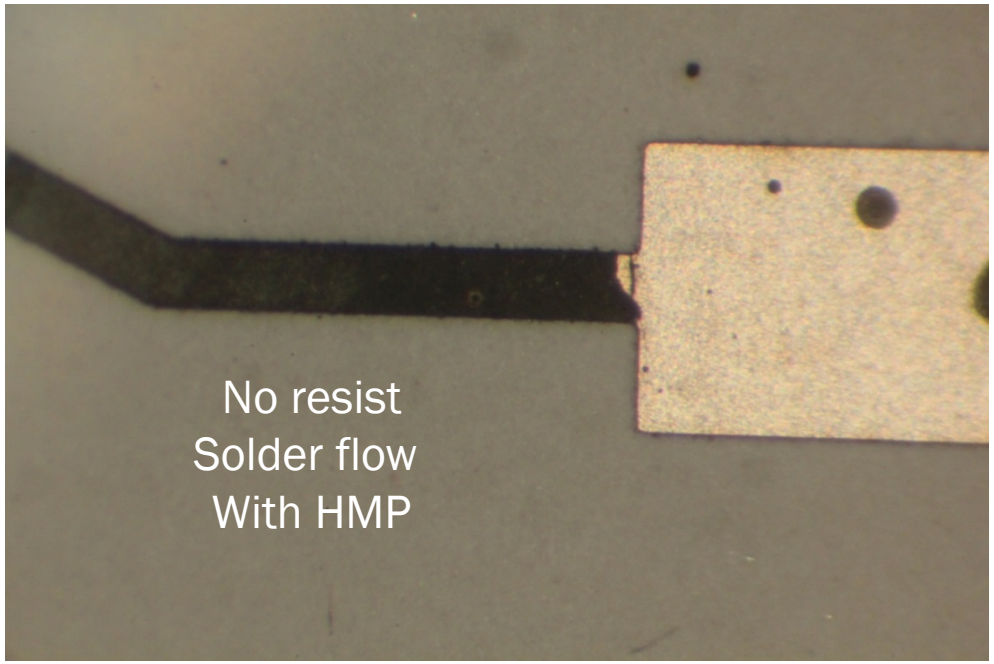


# Ageing at 250ºC - Cu failures



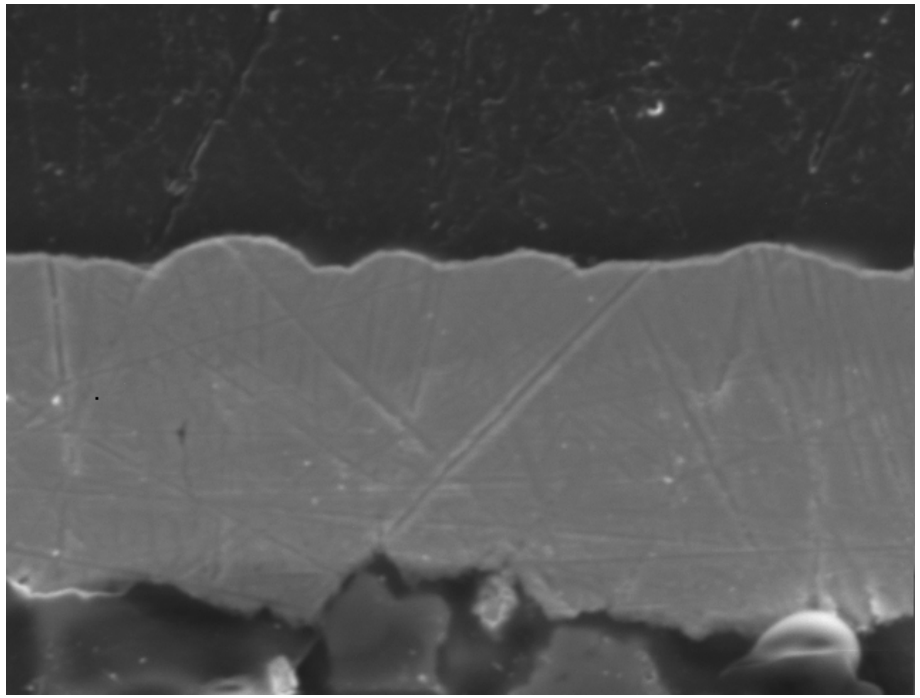
# Advantages of forming interconnect at or below operating temp

- Earlier track failures for HMP than for Silicone/Ag samples
- Under investigation but hypothesis is that increased temperatures of HMP reflow (peak ~ 325$^{o}$C) have caused extra degradation of PCB

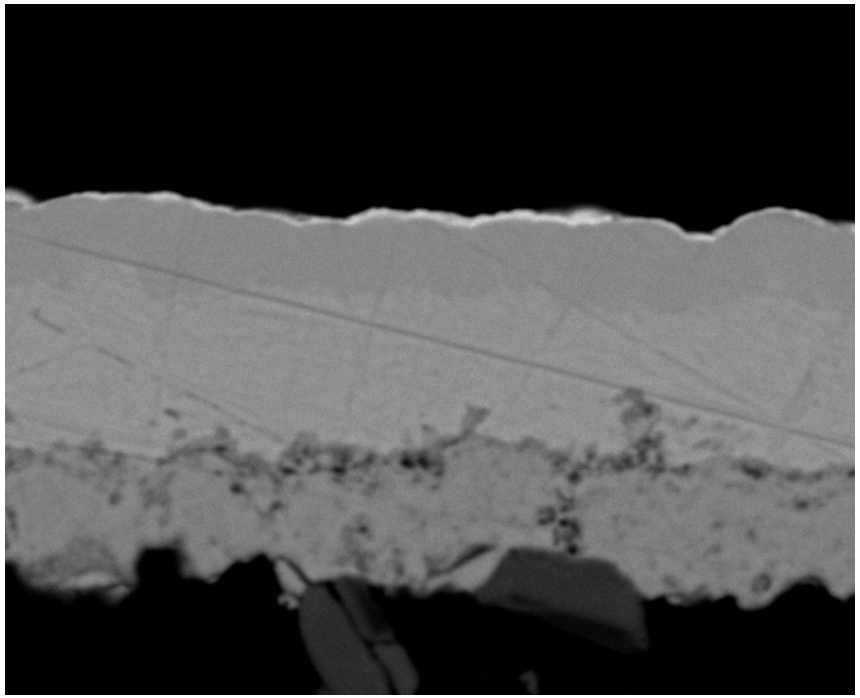


# Oxide growth – ENIPIG

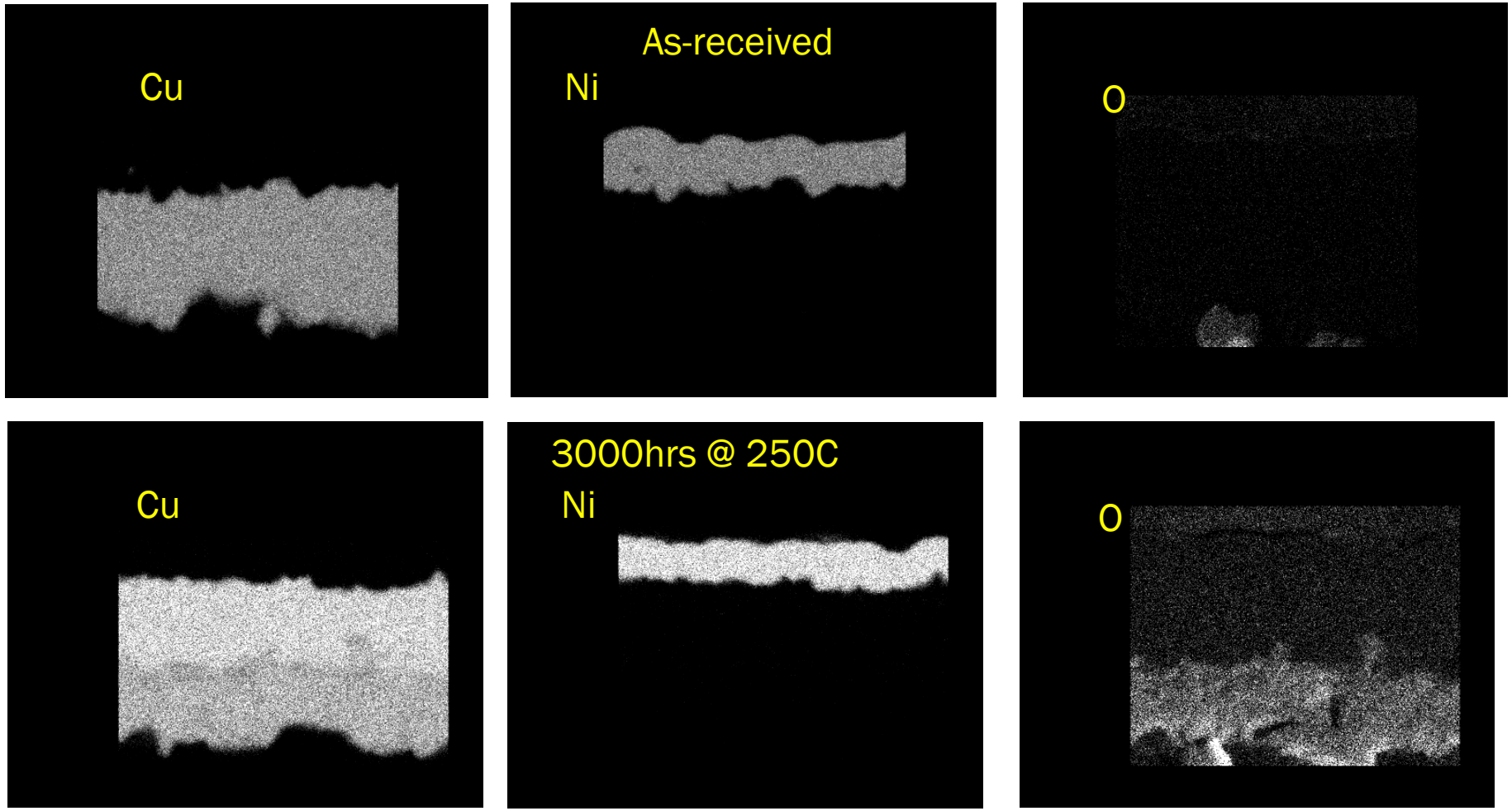
As-received



3000hrs @ 250C



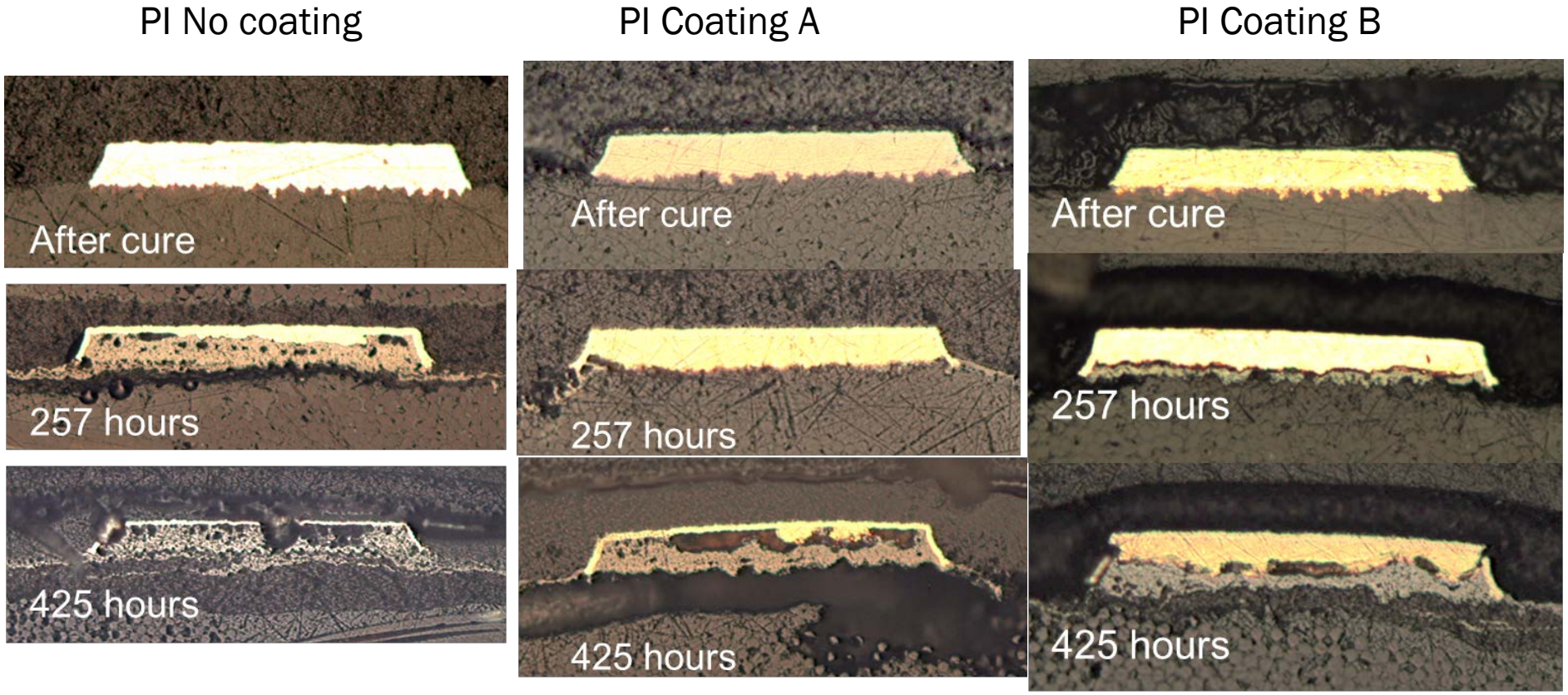
# Oxide growth – ENIPIG EDAX scans



# High temperature protective coatings project [Reference 3]

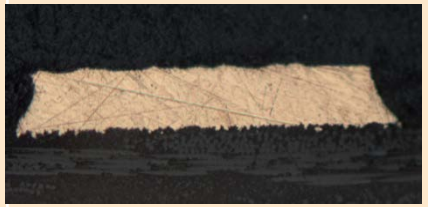
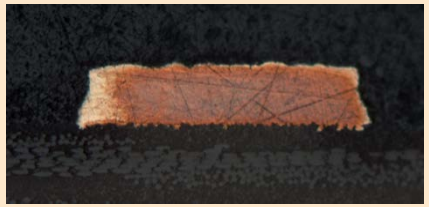
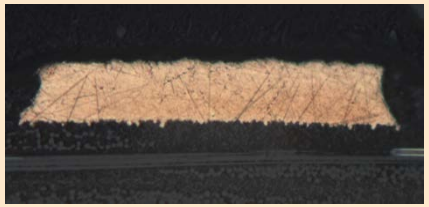
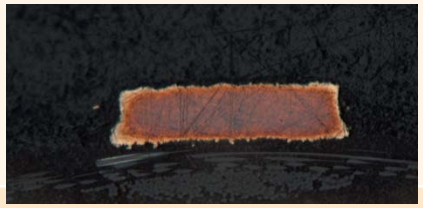
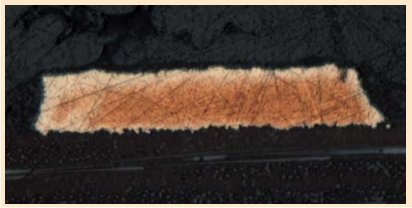
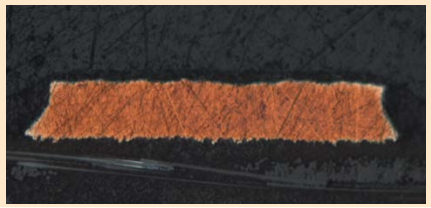
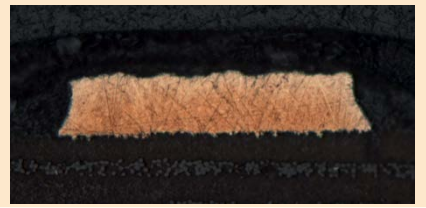
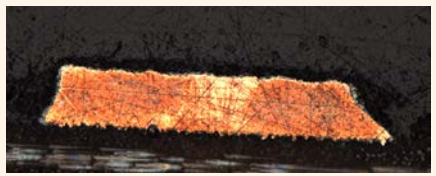
- Development of protective coatings to improve performance of organic PCBs at high temperatures
- Inhibiting copper track oxidation
- Potential for high temperature solder resist applications
- Based on silicone resin systems
- Initial trials using immersion coatings

# Phase 1: Improved High Temperature PCB Performance, Isothermal Ageing at 250°C




- Upper surface of exterior tracks protected by Ni/Au finish

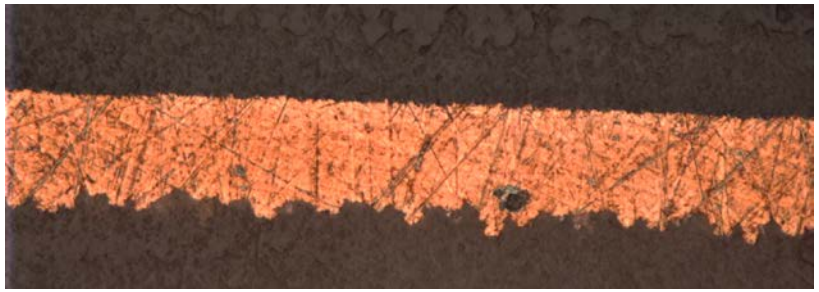
# Long Term Ageing: High temperature PCB Material

| Aged at 250 °C | No Coating | D2 | D3 |
|---|---|---|---|
| 257 hours |  |  |  |
| 425 hours |  |  |  |
| 1000 hours |  |  |  |
| 2000 hours |  |  |  |

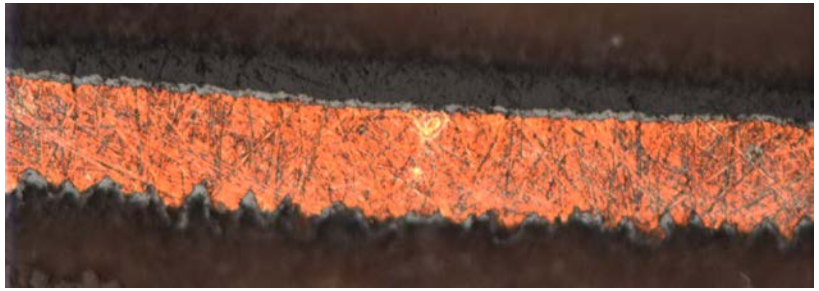
*All boards discussed in this presentation were put through a curing process: this was 30 minutes at 250 °C .

# Inner layer comparison 2000 hrs at 250C
# High temperature PCB material

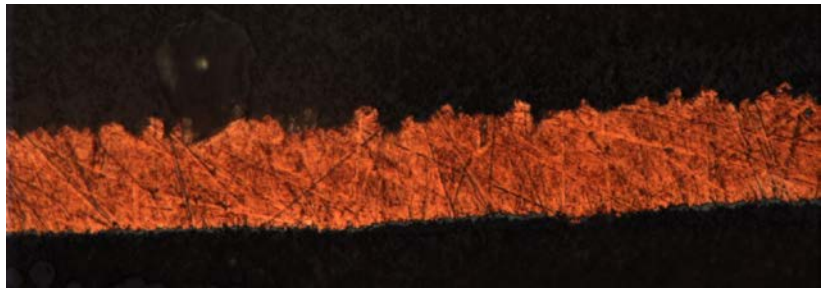
No coating



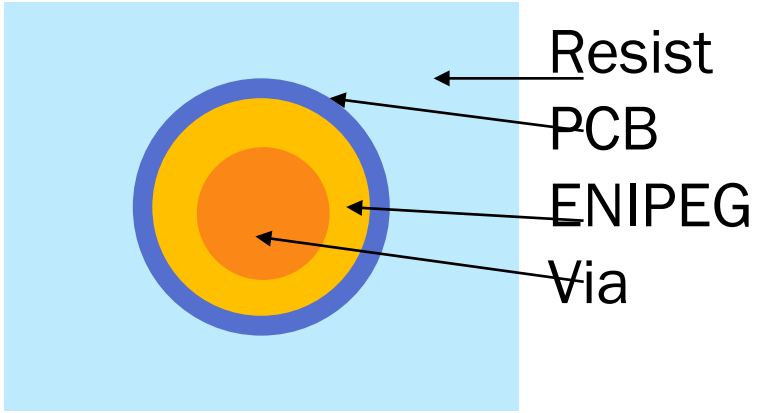
D2



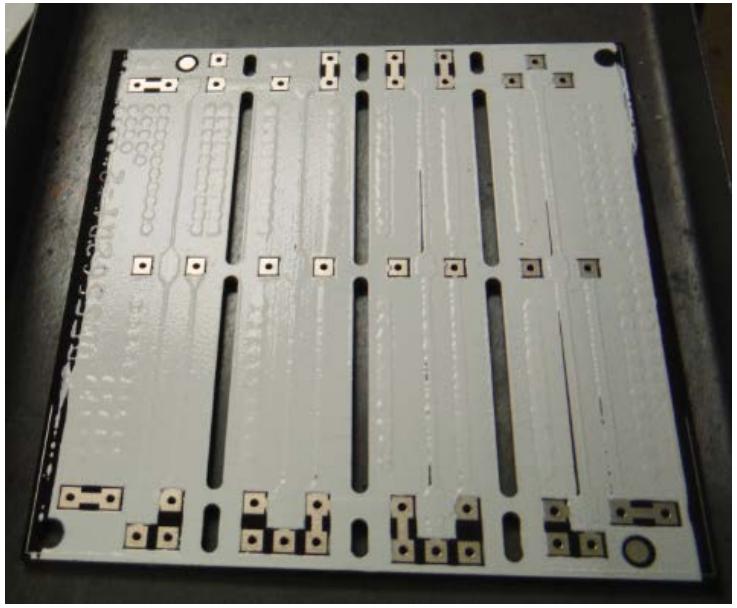
D3



# Phase 2: Coating and resist ageing




- Test vehicle incorporating variety of features and sizes inc. inner layers, vias and μvias
- D3 coating applied by immersion after connection of test leads using high temperature solder.
- Resist version applied by screen printing on both sides
  - *Edges of PCBs exposed*
  - *Annual ring around vias*



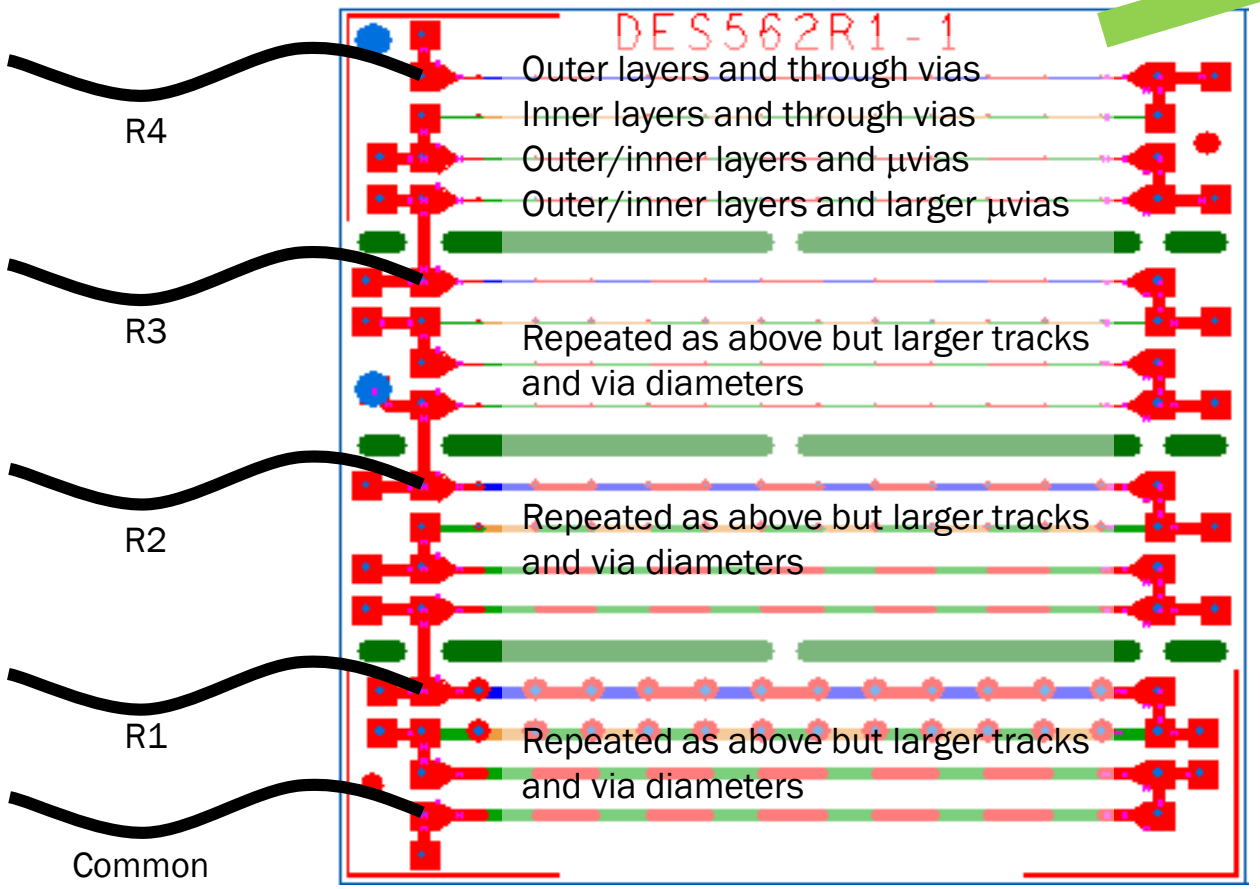
[Reference 6]

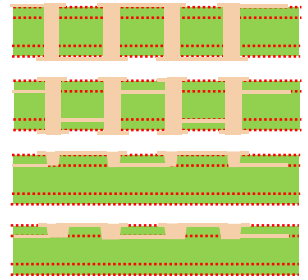
# Resistance monitoring at 250ºC

- 40 channel multiplexers capable of 2-probe resistance measurements were purchased.
- Base units can accommodate 3 multiplexing cards, hence 120 channels per base unit.
- 4 base units, totalling 480 channels.

# Test Vehicle Design

Each measured channel incorporates outer tracks, inner tracks, µvias and through vias



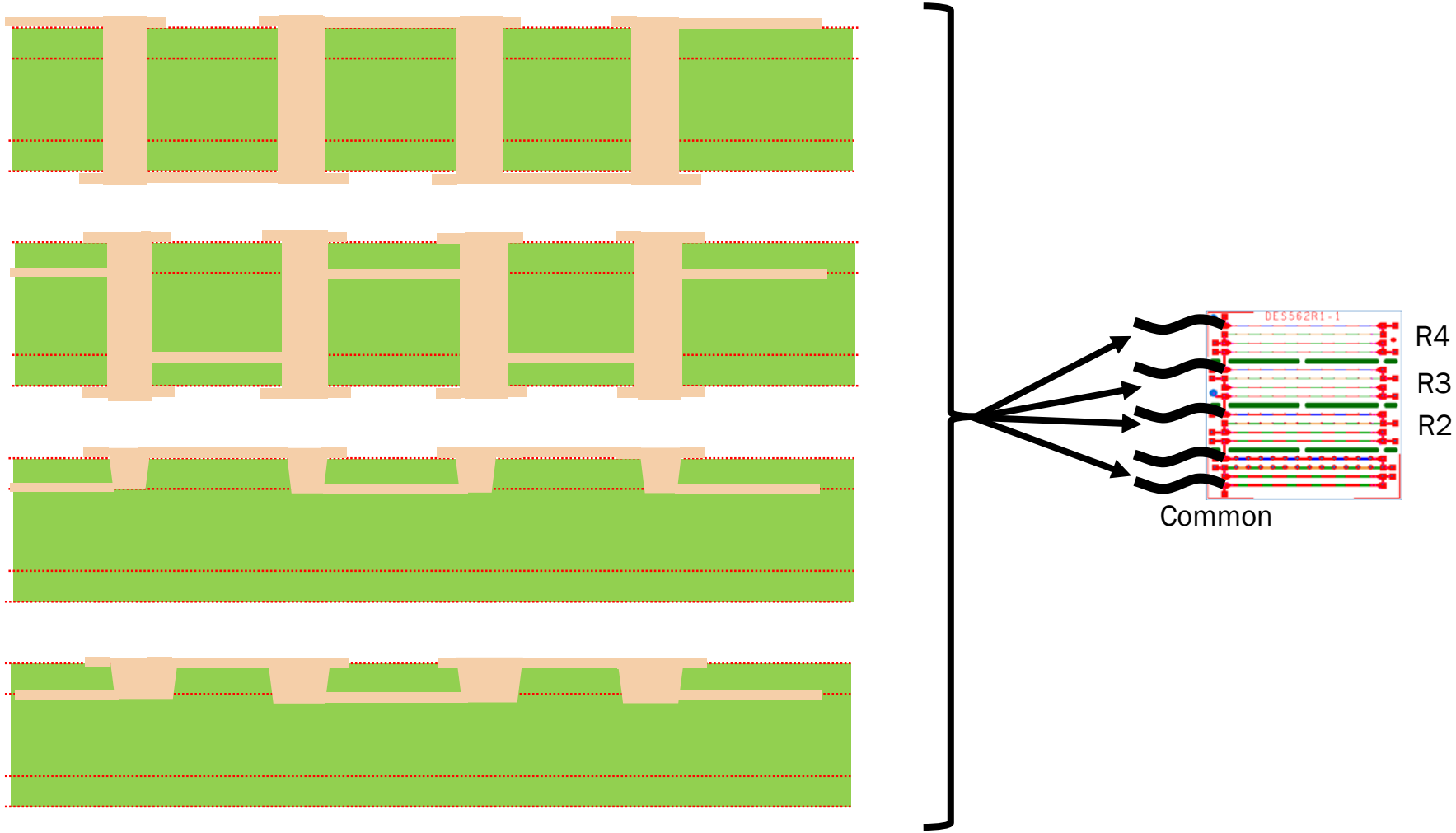
Vias = Xmm Ø
Tracks = Ymm

Vias = 1.5Xmm Ø
Tracks = 2Ymm

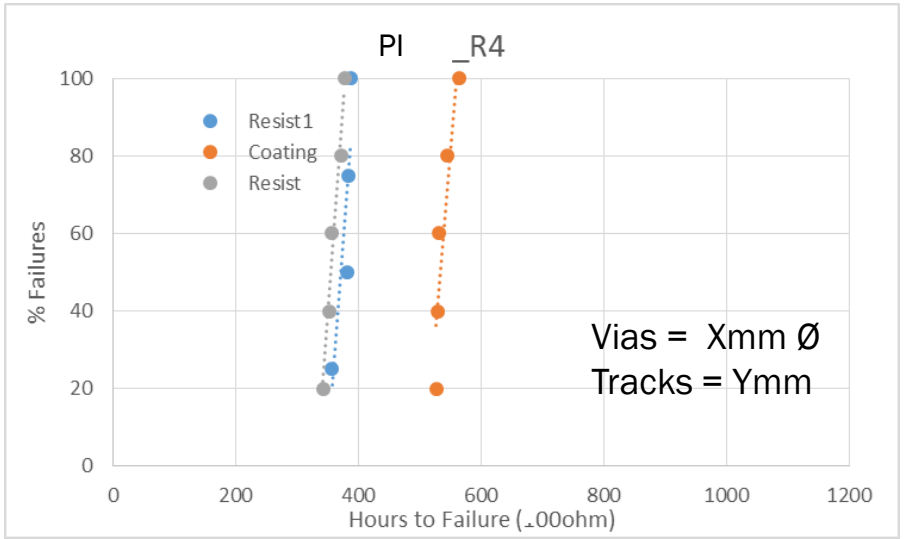
Vias = 2.5Xmm Ø
Tracks = 4Ymm

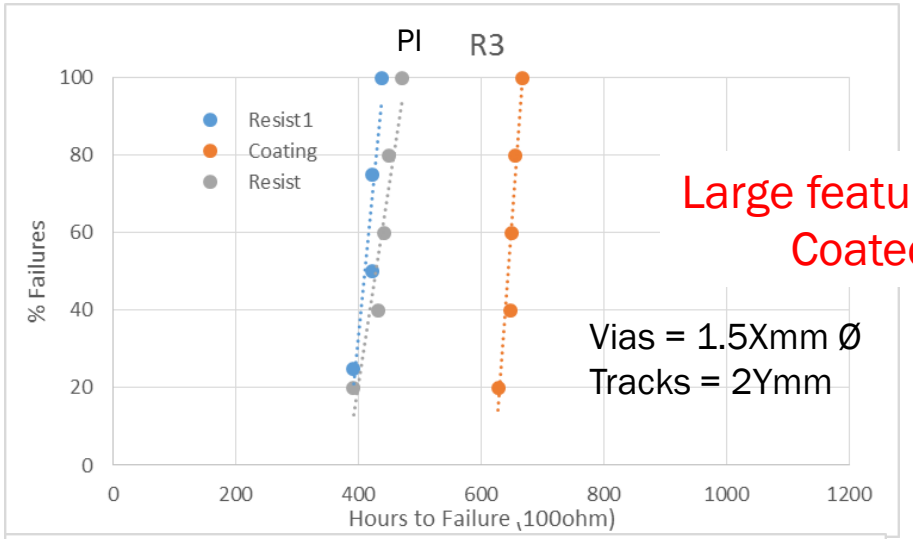
Vias = 5Xmm Ø
Tracks = 8Ymm

# Structure within each group (R1, R2, R3, R4)

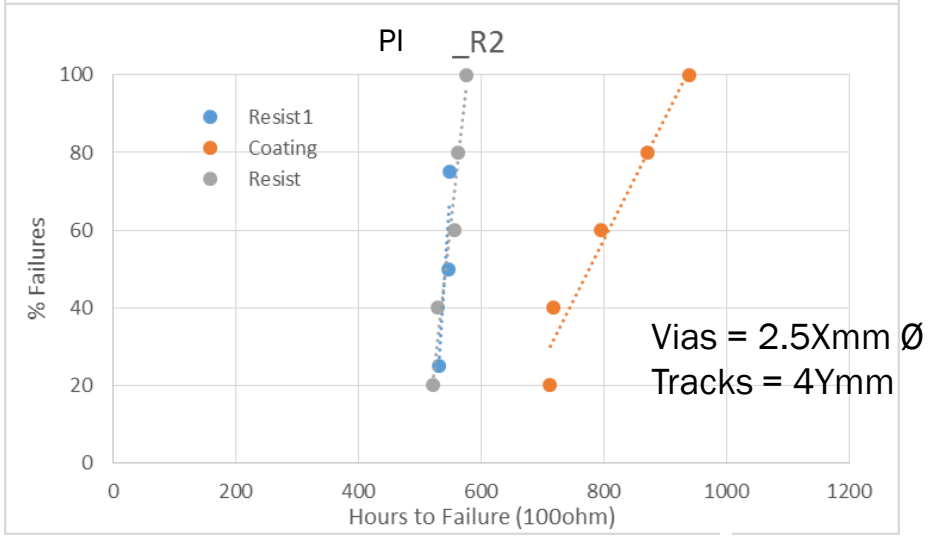


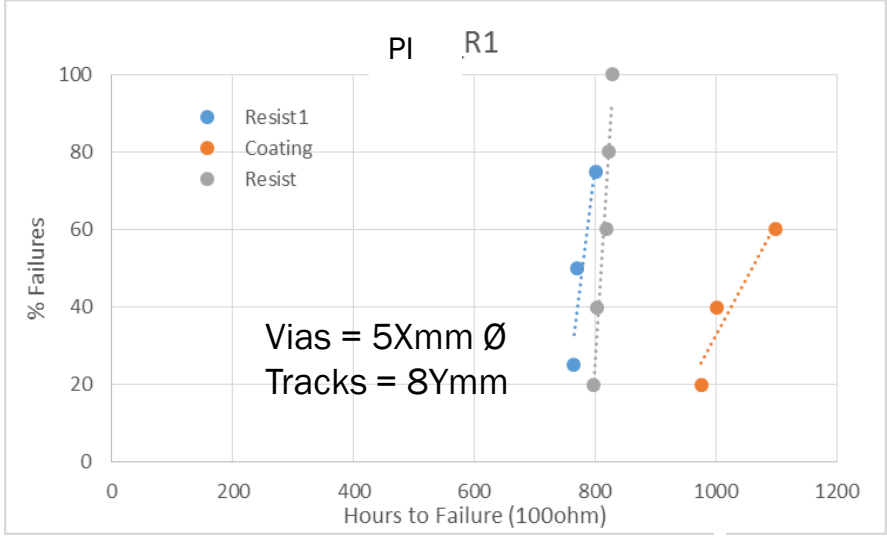
# Polyimide comparison @ 250C



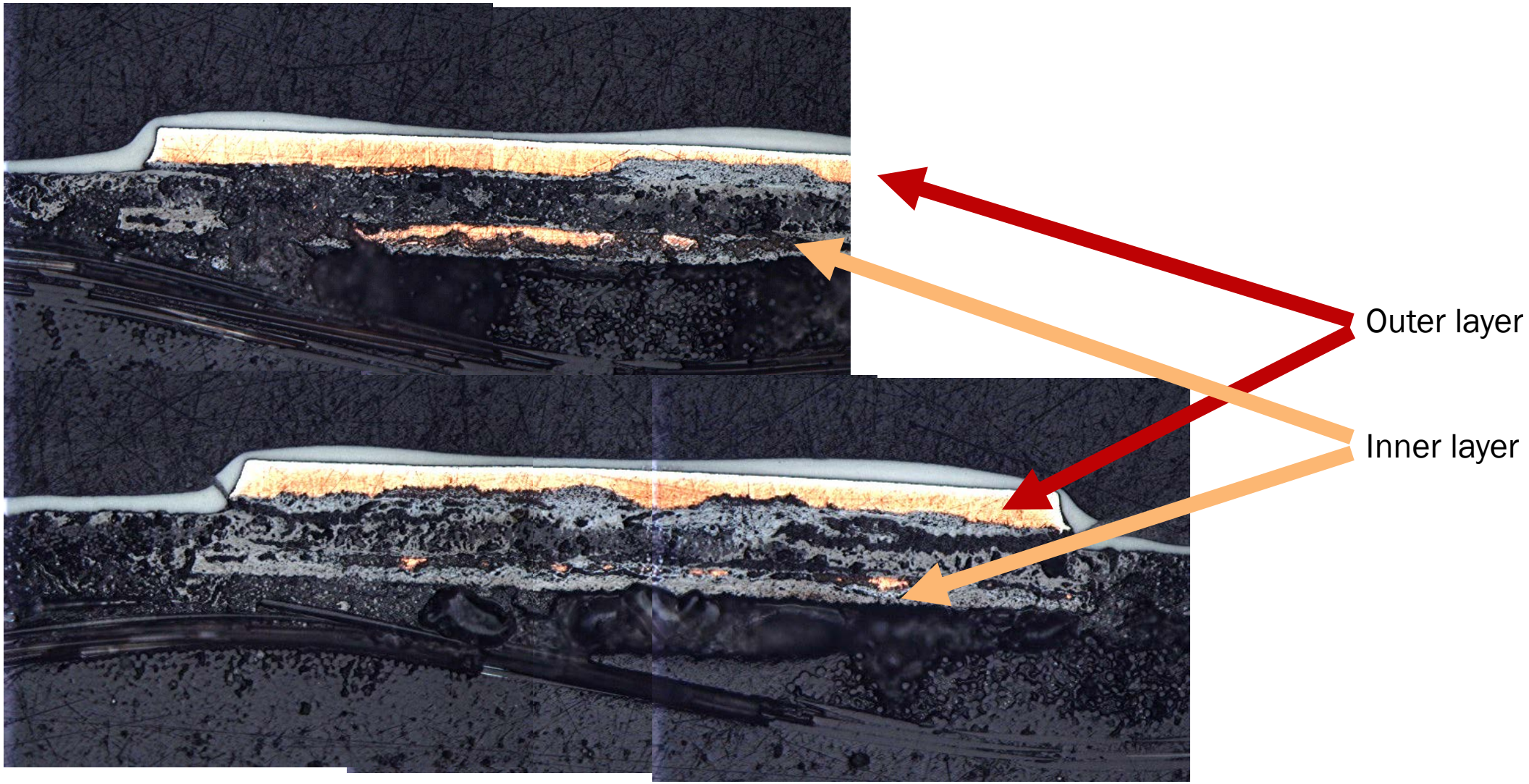




Large feature size better
Coated better

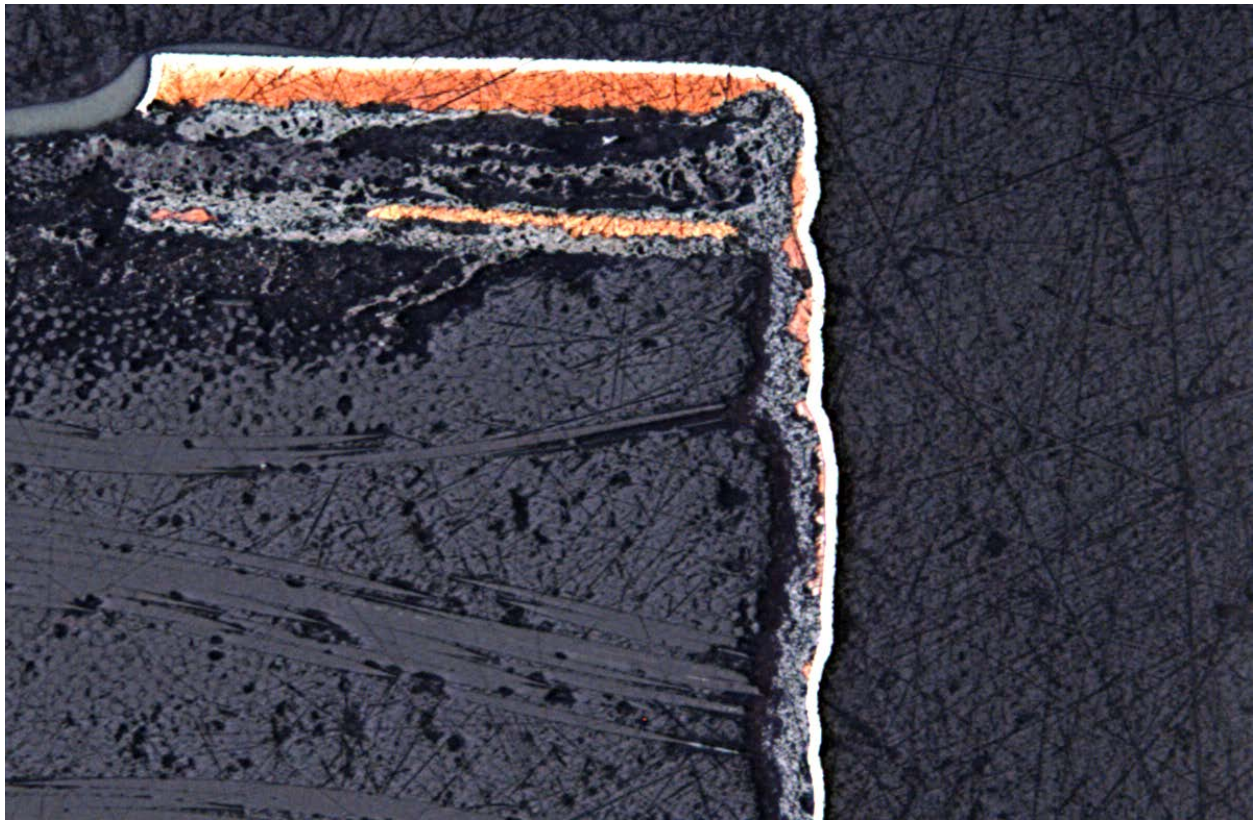


# Polyimide Resist PCB - 1100 hours at 250ºC

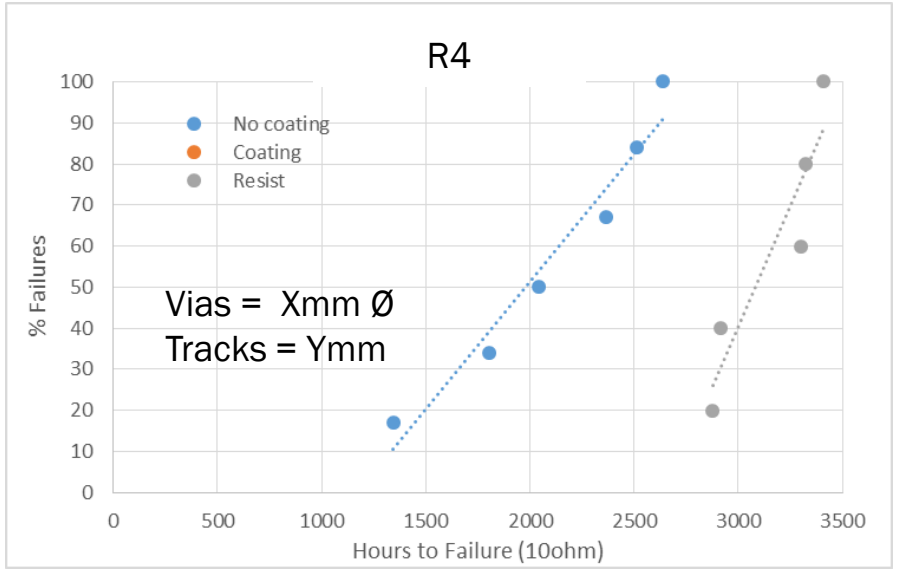


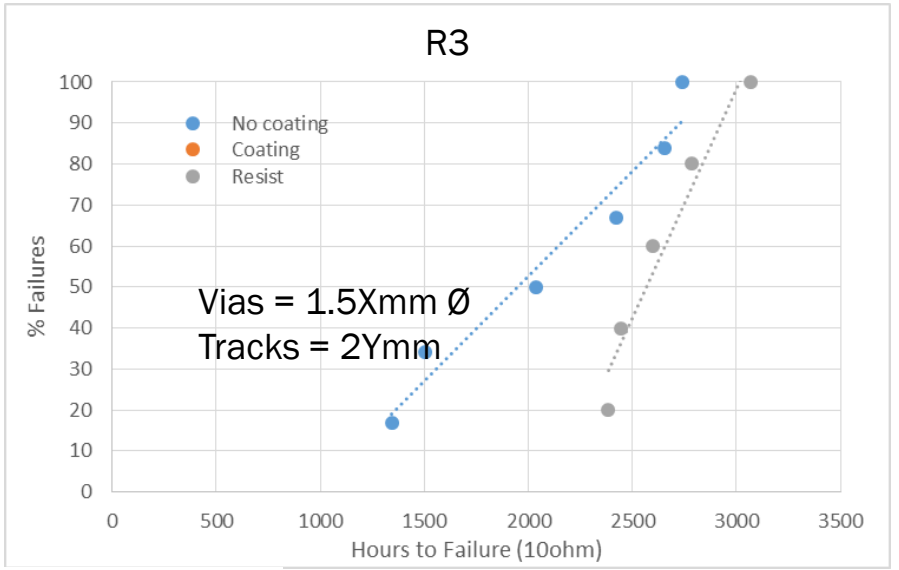
# Significant inner layer and via wall oxidation



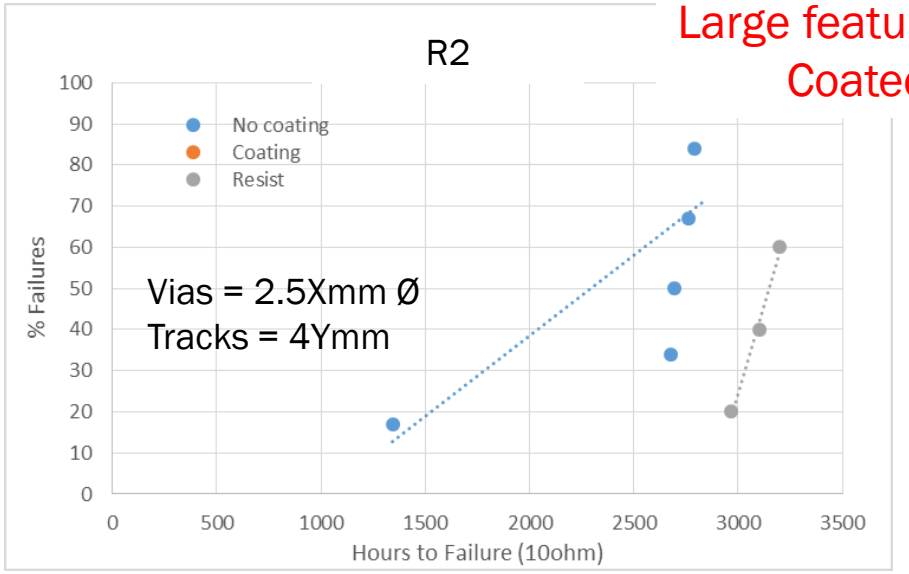
Polyimide Resist PCB - 1100 hours at 250°C

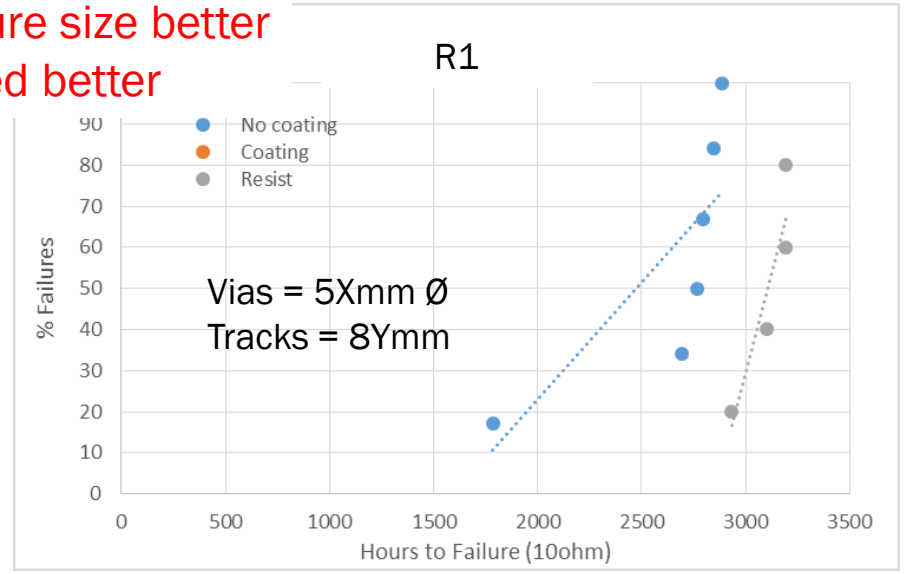
# High temperature PCB material comparison @ 250C



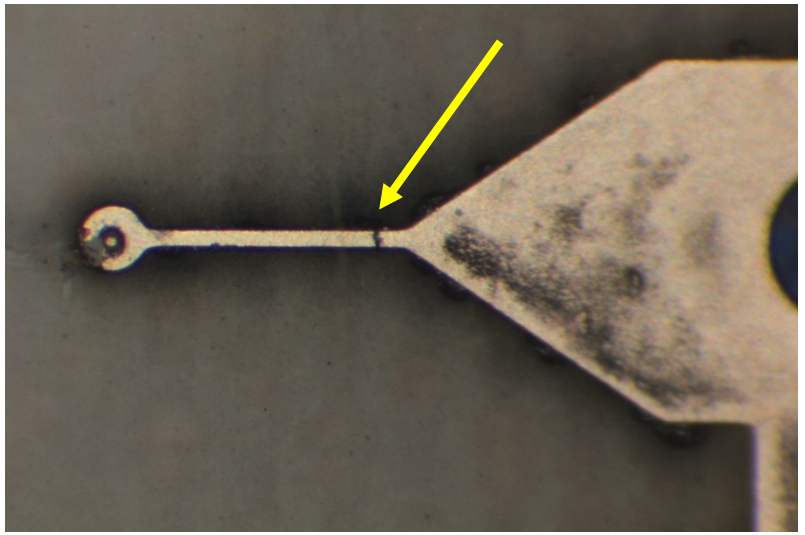

Large feature size better
Coated better



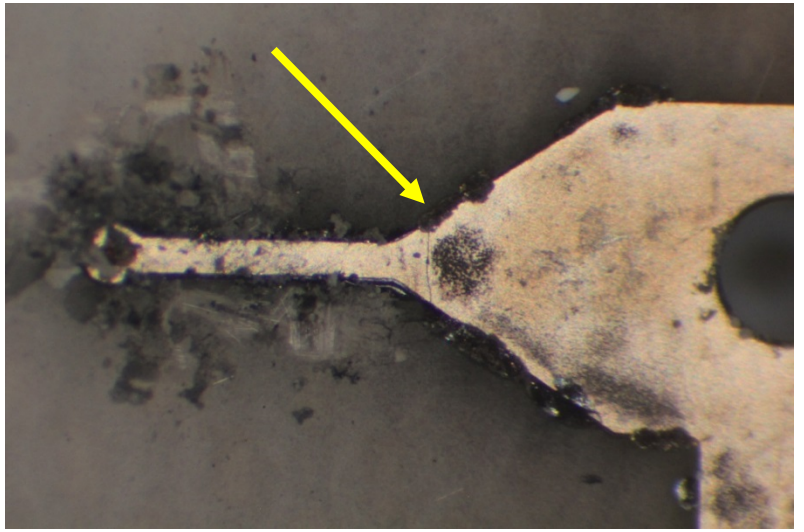



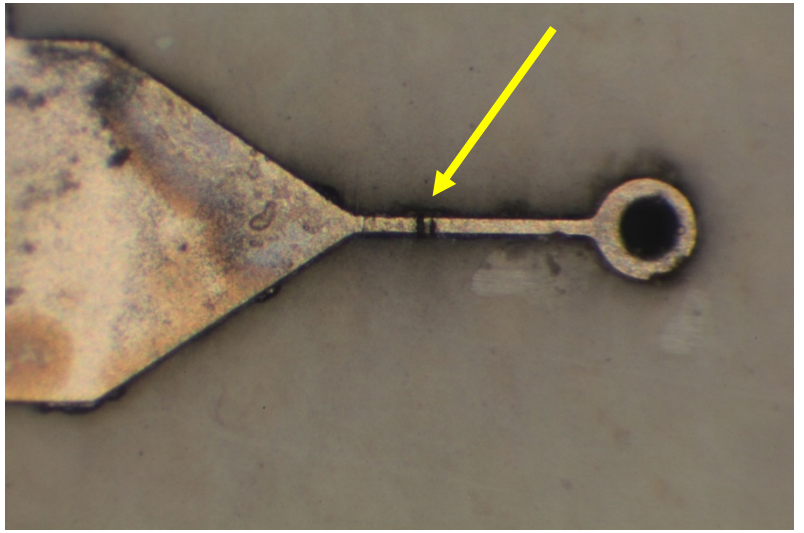

No failures for coated samples at 3500 hrs

# High temperature PCB Material, uncoated



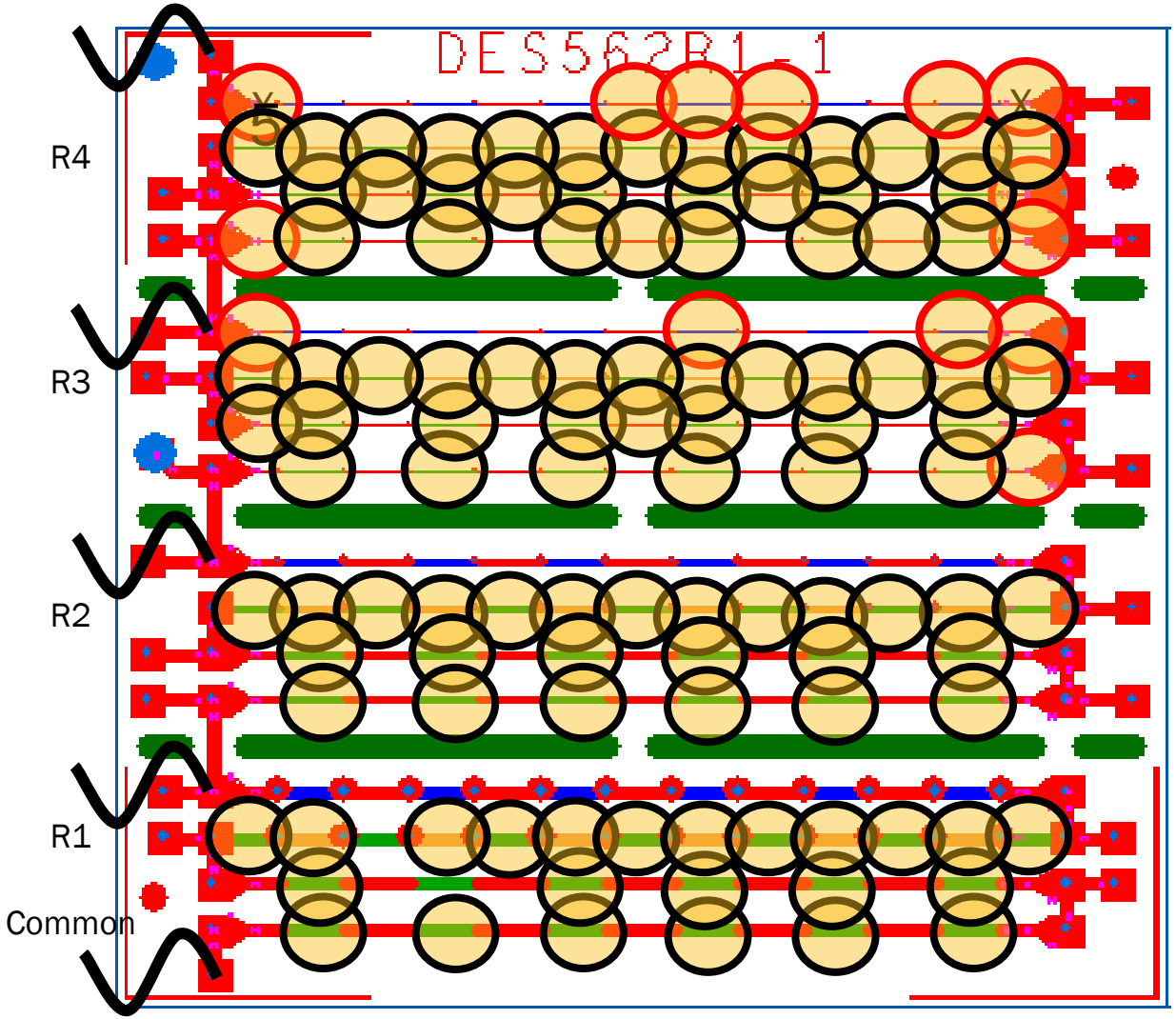
3500 hours @ 250°C





# High temperature PCB Material, uncoated

3500 hours @ 250°C




X
X
X
X
Some via failures

X
X
X
X
Some via failures

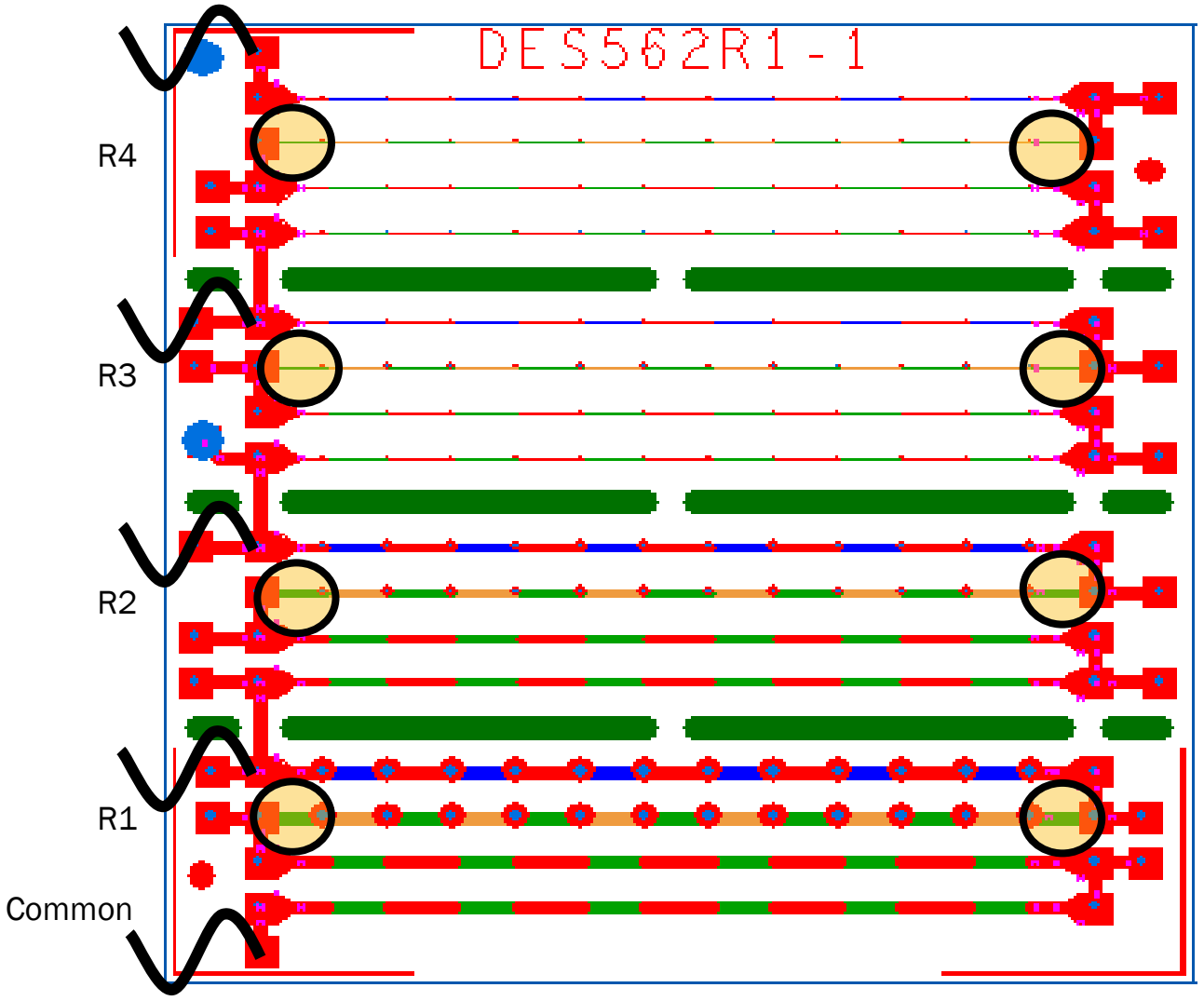
OK
X
X
X
No via failures

OK
X
X
X
No via failures

Outer layer failures

Inner layer/via/µvia failures

# High temperature PCB Material PCB Material Resist Coated




3500 hours @ 250°C

No via failures

No via failures

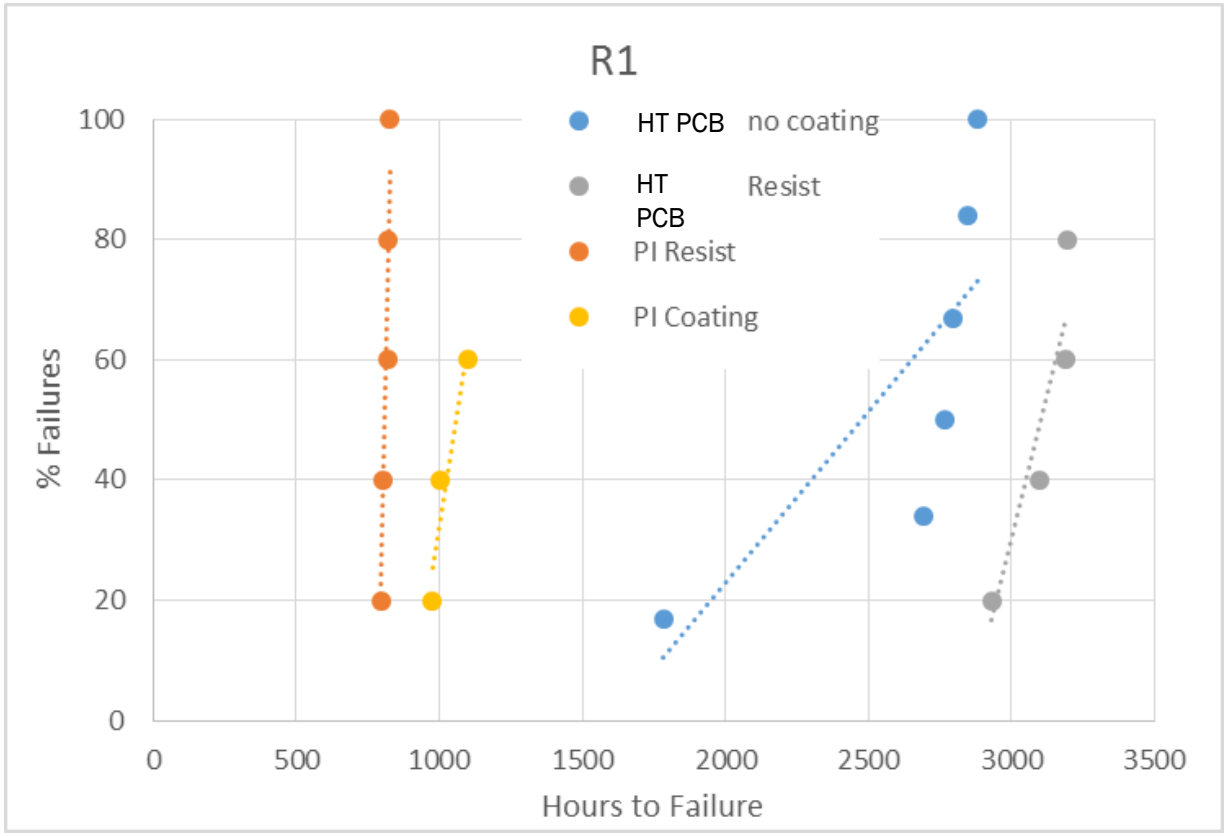
No via failures

No via failures

Outer layer failures

Inner layer/via/µvia failures

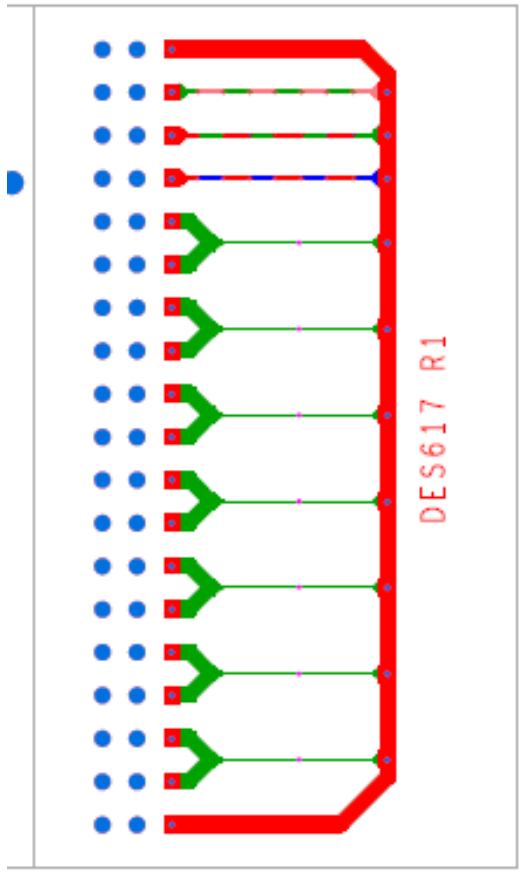
# Polyimide and High Temperature PCB Material Comparison




Vias = 5Xmm Ø
Tracks = 8Ymm

# Conclusions

- Substrate material and coating has shown performance better than 3500hrs at 250ºC even at smallest feature sizes
  - *Coating has shown at least 100% increase in lifetime*
- Design rules can improve this
  - *Inner layer copper weight*
- Work continuing to understand potential performance enhancements associated with high temperature coatings
  - *Design rules*
  - *Improvement in attachment reliability*
  - *Test vehicle development to determine rate of oxidation of inner layer using electrical resistance measurement*



# References


- [1] Source:Indium Corporation
- [2] Elcosint Project
- [3] Tamessa Project
- [4] ORCA Project
- [5] Proprietary to Microsemi
- [6] Source: Microsemi