Analyzing a Printed Circuit Board Weave Exposure Condition and its Effects on Printed Wiring Assembly Functional Performance

Wade Goldman P.E.[1], Andrew Dineen[1], Hailey Jordan[1], Curtis Leonard[1],
Timothy Redling[1], Edward Arthur[2]
[1]The Charles Stark Draper Laboratory, Inc., Cambridge, Massachusetts
[2]Raytheon Company, Space and Airborne Systems, El Segundo, California

Abstract
Printed Circuit Board (PCB) weave texture and weave exposure are conditions that may appear similar if appropriate inspection techniques are not applied in a manner that can differentiate between the two. Weave texture is an area where the glass bundles of the PCB are visible beneath the intact resin of the PCB surface. Weave exposure is when there are openings in the resin of the surface layer of the PCB that expose the glass fiber bundles. Either condition is generally acceptable per MIL-PRF-31032/1 or IPC 6012 (Class 1 & 2), as long as 1) exposed or disrupted reinforcement fibers on the horizontal surface of the PCB do not bridge conductors, and 2) the minimum conductor spacing is not violated due to the condition.

The objectives of this paper are to describe and provide a summary of methods, approaches and techniques engaged in determining whether the functional performance of the printed wiring assemblies (PWAs) would be impacted by the condition found in a recent case history of weave exposure.

Due to soldermask hiding the condition on the majority of the PCBs surface, it was initially thought the condition was weave texture. Some of the PCBs were then built into PWAs. Later it was determined that weave exposure was the condition, (with some weave texture). Due to the risks posed by this type of issue, including contamination and Conductive Anodic Filament (CAF) growth, a variety of techniques were utilized to evaluate the issue and determine the viability of using impacted PWAs. These techniques included, but were not limited to: visual examinations, PCB cross-section analysis, acoustic microscopy, scanning electronic microscope (SEM) evaluation with Energy Dispersive Spectroscopy (EDS), dielectric breakdown testing, Conductive Anodic Filament (CAF) testing, and Ion Chromatography testing.

This paper provides a structured and methodical approach to determine the impact of weave exposure. The techniques described below may be utilized as a guideline for others facing a similar predicament to determine final acceptability of the product.

Introduction
The genesis of this paper is derived from a case history which is discussed below. The PWAs are used in the assembly of an extremely complex and highly accurate system (CS), consisting of approximately 20,000 individual piece parts and over 30 PWAs. This CS is comprised of two subsystems which include 1) a sophisticated electromechanical assembly and 2) a computer.

Defects in PCBs that are inappropriately dispositioned and ultimately get assembled into PWAs and then the CS, can create situations where the functionality of the CS can become degraded and fail to meet specification requirements. Problems such as current leakage, insufficient voltage, timing variations, dielectric breakdown, amongst others things are all possible scenarios that could be caused by defective PCBs. The main focus of this paper is to provide guidelines to others who may also be working with PWAs with similar exposed weave conditions with some very specific analysis techniques to determine if PWA functionality is affected due to the weave exposure.

Background
As mentioned previously, weave texture and weave exposure may appear similar if appropriate inspection techniques are not employed at the time of the inspection. Also, depending upon soldermask coverage on the PCB, or conformal coat coverage on the subsequent PWA, this may also drastically affect the ability to discern between texture and exposure. For this case study, the product affected was a 16-layer PCB, polyimide construction, with liquid photo imageable (LPI) solder mask applied. These are manufactured in accordance with MIL-PRF-31032/1 requirements. There are plated through holes, microvias and buried vias in this design. This PCB also had some components with very fine pitched component lead pads that were approximately 152µm (0.006 in) apart. Between these pads, by design, there was no soldermask applied. See Figure 1 for an overall view of a representative sample, without the weave condition. The condition was initially observed as weave texture and seemed to only affect a single manufacturing lot of PCBs manufactured a few years ago.

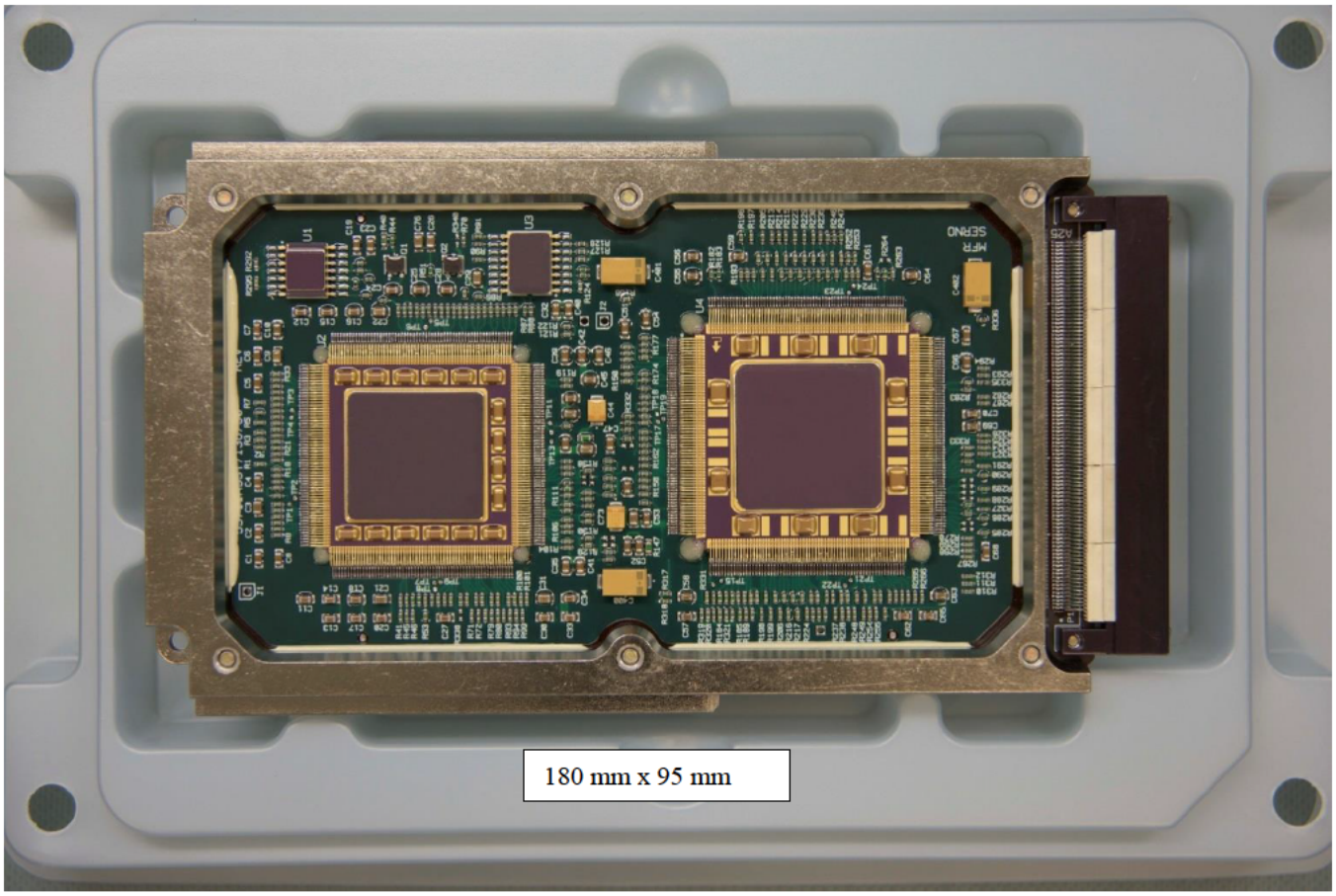


Figure 1- Example of a non-impacted PWA

These PCBs are procured by a subcontracted procurement agent then supplied to another subcontracted company for PWA assembly. The PWA assembly manufacturer first noticed this condition in October 2014 after a number of the PCBs had already been assembled with components. Initial inspection was performed in accordance with IPC-A-600H (2010) paragraph 2.2.2 weave texture criteria. At that time, it was deemed an acceptable condition. Weave texture again is defined as areas where the glass bundles of the PCB are visible beneath the intact resin of the PCB surface layer (commonly seen as white discolorations). It was observed mostly at locations on the PCB surface layers that were not covered with soldermask. Figure 2 and Figure 3 shows representative areas of the PCB with the condition. Figure 4 is a highly magnified photo showing the knuckles at perpendicular glass bundle intersection points.

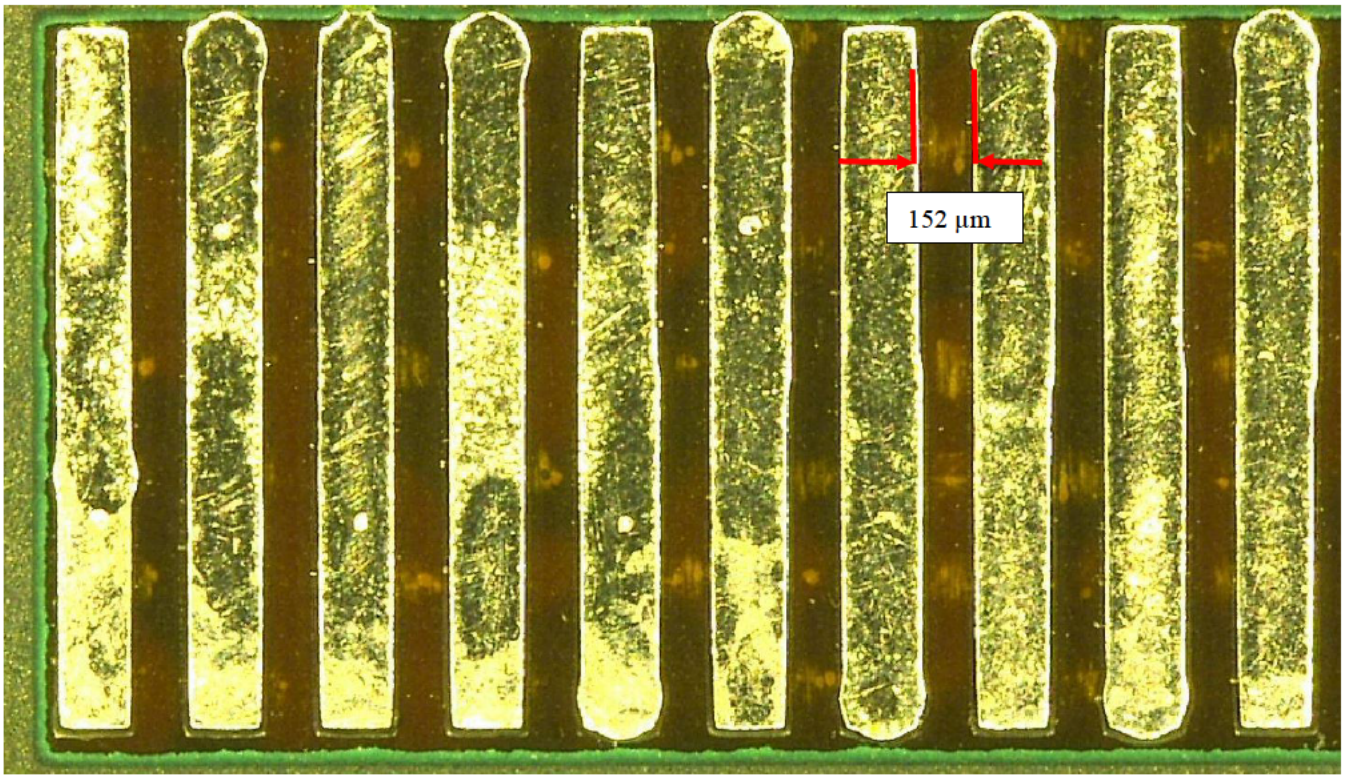


Figure 2 – PCB Component pads (no soldermask) – weave texture

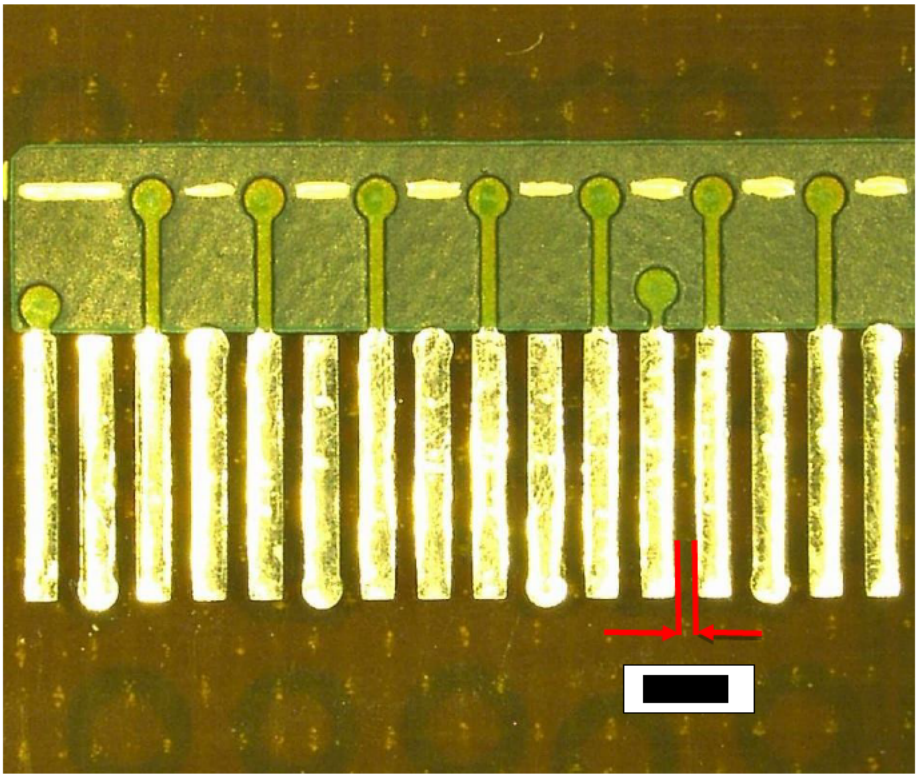


Figure 3 – PCB connector pads and adjacent areas (no soldermask) – weave texture

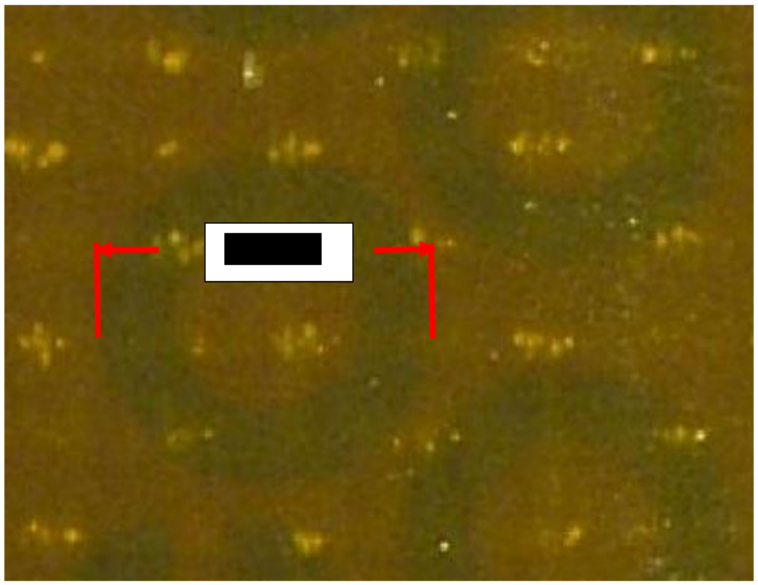


Figure 4 – Knuckle pattern of perpendicular glass bundles at intersection – weave texture

The original PCB manufacturer as well as the procuring activity reviewed results (remotely) and confirmed the PWA manufacturers observations. There was a concern raised that the weave texture condition could potentially reduce the minimum electrical spacing between conductors (especially the component leads). Typically for this design, the minimum conductor clearance is 127µm (0.005 in.). Several unassembled PCBs were provided for evaluation. Very high magnification (200X and 400X) was used to view the weave condition. The result was a confirmation that not only weave texture existed, but also the more problematic condition of weave exposure. Weave exposure is when there are openings in the resin of the surface layer of the PCB that actually expose the glass fiber bundles. Weave exposure is acceptable to MIL-PRF-31032/1 as long as 1) exposed or disrupted reinforcement fibers on the horizontal surface of the PCB do not bridge conductors, and 2) the minimum conductor spacing is not violated due to the condition. In IPC-6012, weave exposure is also acceptable for Class 1 & 2, but is not allowed for Class 3. See Figure 5 and Figure 6 for high magnification photos. The weave exposure condition was in violation of minimum conductor spacing requirements.

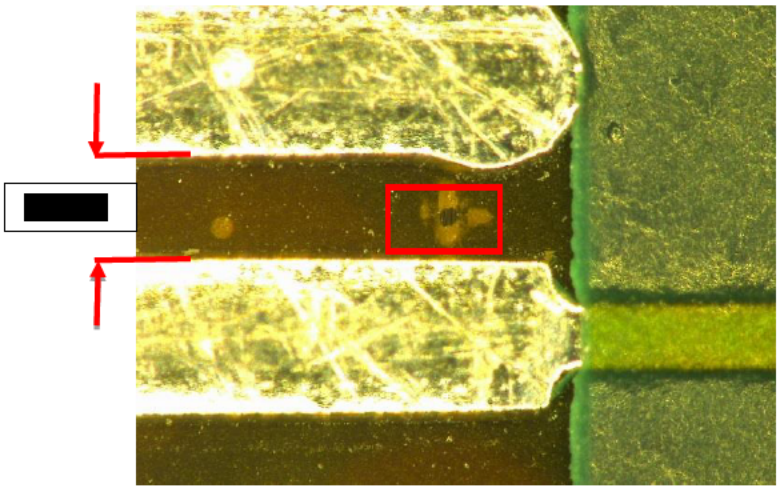


Figure 5 – Exposed weave between connector lead pads

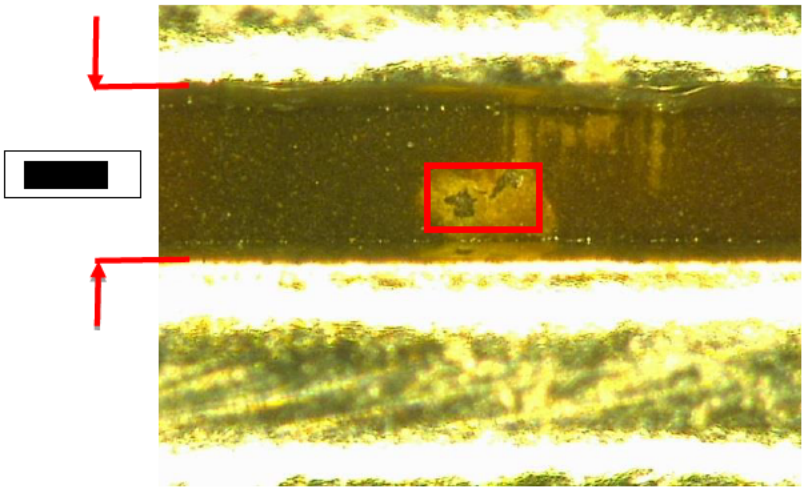


Figure 6 – Exposed weave between component lead pads

Since it could not be determined at this point as to the real impact of this condition on the functionality of the PWA and CS, it was recommended to place product on hold for further analysis.

The weave texture and weave exposure issues are strictly a surface condition that can be visually inspected. It was not clear at this point whether this surface condition could ultimately be tied a condition that may lie beneath pads and therefore impact surface pad integrity. This was explored during the analysis phase.

Root Cause Investigation

A thorough investigation was initiated with the PCB manufacturer. The PCB manufacturer traced the issue to a cured soldermask stripping process. During manufacturing, it was discovered that there was illegible legend marking resulting from the silkscreen process. It was determined by the process engineer that the lot should be reworked by stripping the cured soldermask (and cured epoxy ink marking) in accordance with an in-house approved procedure using a caustic stripper and then using a pumice scrubber as part of the wash down procedure. This process is done as full up panels. It is strongly believed that the result of this process attacked the resin on top of the glass fibers, resulting in weave texture and weave exposure. The chemical stripper employed was an aggressively caustic solution using dipropylene glycol monomethyl ether as a water soluble solvent. The glycol ether swells the surface and allows the hydroxide to diffuse into the polymer and to hydrolyze the backbone; either of the epoxy solder mask or the polyimide PCB material. The stripping process has many variables with tolerances associated with them. Some of these variables are the chemistry of the stripper, the temperature and dwell time in the stripper tank, as well as the speed through the pumice scrubber. Although not precisely determined, it was theorized that one of the variables was less controlled than usual and it exacerbated the weave condition.

The manufacturer reviewed documentation for all product previously delivered, not just this particular PCB part number. They indicated that other lots of PCBs also had used this cured soldermask strip process. Since all coupons are retained at our testing agent, the coupons were reviewed to determine if the weave condition existed on those PCB lots. Since most of these designs utilize product requiring a foil construction, these lots all have surface peel coupons in which a large portion of the coupon has no soldermask coverage. The lack of soldermask coverage of the surface peel coupon makes it ideal to examine, at very high power magnification, for the weave exposure and weave texture condition. No other cured soldermask stripped PCB lots were found to have the weave condition previously found on the one affected lot.

Evaluation and Analysis

Once the weave exposure condition was confirmed, a thorough analysis was performed to determine if the product could be released from hold or ultimately needed to be scrapped. The ultimate goal was to determine the usability of the product. The two acceptance criteria listed in MIL-PRF-31032/1 for weave exposure may suffice for typical applications but may not be adequate for critical processing and performance. Since the weave exposure was considered a nonconformance to the minimum conductor spacing requirement, it was imperative that ultimate functionality could not be affected by this condition, if the PCBs/PWAs were to be dispositioned as acceptable. We used a variety of techniques to analyze the condition. The various analysis techniques used included the following: visual examinations, PCB cross-section analysis, acoustic microscopy, pad removal, scanning electronic microscope (SEM) evaluation with Energy Dispersive Spectroscopy (EDS), dielectric breakdown testing, Conductive Anodic Filament (CAF) testing, and Ion Chromatography testing utilizing a mock PWA. This section will briefly describe these methods.

Visual examination

As described above, visually examining areas of a PCB (or a panel conformance coupon) at high magnification that contains no soldermask was one of the initial techniques used. Figure 7 depicts the peel strength conformance coupon previously discussed. As seen in the figure, there is no soldermask so high magnification of the coupon is a reasonable method to screen for the condition on a panel without necessarily inspecting the actual PCBs. Maintaining the use of industry acceptable inspection standards was not a driving requirement. Rather, using a method required to positively identify the condition of either weave texture or weave exposure was of paramount importance. For example, to confirm the condition, the inspection magnification was increased from industry standards of 7X to 40X to as high as 200X and 400X. This was performed on the four additional lots the PCB manufacturer identified as having gone through the cured soldermask strip process as described previously.

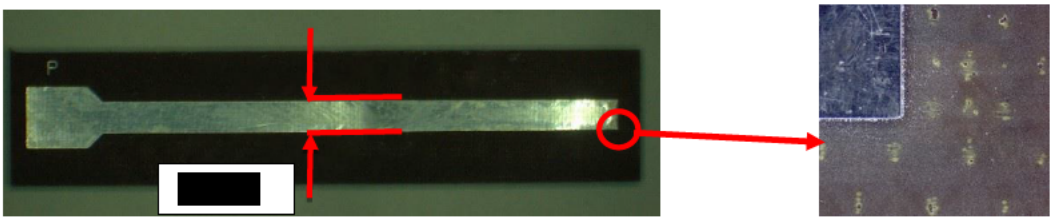


Figure 7–Visual Inspection of Peel Strength Coupon (31.25X)

In addition to inspecting the peel strength coupons, buried via conformance coupons were reviewed. The coupons from the affected lot underwent additional microsectioning where additional evidence of exposed weave was found. In general, areas under the soldermask had less damage to the resin than those areas of the surface laminate that had no soldermask. This is likely due to the fact that the soldermask, when originally subjected to the stripping solvent, masked that part of the laminate and prevented the damage from being as extensive as those areas with no soldermask. See Figure 8 for example of a buried via microsection conformance coupon.

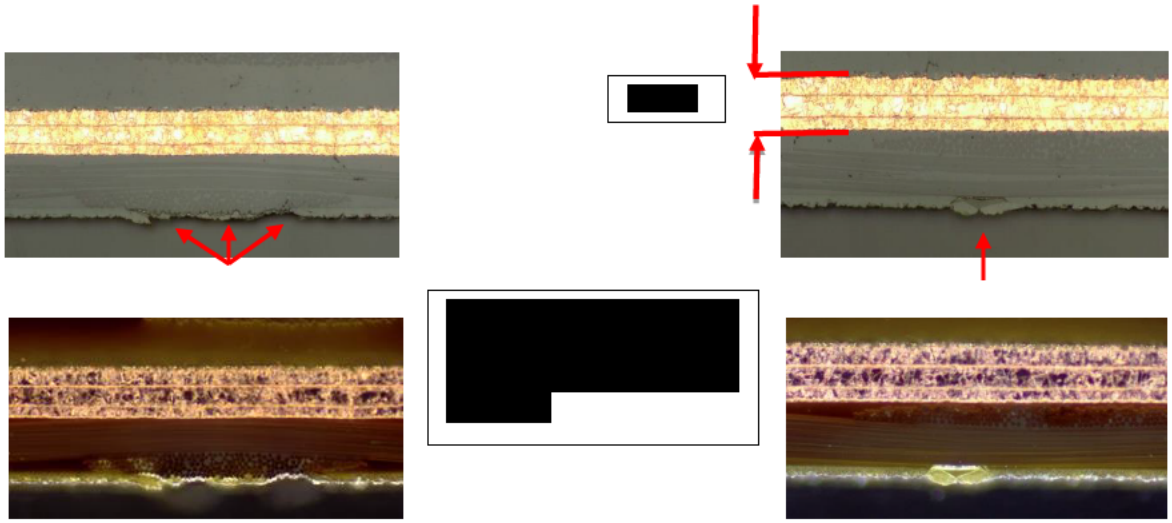


Figure 8–Buried via microsection evaluation (top-bright field, bottom-dark field, 250X)

Acoustic Microscopy

This is a non-destructive technique often used in failure analysis. It uses reflected ultrasound scanning pulses, to penetrate solid objects, and is able to image internal features, such as cracks, delaminations and voids. In this case, a PWA, with weave exposure, was submerged in a shallow bath of water while an ultrasonic transducer was used to generate the reflected ultrasound pulses. There was no protection afforded to the PCB or electronic parts. This was performed on a PWA that had been rendered as no longer fit for purpose simply to see if this was a viable method of analysis. No control sample was used. The green squares in Figure 9 indicate weave exposure conditions that was seen optically (on the left) as well by the acoustic microscopy device (on the right). The red square indicates what maybe a void or other internal defect (seen with the acoustic microscopy method) but not able to be seen optically. The actual extent/depth of this anomaly is indeterminate without a great deal of work by repeatedly indexing the ultrasonic transducer by a height distance, acquiring sonographs and correlating images. For the purposes of this investigation, no additional acoustic microscopy was pursued.

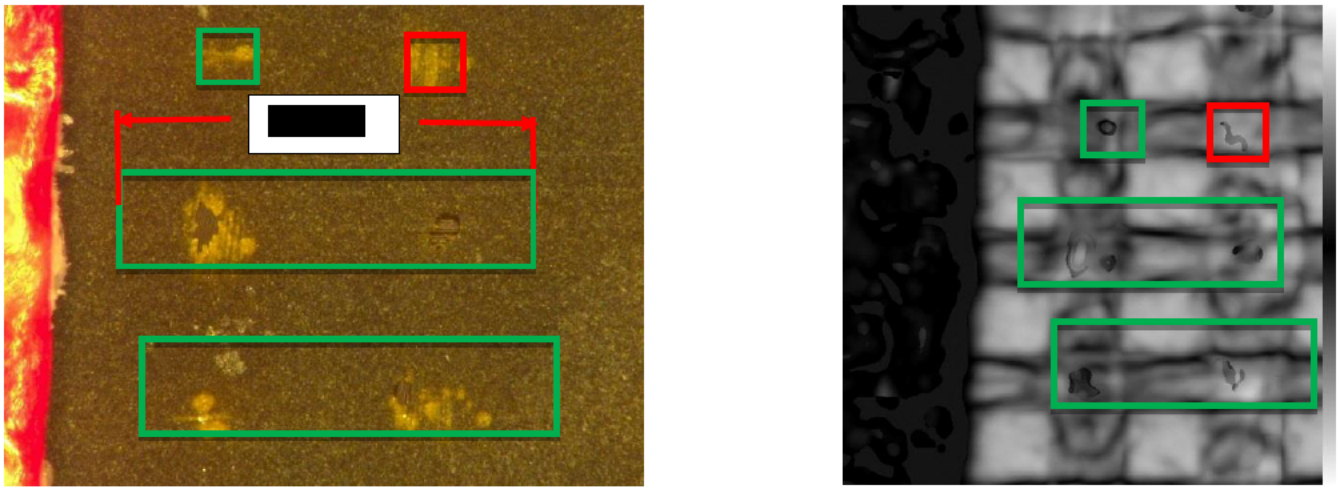


Figure 9–PWA (optical view on left, sonograph on the right)

Pad Removal

The pad removal was done to prove out the theory that the root cause was the soldermask removal process that caused the breakdown of the dielectric material and not something earlier in the manufacturing process, prior to plating. Since the soldermask removal process would not impact the dielectric under the copper, if the damage was present in the dielectric under the copper, then the condition had to be present prior to copper plating. A total of 6 surface pads were removed from an affected PWA. Upon visual inspection of the areas where the pads were removed, there was no evidence of dielectric erosion or exposed weave present at those pad locations. See Figure 10. This finding was also validated by our testing agent.

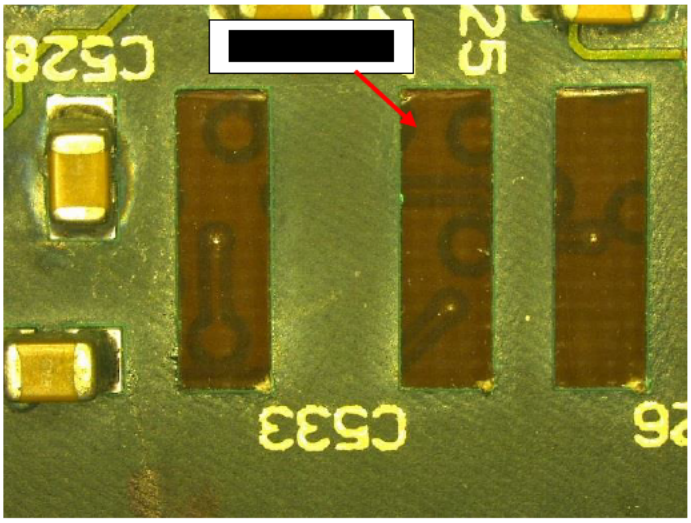


Figure 10 – Laminate condition after pad removal

Scanning Electron Microscopy (SEM)

A section of an affected PWA was subjected to SEM analysis. This section was comprised of a row of pads from the multi-leaded component shown in Figure 1. The analysis focused on random areas between pads where the reinforced glass fibers were overlapping (or perpendicular) to each other. See Figure 11 and Figure 12. The results depicted a number of areas where the surface laminate was separating and lifting from the PCB weave. It also shows areas where the surface laminate had ruptured. These findings provided confirmation that not only did weave exposure exist, but also lamination separation occurred, which is not a desirable outcome.

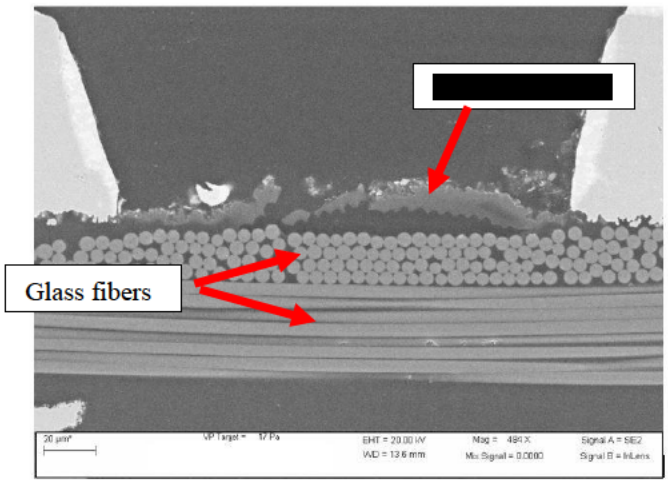


Figure 11– SEM photograph of area between surface pads, surface delamination, 484X

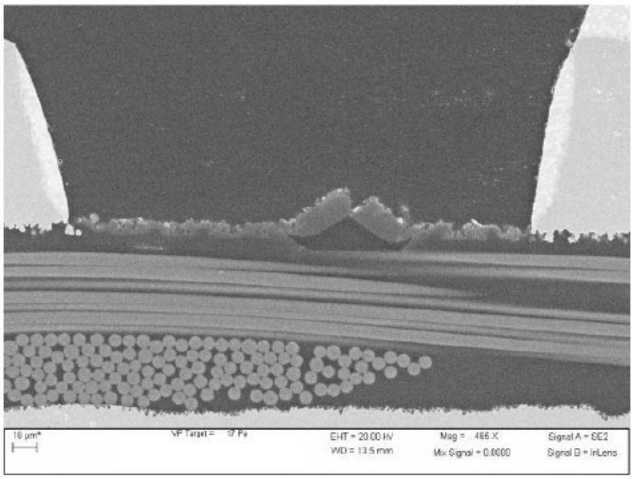


Figure 12 - SEM photograph of area between surface pads, surface rupture, 465X

Scanning Electron Microscopy (SEM) with Energy Dispersive Spectroscopy (EDS)

Sections of the same PWA were sent to our testing agent where they performed SEM with EDS. No control sample was used. Specifically, areas of the open weave were analyzed. EDS provides elemental analysis of the areas being examined. See Figure 13 and Figure 14 below. The analysis showed unusually high concentrations of silicon, calcium and bromine. This sample had previously been subjected to assembly processing as well, acoustic microscopy and it had been micro sectioned, so it was difficult to determine at what stage these high concentrations may have been deposited. It would have been beneficial to have run a control such as a piece of affected PCB that had not seen assembly and other post assembly handling. A control sample was used in mock assembly and cleanliness testing which is described later to better determine if the weave exposure trapped cleaning and assembly solvents.

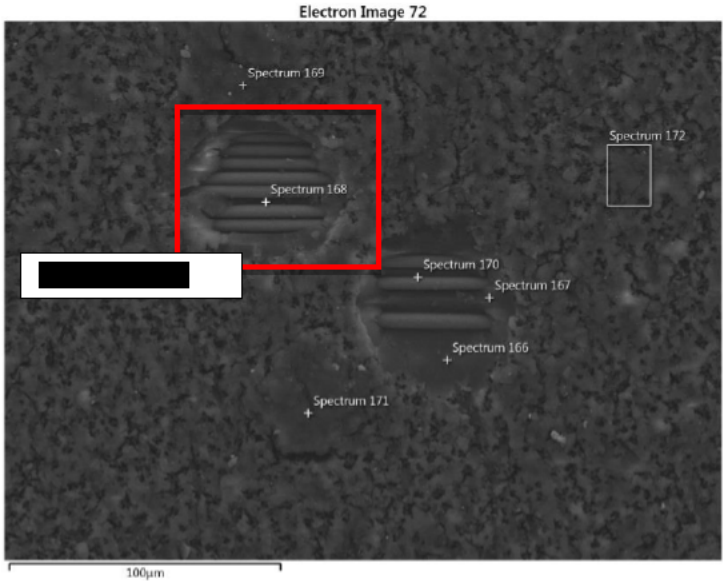


Figure 13 - SEM EDS Sample of Open Weave

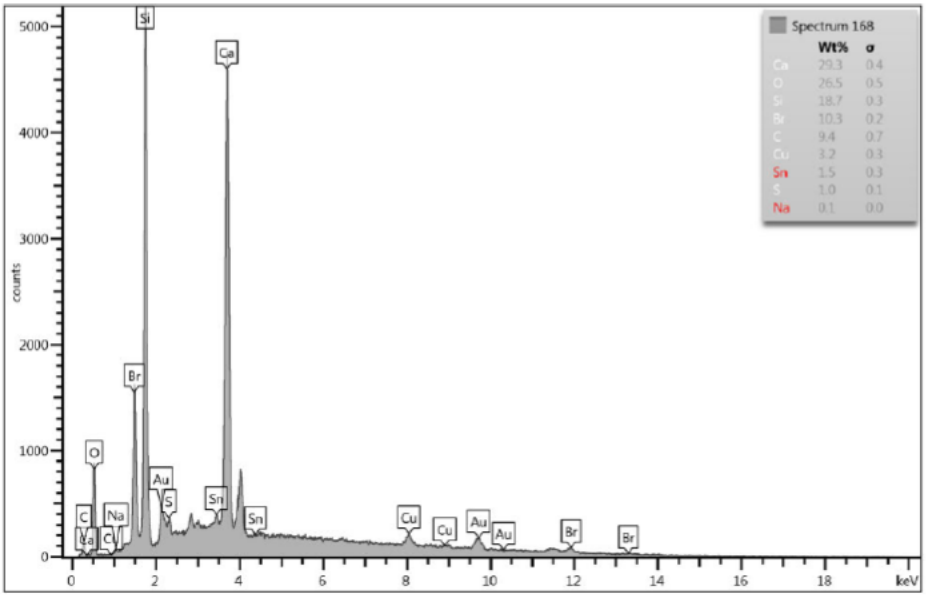


Figure 14–EDS analysis of Spectrum 168

Dielectric Breakdown Testing

This testing was performed on samples from an impacted PWA. The test was conducted consistent with IPC-TM-650 method 2.5.6.3. This test characterizes the PCB materials ability to resist electrical breakdown, not only between layers, but also between conductors. We already knew that with open weave between component pads, we were below the limit of the minimum conductor distance, one of the criteria listed above for determining open weave acceptability. It was anticipated that the dielectric breakdown test would provide useful data.

A test was designed using one row of the closely pitched component pads in Figure 1. The test was designed so that the leads from a component on one side were configured in such a way to provide a two-row pattern where the leads were bussed together to form two circuits. See
Figure **15**. Voltage was applied using a Hi-Pot tester capable of reaching 6kV DC and gradually increased until the tester tripped. The voltage was captured using a digital multi-meter.

The data sheets for the material used reported that the dielectric breakdown is 4.7 x 10E4 V/mm (1200 V/mil). Two separate samples were tested. The results ranged from 0.8 – 1.1 x 10E4 V/mm (215 V/mil to 277 V/mil). These values were far below the data sheet reported values and orders of magnitude greater than the typical voltage on the component pins. This indicates that PWAs with this weave exposure condition have severely compromised electrical strength and are susceptible to

electrical breakdown between adjacent conductors. Even though no control sample was used for this test, it did provide useful information to the analysis and led us to investigate CAF and cleanliness testing.

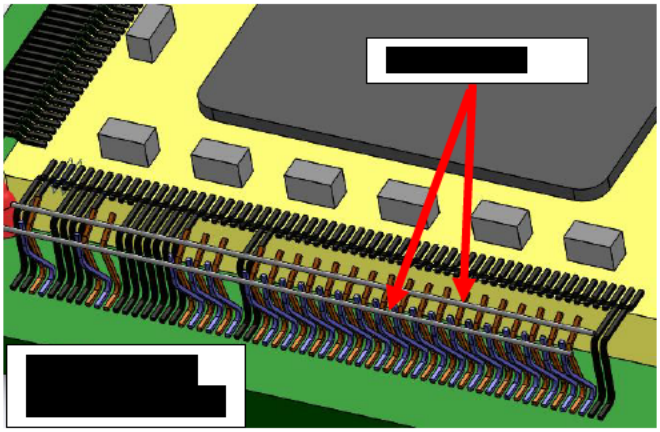


Figure 15–Dielectric breakdown setup – two circuits

Conductive Anodic Filament (CAF) Testing

Conductive Anodic Filament is an electrochemical process involving the transport of a metal through, or across, a nonmetallic medium under the influence of an applied electric field. In this context, it would involve the formation of conductive filaments, within the PCB material, that could bridge two conductors, resulting in shorts and failures during the life of the PWA. This is typically a long-term issue with main contributing factors including time, temperature, voltage bias and moisture.

Similar to the dielectric breakdown test described above, this test utilized an affected PWA that was sectioned, and specially configured. It was prepared identically to the dielectric breakdown test, Figure 15, except the leads, pads and buss wire were conformally coated. The test was performed to IPC-TM-650, method 2.6.25 using 100V, 85% RH and 85°C. We used the criteria in the test method that specifies a decade drop in insulation resistance as a result of applied bias, is a failure. Utilizing these conditions, the test lasted for 6 days then failure occurred. See Figure 16.

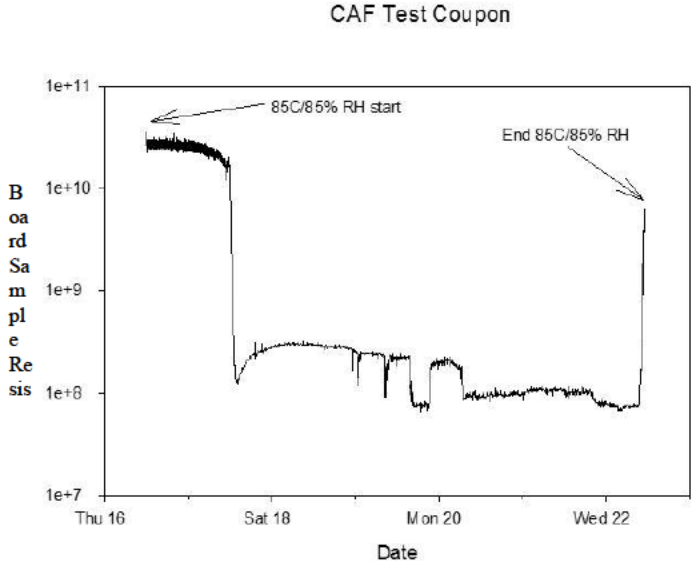


Figure 16– Results of CAF testing

Additional electrical testing was conducted after the CAF test was completed simply to determine the approximate location on the PWA where the CAF growth occurred. This was performed with a megohmmeter set with a short ramp to 100V DC, a 3 second measuring step and a brief discharge period. Power was applied to both circuits and a baseline resistance measurement was taken. Then the leads were clipped one at a time, starting at one end and working down towards the other, with a resistance measurement taken after each clipping. In addition, periodically the testing was paused and a 10M resistor

decade box was measured to ensure measurements on the test vehicle were accurate. The sample had varying stages of dielectric breakdown along the pad pattern, so as the leads were cut to determine location of CAF, the lower end pin count (130s/ 140s/ 150s) didn't show a resistance change when leads were cut so CAF was not in these locations. In the graph, when the resistance jumps with a pin cut, this indicates that CAF is present, so locations 164 & 165, 180 & 181 and 189 & 190 all had some CAF present.
Figure 17 is a bar chart indicating results of this test.

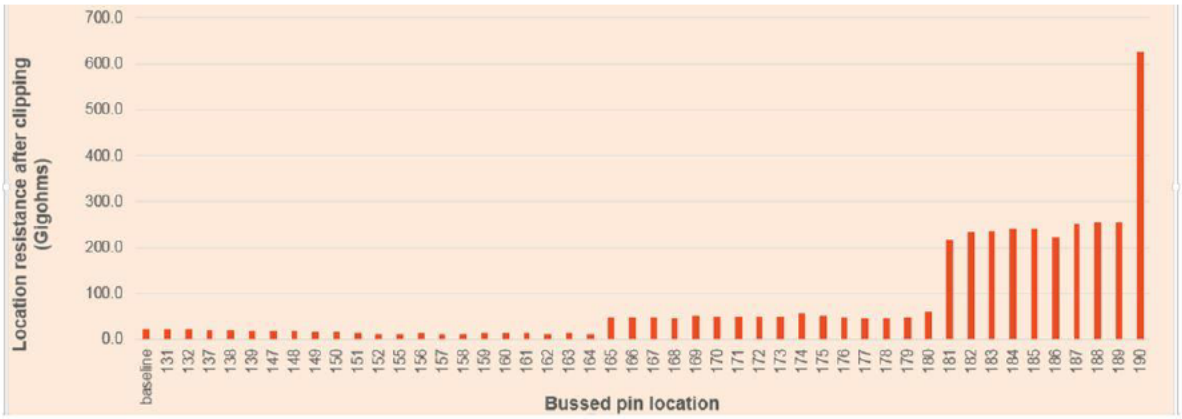


Figure 17 – Location of CAF failure

Cleanliness Testing

A number of sections from an affected PWA were then sent to a company that specializes in analyzing issues that may impact functionality and reliability with respect to residues from the assembly and manufacturing process. Five samples were prepared that covered internal as well as external locations. The testing was conducted in accordance with IPC-TM-650, method 2.3.28. The results of the cleanliness testing showed large amounts of contaminants both externally and internally, such as acetate, chloride, potassium and calcium, that posed a major risk of leakage and corrosion issues. As with the EDS analysis performed above, these samples had been subjected to assembly processing as well as acoustic microscopy and microsectioning, so it is difficult to determine at what stage these high concentrations may have been deposited. No control PCB was used for this test, however, the test did provide us with valuable information in that the ion chromatography has the resolution sufficient for analysis. See Table 1 below.

Table 1 - Ion Chromatography Results

All values in ug/in^2		Ion Chromatography										n/a = Not Applicable						
	Sample Description	Fluoride	Acetate	Formate	Chloride	Nitrite	Bromide	Nitrate	Phosphate	Sulfate	WOA	MSA	Lithium	Sodium	Ammonium	Potassium	Magnesium	Calcium
Recommended for bare PCB's		3	2.5	2.5	2.0	2.5	2.5	2.5	2.5	3.0	n/a	0.5	2	2	2.5	2	n/a	n/a
Recommended for PWA's (clean)		1	3	3	6.0	3	6.0	3	3	3.0	25	1	3	3	3	3	n/a	n/a
Recommended for PWA's (no clean)		1	3	3	3.0	3	6.0	3	3	3.0	150	1	3	3	3	3	n/a	n/a
ID																		
1	Board section B side Area 1	0	3.63	0	13.87	0	0.51	0.33	0	0.94	0	0	0	1.67	0	5.68	1.19	4.67
2	Board section B side Area 2	0	2.81	0	5.24	0	0.72	0.59	0	1.49	0	0	0	1.92	0	6.45	0.18	1.42
3	Board section B side Area 3	0	2.77	0	6.09	0	0.45	1.13	0	1.45	0	0	0	1.18	0	7.79	0.09	0.89
4	Board section A side Inner ayer inside Area 4	0	1.12	0	0.22	0	0.29	0.07	0	2.65	0	0	0	2.61	0	0	0	0
5	Board section A side Outer ayer (weave area) Area 5	0	23.34	0	48.79	0	3.45	1.46	0	12.49	0	0	0	20.33	0	16.72	3.30	18.58

PWA Mock Assembly and Cleanliness Testing

Since we had no control sample to compare to the results of the SEM EDS or the initial trial of the ion chromatography test, a control PCB was used for this next test. We first baselined a PCB that was in stock from the affected lot. Weave exposure areas were photo-documented prior to providing it to the outside source for cleanliness testing. The overall plan was to perform cleanliness testing on a bare PCB, then after reflow component installation, and then after hand soldered component installation. This would allow a detailed review to determine what contaminants are induced at the various stages, as well as determining if normal manufacturing processing exacerbated the weave exposure condition. Figure 18 are examples from the bare board from stock that was used in this test.

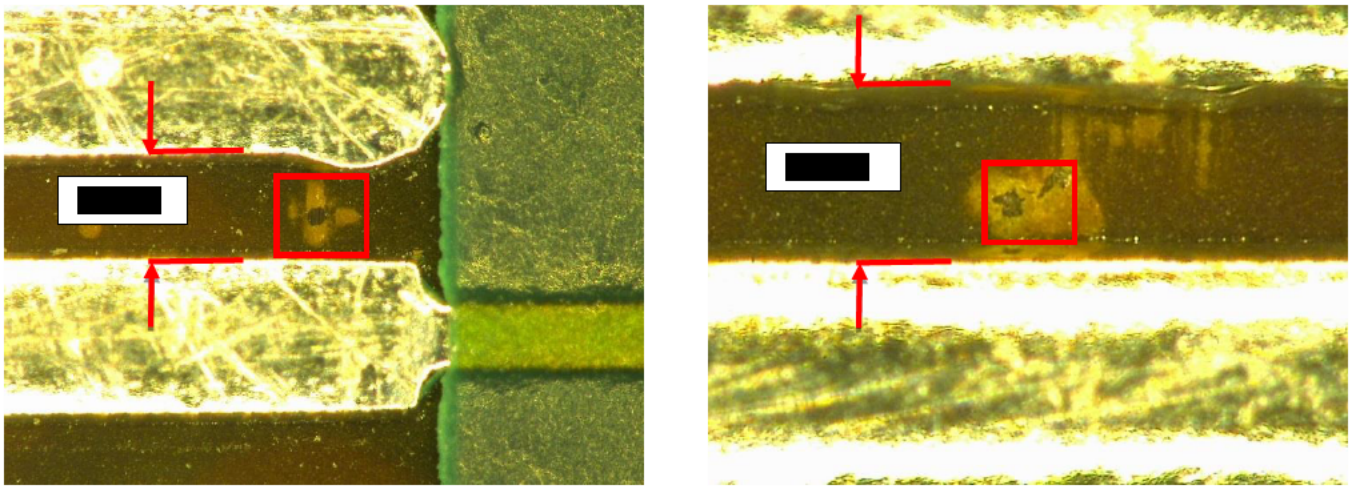


Figure 18 – PCB Exposed Weave – Connector pad (left), Component pad (right)

The PCB was then sent to an outside laboratory (same one as used above) for cleanliness testing. This provided a baseline ionic contamination result which would be very useful in determining if assembly operations increased this baseline level. The cleanliness results indicated that the PCB in the as received condition met recommended levels of contamination and therefore were considered clean.

The next step consisted of a reflow operation to attach the component using reflow techniques that exactly simulated all aspects of the reflow operation at the subcontracted supplier that performs assembly operations for this PWA. The same solder flux, solder paste and reflow profiles were used. Also the same aqueous cleaning, using the same machine and saponifier was used. Again, photos were taken and compared to the baseline, pre-assembly condition. See Figure 19 and Figure 20. No discernable visual changes were noted.

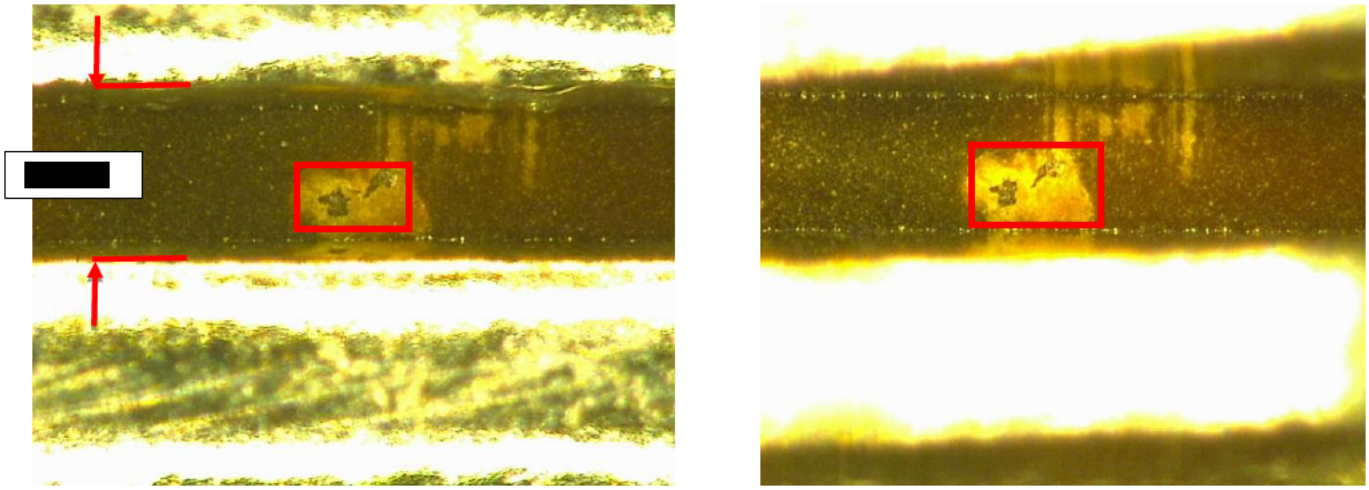


Figure 19 – PCB Exposed Weave (Component pads) before (left) and after (right) assembly

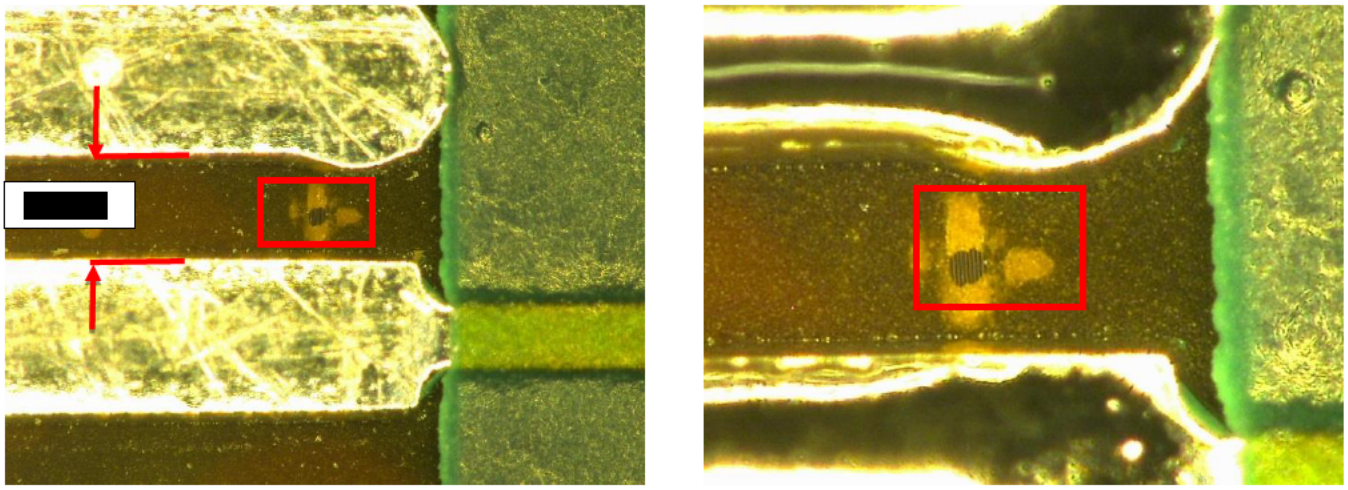


Figure 20 - PCB Exposed Weave (Connector pads) before (left) and after (right) assembly

The PWA was returned to the outside laboratory for cleanliness testing. The exact same locations were analyzed. The results indicate that the sample areas reviewed show an increase in ionic residues from the baseline. Specifically, acetate, chloride and ammonium levels were increased above recommended limits, indicating the PCB material contains residue after cleaning that pose a moderate to high risk of electrical leakage and corrosion problems. See Table 2 below.

Table 2 - Ion Chromatography Results post assembly cleaning

All values in ug/in^2		Ion Chromatography										n/a = Not Applicable							
	Sample Description	Fluoride	Acetate	Formate	Chloride	Nitrite	Bromide	Nitrate	Phosphate	Sulfate	WOA	MSA	Lithium	Sodium	Ammonium	Potassium	Magnesium	Calcium
Recommended limits for bare PCB's		3	2.5	2.5	2.0	2.5	2.5	2.5	2.5	3.0	n/a	0.5	2	2	2.5	2	n/a	n/a
Recommended limits for PWA's (clean)		1	3	3	6.0	3	6.0	3	3	3.0	25	1	3	3	3	3	n/a	n/a
Recommended limits for PWA's (no clean)		1	3	3	3.0	3	6.0	3	3	3.0	150	1	3	3	3	3	n/a	n/a
ID	Bare board prior to processing																	
1	S/N 0704M U4 pin 62-63 area	0	0.22	0	0.36	0	1.16	0.28	0	0.28	0	0	0	0.37	0.50	0	0	0
2	S/N 0704M P1 pin 88-89 area	0	1.67	0	1.92	0	1.43	0.40	0	0.85	0	0	0	1.73	1.04	0	0	0
	Addendum samples – processed and cleaned then tested in the same location																	
3	S/N 0704M U4 pin 62-63 area	0	4.11	1.30	11.54	0	3.52	1.28	0	1.84	0.28	0	0	0.48	7.47	0	0	0
4	S/N 0704M P1 pin 88-89 area	0	2.54	0	4.98	0	2.87	1.08	0	0.29	0.78	0	0	0.56	5.91	0	0	0

Results Summary

From the methods and analysis conducted on affected PCBs as well as PWAs, the following comprise a summary of the findings:

- Visual examination with high power magnification confirmed the weave exposure condition on PCBs as well as panel conformance coupons.
- Acoustic microscopy verified that there can be internal issues (such as voiding) with no visible external indicator. No determination was made as to what may have caused the internal void.
- Surface pad removal confirmed that the cured soldermask strip process impacted bare surface laminate and cured soldermask. There is no evidence to suggest that raw material or any process other than the soldermask rework, was the root cause of the weave exposure condition.
- SEM analysis further verified the weave exposure issues and associated with that could be delamination and eruption of the surface resin.
- EDS analysis was not conclusive without performing the same analysis on a standard, stocked PCB from this lot.
- Dielectric breakdown testing indicated PCBs with weave exposure were susceptible to electrical breakdown between conductors after samples had seen assembly processing, cleaning and post assembly tests such as acoustic microscopy.
- CAF testing showed susceptibility to CAF failures under IPC TM-650 conditions with PWA samples post assembly operations, similar to dielectric breakdown samples.
- Cleanliness testing confirmed that as a result of normal assembly processing, a significant amount of residue remained in weave exposure areas that pose a moderate to high risk of electrical leakage and corrosion problems

Corrective/Preventive Actions:
As stated above, the root cause was deemed to be the cured soldermask strip process employed at the supplier for this lot of PCBs. It was determined that the other PCB lots that used this cured soldermask strip process were unaffected by the caustic stripper used. Although not precisely determined, it was theorized that one of the stripping variables was less controlled than usual and it exacerbated the weave condition.

The procurement of PCBs for this program uses written process agreements that the supplier agrees to with the design, procurement and ultimate customer, which locks in a number of critical procedures at designated revisions. Changes to this agreement must be approved by all parties.

1. The written agreement has been revised so that cured soldermask stripping cannot be performed on any product unless authorized in writing.
2. This has been agreed to with other PCB manufacturers. The written process agreements with other suppliers now include a similar prohibition.
3. All suppliers received a quality alert that requested a heightened sense of awareness for weave texture conditions that may actually be weave exposure at higher levels of magnification.
4. A formal review of all types of rework procedures has been conducted with the PCB manufacturers so that levels of risk can be associated with certain rework processes.

Conclusion
A concise approach was used to determine if the product affected by the soldermask strip process could be used. The culmination of all the investigation and evaluation during this process indicated that as a result of the original weave exposure condition coupled with typical assembly processes, these conditions would likely result in significant issues/failures for the affected assemblies. Therefore, it was recommended that all PCBs and PWAs already built with this date code would not be used in the CS in which these PWAs are used.

Acknowledgments
The authors thank Ted Jones and his team at the Crane Division, Naval Surface Warfare Center, our testing agent, for their outstanding contribution in providing technical expertise during the execution of the some of the analysis work during this investigation.

APEX EXPO IPC 2018
SUCCEED AT THE VELOCITY OF TECHNOLOGY

Analyzing a Printed Circuit Board Weave Exposure Condition and its Effects on Printed Wiring Assembly Functional Performance

Wade Goldman P.E.[1], Andrew Dineen[1], Hailey Jordan[1],

Curtis Leonard[1], Tim Reddling[1], Edward Arthur[2]

[1]The Charles Stark Draper Laboratory, Inc., Cambridge, Massachusetts

[2]Raytheon Company, Space and Airborne Systems, El Segundo, California

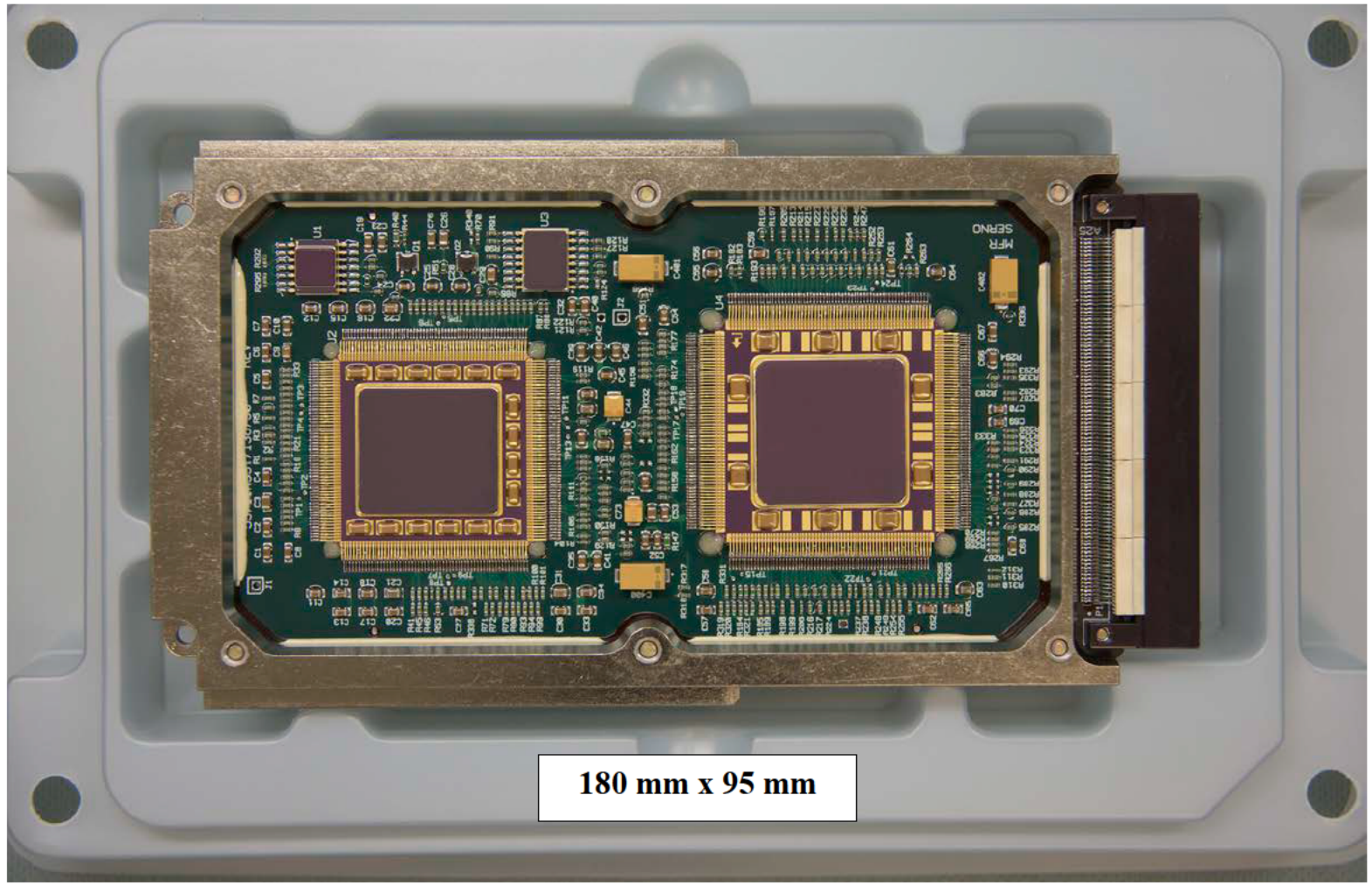
Introduction

- Weave texture is defined as areas where the glass bundles of the PCB are visible beneath the intact resin of the PCB surface layer.
- Weave exposure is when there are openings in the resin of the surface layer of the PCB that expose the glass fiber bundles.
- Genesis for this paper – Actual case history for a PWA used in a very complex electro-mechanical system (CS).
- This CS is comprised of two subsystems which include 1) a sophisticated electromechanical assembly and 2) a computer.
- Weave texture and weave exposure are acceptable to an extent.
- Provides guidelines for analyzing the weave condition to determine acceptability of the product based on functionality.

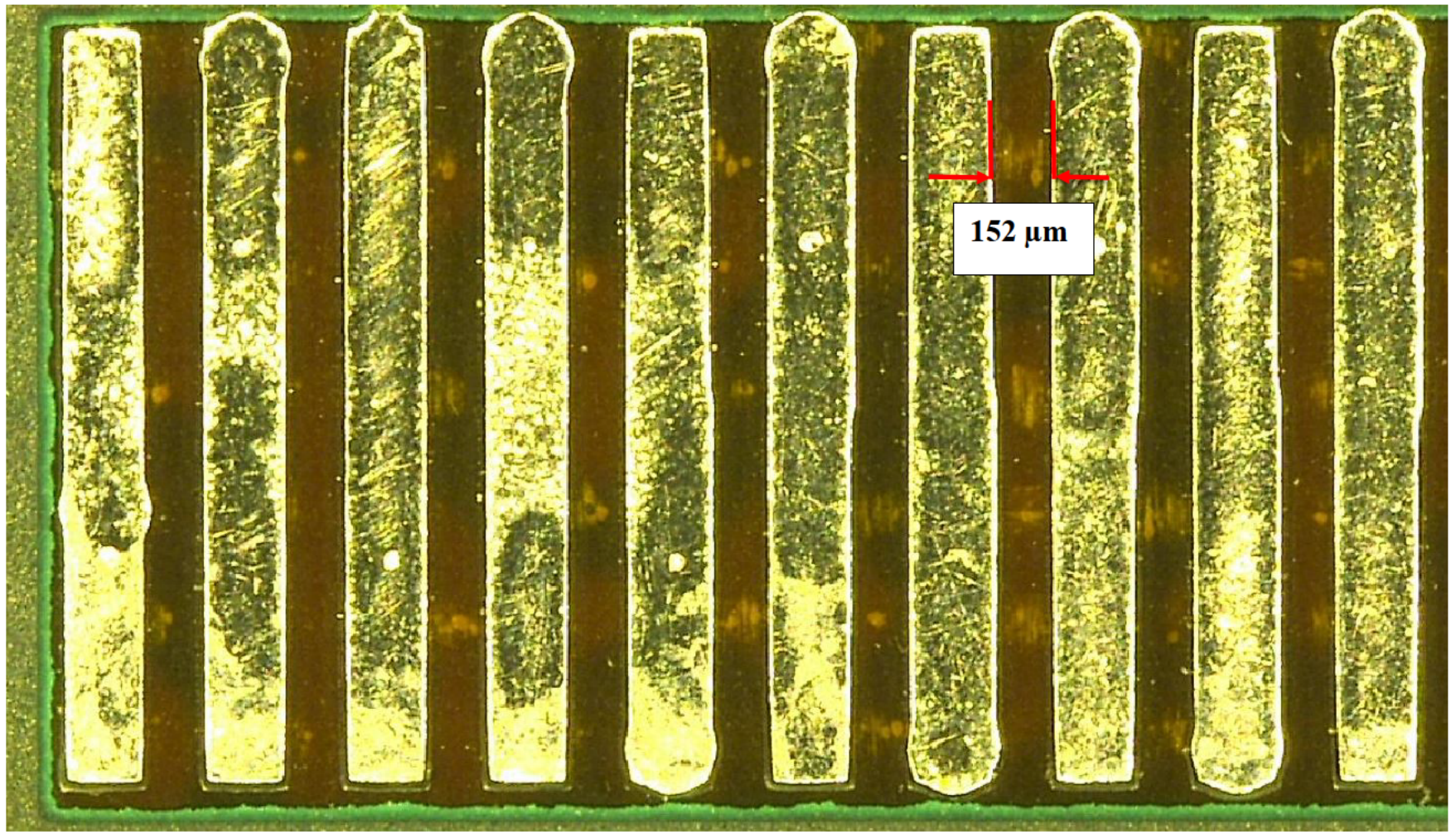
Background

- PCBs, manufactured a few years ago, were found to have weave texture. Condition was not noticed until a number of PCBs were assembled into PWAs. IPC-A-600 was the visual workmanship standard used.
  - *16 layer, polyimide, liquid photo imageable soldermask, MIL-PRF-31032/1*
- Weave exposure may appear similar if appropriate inspection techniques are not employed at the time of the inspection. Soldermask or conformal coat coverage may drastically affect the ability to discern between texture and exposure.
- The PCB manufacturer and procuring agent remotely reviewed pictures from the PWA manufacturer and agreed with the initial assessment.
- Observed mostly on areas not covered with soldermask.

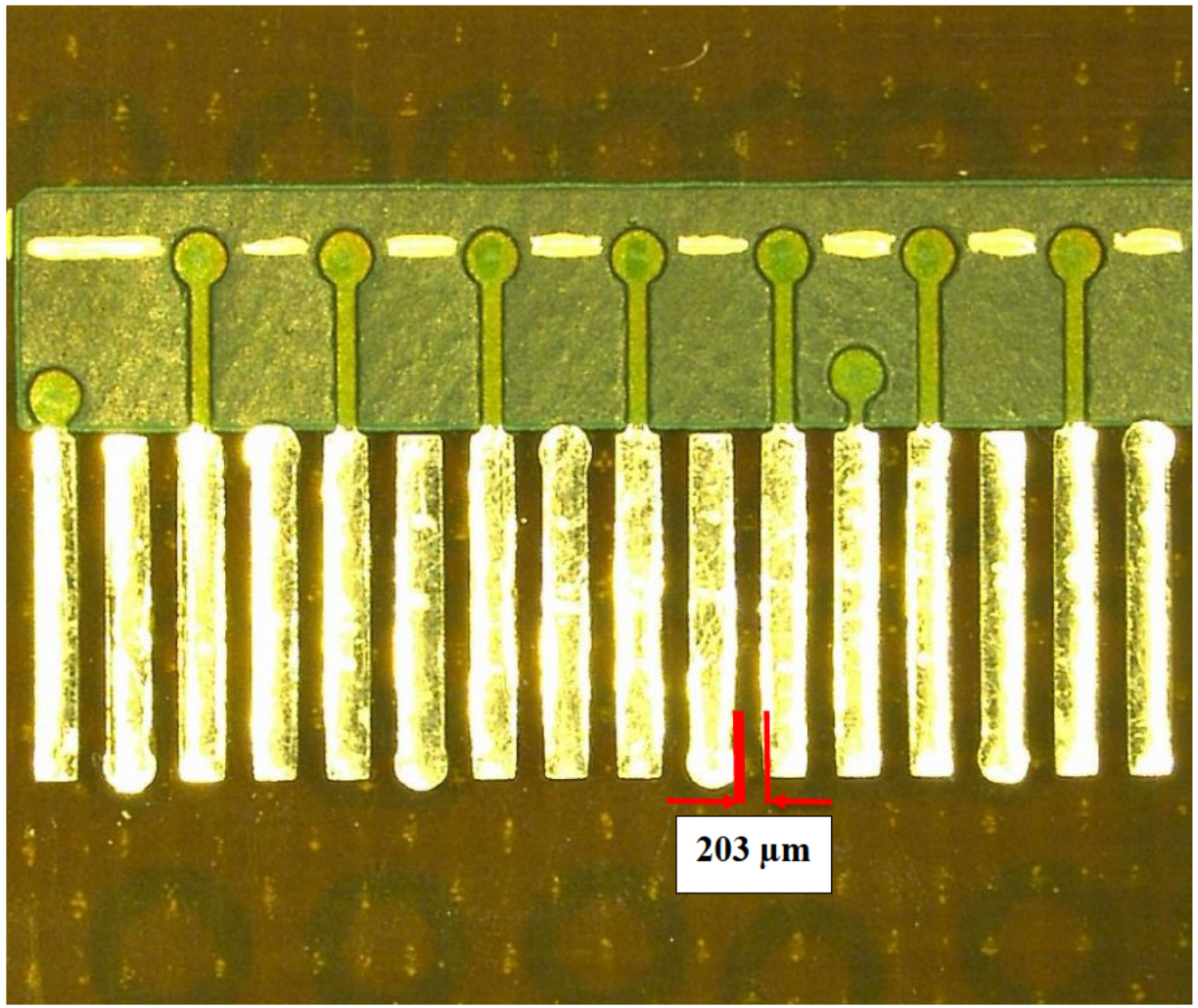
PWA Overview



Weave Texture – Component lead pads



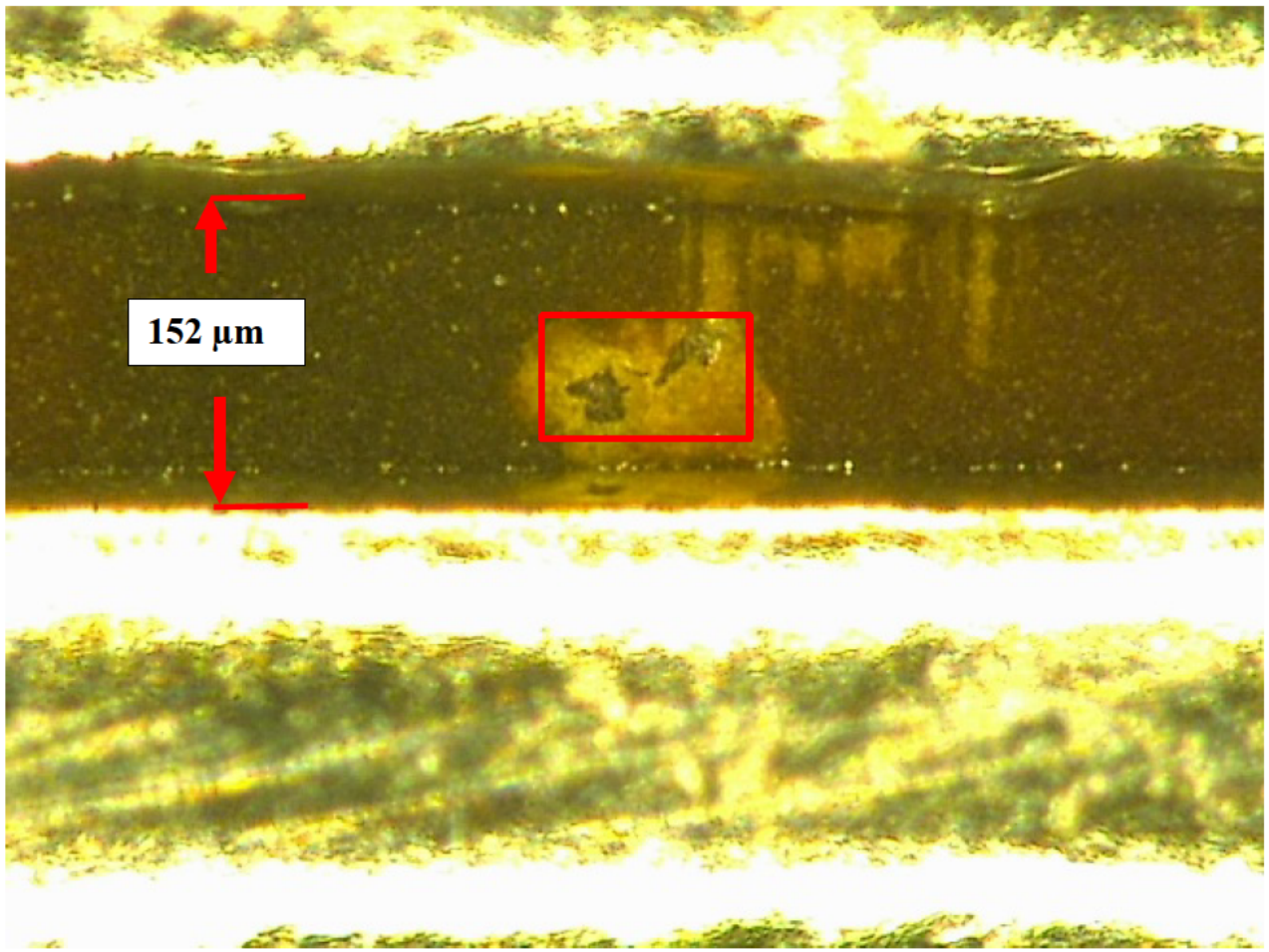
Weave Texture – Connector lead pads



Background

- A concern was raised by the design agent that the weave texture could potentially reduce the conductor spacing to an unacceptable value or < 127µm.
- Several loose PCBs were examined closely at 200X and 400X magnification.
- Weave texture was confirmed. The more problematic weave exposure was also confirmed.

Weave exposure – Component lead pads



Background

- Criteria:
  - *MIL-PRF-31032/1:*
    - Acceptable if 1) exposed or disrupted fibers on horizontal surface do not bridge conductors and 2) if minimum conductor spacing is not violated
  - *IPC-6012*
    - Acceptable for Class 1 & 2
    - Not acceptable for Class 3
- The condition was in violation of the minimum conductor spacing, 127 µm, so disposition of the product was required.
- There was an unknown functional impact to the PWAs and the CS.
- Recommendation was to place all affected product on hold pending further analysis.

Root Cause Investigation

- The root cause was traced to a cured solder mask stripping operation at the PCB manufacturer.
- Illegible legend marking led to the use of this infrequently used standard process.
- All panels from this lot were stripped using an approved caustic stripper (tank) and pumice scrub as part of the wash down procedure. It is strongly believed that the result of this process attacked the resin on top of the glass fibers, resulting in weave texture and weave exposure.

Root Cause Investigation

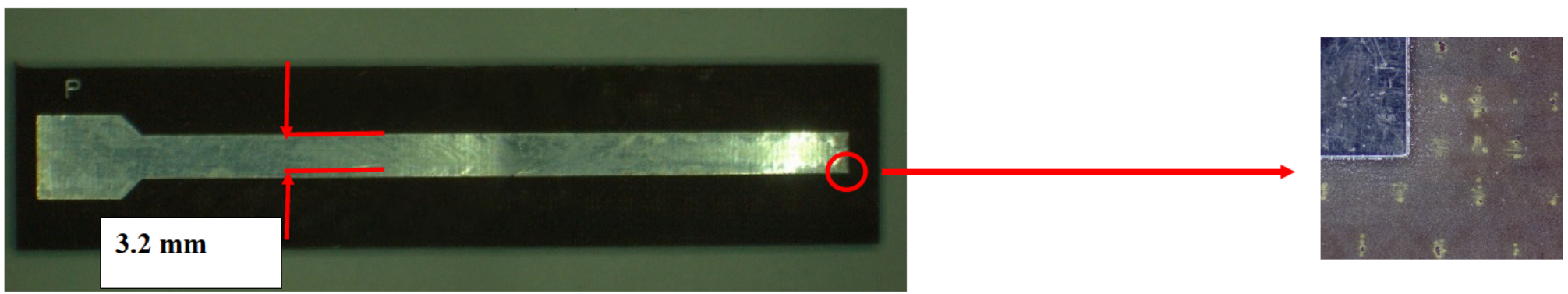
- The chemical stripper used was dipropylene glycol monomethyl ether as a water soluble solvent. The glycol ether swells the surface and allows the hydroxide to diffuse into the polymer and to hydrolyze the backbone. It attacks either the epoxy solder mask or the polyimide PCB material.
- Variables include the chemistry of the stripper, the temperature and dwell time in the stripper tank, as well as the speed through the pumice scrubber.
- Although not precisely determined, it was theorized that one of the variables was less controlled than usual and it exacerbated the weave condition for this lot.
- A small number of other lots previously delivered used this same process. Surface peel coupons from these lots were inspected and found to have no evidence of weave texture or weave exposure.

Evaluation and Analysis

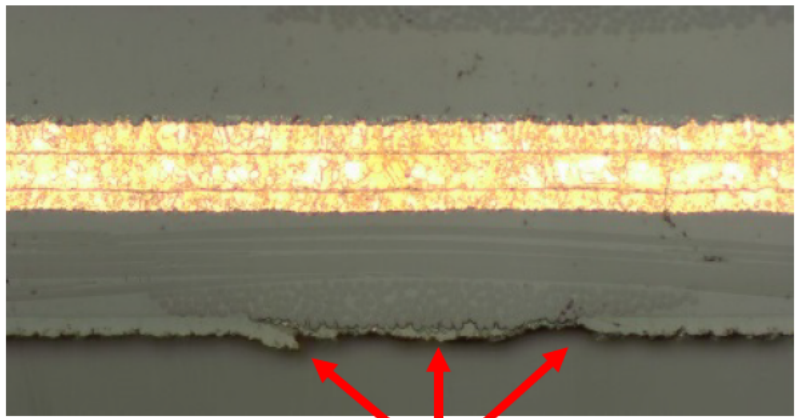
- Goal: Determine usability of the product despite minimum conductor spacing violation.
- Utilized non destructive and destructive techniques.
- The various analysis techniques used included the following: visual examinations, PCB cross-section analysis, acoustic microscopy, pad removal, scanning electronic microscope (SEM) evaluation with Energy Dispersive Spectroscopy (EDS), dielectric breakdown testing, Conductive Anodic Filament (CAF) testing, and Ion Chromatography testing utilizing a mock PWA.

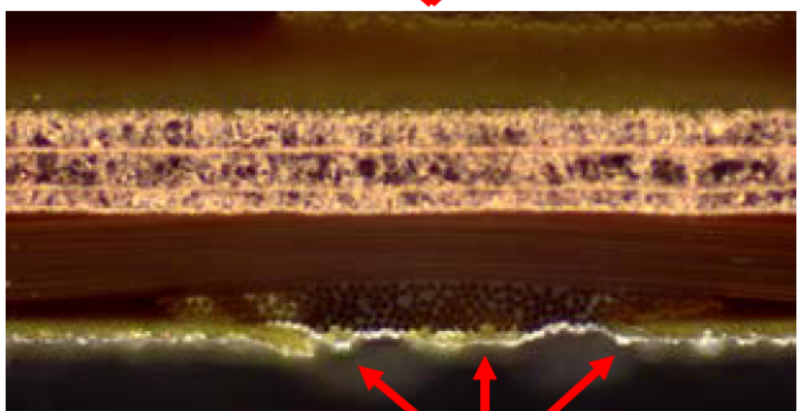
Evaluation and analysis – Visual inspection

- Peel strength coupons provide a soldermask free coupon for visual examination by high power (200X to 400X)
- Buried via conformance coupons were microsectioned and reviewed
- Areas under soldermask had significantly less damage than areas of surface laminate that were directly subjected to the stripper solvent.

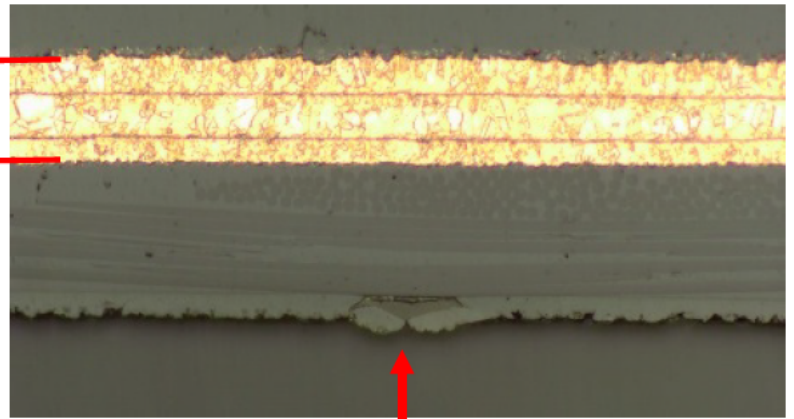


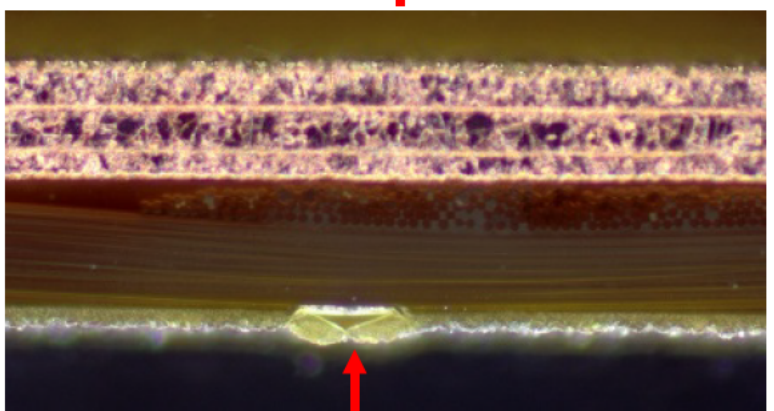
Evaluation and analysis – Microsection





46 µm





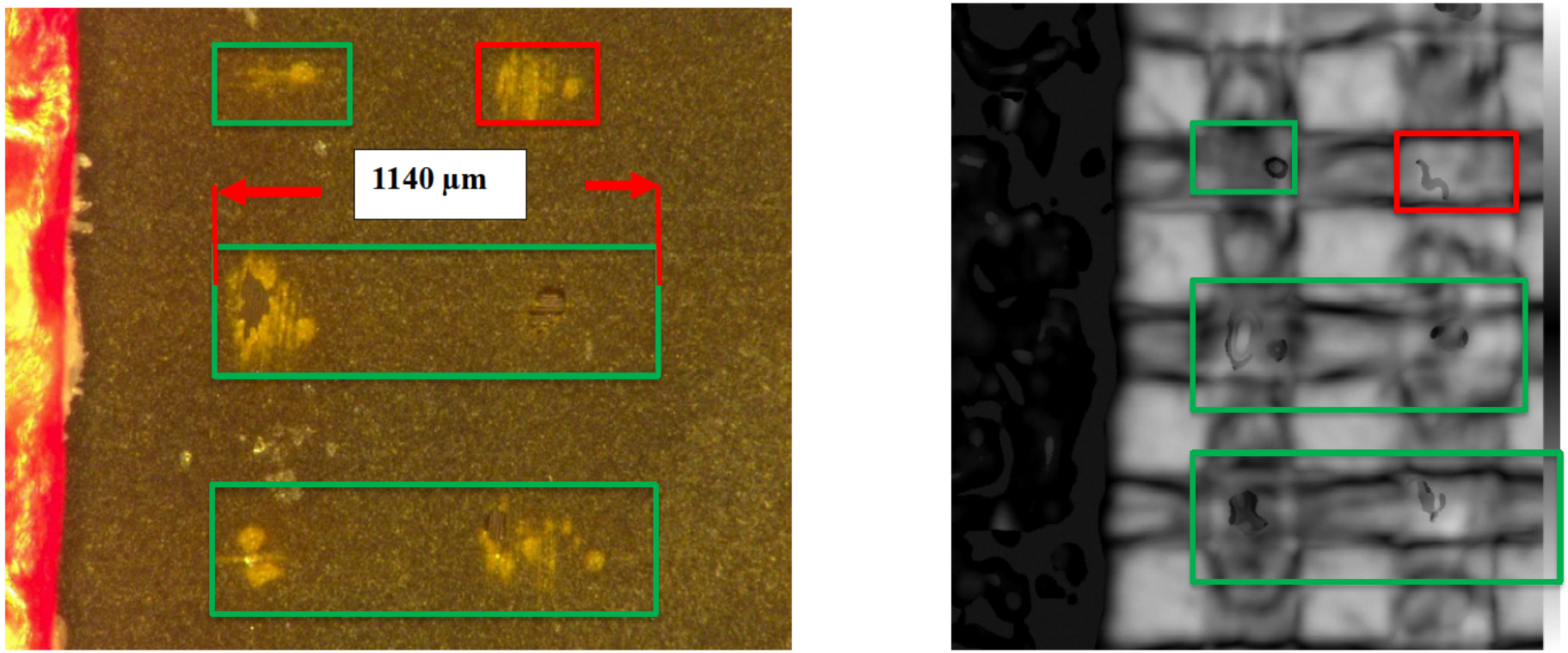
The red arrows indicate disruptions in the surface laminate creating weave exposure.

Buried via microsection evaluation (top-bright field, bottom-dark field, 250X)

Evaluation and analysis – Acoustic Microscopy

- Acoustic Microscopy uses reflected ultrasound scanning pulses to penetrate solid objects and images features such as cracks, delaminations, or voids.
- An affected PWA was subjected to this test. No control sample was used.
- The actual extent/depth of any anomaly is indeterminate without a great deal of work by repeatedly indexing the ultrasonic transducer (in the z direction) by a height distance, acquiring sonographs and correlating images.

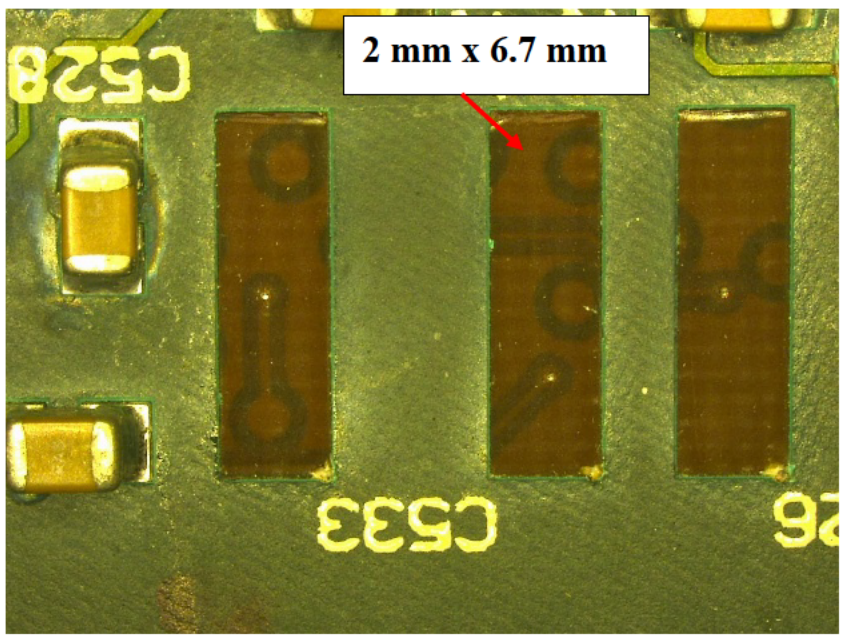
Evaluation and analysis – Acoustic Microscopy



PWA (optical view on left, sonograph on the right)

Evaluation and analysis – Pad removal

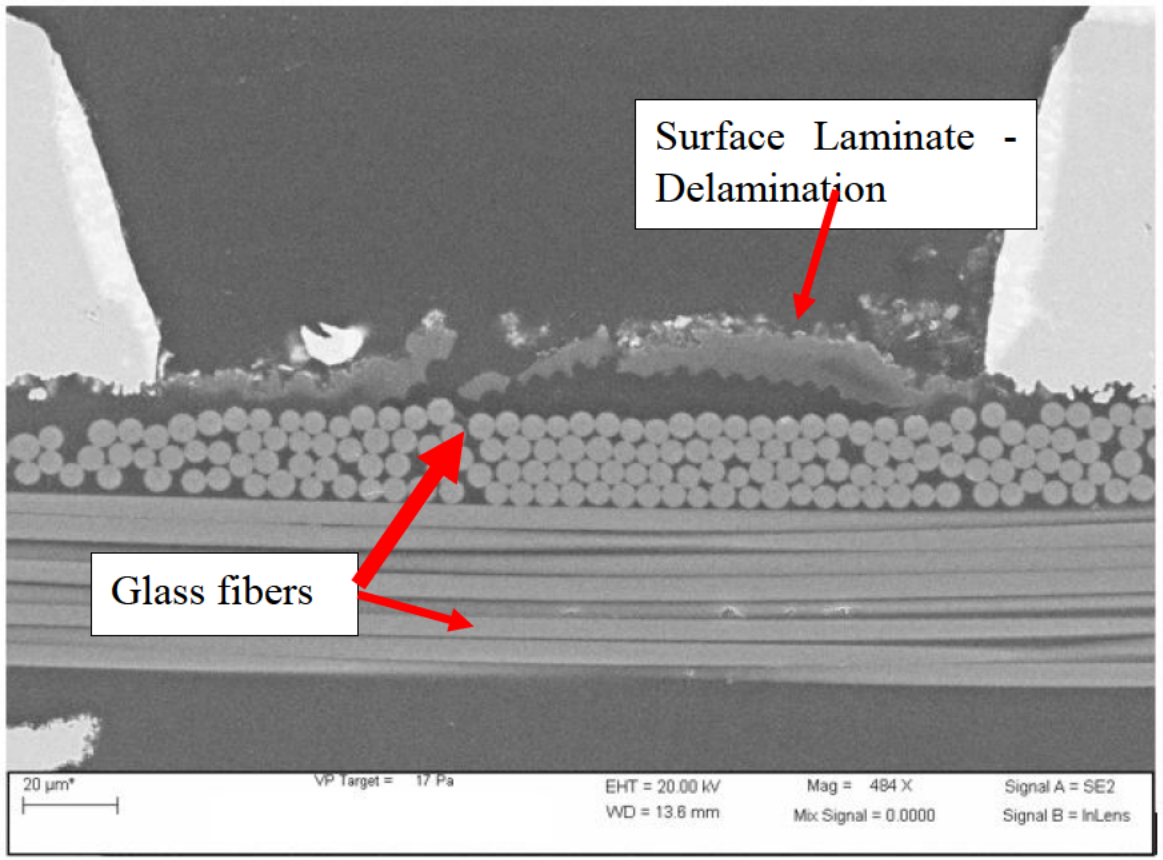
- To validate that the strip process did not disturb areas of the laminate underneath plated copper, surface pads were removed from an affected PWA.
- There was no evidence of dielectric erosion or exposed weave present at those pad locations.



Evaluation and analysis - SEM

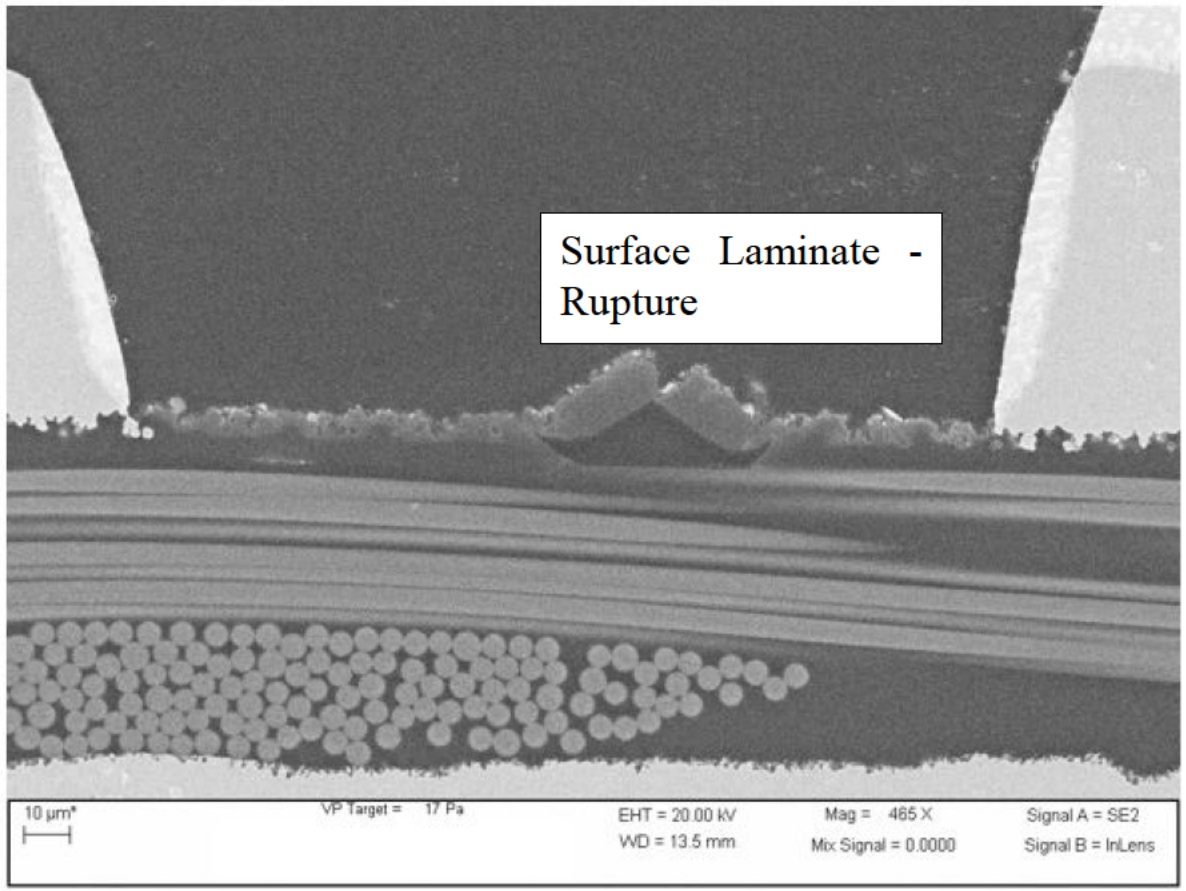
- A section of an affected PWA was examined between pads of a leaded component.
- The results depicted a number of areas where the surface laminate was separating and lifting from the PCB weave. It also shows areas where the surface laminate had ruptured.

Evaluation and analysis - SEM



SEM photograph of area between surface pads, surface delamination, 484X

Evaluation and analysis - SEM



SEM photograph of area between surface pads, surface rupture, 465X

Evaluation and analysis – SEM with EDS

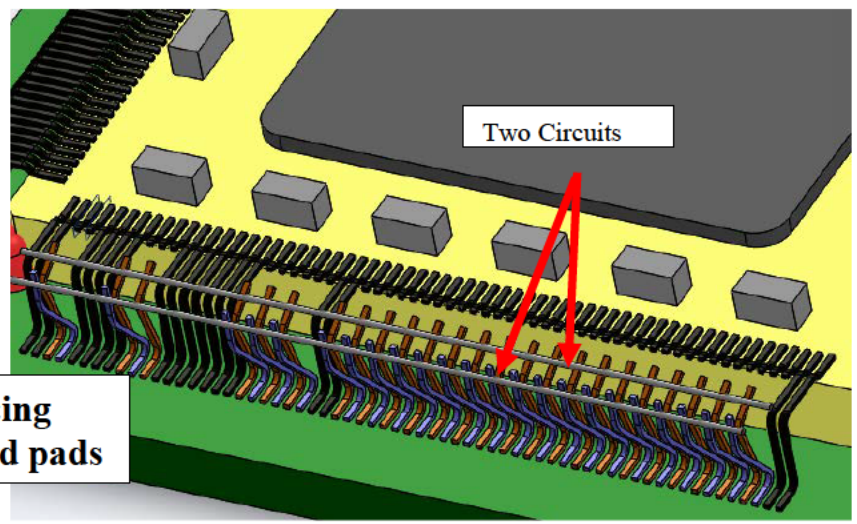
- A section of an affected PWA was examined where there was visually open weave. EDS provides elemental analyses of the area.
- The analysis showed unusually high concentrations of silicon, calcium and bromine. No control sample was used.
- This sample had previously been subjected to assembly processing, acoustic microscopy and it had been micro sectioned, so it is difficult to determine at what stage these high concentrations may have been deposited.
- A control sample was later used in mock assembly and cleanliness testing which is described later to better determine if the weave exposure trapped cleaning and assembly solvents.

Evaluation and analysis – Dielectric Breakdown

- A section of an affected PWA was examined where there was visually open weave.
- This test characterizes the PCB materials ability to resist electrical breakdown, not only between layers, but also between conductors.
- The test was configured so that the leads from a component on one side were configured in such a way to provide a two-row pattern where the leads were bussed together to form two circuits.

Evaluation and analysis – Dielectric Breakdown

- Test performed in accordance with IPC-TM-650, method 2.5.6.3
- Material data sheet: 4.7 x 10E04 V/mm (1200 V/mil)
- Results: 0.8 -1.1 X 10E04 V/mm (215 V/mil to 277 V/mil). Orders of magnitude greater than typical voltages on the pins.
- No control sample was used. Results indicated electrical breakdown between adjacent conductors and led us to CAF and cleanliness testing.

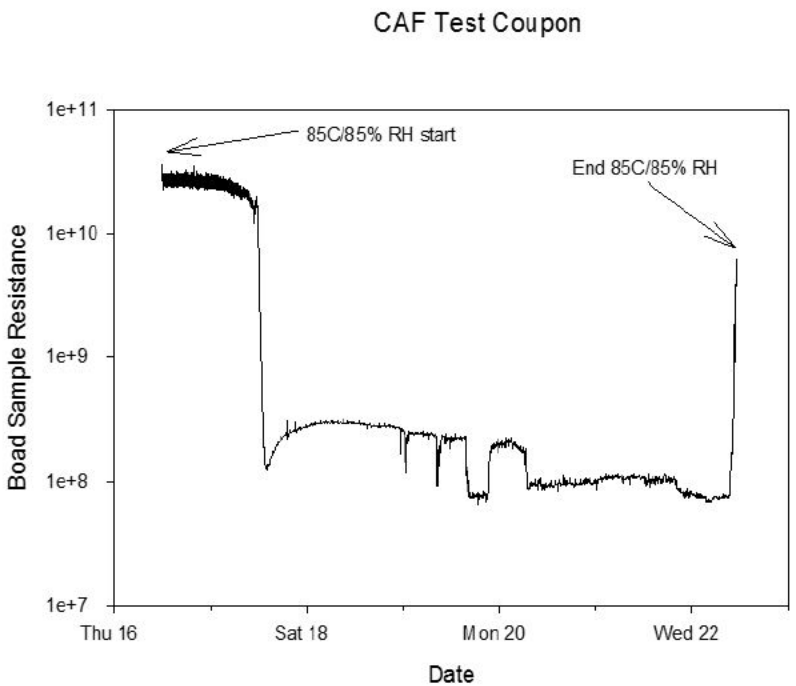


Evaluation and analysis – CAF Testing

- CAF is an electrochemical process involving the transport of a metal through, or across, a nonmetallic medium under the influence of an applied electrical field.
- In this context, it would involve the formation of conductive filaments, within the PCB material, that could bridge two conductors, resulting in shorts and failures.
- Typically this is a long term issue as a function of time, temperature, voltage bias and moisture.
- The affected PWA section was prepared identically to dielectric breakdown test sample, except the leads, pads, and bus wires were conformally coated

Evaluation and analysis – CAF Testing

- Test performed per IPC-TM-650, method 2.6.25 using 100V, 85% and 85C. Similar configuration as dielectric breakdown. A decade drop in insulation resistance as a result of applied bias constituted a failure.
- Test lasted for 6 days then failed. Baseline testing not shown below.



Evaluation and analysis – Cleanliness testing

- SEM EDS, dielectric breakdown and CAF were done with no control samples.
- Simulated assembly operations, using a control sample, was analyzed using ion chromatography to determine if standard manufacturing operations had a deleterious affect on PCBs with open weave condition.
- An independent lab was sent an impacted PCB from stock (no assembly operations) after being photo documented. Two areas were to be analyzed. Weave exposure between component pads as well as connector pads.

Evaluation and analysis – Cleanliness testing

- Results indicated that in the as received condition, the locations analyzed met recommended levels of contamination.
- Assembly reflow operations were then performed using same solder flux, paste, reflow profile, aqueous cleaning, and saponifier as what is used in production.
- The results indicate that the sample areas reviewed show an increase in ionic residues from the baseline.
- Specifically, acetate, chloride and ammonium levels (residuals from cleaning solutions) were increased above recommended limits posing moderate to high risk of electrical leakage or corrosion problems.

Corrective/Preventive Actions

- All suppliers received a quality alert that requested a heightened sense of awareness for weave texture conditions that may actually be weave exposure at higher levels of magnification.
- All suppliers have agreed (in writing) that cured soldermask stripping can not occur on product without authorization from the procuring agency.
- A formal review of all types of standard rework procedures has been conducted with the PCB suppliers so that risk levels can be associated with certain rework procedures.

Conclusion

- A concise approach was used to determine if the product affected by the soldermask strip process could be used.
- The culmination of the investigation and evaluation indicated that the original weave exposure condition, coupled with typical assembly processes, would likely result in significant issues/failures for the affected assemblies.
- Therefore, it was recommended that all PCBs and PWAs built with this date code would not be used in the CS in which these PWAs are used.

Acknowledgements

- Crane Division, Naval Surface Warfare Center, Crane, Indiana
  - *Ted Jones*