Comparison of Finite Elements Based Thermal Shock Test Reliability Assessment with a Specimen Based Test Approach

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1 Abstract

When it comes to reliability assessment of an electronic system, consisting of several components, such as an assembled printed circuit board (PCBA), this often turns out to be a challenging task. The more different partners within the supply chain are involved the more a specimen and testing based approach becomes difficult, causing increased time demand and higher testing cost.

One way to tackle this topic is to intensify the use of finite element based simulation for reliability assessment. While state of the art in many areas of industry, from aerospace industries to construction works the use of Finite Element Analysis (FEA) is still somewhat uncommon in printed circuit board (PCB) industry.

The current paper presents a good use case for the application of FEA for the assessment of the thermal reliability of PCBAs. The samples have been stressed by thermal shock test (TST), with a distinct focus on the failure modes of the solder connections between surface mount devices (SMD) and the PCB.

The defined PCBA systems were transferred into 3D finite element models, considering major material parameters such as the orthotropic behavior of the laminate layers or the highly non-linear behavior of copper and solder. The established models were then subjected virtually to TST in order to investigate the reliability performance of the systems. Based on the initial models the main phenomena influencing solder failure were identified and investigated more closely.

Finally, the results obtained from the finite element based virtual assessment were compared to the results of the actual hardware based test series regarding the solder failure mode and system lifetime in order to show the current capabilities of FEA as a tool for reliability assessment.

2 Introduction

PCBs are needed principally for all electronic devices. According to the acceptance criteria [1], the PCBs have to be subjected to the TST in accordance with IPC-TM-650 [2] and no more than 10% increase of the electrical resistances of the test structures on the PCBs are allowed. Cracks in the plated through holes (PTH) and/or the laser vias are most commonly occurring failure modes, which can be mainly attributed to the coefficient of thermal expansion (CTE) mismatch between the copper and the FR4 materials (i.e., glass fiber-reinforced epoxy laminate sheets). Thanks to the technology advancement, the glass transition temperatures (Tg) of the PCB raw materials are getting higher and the CTEs are getting smaller. For instances, the Tg of the materials used in this study are ranged between 150°C and 290°C, which are all higher than the maximum testing temperature (125°C) of TST. Their out-of-plane CTEs before Tg are rather low ranging from 18 to 61 ppm/°C. That means, the CTE mismatch within PCB shall not be the fatal factor in terms of TST failures.

On the other side, many authors [3, 4, 5] have been putting their efforts to investigate the reliability of the solder joints between the components/packages and the PCB. The reliability of the solder joints is the ability of the joints to function correctly as designed under defined application environments for the given lifetime of the electronic device. Because of the increase of the amount of joints accompanied by the reduction of the geometries, the reliability of the solder joints becomes more and more critical [6]. Therefore even for the PCB manufacturers, it is important to design and select the materials on the basis of the assembled printed circuit board (PCBA).

Since Motorola and Citizen jointly developed the plastic ball grid array (BGA) technology in 1989 [7], it has being widely used for board connection of microprocessor devices. Many literatures [3, 8, 9] are available for the reliability prediction of BGAs under different loading conditions, such as mechanical vibrations and drops, thermal cycling and shock etc. In this study, the PCBA samples, comprising one rigid PCB and four chips which were surface mounted onto the PCB via the BGA technology. The samples were tested under the thermal shock loading in the temperature range between -55°C and +125°C. Test structures were monitored with an in-situ resistance measurement system so that the temperature cycle-number of failure based on the resistance change rate can be accurately determined.

The PCBA system involves different materials, which impose thermally induced displacement onto the solder interconnections. The purpose of performing the TST was to identify the best material out of seven candidates for a specific PCBA design/application. This experimental driven material selection was time consuming and expensive in cost. For example, nine months were spent for figuring out the best material. In order to utilize the learnings out of these experiments, an FEA based method was developed. Compared to the conventional TST test, this simulation methodology was expected to give a fast response in terms of the PCB build-ups and material selection.

3 Experiments

1 Test setup

The PCB is a standard 10-layer board with four identical chips assembled on the top surface via SAC305 solder balls. PCBs were produced with seven different prepreg materials. Depending on the material thicknesses, the final thicknesses of the PCBs varies from 0.864mm to 1.004mm. The nominal thickness of the chip is 0.57mm. Other dimensions are presented in Figure 1. Each chip includes a daisy chain design so that a complete circuit with 5Ω initial electrical resistance, which connects chip and PCB, can be formed after SMT process. Chips were first dipped into the 100µm flux without solder paste and then were reflow soldered within a nitrogen atmosphere. After reflow, the quality of the soldering was checked by 100% X-ray inspection and 100% resistance measurement in order to avoid any solder joint failures before TST. An example of the BGA area under X-ray inspection is shown in Figure 2.

The TST equipment consists of one cold chamber, which was set to -55°C, and one hot chamber, which was set to 125°C. The in-situ resistance monitoring was conducted always in the hot chamber with a 1A measurement current. By default, the dwell times in both chambers were 15min. However, in case of more samples, the dwell time in the hot one was extended to 20min in order to complete the resistance scanning. The test-till-fail strategy was applied to all the samples. The samples were divided into seven groups in line with the prepreg material types and were marked as Mat01, Mat02, Mat03, Mat04, Mat05, Mat06 and Mat07. Eight samples per group were tested. Since each sample has four chips/circuits, finally 32 measurements per material type were performed. The resistances of the circuits at the first cycle were referred to as their original resistances and the resistance change rates were calculated after the test according to Equation 1:

$$\Delta R_n = \frac{R_n - R_1}{R_1} \times 100\%$$

Equation 1

Where, ΔR_n is the resistance change rate at the n-th cycle, [%];
R_n, R_1 are the resistance at the n-th and first cycle respectively, [Ω].

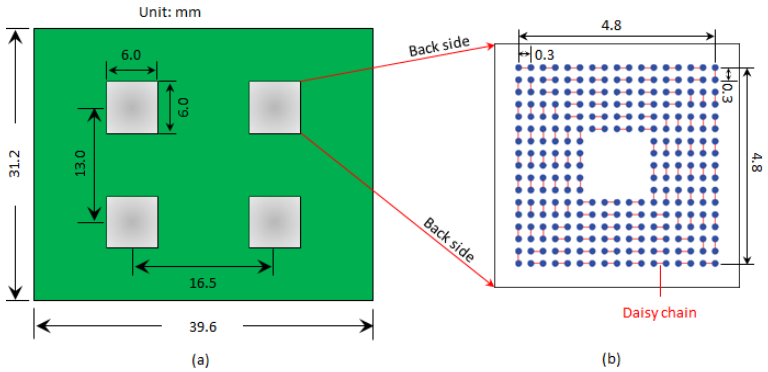

Figure 1 Setup and dimension of PCBA (a) and bottom view of the chip (b)

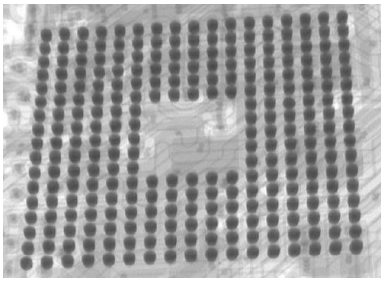

Figure 2 Example of a BGA area after SMT under X-ray inspection

3.1 Results and analysis

3.1.1 Data handling

The online resistance measurement data can be used for determining the cycles to failure, because the resistances will increase slowly at low number of cycles and start to jump up when failures propagate as exemplified in Figure 3. However, the criteria of 10% resistance change according to IPC [2] is obviously not suitable for this case: on the one side, certain abnormal jumps due to the in-situ resistance measurement device shall not be considered as failures (marked by the red circles in Figure 3); on the other side, all the samples experienced the sudden change of the resistance at the change rate of 1-2% excluding the abnormal jumps. Therefore, instead of applying a fixed total resistance change (3% or 5% for instances) as the criteria, a resistance change rate greater than 0.5% per cycle was defined as the failure criteria in this study and its corresponding cycle was recorded as the cycle to failure. Figure 4 shows cycle to failure (indicated by the end of each curve) of Mat01 and Mat06 by removing the data after failure based on the new rule.

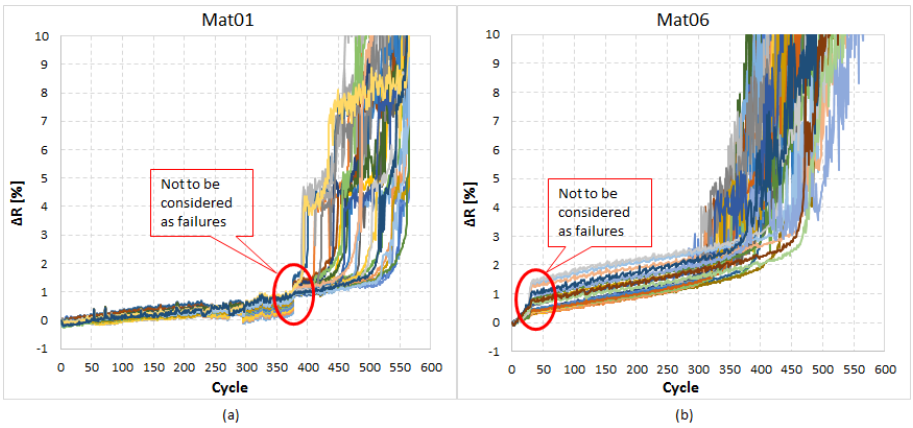

Figure 3 Resistance change of Mat01 (a) and Mat06 (b) directly calculated based on the online resistance measurement data

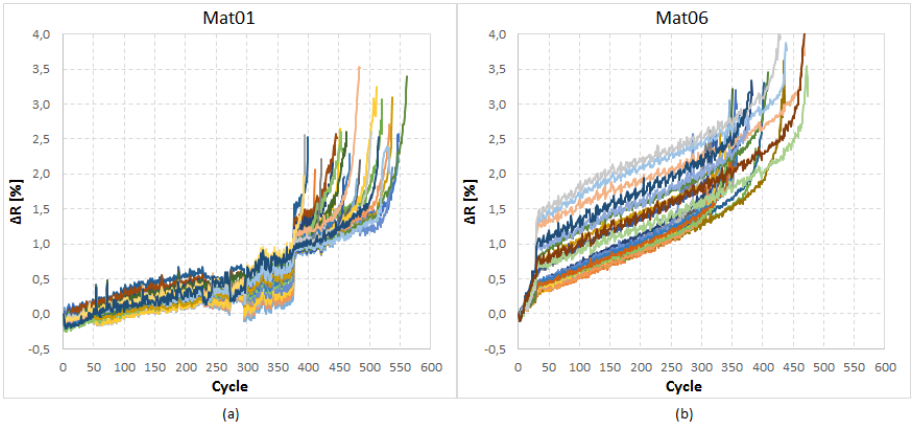

Figure 4 Resistance change of Mat01 (a) and Mat06 (b) by removing the data after failure so that the cycle to failure (end of each curve) can be visualized

3.1.2 Weibull analysis

The Weibull distribution is one of the most commonly used [10, 11, 12] reliability distribution in the electronics industry for modelling the cycle to failure of electronic components or devices. The most often found two-parameter Weibull distribution, or the so-called scale-shape-version was used in this study, which is given by [13]:

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}}$$

Equation 2

Where, f(t) is the probability density function (pdf) of failure at t number of cycles, [%];

β is the shape parameter (β>0), [-];
η is the scale parameter (η>0), [-].

The Weibull charts shown in Figure 5 were plotted in a statistical software. Originally, each group contained 32 data points. Some obviously bad points due to measurement artefacts have been excluded. The right-censored data was estimated with the maximum likelihood (ML) method. Two-sided 90% confidence bounds were applied in the analysis in order to obtain a closed interval, where 90% of the population is likely to lie. Therefore, the confidence level of the lower bound is 95%. Many different indicators can be used for the life prediction, such as the median, η, the mean, or the Mean-Time-To-Failure (MTTF). However, in this study B5, i.e., 5% failure rate was taken as the criteria for the purpose of a better control of the product quality.

Furthermore, the shape of the Weibull distribution is an important indicator of the failure mode, i.e., different shapes indicate different failure modes. It can be seen clearly from Figure 5 that the shape of Mat02 is different with all the other six groups. It means that the failure mode of Mat02 is expected to be different from the others.

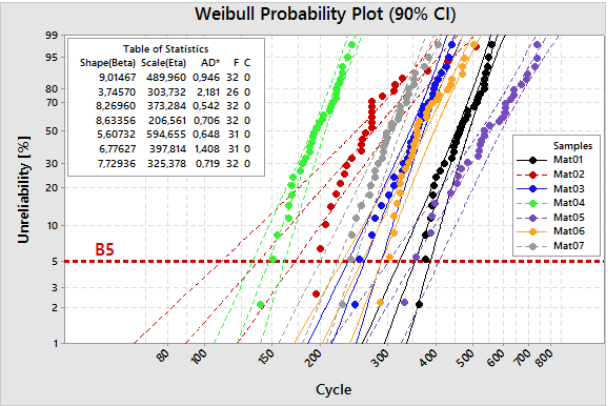

Figure 5 Weibull probability plot with 90% confidence interval

Three cross-sections for each group were made, which were taken from the early, median and late failures respectively. Because solder joint cracks were found for all failed samples in the outermost rows/columns of the BGA regions, no further investigation was carried out and some typical images are shown in Figure 6. Most of the cracks occurred on the top side where the chips sit. This might be due to the test-till-fail strategy, the initiation of the cracks cannot be observed and therefore no significant differences can be found in the cross-section images between Mat02 and others. Nevertheless, the other six can be assumed to have the same shape parameter, which is 7.43815. This have been proofed using a hypothesis test which gives a p-value of 0.155 (p>0.05 means that the Null-hypothesis cannot be rejected using a risk level of α = 0.05).

The cycle to failures with 5% unreliability (B5) of each group are shown in Figure 7 by black circles. The error bars stand for the upper and lower limits of B5. Additionally, the resistance change rates per cycle are exhibited. These were calculated based on the slopes of the best-fit lines for the parts, which stand for the stable increase of the resistance as shown in Figure 4. Obviously, the correlation between the lifetime and the resistance change rate per cycle is strong. That means, the faster the resistance change rates the shorter the lifetime of the solder joints will be. It fits for all the groups except Mat02, which has a different failure behavior as shown in Figure 5.

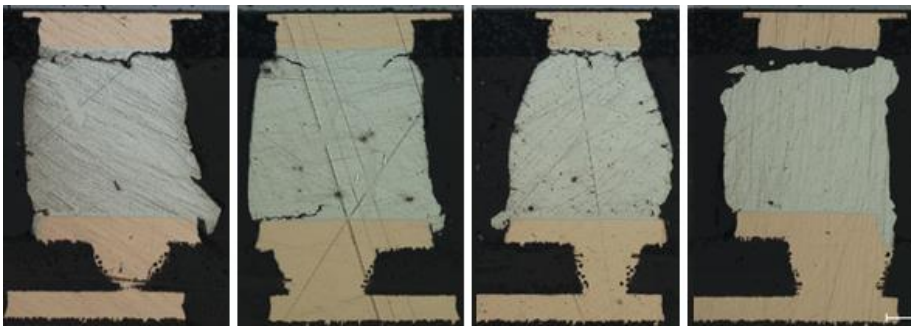

Figure 6 Typical cross-section images for the solder joint failures (chips are on the top side)

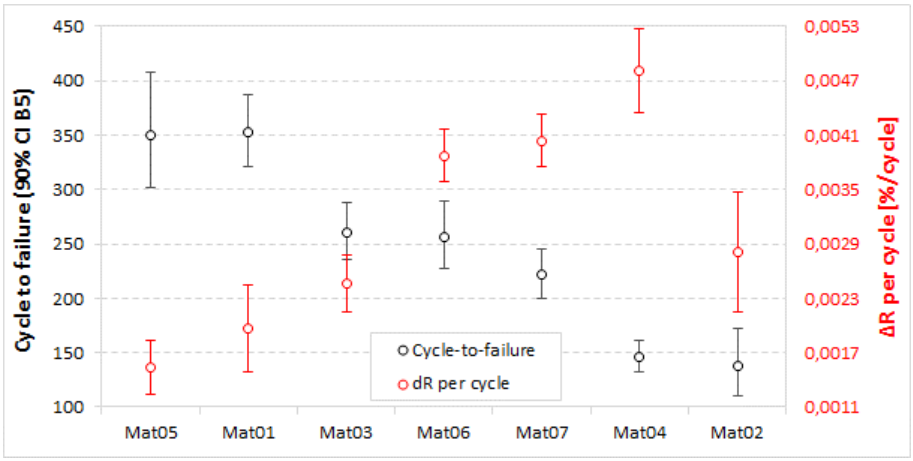

Figure 7 Relationship between cycle to failure and the resistance change rate per cycle

4 Simulation

4.1 Modelling

The PCB was modelled via the Virtual PCB Builder™ [14], which facilitated the generation of PCB models for FEA and reduced their complexities significantly by applying the rules of material homogenization. Furthermore, shell approach was applied for each layer because less equations are required to solve in shell models since the wall thickness is captured as a mathematical value instead of actually modelling the thickness and consequently the calculation will be fast. The PCB layer thicknesses used in the models vary among different groups according to the value measured via cross-sectioning. But the layer designs for all groups are the same. The original design with the dimensions of 5262px × 4184px and each 32px × 32px were homogenized into one material. Since the real PCB size is 39.6mm × 31.2mm, the final resolution of a PCB layer is around 4.1px/mm or 244μm/px.

A commercial FEA software was utilized for the simulations. The element type of the PCB was the linear quadrilateral type S4R (4-node, reduced integration). The chips and solder joints were modelled directly in the CAE (Computer Aided Engineering) of the software with the quadratic hexahedral element type C3D20R (20-node, reduced integration). The completed PCBA consists of 406680 S4R elements and 25344 C3D20R elements.

Figure 8 presents the PCBA model in the CAE. Three boundary conditions on the corner nodes of the bottom side of the PCB were applied: 1) BC1 fixed all degrees of freedom for the lower-left corner node (U1=U2=U3=UR1=UR2=UR3=0). 2) BC2 locked the movement of the lower-right one along Y and Z directions (U2=U3=0). 3) BC3 locked the movement of the upper-right one in Z direction (U3=0). Three temperature profiles were used in this study as shown in Figure 9: Profile 1 represents one TST cycle including two steps, i.e., a ramp-up from -55°C to 125°C and a cool-down from 125°C to -55°C; Profile 2 stands for four TST cycles; Profile 3 contains only one heating step from 20°C to 125°C. The temperature profiles were always applied to the whole model so that the equilibrium states of the model at the specified temperatures were simulated.

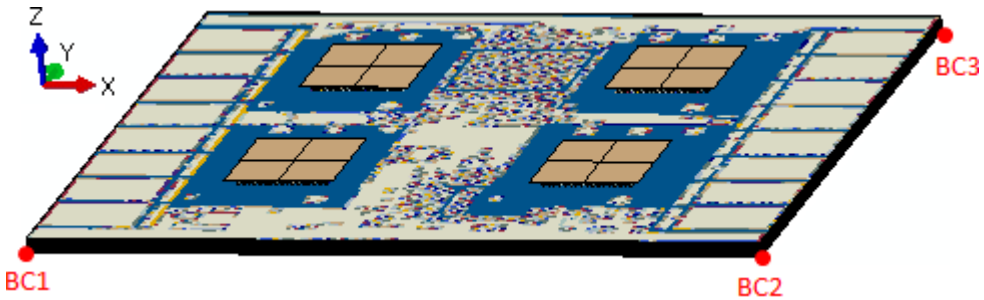

Figure 8 PCBA model in the FEA software with three boundary conditions

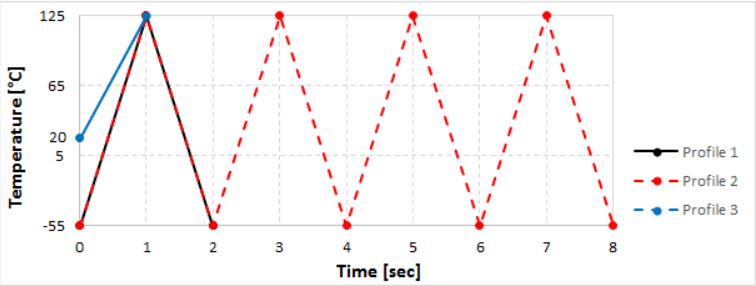

Figure 9 Temperature profiles used in the simulation

4.2 Materials

The temperature dependent elastic properties (Young's modulus, E, Poisson's ratio, ν, and CTE) of the isotropic (solder mask, resins, copper) and orthotropic (prepregs) materials have been measured and applied for the simulation. The properties of silicon was considered as temperature independent (E=160GPa, ν=0.3, CTE=2.6ppm/°C). The temperature dependent elastic properties of the solder joint SAC305 were taken from the literature [15]. Furthermore, the isotropic/kinematic hardening model for SAC305 and copper were implemented according to the literatures [16] and [17] respectively.

4.3 Strategy

Since not all the PCB material properties were available in the time period of the study, only Mat02, Mat04 and Mat05 were modeled and simulated. The simulation strategy can be divided into three steps:

1) Simulate one cycle of TST with the PCBA model by applying Profile 1 (black solid curve in Figure 9) in order to figure out the critical location of the solder joints. This model will act as a global model and offer the displacement boundary conditions to the sub-model in the next step. In this first step, the cyclic hardening properties of the solder joints and copper were not taken into account considering mainly the computational time.

2) Create a sub-model for the critical location based on the previous step and simulate four cycles of TST by using Profile 2 (red dashed curve in Figure 9) for the purpose of investigating its stress/strain condition in detail and calculating the strain increment per cycle for the lifetime prediction under the low-cycle fatigue condition. Since the sub-models were much smaller in size compared to their global PCBA models, the cyclic hardening properties can be introduced and more realistic and detailed results for a single solder joint can be obtained.

3) Simulate the thermal strain of the PCB (excluding chips and solder joints) at 125°C by applying Profile 3 (blue solid curve in Figure 9) so that its correlation to the lifetime can be investigated. It turned out eventually that the correlation is obvious and therefore the thermal strain can be considered as an indicator in the future for the selection of PCB materials in order to enhance the reliability of the PCBA regarding cyclic thermal loading.

4.4 Results and analysis

4.4.1 PCBA global models

The plastic behavior of the solder joints and copper were not considered in the global models due to the complexity of the PCB model in terms of structure and material property. Because the goal of this study was to find out an affordable computational time (within one day) for engineering applications in the future. The consideration of the calculation time was also the reason that only one cycle of TST was simulated instead of four as the sub-model. In general the nonlinear effects from large displacements and deformations should be taken into account. However, in this case, linear procedure has to be applied in order to perform the cyclic simulation for the sub-models afterwards. As exemplified in Figure 10 (a), the PCBA model of Mat05 cannot return back to its original position (0mm) with a maximum displacement of 5.99e-6mm after one TST cycle by using nonlinear procedure. Therefore, the sub-model will not find its coordinate in the global model after one cycle simulation. The situation with the linear one is much better, its maximum displacement (7.877e-12mm) can be treated as zero. Furthermore, the displacements at 125°C are compared between the linear and nonlinear procedures as shown in Figure 10 (b): both show similar displacement conditions concerning the magnitude and distribution. It is believed that the fine mesh (0.298mm × 0.298mm per element) and relatively small displacement (max 0.1274mm) relative to the geometry (39.6mm × 31.2mm) contribute to the good similarity.

The stress/strain conditions of the solder joints in the four BGA areas are rather similar. Solder joints on the lower-right area of the PCBA were chosen for all three models and their von Mises stresses are presented in Figure 11. It can be seen that the stresses in the outermost solder joints are higher than the inner ones. The highest stresses are all occurred in the solder joints

which are located at the BGA corners. These simulation results fit to the experimental findings well. Mat04 shows slightly higher stress than Mat02 and Mat05 has the lowest stress. The solder joints at the lower-right corners, as marked by red arrows in Figure 11, were selected for further investigation by means of sub-modelling approach.

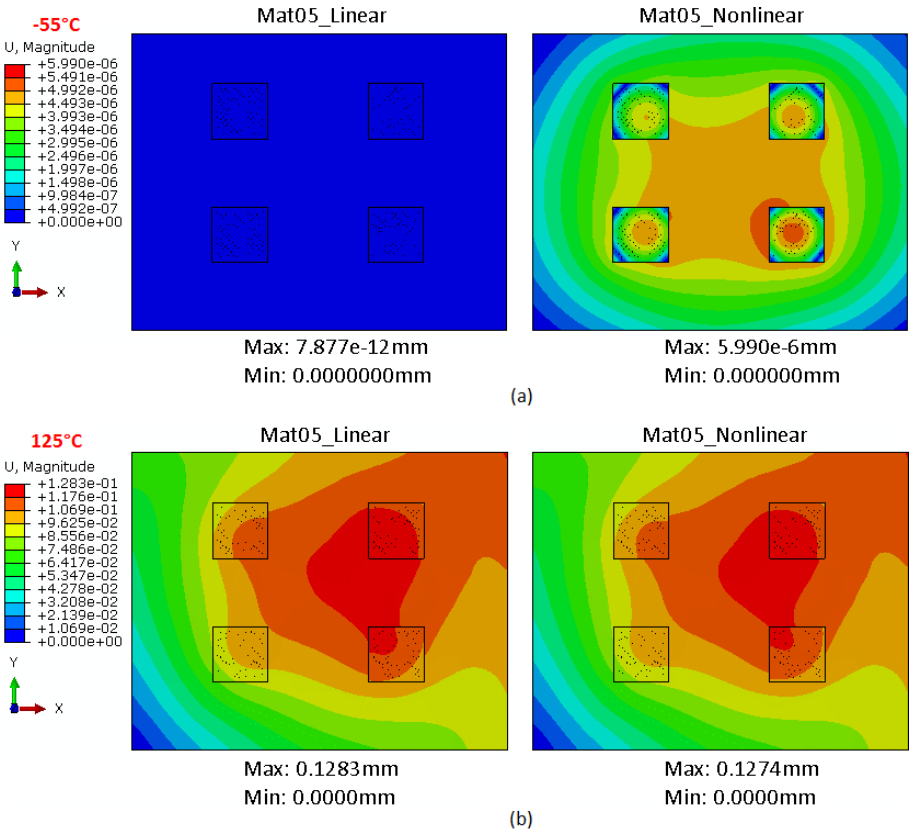

Figure 10 Top view of deformation comparisons between the linear and nonlinear procedures for Mat05 at the end (a) and at the middle (b) of one TST cycle

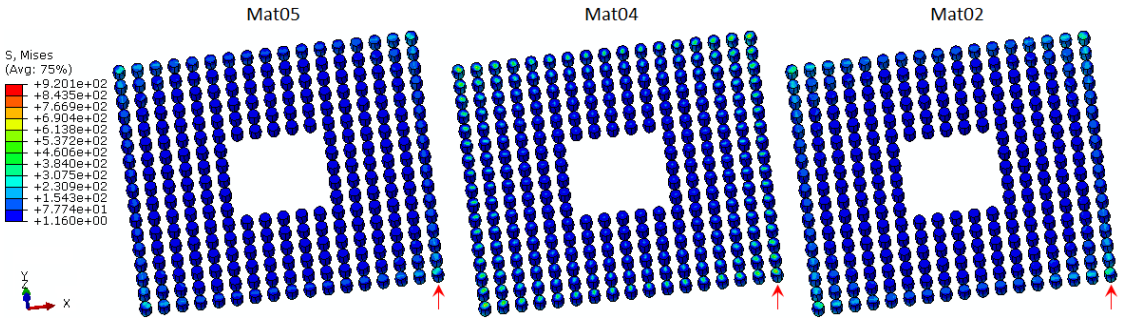

Figure 11 Von Mises stresses of the solder joints on the lower-right area of the PCBA for Mat05, Mat04 and Mat02 (chips are on the top side)

4.4.2 Solder joint sub-models

The accumulated plastic deformation is the key to predict the material lifetime under low-cycle fatigue loadings according to the strain-based Coffin-Manson model [18, 19], as described in Equation 3:

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon_f'(2N)^c$$

Equation 3

Where, $\Delta\varepsilon_p/2$ is the plastic strain amplitude, [-];
ε_f' is fracture strain [-];

N is the number of cycles to failure;
c is an empirical constant ranging from -0.5 to -0.7 for metals.

In order to obtain a constant $\Delta\varepsilon_p$ between successive cycles, four cycles of TST were simulated for the selected solder joints as marked in Figure 11. The accumulated plastic strain (PEEQ is the term used in the FEA software) at 125°C of the 4th cycle for the three sub-models are presented in Figure 12. It is clear that the critical areas are always on the top side where the chips sit. This aligns well with the cross-section findings since most of the cracks were found at the chip side of the solder joint.

Furthermore, it was found that the increase of the accumulated plastic strain starts to be stable after the first cycle. Therefore, the averaged $\Delta\varepsilon_p$ of the element, which has the max PEEQ, from the last three cycles was used for calculating the number of cycles to failure according to Equation 3. The predicted lifetimes for Mat05, Mat04 and Mat02 are shown in Figure 14 (filled red diamonds) as well as the calculated $\Delta\varepsilon_p$ and other applied parameters for each model. The actual lifetimes of all groups are plotted for the purpose of comparison. Although the results match surprisingly good, the intension was to show the tendency instead of absolute values. Because the predicted results strongly depend on the selection of the parameters, which were unknown/not measured for the actually applied solder joints.

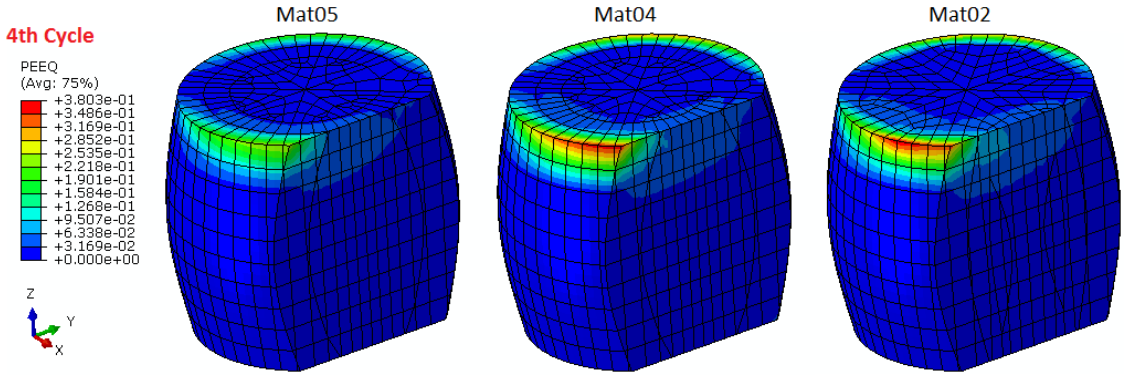

Figure 12 Accumulated plastic strain (PEEQ) of the solder joints at 125°C of the 4th cycle in the lower-right corner of the BGA area as shown in Figure 11 (chips are on the top side)

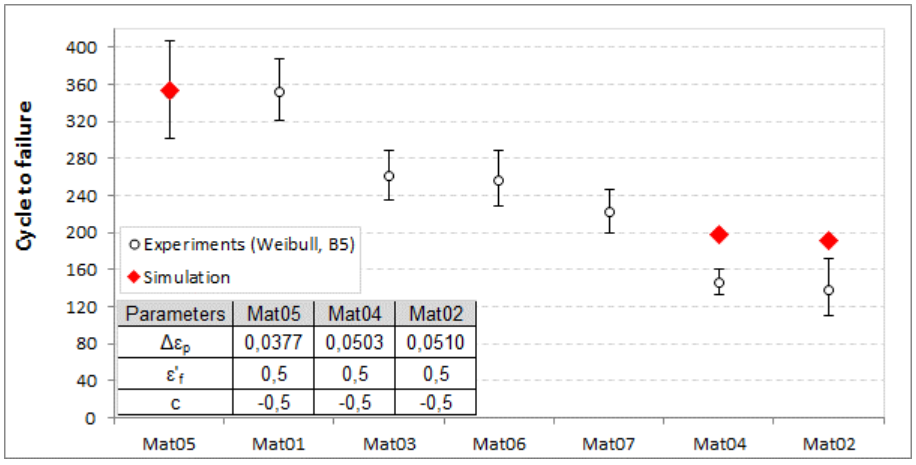

Figure 13 Comparison of the cycle to failure between the experiments and the simulation

4.4.3 PCB thermal strain

The maximum thermal strains during TST occurred at 125°C and were calculated based on all the nodes in the four BGA areas on the top layer of the PCB according to Equation 4:

$$\varepsilon_{max} = \frac{\sum_{i=1}^{m} \varepsilon_{x,i} + \sum_{i=1}^{m} \varepsilon_{y,i}}{2m}$$

Equation 4

Where, ε_{max} is the maximum thermal strain during TST test, i.e., at 125°C, [-];

$\varepsilon_{x,i}$ and $\varepsilon_{y,i}$ are the thermal strain of node i at 125°C in X and Y directions respectively, [-];
m is the total number of the nodes in the four BGA areas on the top layer of the PCB.

Additionally, the thermal in-plane expansions of the samples were investigated using a digital image correlation (DIC) technique. One sample was measured for each group and their thermal strains at 125°C were obtained using the DIC-based software. Figure 14 presents the measured seven thermal strains (unfilled red circles) and the simulated three ones (filled red diamonds). The error bars are their standard deviations. The measured mean thermal strains vary between 0.104% and 0.163%.

The simulated ones for Mat05, Mat04 and Mat02 are 0.133%, 0.159% and 0.160% respectively. Except for Mat04, the other two show obvious differences to the measured ones. But the deviations are acceptable in terms of engineering application considering following three aspects: 1) the simulation was based on the 10-layer PCB built-up with rather complex structures and material properties. 2) the variation of the materials cannot be considered since only one sample was measured for each group. 3) the thermal strain values are still in the same range as the measured ones.

It can be seen from Figure 14 that the thermal strain generally shows a good correlation with the life cycle time of the PCBA under thermal shock condition. The lower the thermal strain at 125°C, the longer the lifetime will be. It means that failure should be dominated by the in-plane CTE mismatch between the PCB and the chips.

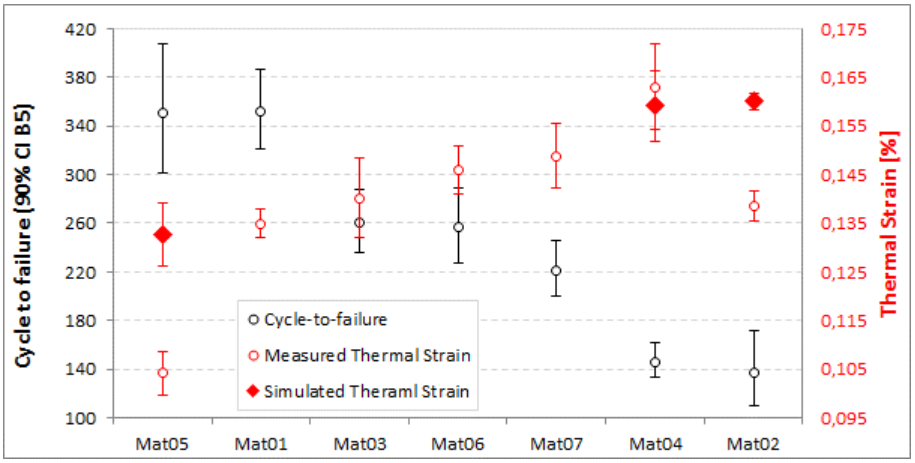

Figure 14 Relationship between cycle to failure and the thermal strain at 125°C

5 Conclusion

In this study, seven groups of PCBA samples, which differ from each other in terms of the PCB raw materials (resin and prepreg), were subjected to the conventional TST for the purpose of assessing their lifetimes, or number of cycles to failure, under the cyclic thermal loadings. Instead of applying the criteria of 10% resistance change according to IPC [2], 0.5% per cycle of the ΔR increase was found to be more suitable for the judgement of a failure. Excluding the shifting/increase of the resistance due to the measurement device, all samples failed between 1-2% of resistance change. The initiation of the failures cannot be analyzed since the failed ones have to wait until all the others fail (test-till-fail testing strategy). This should be improved in the future work in order to distinguish different failure modes via cross-sectioning after the testing.

Weibull analyses were carried out for all groups. B5 (failure rate of 5%) was chosen as the criteria for the lifetime evaluation according to the internal rule of quality control. A clear correlation between the resistance change rate per cycle and the lifetime of the PCBA sample was observed, except for the group of Mat02 that showed different failure behavior according to the Weibull analysis. However, the criteria selection for the Weibull analysis will influence the lifetime prediction. A further study based on different criterion is suggested, especially, in terms of comparing sample groups with different failure modes.

Three out of seven groups, whose PCB material properties were available, were chosen for the FEA simulation. One cycle of TST for each PCBA was simulated without consideration of the plastic behavior of the solder joints and copper in order to limit the computational time to an acceptable level. The results show that the outermost solder joints in the BGA areas suffer the highest stresses, which aligns well with the experimental findings. One sub-model for each group was made for the most critical solder joint and four cycles of TST were simulated subsequently. Both the simulated and the real failure modes show that the top side (chip side) of the solder joints experienced higher shear forces during TST.

The Coffin-Manson model was used for predicting the lifetimes of the PCBA samples. The predicted lifetimes show good alignment with the ones based on the Weibull analysis. Furthermore, an additional thermal strain simulation of the PCB at 125°C was conducted and the results indicate good correlation to the lifetime of the PCBA. This finding can be utilized for optimizing the PCB material build-up in the future.

6 Reference

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Comparison of Finite Elements Based Thermal Shock Test Reliability Assessment with A Specimen Based Test Approach

Qi Tao, Thomas Krivec, Manfred Riedler, Markus Frewein

Austria Technologie & Systemtechnik AG

Leoben, Austria

Contents

Motivation

- Development of a specimen-based PCBA level TST approach
  - Design of test vehicle
  - Evaluation method
  - Criteria of acceptance
- Development of an FEA-based TST approach
  - Modelling technique
  - Material properties
  - Simulation strategy
- Comparison of the FEA-based TST with the specimen-based approach
  - Simulation capability
  - Further development direction

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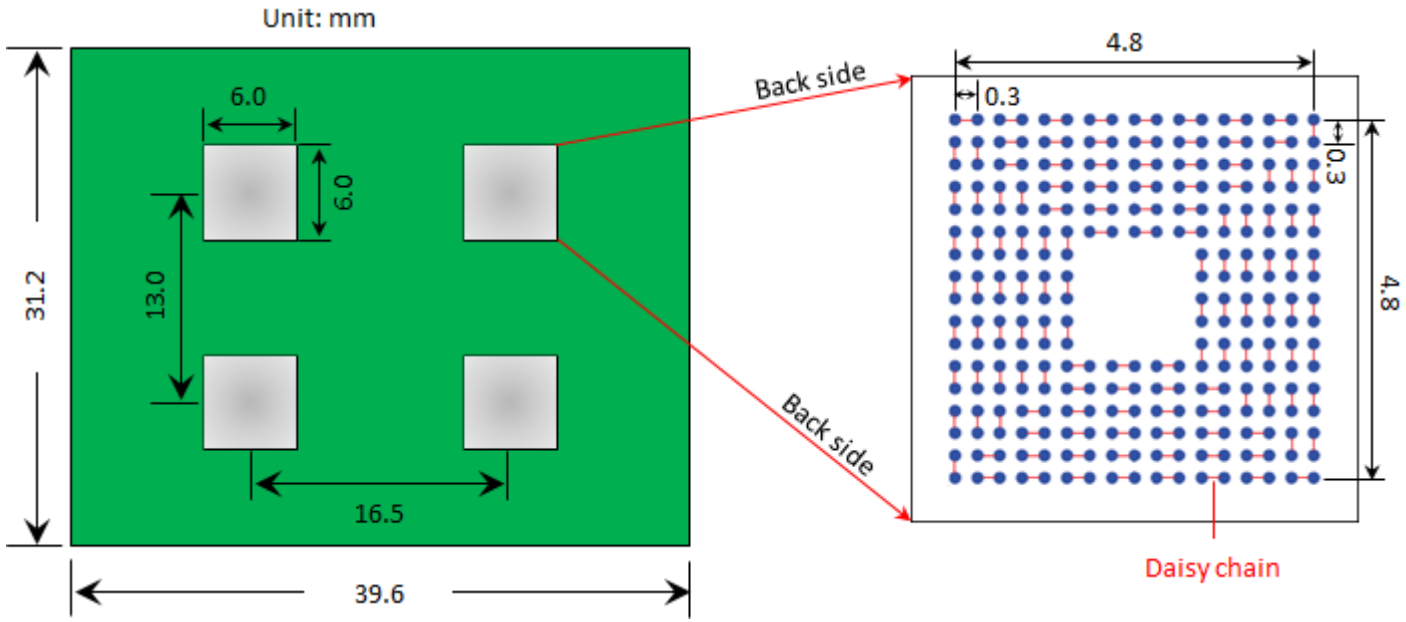
Contents

Experiments – Test setup

PCBA = PCB + 4 Chips

BGA: 17 x 17 – 5 x 5

Layer Thickness



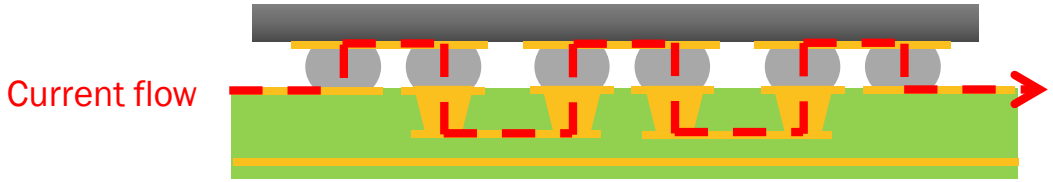
Layer	Material	Thickness [mm]
Die	Silicon	0,570
Solder	SAC305	0,170
L01	Cu	0,023
D01	PP	0,066
L02	Cu	0,017
D02	PP	0,065
L03	Cu	0,020
D03	PP	0,078
L04	Cu	0,020
D04	PP	0,067
L05	Cu	0,017
D05	PP	0,061
L06	Cu	0,020
D06	PP	0,067
L07	Cu	0,020
D07	PP	0,065
L08	Cu	0,021
D08	PP	0,073
L09	Cu	0,020
D09	PP	0,068
L10	Cu	0,026
Total	PCB	0,814
	PCBA	1,554

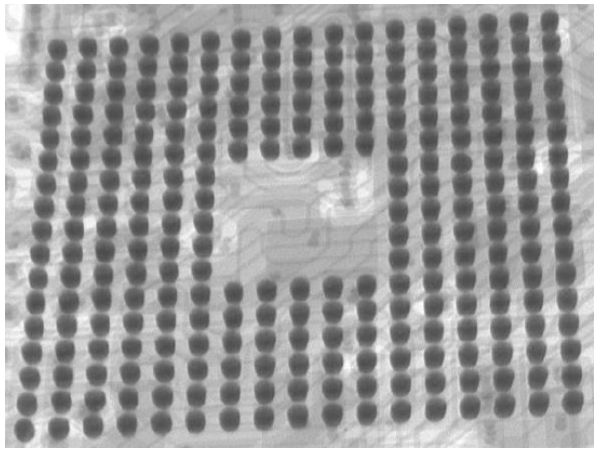
Experiments – Test setup

Reliability Test Parameter

Parameter	Setting
Temperature Range	-55 °C … +125 °C
Chamber Type	Two chamber design
Cycle Duration	Run 1: 30min (15min hot, 15min cold) Run 2: 35min (20min hot, 15min cold)
Resistance Measurement	@ hot temperature
Resistance of DUTs	Initial resistance approx. R ~ 5Ω
Measurement Current	I = 1A [2)]
Failure Criteria	Change of resistance (ΔR) > 5% $\Delta R_n = \frac{R_n - R_1}{R_1} * 100\%$ (ΔR_n … Resistance change @ cycle n, R_1 … Resistance @ cycle 1, R_n … Resistance @ cycle 1)
Test Stop	Test-till-fail strategy
Pre-check	100% X-ray inspection on the solder joints 100% electrical resistance measurement

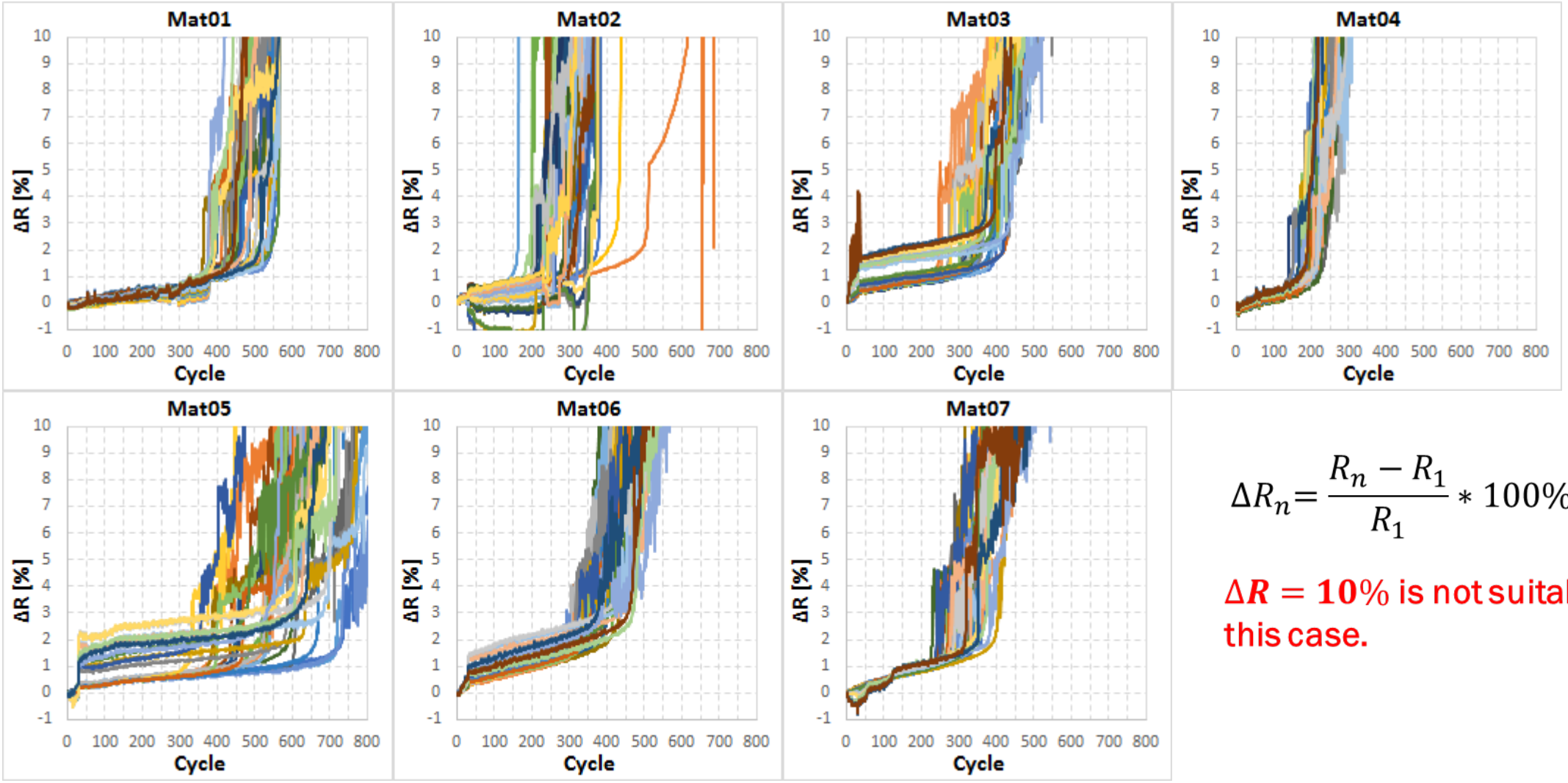
Schematic view of the DUT:





Contents

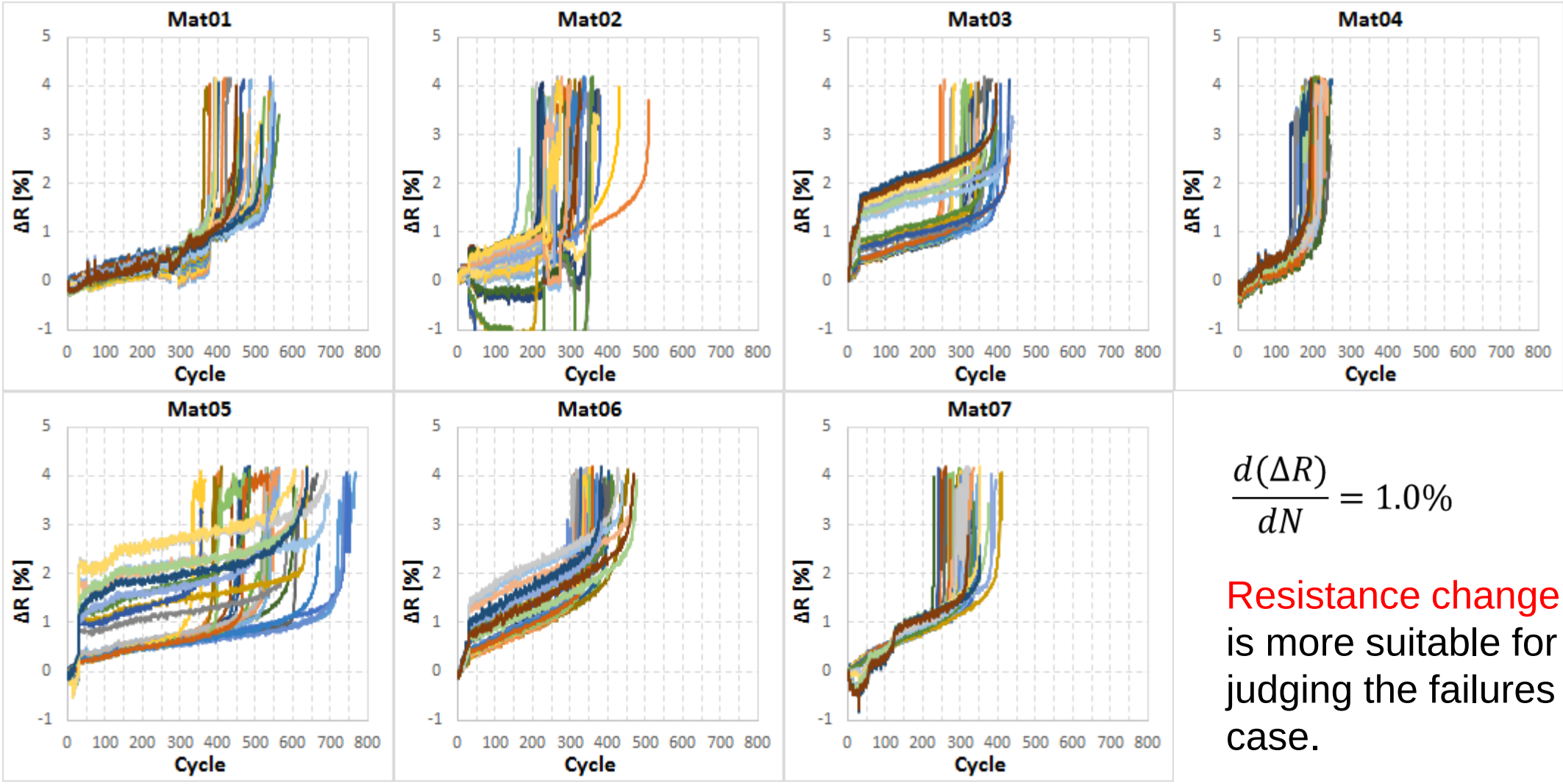
Experiments – Data handling



$$\Delta R_n = \frac{R_n - R_1}{R_1} * 100\%$$

$\Delta R = 10\%$ is not suitable in this case.

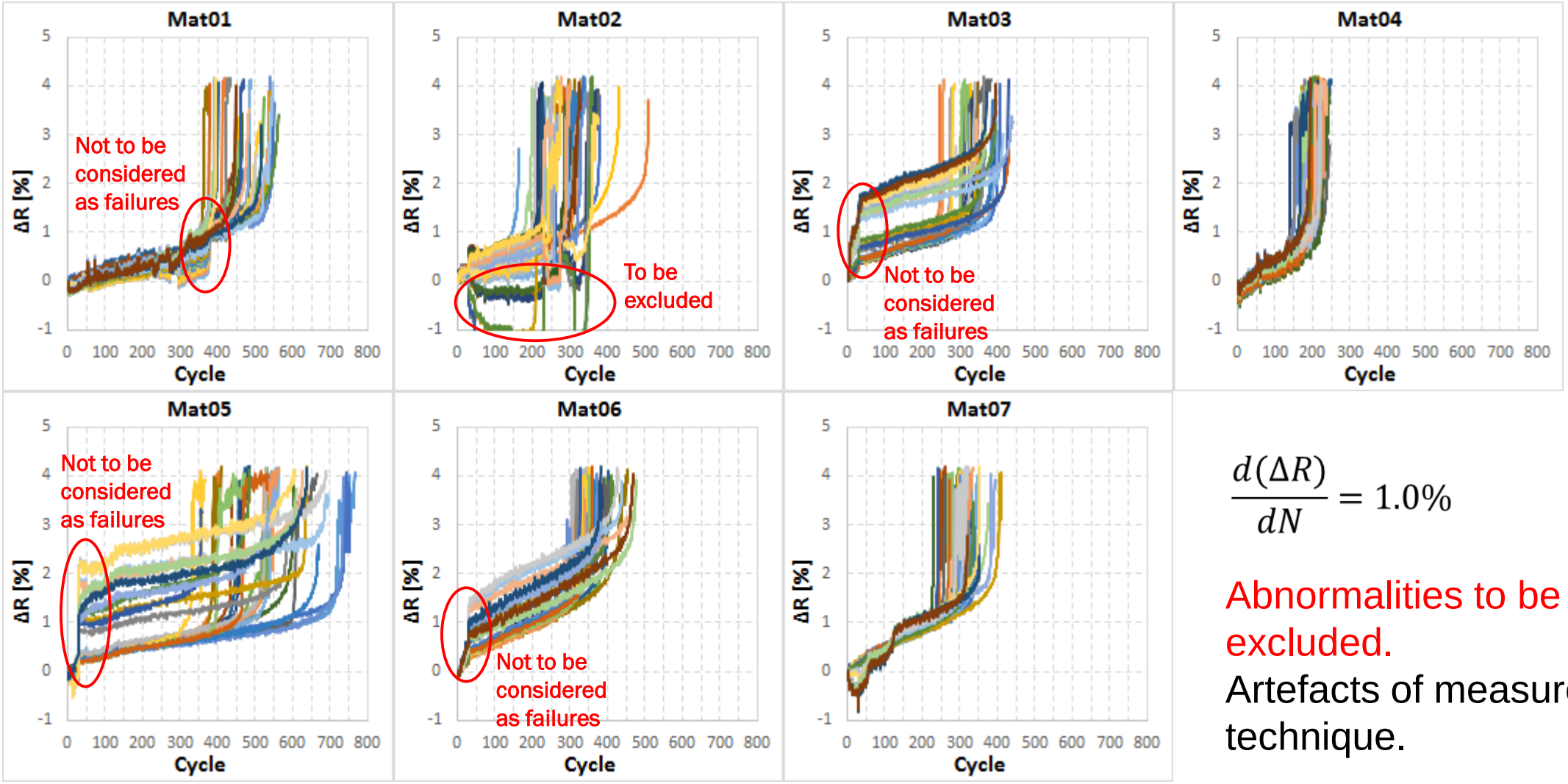
Experiments – Data handling



$$\frac{d(\Delta R)}{dN} = 1.0\%$$

Resistance change rate is more suitable for judging the failures in this case.

Experiments – Data handling

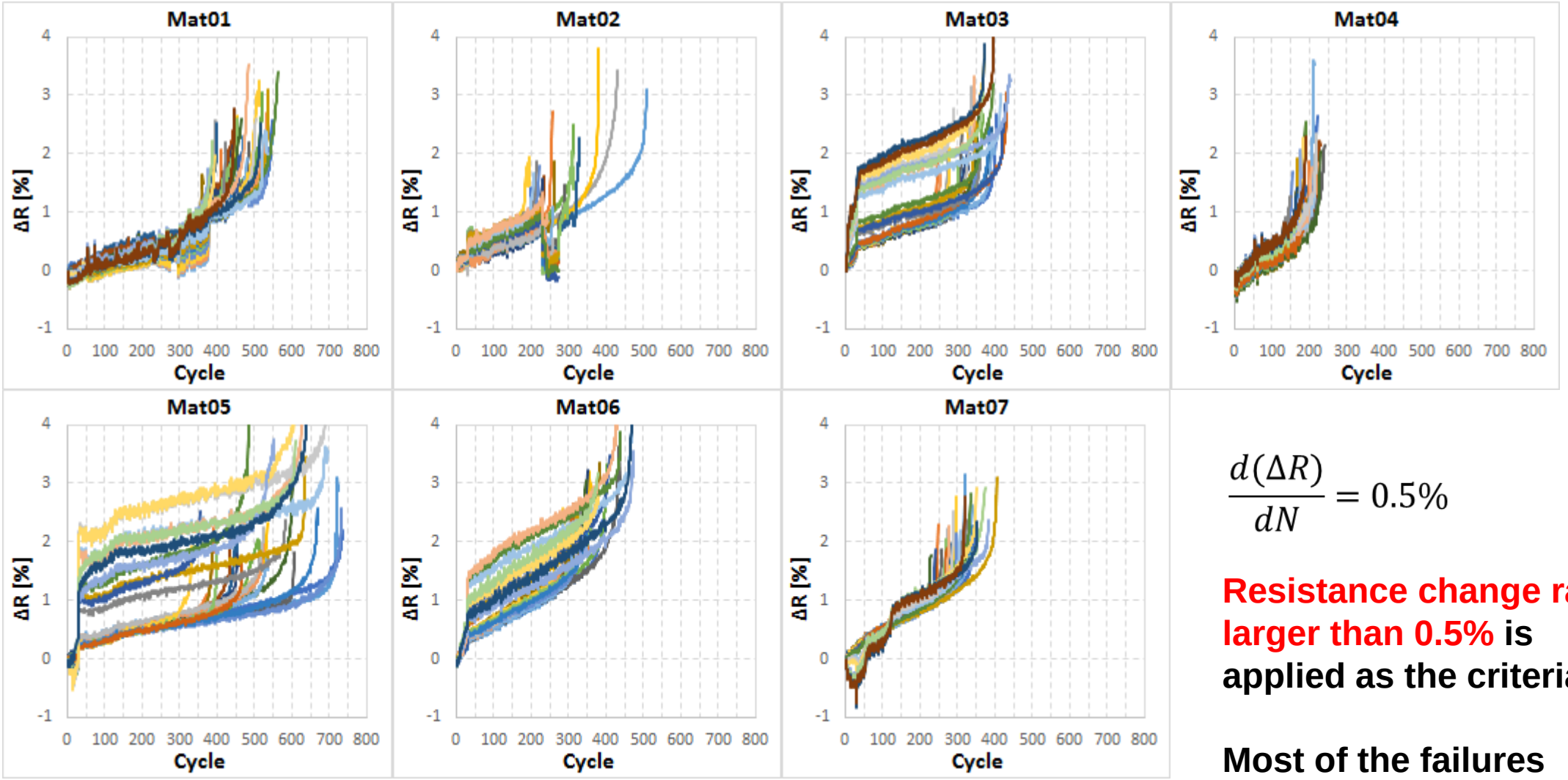


$$\frac{d(\Delta R)}{dN} = 1.0\%$$

Abnormalities to be excluded.

Artefacts of measurement technique.

Experiments – Data handling



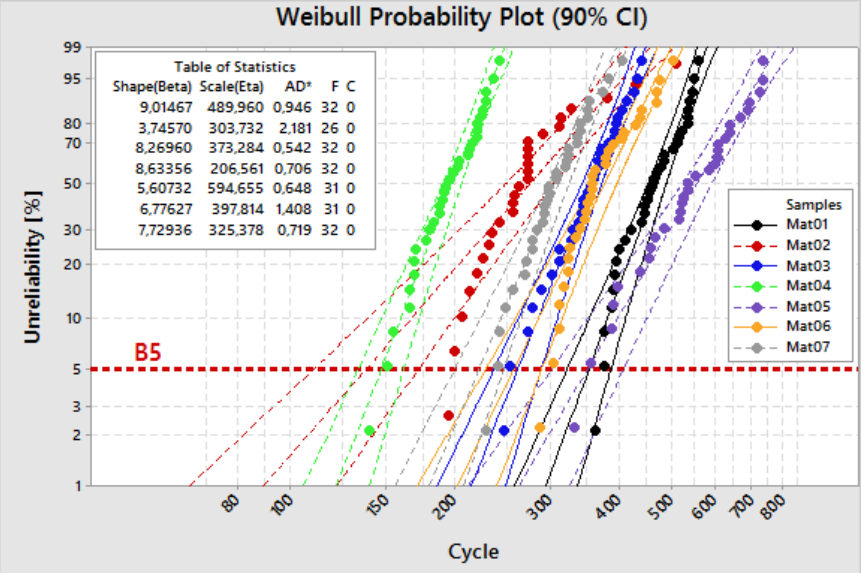
$$\frac{d(\Delta R)}{dN} = 0.5\%$$

Resistance change rate larger than 0.5% is applied as the criteria.

Most of the failures occurred when ΔR>1-2%

Contents

Experiments – Weibull analysis

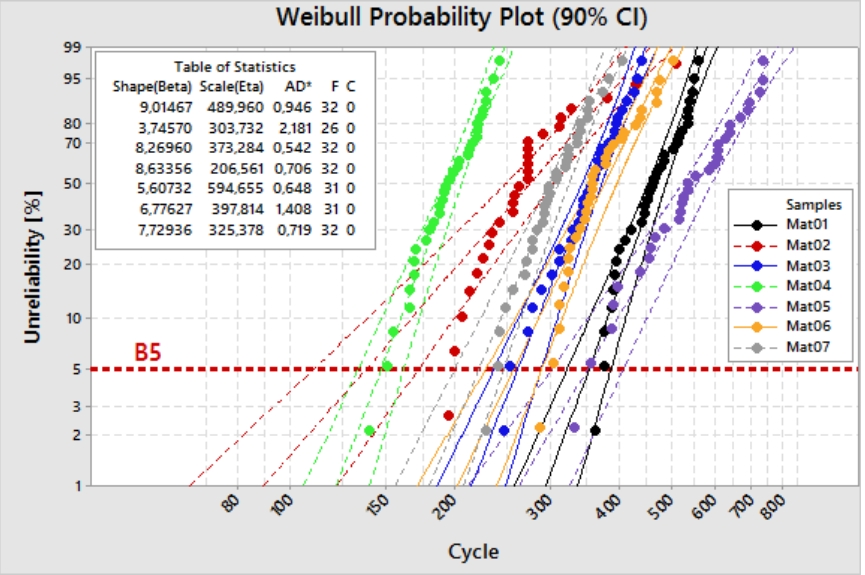


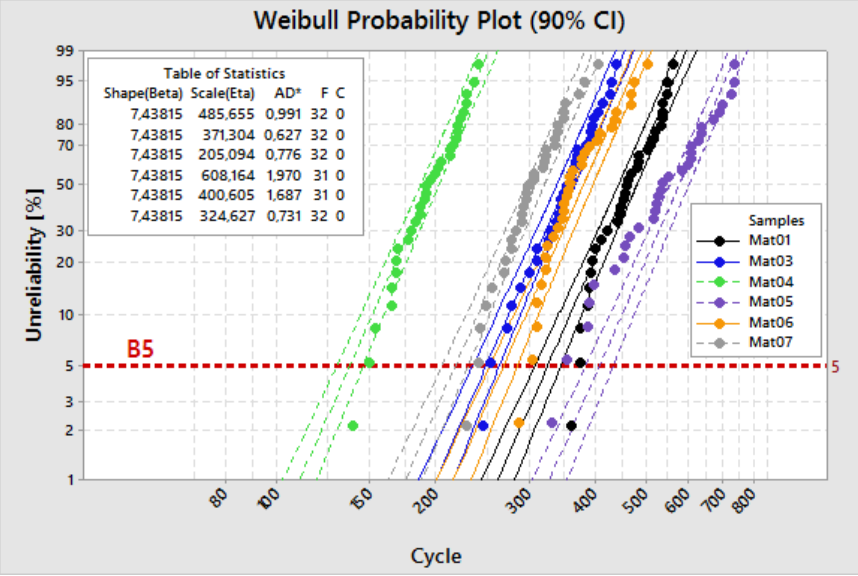
$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}}$$

Where, f(t) is the probability density function (pdf) of failure at t number of cycles, [%];
β is the shape parameter (β>0), [-];
η is the scale parameter (η>0), [-].

- Mat02 shows different failure mode.
- Without Mat02, the failure modes can be assumed to be the same with P=0.155. *(P>0.05 means that the Null-hypothesis cannot be rejected using a risk level of α = 0.05).*
- B5 (5% failure rate) is chosen as the criteria according to the internal quality control rule.

Experiments – Weibull analysis





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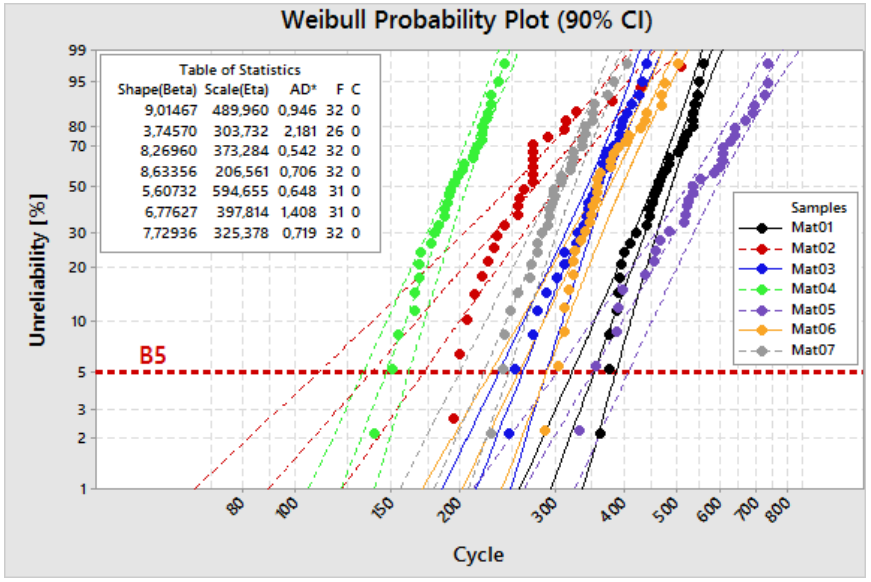

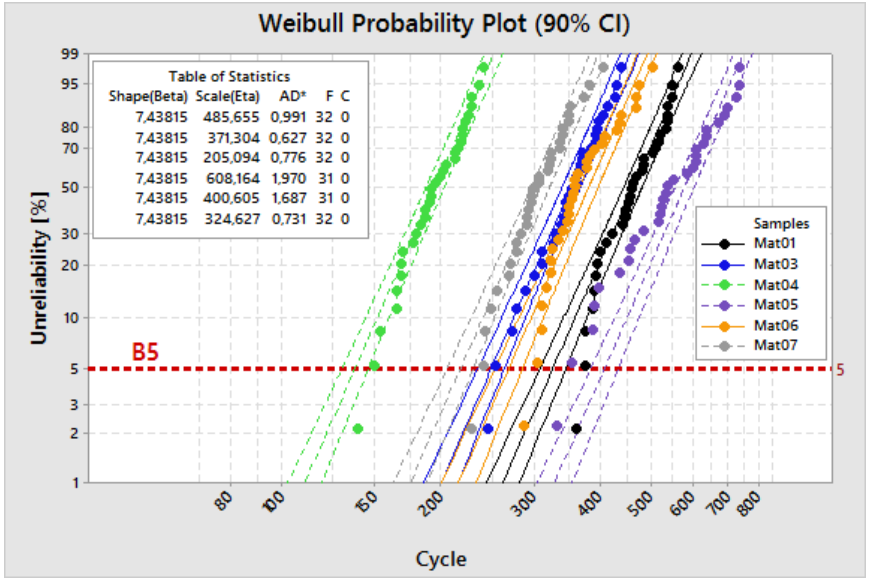

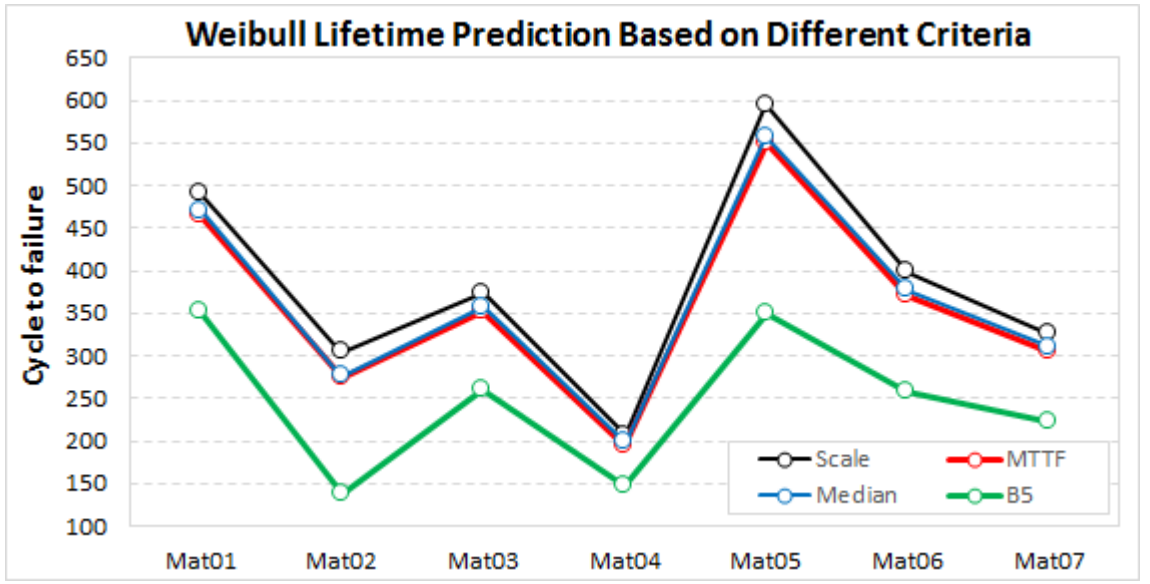

Failure rate

Scale – 63.2%

Median – 50%

MTTF – 40-50%

B5 – 5%

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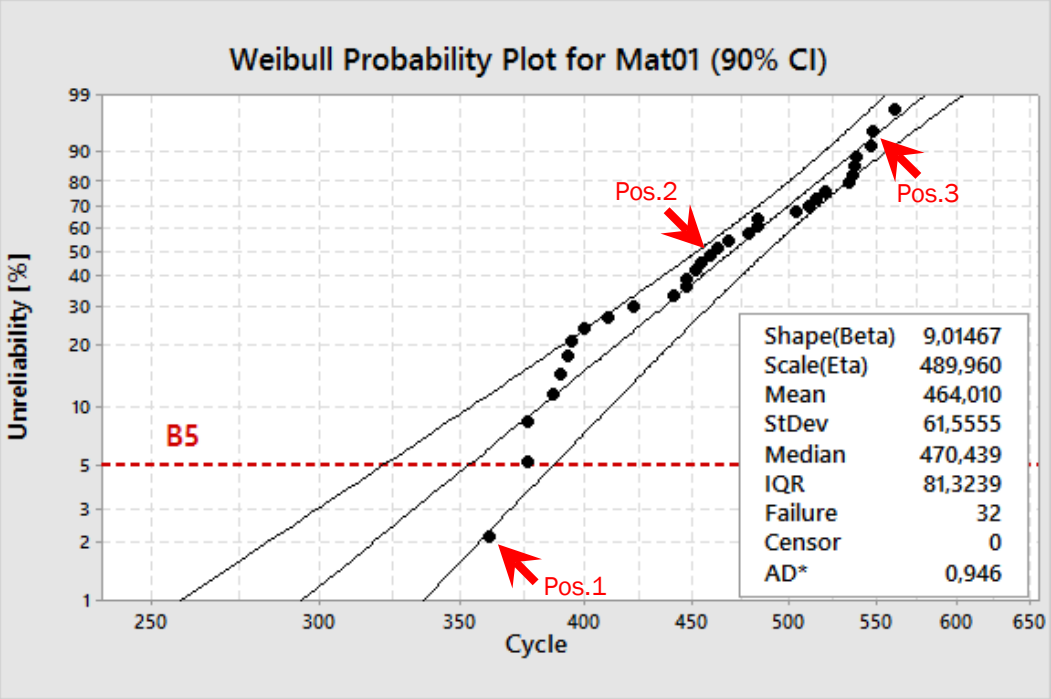
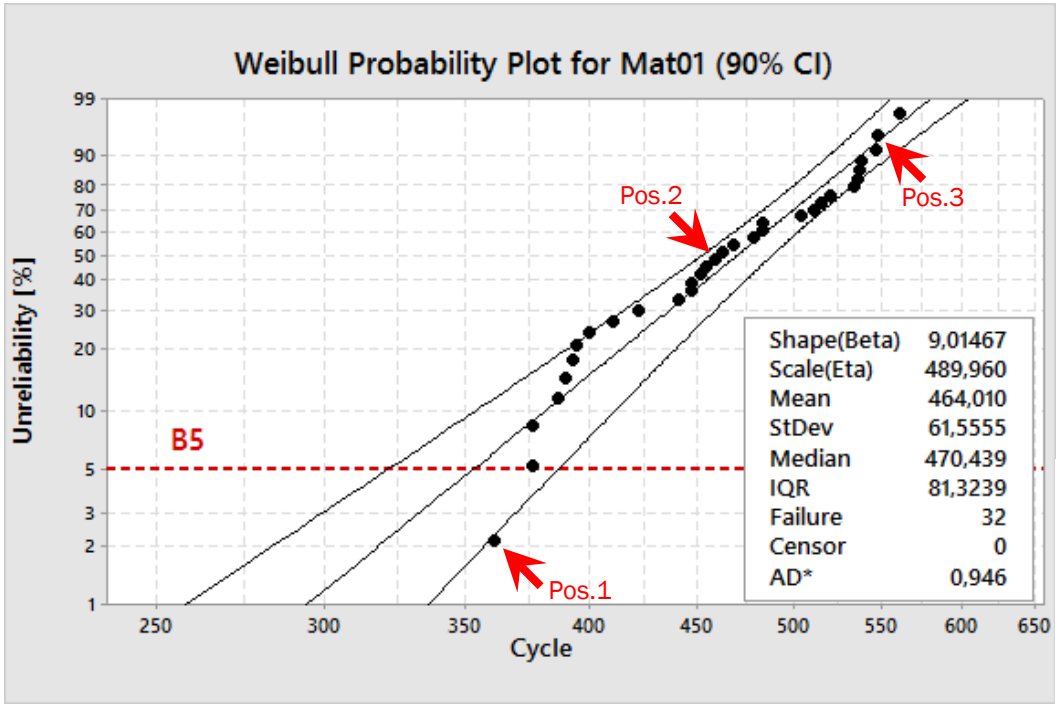
Contents

Experiments – Cross section (Mat01)

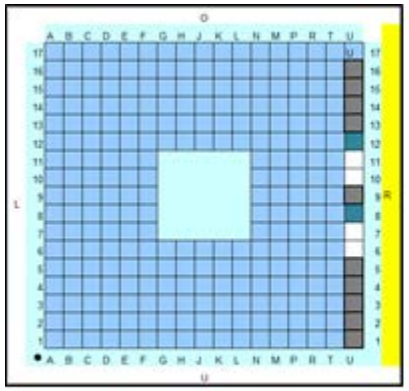


- 3 cross-sections for each group were made, which were taken from the early, median and late failures respectively.
- Most of the cracks occurred on the top side where the chips sit.
- Due to the test-till-fail strategy, the initiation of the cracks cannot be observed.

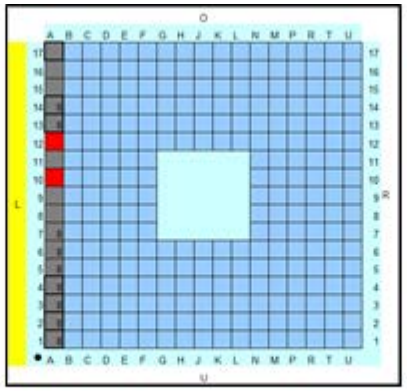
Experiments – Cross section (Mat01)



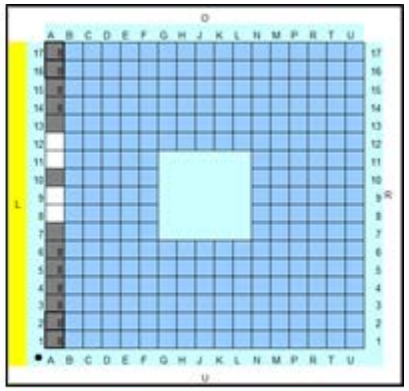
Pos.1



Pos.2



Pos.3



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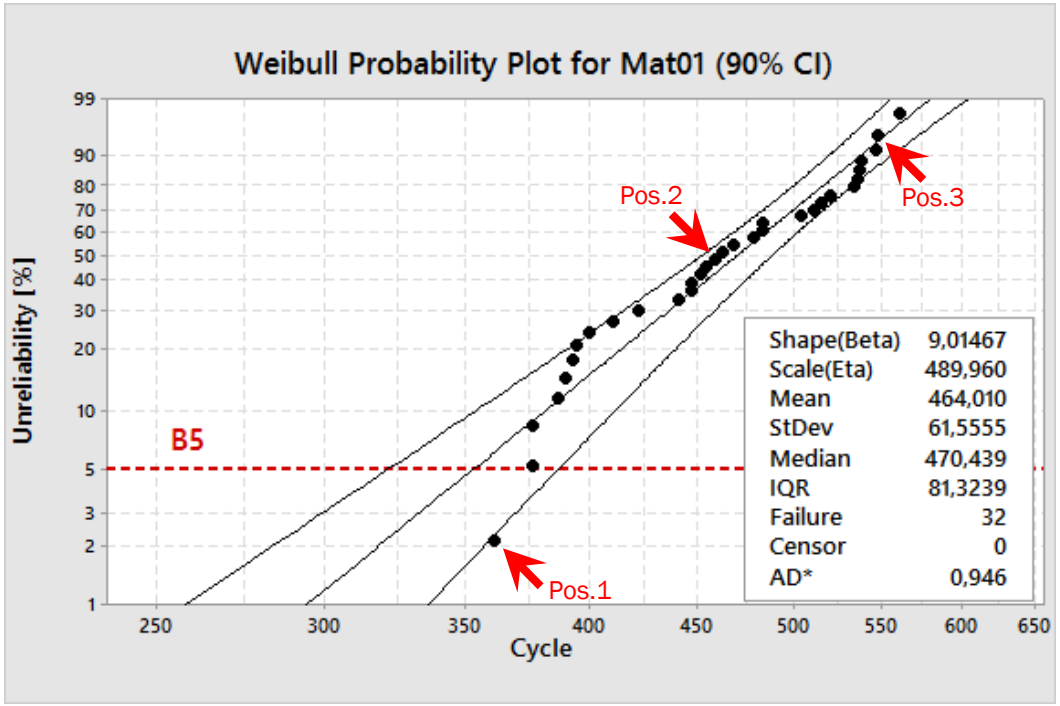

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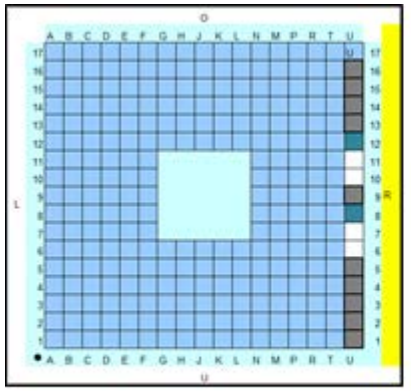
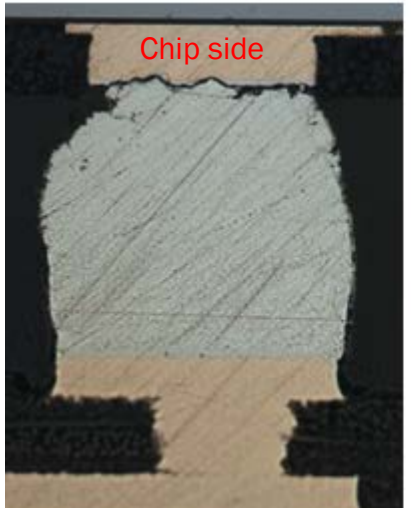
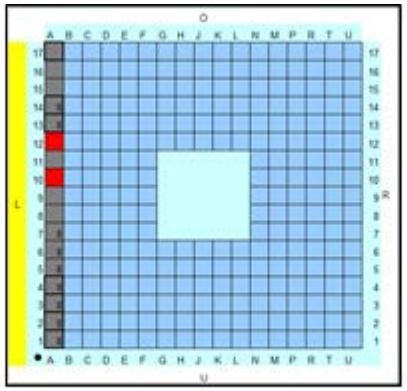
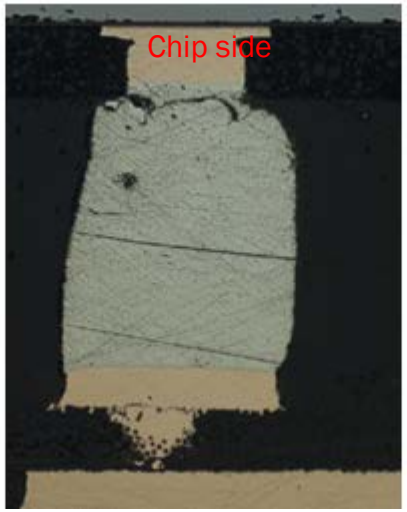


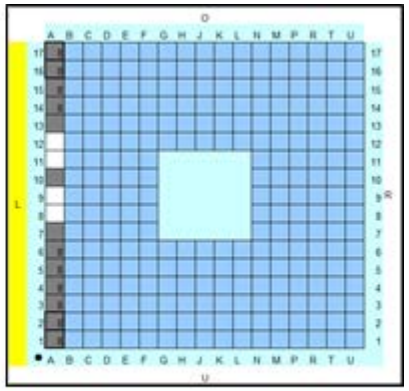


Pos.2





Pos.3



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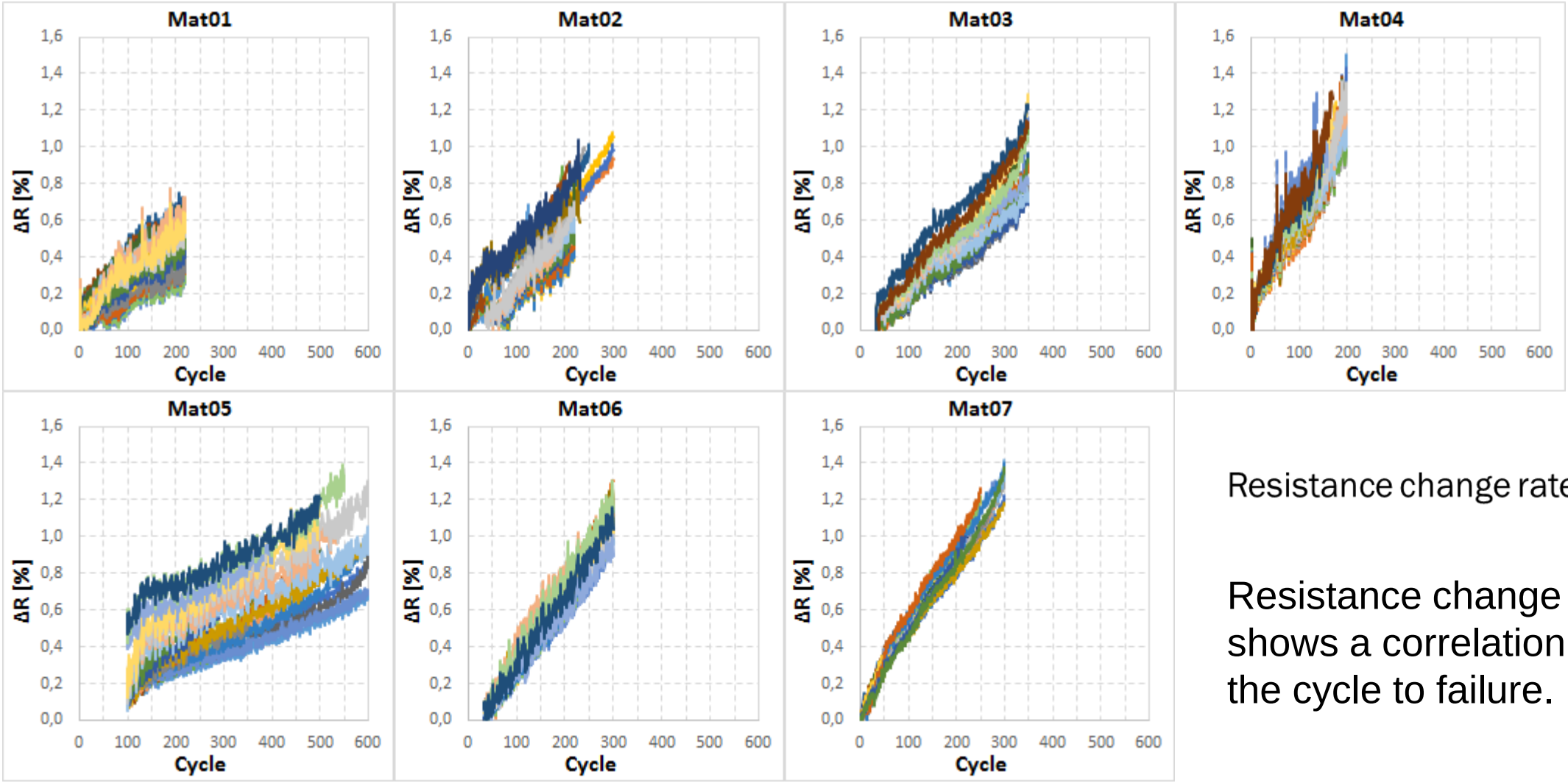
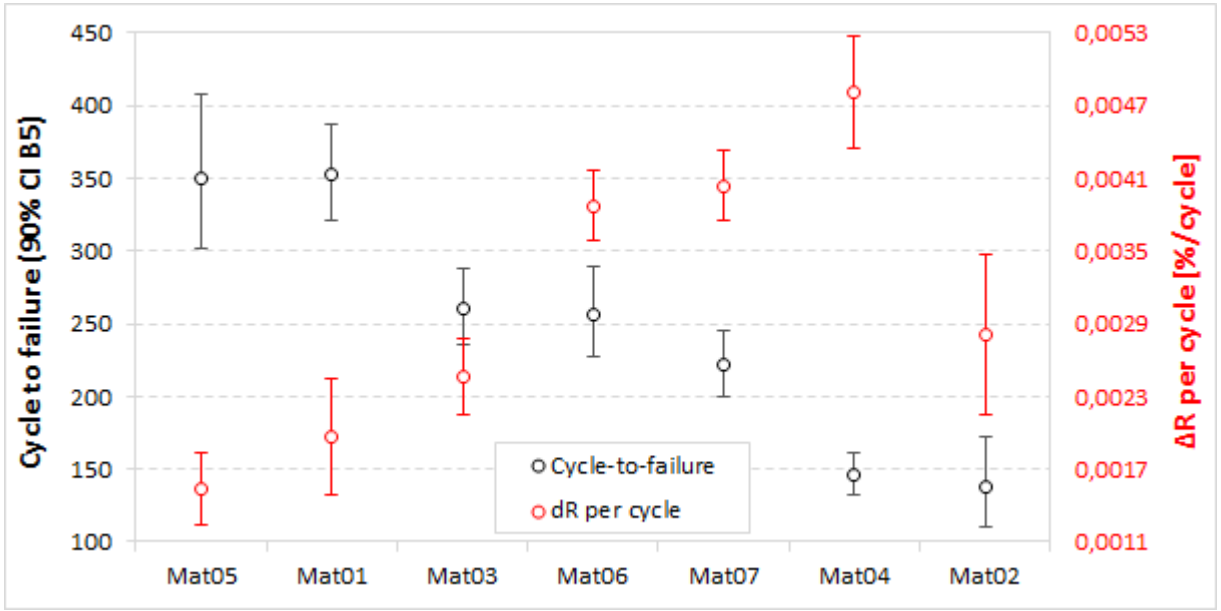
Experiments – Resistance change rate



Resistance change rate: $\frac{d(\Delta R)}{dN}$

Resistance change rate shows a correlation to the cycle to failure.

Experiments – Resistance change rate



- The resistance change rates are calculated based on the slopes of the best-fit lines for the parts, which stands for the stable increase of the resistance.
- Obviously, the correlation between the lifetime and the resistance change rate per cycle is strong.
- The faster the resistance change rates the shorter the lifetime of the solder joints will be.
- It fits for all the groups except Mat02, which has a different failure behavior.

Contents

Simulation – Modelling/BC

- Modelling

PCB:

-- Modelled via production modelling software

-- Real design / thickness

-- Material homogenized (244µm/px)

-- Linear quadrilateral S4R (4-node, reduced integration)

Solder joint:

-- Modelled in a commercial FEA software

-- Real dimension

-- Quadratic hexahedral C3D20R (20-node, reduced integration)

Chip:

-- Modelled in a commercial FEA software

-- A homogeneous plate with real dimension

-- Quadratic hexahedral C3D20R (20-node, reduced integration)

- Boundary Conditions:

BC1:

-- Fixed

-- U1=U2=U3=UR1=UR2=UR3

BC2:

-- Movement along Y and Z are locked

-- U2=U3=0

BC3:

-- Movement along Z is locked

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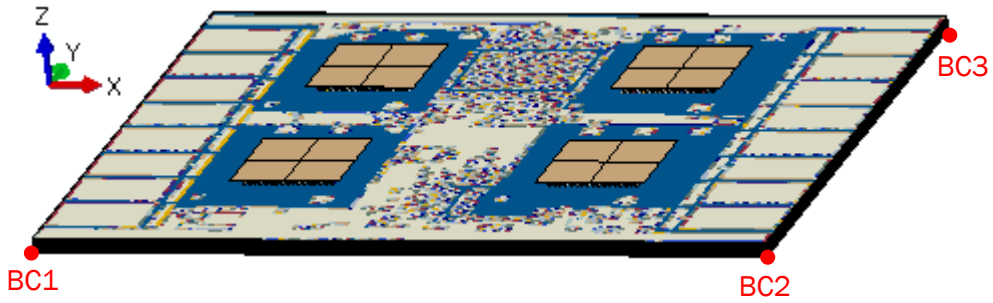

Elements: 432,024 (406,680 S4R + 25,344 C3D20R)

Simulation – Modelling/BC

➢ Modelling

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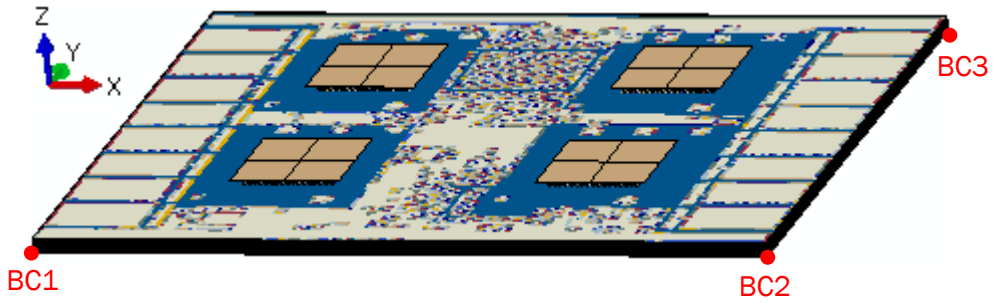

Elements: 432,024 (406,680 S4R + 25,344 C3D20R)

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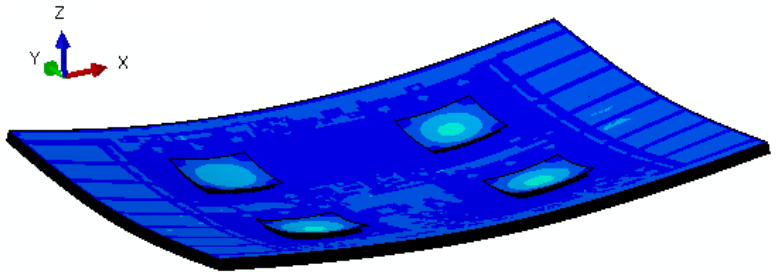
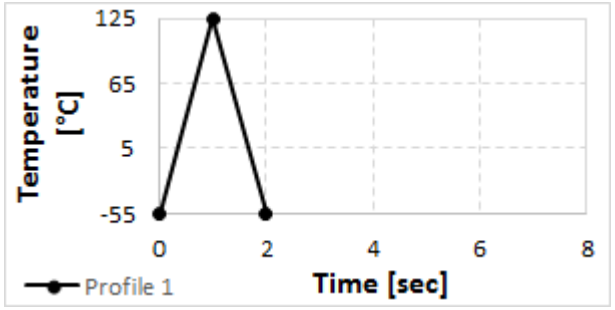
Simulation – Strategy

- Mat02, Mat04 and Mat05 were simulated *
- Three steps included:

  1) PCBA global model





-- Linear procedure
-- Cu/Sn: no cyclic hardening

*: The PCB material properties of the others were not available in the time period of the study.

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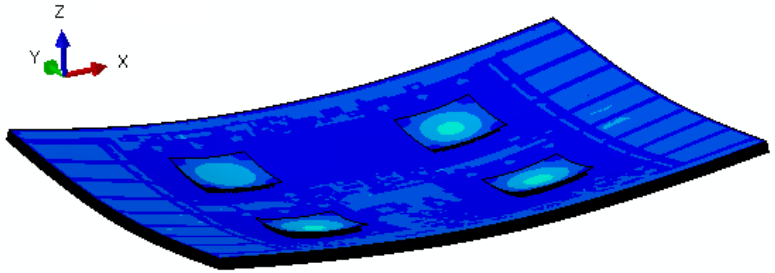

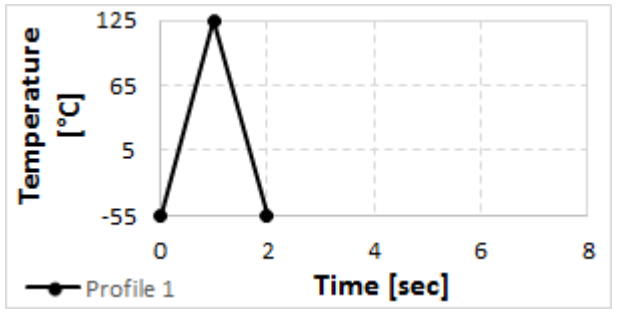

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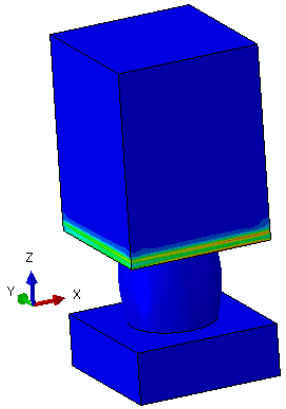
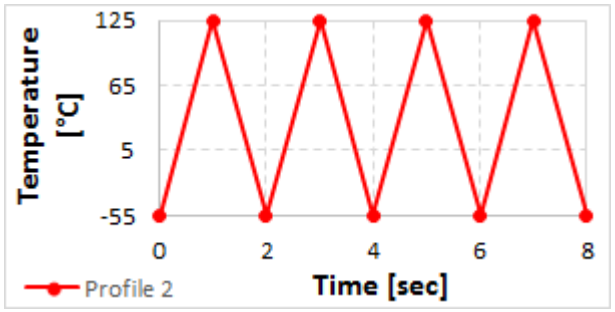
2) Solder joint submodel





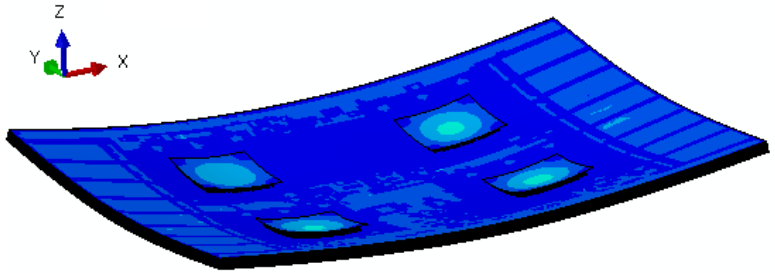
-- Nonlinear procedure
-- Cu/Sn: with cyclic hardening

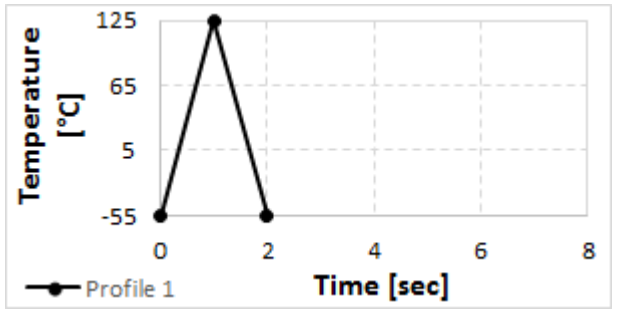
*: The PCB material properties of the others were not available in the time period of the study.

Simulation – Strategy

- Mat02, Mat04 and Mat05 were simulated *
- Three steps included:

1) PCBA global model





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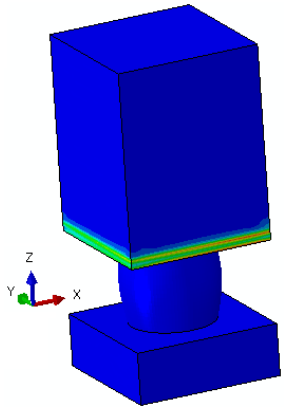

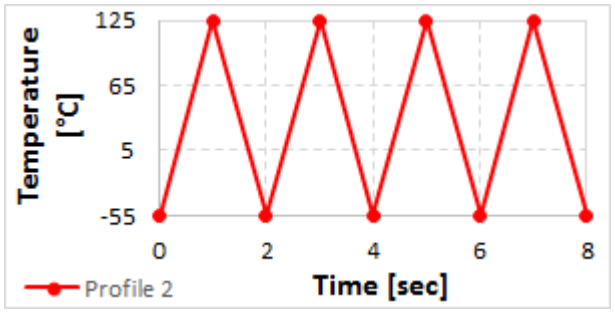

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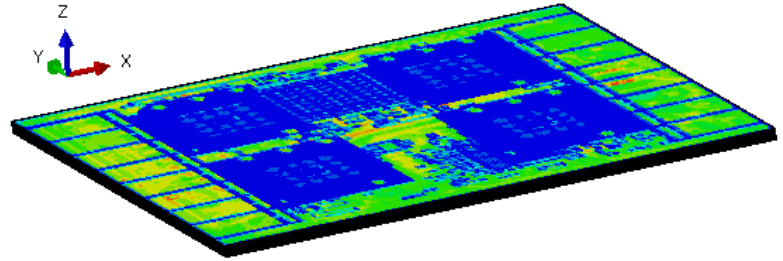
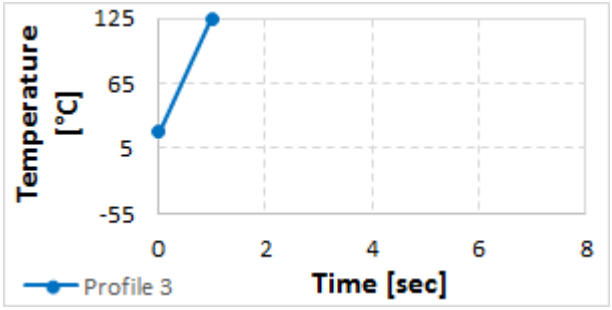
3) PCB global model





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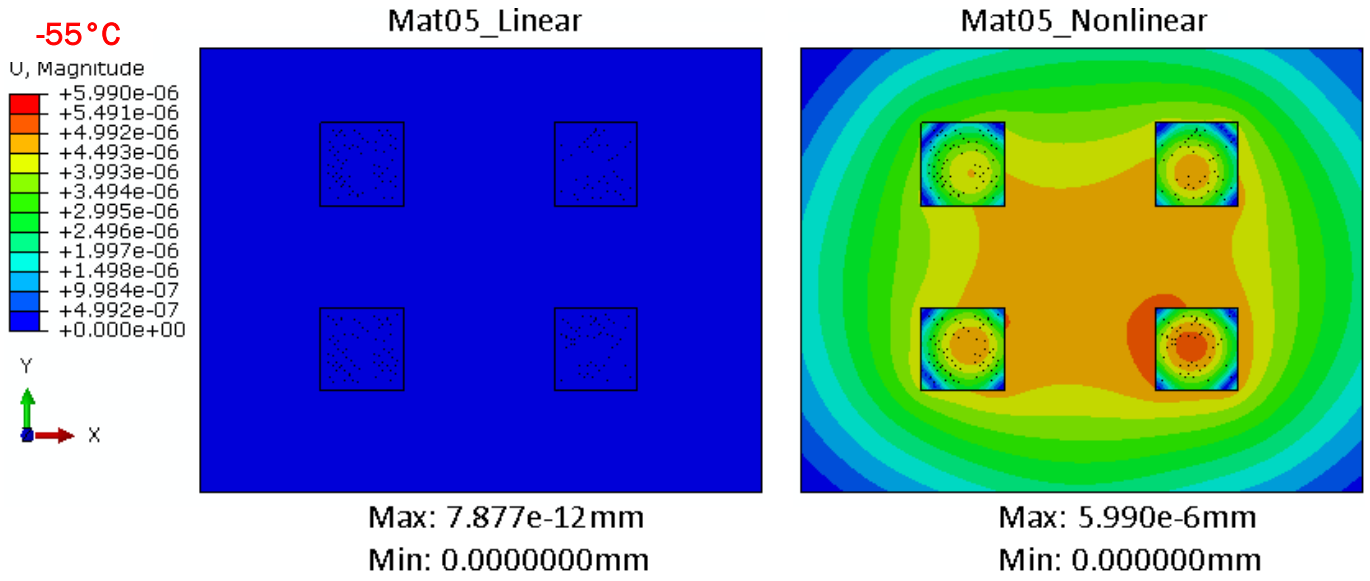
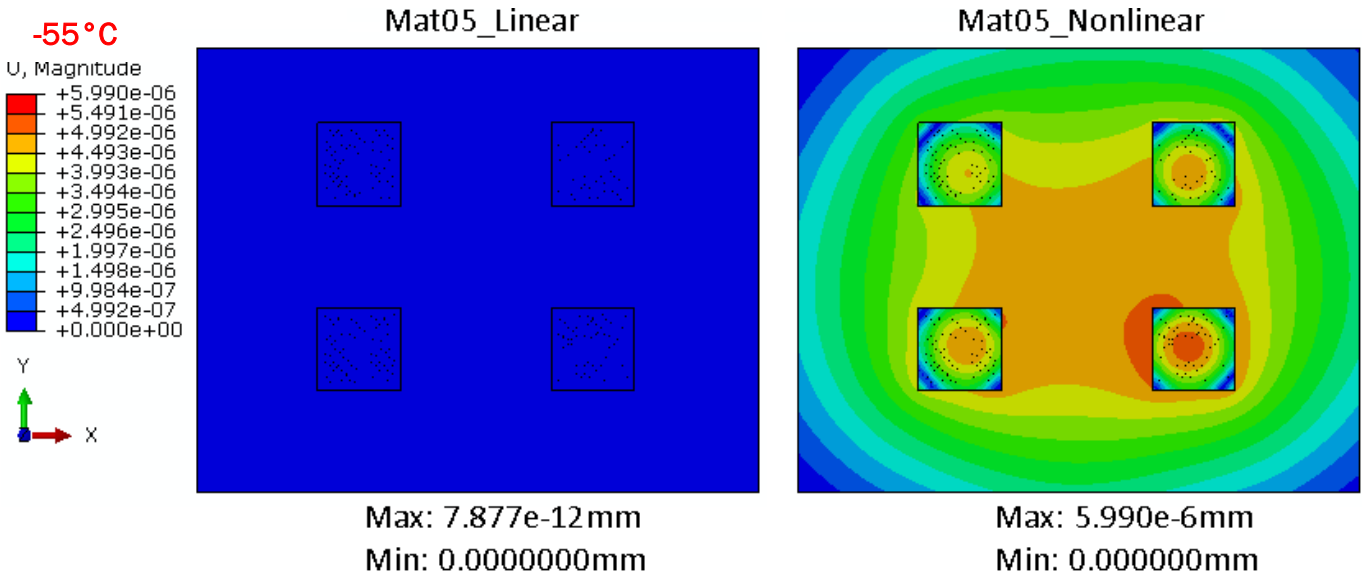
Simulation – Linear/Nonlinear procedure



- With nonlinear procedure, the model cannot return back to its original position (max. displacement: ~0.006μm) after one TST cycle.

Simulation – Linear/Nonlinear procedure



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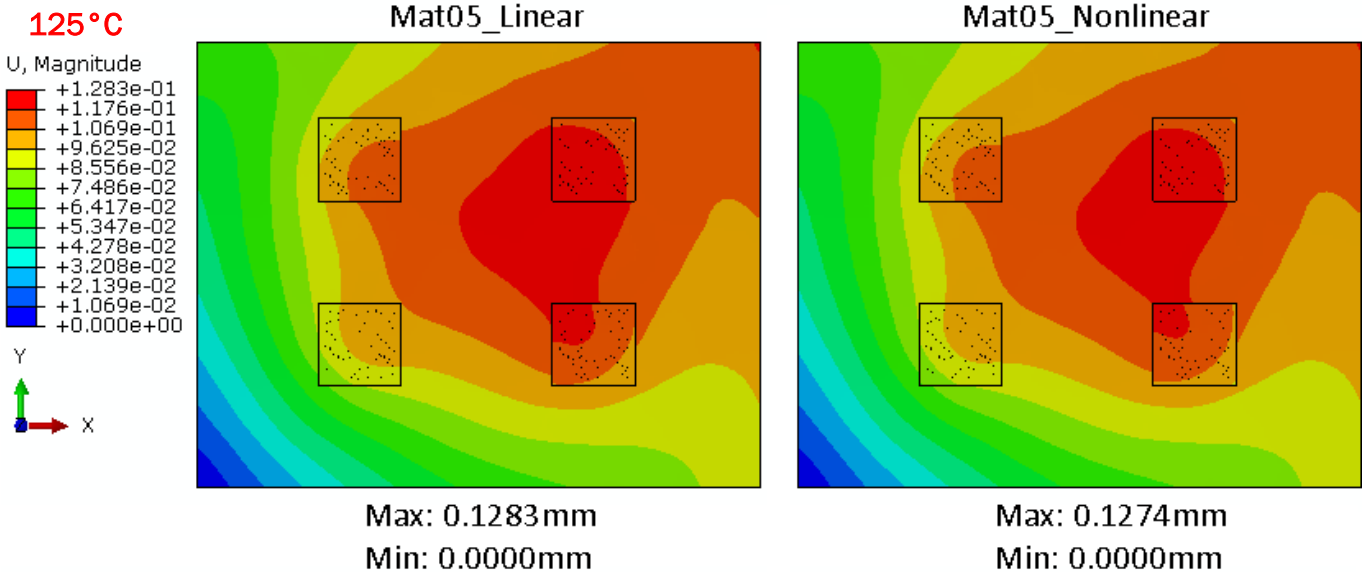
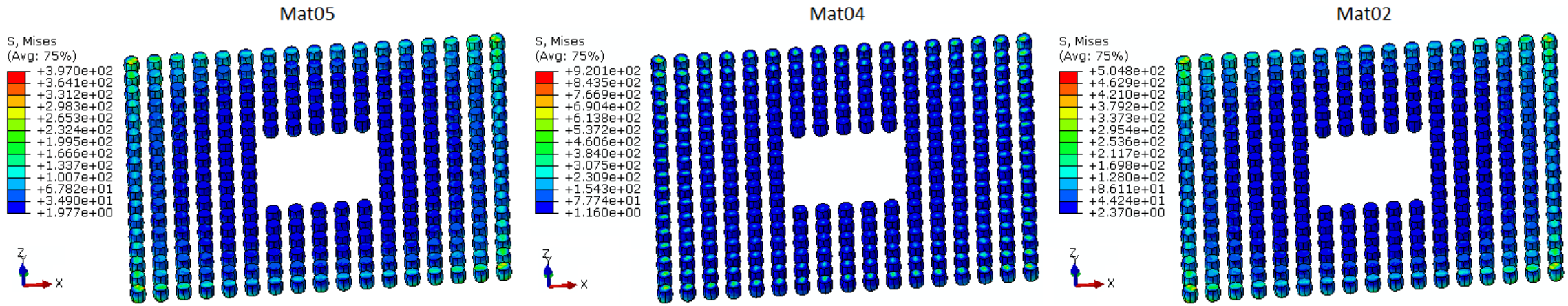


- Both procedures show good similarity of displacement at 125°C in terms of the magnitude and distribution.

Simulation – Results of PCBA global model

- The stress/strain conditions of the solder joints in the four BGA areas are rather similar.
- The stresses in the outermost solder joints are higher than the inner ones, which fit to the experimental findings.
- The solder joints at the lower-right corners are chosen for further investigation by means of submodelling approach.



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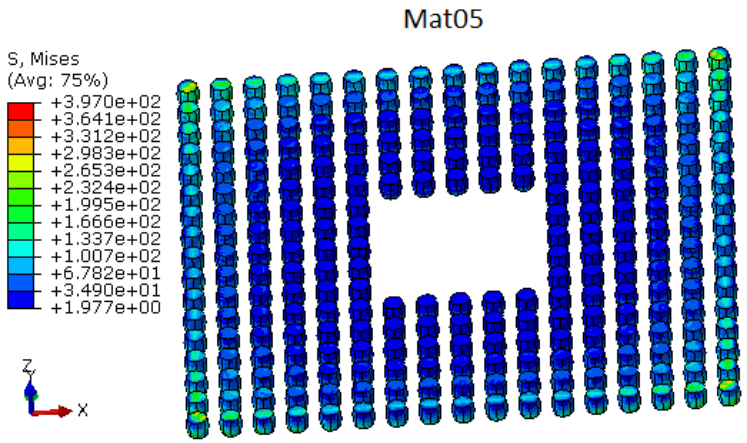

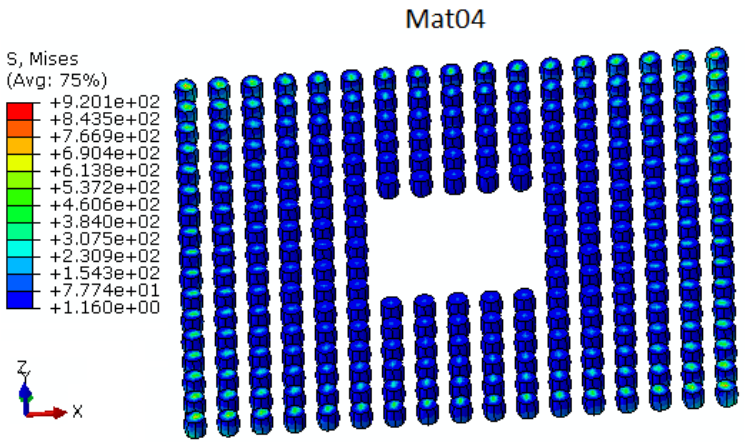

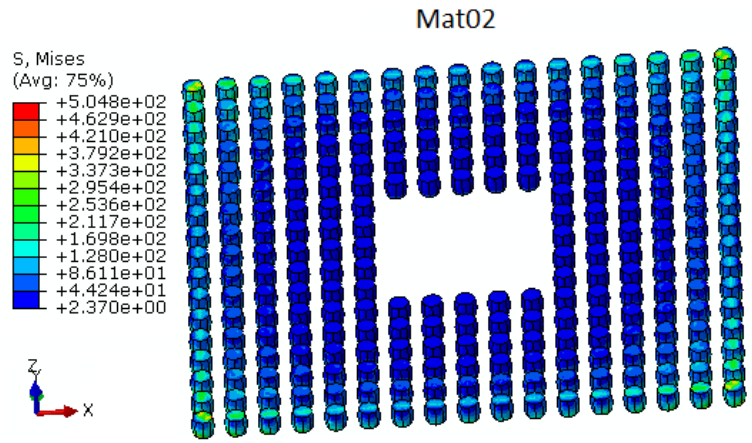

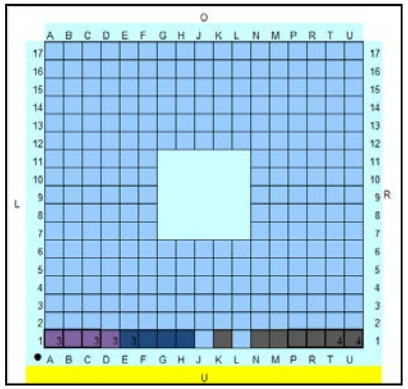

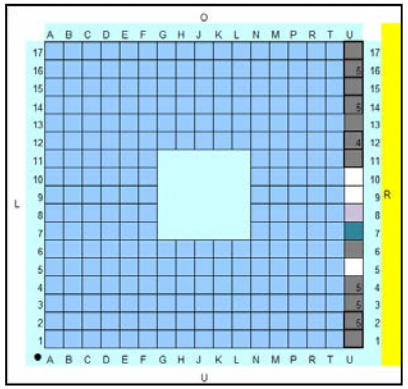

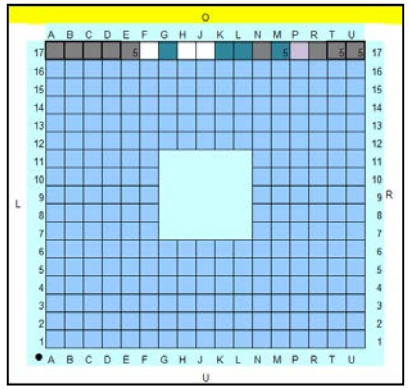

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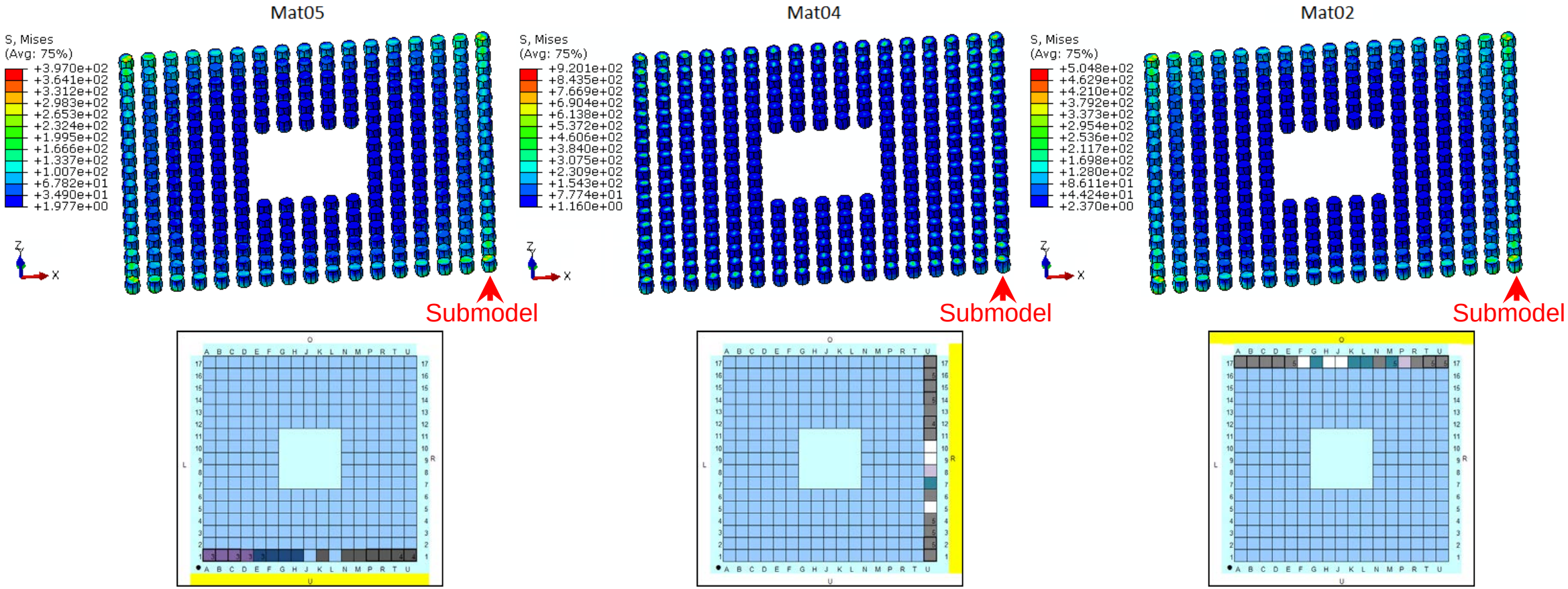
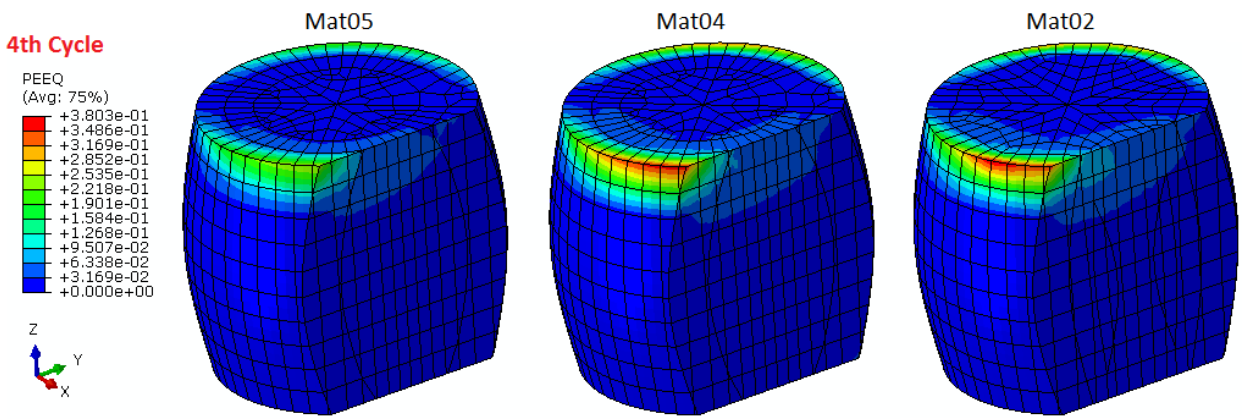
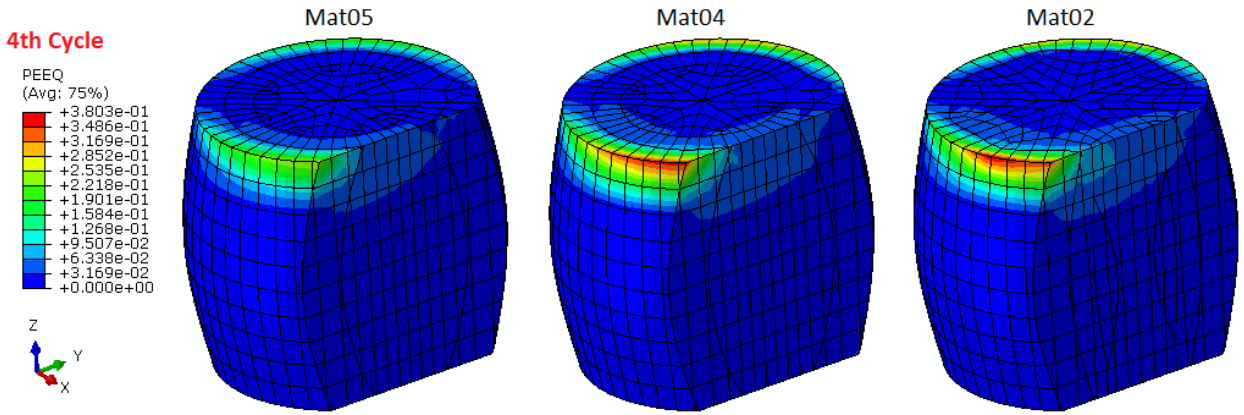


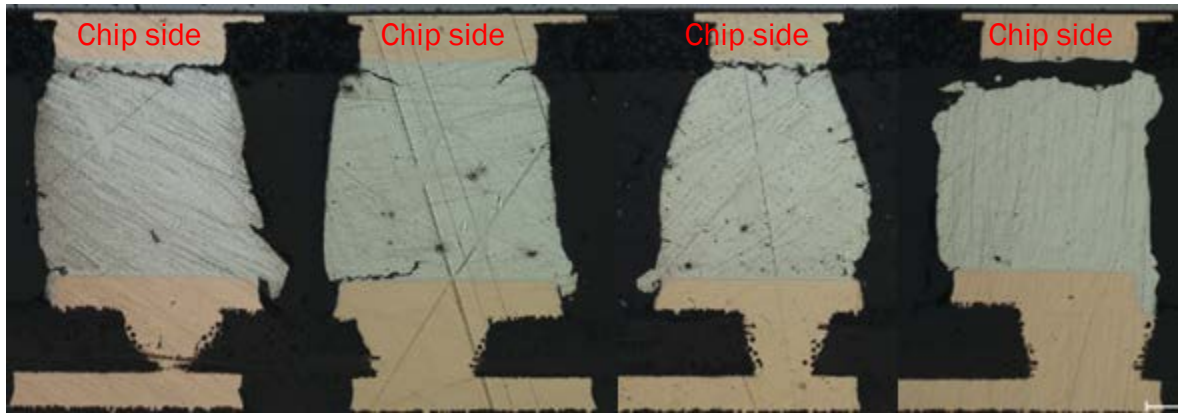
Simulation – Results of solder joint submodel



- The critical areas are always on the top side of the solder joints where the chips sit.
- The simulated results fit the cross-section findings well.
- After the 1st cycle, the increment of the accumulated strain starts to be stable.

Simulation – Results of solder joint submodel





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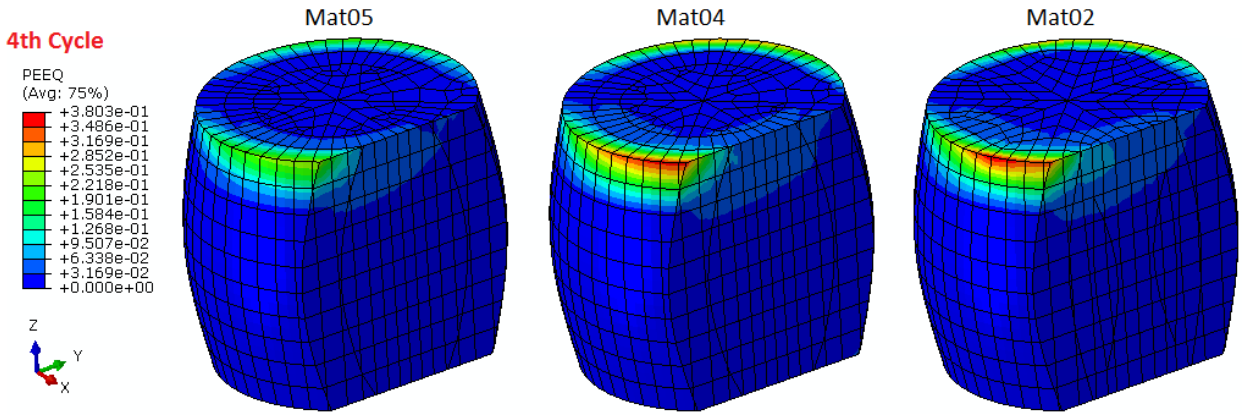

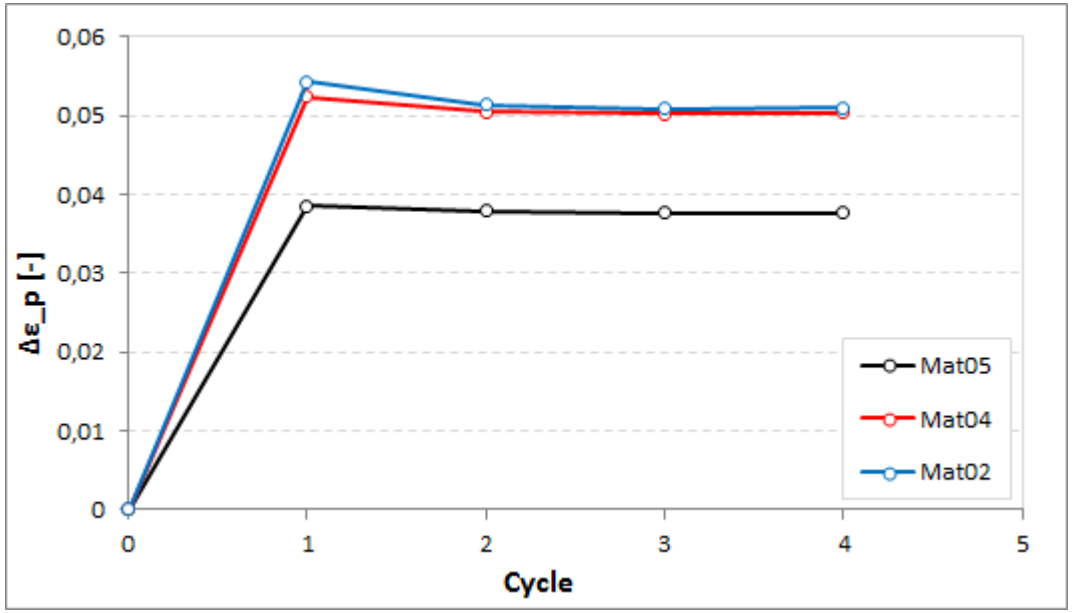

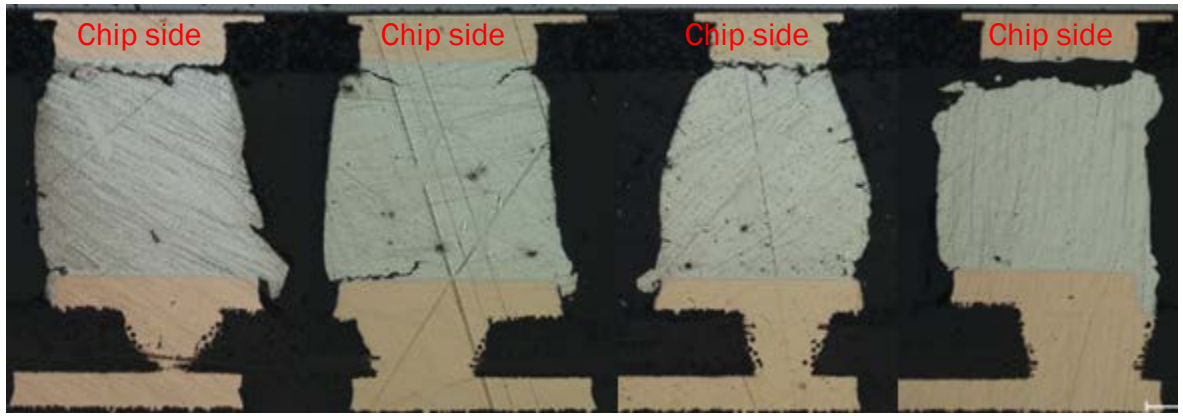

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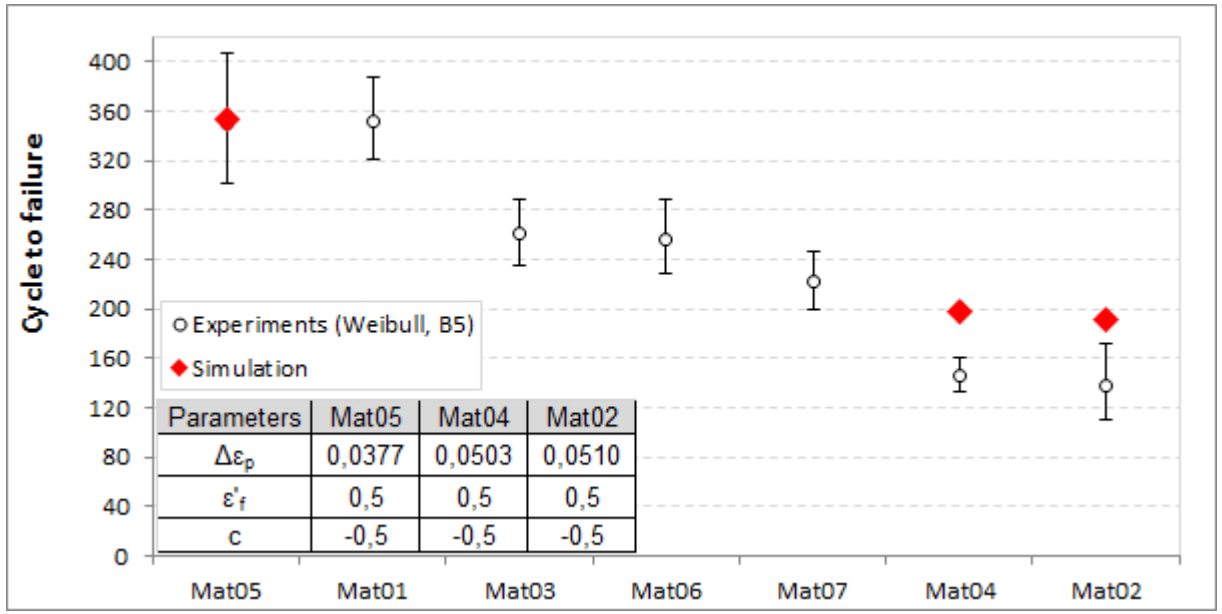
Simulation – Fatigue lifetime prediction



Parameters	Mat05	Mat04	Mat02
$\Delta\varepsilon_p$	0,0377	0,0503	0,0510
ε'_f	0,5	0,5	0,5
c	-0,5	-0,5	-0,5

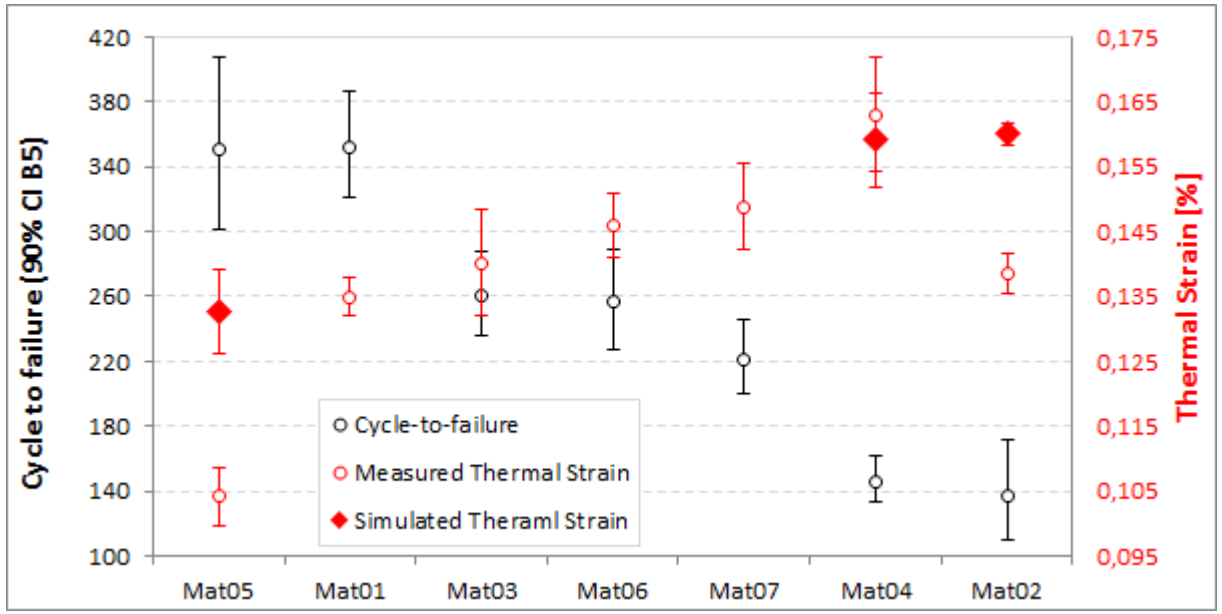
- The predicted lifetimes match the experimental results surprisingly good.
- DO NOT take the predicted absolute values as “true” results, since they strongly depend on the selection of the parameters, which were unknown/not tested for the real applied solder joints.
- The tendency of the predicted lifetimes is more meaningful.

Strain-based Coffin-Manson:

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon'_f(2N)^c$$

Where, $\Delta\varepsilon_p/2$ is the plastic strain amplitude, [-];
ε'_f is fracture strain [-];
N is the number of cycles to failure;
c is an empirical constant ranging from -0.5 to -0.7 for metals.

Simulation – Results of PCB global model

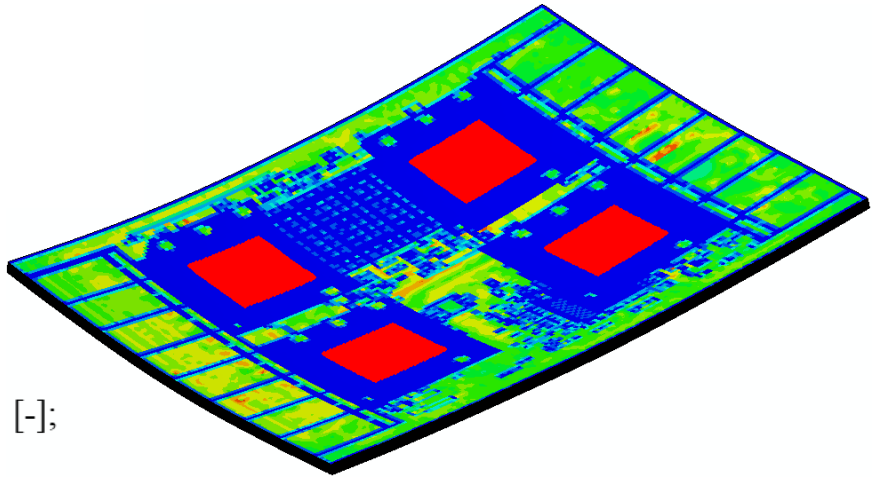


- The max. thermal strains during TST occurred at 125°C.
- One sample was measured for each group using the digital image correlation (DIC) technique.
- Thermal strain shows a good correlation with the lifetime of the PCBA under cyclic thermal loading.

Thermal strain:

$$\varepsilon_{max} = \frac{\sum_{i=1}^{m} \varepsilon_{x,i} + \sum_{i=1}^{m} \varepsilon_{y,i}}{2m}$$

Where, ε_{max} is the maximum thermal strain during TST test, i.e., at 125° C, [-];
$\varepsilon_{x,i}$ and $\varepsilon_{y,i}$ are the thermal strain of node i at 125° C in X and Y directions respectively, [-];
m is the total number of the nodes in the four BGA areas on the top layer of the PCB.



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Conclusion

- Specimen-based PCBA level TST approach
  - 10% resistance change cannot be applied as a criteria in this study
  - 0.5% resistance change rate per cycle is more suitable for the judgement of failures
  - Resistance change rate per cycle can be correlated to the lifetime of PCBA samples
  - An improvement is needed in order to investigate the initiation of the failures
  - Criteria selection for the Weibull analysis regarding different failure modes should be studied further
- FEA-based TST approach
  - PCBA global model (1 cycle) + Solder joint submodel (4 cycles).
  - The outermost solder joints in the BGA areas suffer the highest stresses.
  - The top side (chip side) of the solder joints experienced higher shear forces during TST.
  - Thermal strain at 125°C can be used as an indicator to the lifetime of the PCBA.
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Thank you for your attention!

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