A Study of PCB Insertion Loss Variation in Manufacturing Using a New Low Cost Metrology

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Abstract
Signal integrity analysis has shown that printed circuit board (PCB) insertion loss is a key factor affecting high speed channel performance. Determining and controlling PCB insertion loss have thus become critical production requirements for achieving multi-gigabit per second data rates. The traditional laboratory method of measuring PCB insertion loss is difficult to adopt in high volume manufacturing (HVM) environments because it requires expensive equipment while providing very slow throughput times. In this study we assessed the feasibility of implementing a simpler and lower cost process to measure insertion loss. Through the use of a new metrology developed by Intel engineers, we demonstrated it is capable of quickly and accurately measuring PCB insertion loss and is suitable for use in an HVM environment. Applying this method to a first time study of insertion loss variation in HVM, we measured lot to lot loss variation to be ~±0.05 Decibels (dB)/inch at 4GHz.

Introduction
PCB insertion loss has long been recognized as a critical factor [1] in high speed channel performance. As data rates continue to increase in each generation of Intel's server platforms, determining and controlling insertion loss in PCB production have emerged as requirements for multi-gigabit per second signaling. This new requirement immediately raises the question of how to determine loss compliance in manufacturing. Complicating this issue is the authors' anecdotal observation that PCB fabricators often do not have as good an understanding of the impact of materials, processes and metrology capability on insertion loss as they do on impedance. The traditional laboratory metrology to measure PCB insertion loss is expensive and provides very slow throughput times; thus, an alternative method is necessary for use in HVM PCB environments by PCB suppliers or incoming inspection in board assembly factories.

This study was conducted to establish an alternative lower cost method to determine and track the compliance of insertion loss in an HVM PCB environment. A manufacturing study was constructed to understand the important issue of lot-to-lot variation of insertion loss with respect to the specification tolerance. This, in turn, helped determine how often loss measurements would need to be performed during production, with clear implications for the potential PCB unit cost adder associated with loss testing.

Two products and three PCB suppliers were included in the study. Dedicated coupons were designed and incorporated in the manufacturing panels at the suppliers during PCB fabrication. Insertion loss data was then measured and compiled at an outside testing service. Data from over 800 coupons in 46 different manufacturing lots was collected. From the data gathered, statistical measures of the metrology's capability, PCB construction capability, impedance, PCB insertion loss, lot mean distribution, coupon to coupon variation, and the relationship between loss and frequency and between loss and impedance were developed.

Raw PCB materials used in this study all had "mid loss" characteristics [2] with 0.010-0.015 dielectric loss (Df) at ambient condition. All coupons in this study were pre-conditioned to eliminate moisture before the measurements were taken.

This is the first known experiment conducted to understand the variations of PCB insertion loss in manufacturing. The results from this study have already provided the critical data to guide the decisions on the implementation for PCB insertion loss compliance testing for Intel server products.

Background
Signal attenuation and distortion from dielectric and conductor losses are key factors in proper high speed differential bus simulation and design. PCB insertion loss is a measure of how much the signal is attenuated when

going through the PCB. Insertion loss is expressed in units of dB's and is given by the expression -20 $\log_{10}|S21|$, where S21 is the transmission coefficient. For differential signals, it is also commonly referred to as SDD21.

PCB insertion loss increases approximately exponentially with trace length and data transfer frequency [3]. As the data rate approaches ~10 gigabits per second on traces with routing lengths often greater than 12 inches in today's typical server platforms, the amount of insertion loss has become a critical performance attribute and is now specified in server platform design guidelines. A unique new specification for SDD21 has been established for each of Intel's server platforms.

This new requirement for limiting PCB insertion loss raises the question of how to determine compliance in manufacturing. Today, many PCB fabricators do not have a well developed comprehension of PCB insertion loss with respect to the metrology, materials, and process. Furthermore, they lack the resources and expertise in implementing insertion loss compliance with associated measurement metrology. The traditional method of measuring differential insertion loss is performed using a 4-port Vector Network Analyzer (VNA). This requires expensive equipment investment, precise calibration, and operation by highly skilled technicians. Also, in practice, it produces low throughput for loss measurements. As a result, this traditional laboratory method of insertion loss measurement is considered inappropriate for use in PCB HVM environments.

A novel method to derive SDD21 using only single-ended Time Domain Reflectometry / Transmissometry (TDR/TDT) measurements at a single probe location was developed by two Intel engineers. This method uses inexpensive 2-port TDR/TDT equipment and Intel-developed software. It is referred to as Single-Ended Time domain To Differential Insertion Loss (SET2DIL). However, a Gauge Repeatability and Reproducibility (R&R) study [4] is required to establish that this metrology is capable as a measurement standard before it can be adopted in practice.

For insertion loss compliance implementation in an HVM PCB environment, the primary issue of lot-to-lot variation of insertion loss should be determined. This would, in turn, determine where and how loss measurements should be performed, as well as the likely PCB unit cost adder. We decided to conduct a manufacturing study to collect data so that a decision could be made for the compliance implementation.

SET2DIL Measurement Method

The SET2DIL test method was developed as a low cost alternative to the more traditional approach of using a 4-port VNA for PCB insertion loss measurement [5]. To facilitate acceptance by PCB manufacturers, the SET2DIL test method employs familiar TDR/TDT test equipment and a test coupon design that is comparable to that of a standard impedance test coupon and is illustrated in Figure 1. The SET2DIL test method is intended to provide a means for rapid pass/fail grading of PCB constructions.

Figure 1. SET2DIL coupon design.

The SET2DIL method achieves the reduction to a simpler 2-port measurement by exploiting the symmetry present in a differential PCB trace pair test structure. With the four ports and signal directions of a differential line structure as shown in Figure 2, differential insertion loss, SDD21, shown in (1) below, is defined [6] by the individual output port frequency domain measurements S21, S23, S41, and S43 as follows:

$$SDD21 = \frac{1}{2}\left(S21 - S23 - S41 + S43\right) \qquad (1)$$

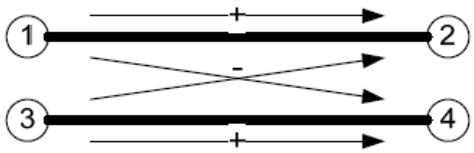

Figure 2. SDD21 parameters.

Since the test structure is a simple symmetric differential pair, we expect manufacturing variation between the two traces to be small, which yields S21≈S43 and S23≈S41, and thus (1) can be rewritten as in (2) below.

$$SDD21 \approx S21 - S41 \qquad (2)$$

Equivalently, we can arrive at SDD21 through a difference of TDT measurements on ports 2 and 4 with an excitation applied at port 1 as shown in (3),

$$TDD21 \approx T21 - T41 \qquad (3)$$

This is followed by the standard application of a Fourier transform to arrive at (2) above.

In the SET2DIL method, one further measurement convenience is developed: horizontal symmetry allows folding, that is, port 2 and port 4 can be connected together so that measurements are made just on one end of the structure, i.e., at ports 1 and 3. In this case, a TDR measurement is made on port 1 while a TDT measurement is made on port 3. The resultant waveforms measured at ports 1 and 3 will yield the equivalent of T21 and T41 through the SET2DIL algorithm's removal of the TDR voltage offset and near end crosstalk signals on ports 1 and 3, respectively. Folding in this fashion allows the test structure to be one half as long as the original test trace. This helps minimize the board area required for the coupon.

In this study, a SET2DIL measurement was made on each four inch long differential trace pair structure, with their far ends connected together as described above, as follows:

1) The TDR was set for 4000 points of acquisition at 1.25ps sampling intervals yielding a 5ns data capture window.
2) TDR/TDT averaging was set for 512 sweeps.
3) Port 3 data was acquired once on a "thru" structure to establish the input waveform used for calibration.
4) The SET2DIL test structure measurements were then performed by acquiring port 1 TDR and port 3 TDT data.

The measurement setup used in this study is shown in Figure 3.

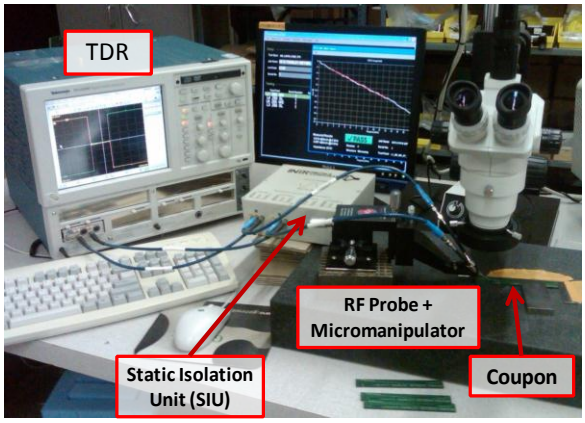

Figure 3. SET2DIL measurement setup (courtesy of Introbotix).

The data files were processed using the SET2DIL algorithm as described above and in [2]. Multiple test line structures on the coupons were then measured by repeating step 4. The values of SDD21 at 4GHz and 8GHz were used for all of this study's statistical data analyses.

Design of Experiment

For this study two production boards were selected, both having an 8-layer stack-up. One board was 0.062 inches thick and is referred to as Product 1. The other one was 0.093 inches in thickness and is referred to as Product 2.

Three different PCB suppliers produced the two products and a unique raw material was used for each board-supplier combination. The board, PCB supplier and material combinations are summarized in Table 1 below.

Table 1. Board-Supplier-Material Matrix.

	Product 1	**Product 2**
Supplier 1	Material 1	Material 2
Supplier 2	Material 3	None
Supplier 3	None	Material 4

A SET2DIL coupon with 85Ω differential pair test traces on each of the four signal layers was designed with dimensions of 0.6 x 4.7 inches to mimic a typical TDR impedance coupon's design width, while maintaining HVM panel spacing requirements. The SET2DIL coupon modifies the ubiquitous impedance coupon's test traces by adding a thin loopback trace at the end of each differential pair. The SET2DIL test trace also was used as the impedance test structure for the 85Ω traces. A Gerber file of the coupon design was created and sent to PCB suppliers for inclusion on their manufacturing panels. If line width compensation was required on the 85Ω traces to meet the impedance specification on the actual board, the suppliers were further instructed to do the same on the coupon. At the end of the PCB manufacturing process, suppliers separated the SET2DIL coupon from the working panel. Each supplier shipped at least 15 coupons from each manufacturing lot to an outside testing service for the PCB insertion loss measurements. Each coupon represented an individual manufacturing panel and the set of 15 were vacuum packaged with desiccant in the bag during shipment.

Coupons were baked at 105 – 120 ^{o}C for six hours to remove moisture followed by a 30-60 minutes ramp down to ambient temperature before measurements were taken. Insertion loss data were collected from over 800 coupons in 46 different lots for this study. In addition, gauge R&R studies were performed on 30 coupons prior to the data collection. Separate gauge studies were performed for impedance and insertion loss of all layers. These studies were conducted across multiple days, operators, and time of day.

Results

Analyses were completed and summarized below.

5.1. Metrology Capability

To determine measurement accuracy at the testing service, six coupons were measured first at Intel using a VNA. The coupons were then measured again at the testing service and found to agree to within 0.013dB/in at 4GHz, or approximately 4% of the tolerance range. The remainder of the results of the Gauge R&R study demonstrated that the SET2DIL metrology is capable of measuring PCB insertion loss by having a Precision / Tolerance (P/T) ratio of less than 10% [4]. Details are summarized in Table 2 below.

Table 2. Metrology Capability.

Insertion Loss Measurement	**Repeatability (dB/in)**	**Precision (P) (dB/in)**	**P/T Ratio**	**P/6σ within lot**
Outer layers 4 GHz	.00699	.0220	8.78% T=.25	21.2% 6σ=.102
Inner layers 4 GHz	.00681	.0240	8.27% T=.29	26.5% 6σ=.0904
Outer layers 8 GHz	.00139	.0353	7.05% T=.50	18.1% 6σ=.194
Inner layers 8 GHz	.00139	.0371	6.29% T=.58	24.1% 6σ=.154

5.2. PCB Construction Capability

For the purpose of this study, PCB construction was defined as a unique combination of stack-up, raw materials, fabrication process, and specific PCB supplier factory. There were four different PCB constructions in this study. Each product has two different PCB constructions as shown in Table 1. The insertion loss measurements for

Product 1 are plotted in Figures 4 and 5 below. For convenience the passing specification range is normalized to ±0.5 since the inner and outer layers have different loss specifications. Supplier 1's PCB construction met the loss requirement while Supplier 2's did not meet. Raw materials selected by the suppliers were believed to be the key factors in whether they met the PCB insertion loss specification.

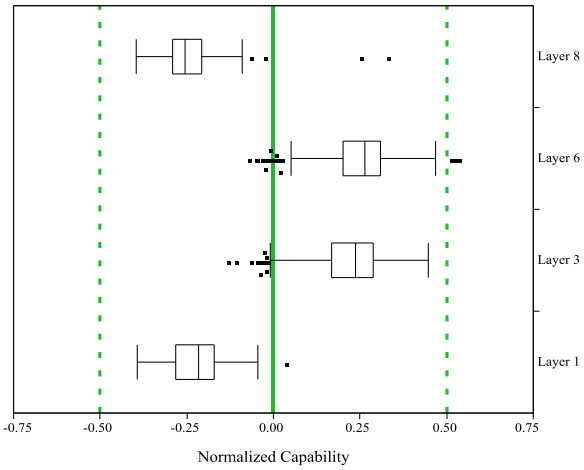

Figure 4. PCB construction capability by Supplier 1 on Product 1.

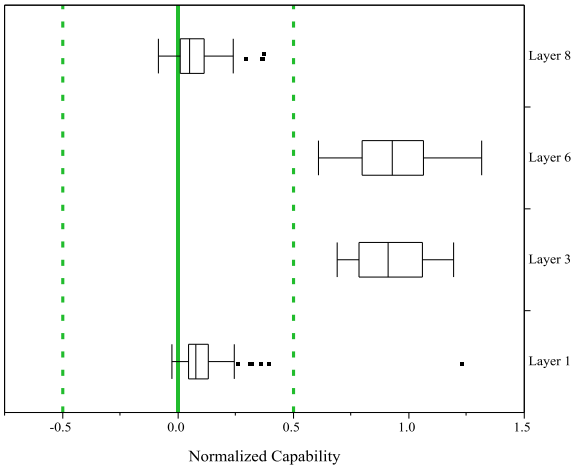

Figure 5. PCB construction capability by Supplier 2 on Product 1.

5.3. Impedance

Impedance measurements on layer 1 of product 1 from two different PCB supplier constructions are shown in Figure 6 below. They met the specification of 85Ω +/- 17.5%. Other signal layers of the same PCB construction also met specifications. Impedance measurements on all signal layers of the other three PCB constructions also met specifications. The results were as expected and matched the historical impedance data.

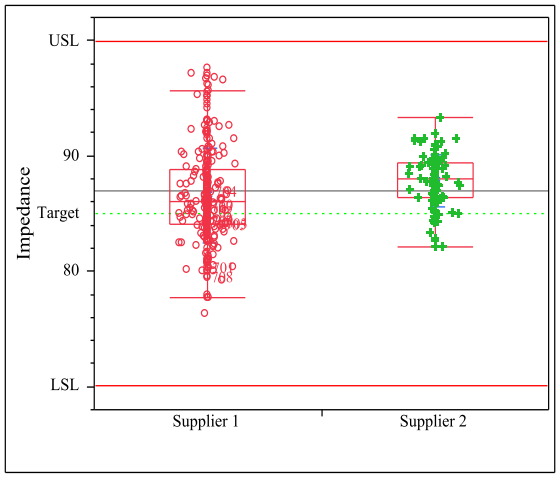

Figure 6. Impedance measurements for layer 1 of Product 1.

5.4. PCB Insertion Loss

PCB insertion loss measurements at 4GHz of Product 1 from two different PCB supplier constructions on four signal layers are shown in Figure 7 below. As expected, they did not match since the fabricators used materials with different loss characteristics. However, for a given PCB construction, the two outer layers performed similarly as did a pair of inner layers. The same trends were observed when Product 2 data were plotted. We also collected insertion loss data at 8GHz on both Product 1 and 2 and the same results were seen. In addition, about ±0.05 dB/inch variation in insertion loss for all four signal layers was observed from lot-to-lot of the same product. In comparison with the impedance results of the previous section, the lot-to-lot variation of insertion loss with respect to the tolerance range is significantly smaller.

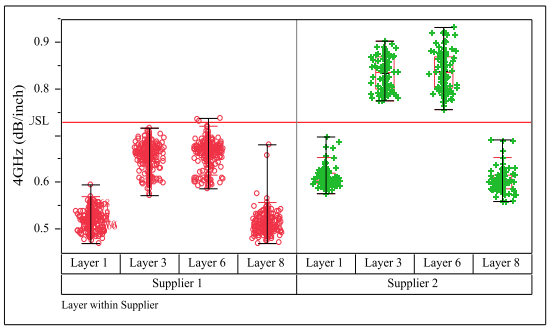

Figure 7. PCB insertion loss for Product 1 at 4 GHz.

5.5. Lot Mean Distribution

PCB insertion loss measurements of Product 1 by PCB Supplier 1 construction on one outer layer (layer 1) and one inner layer (layer 3) at 4GHz are shown in Figures 8 and 9 below. The data demonstrated insertion loss was stable. About ±0.05 dB/inch variations in PCB insertion loss was observed from lot-to-lot of the same construction. With respect to their specifications' tolerance ranges, lot to lot loss variation was found to occupy a smaller fraction of the range, or ~40%, versus nearly 80% for impedance. The same results held true when data from the other three signal layers (layer 3, 6 and 8) were plotted for Product 1 and Product 2. We also collected data at 8GHz on both Product 1 and 2 and they show the same results.

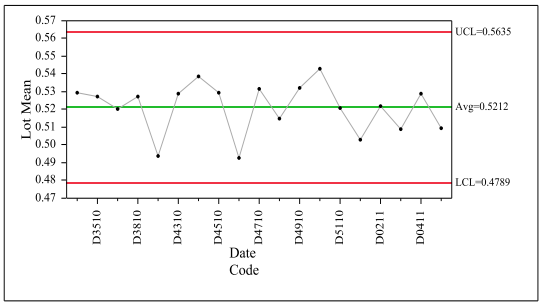

Figure 8. Insertion loss lot mean distribution of Product 1 on layer 1 at 4GHz.

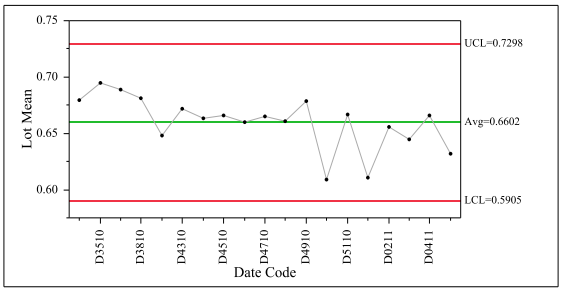

Figure 9. Insertion loss lot mean distribution for Product 1 on layer 3 at 4GHz.

5.6. Coupon to Coupon Variation

Coupon to coupon variations of PCB insertion loss measurements at 4GHz within the same manufacturing lot of Product 1 from two different PCB supplier constructions are shown in Figure 10 below. The insertion loss variation within the lot remained consistent. The same trends were true when data from Product 2 were plotted. The data at 8GHz for both Product 1 and 2 were also collected and the same results observed.

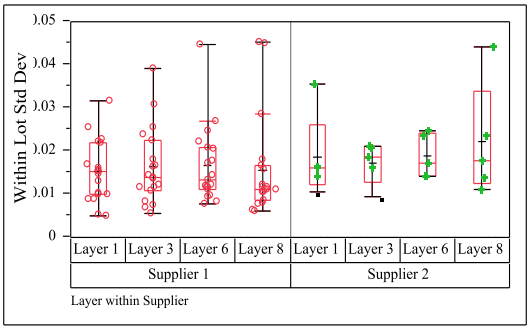

Figure 10. Coupon to coupon loss variation at 4 GHz on Product 1.

5.7. Loss Relationship between Frequencies

PCB insertion loss measurements at 4GHz and 8 GHz of Product 1 from two different PCB supplier constructions on one outer layer (layer 1) and one inner layer (layer 3) are shown in Figures 11 and 12. The relationship between them is consistent and it is true for other layers when plotted. The data from Product 2 are shown in Figures 13 and 14 below. The loss relationship between 4GHz and 8 GHz on layer 3 is consistent but that on layer 1 is not. The inconsistent relationship existed for the other outer layer (layer 8) when plotted. As a result, we need to measure for compliance of insertion loss at both frequencies.

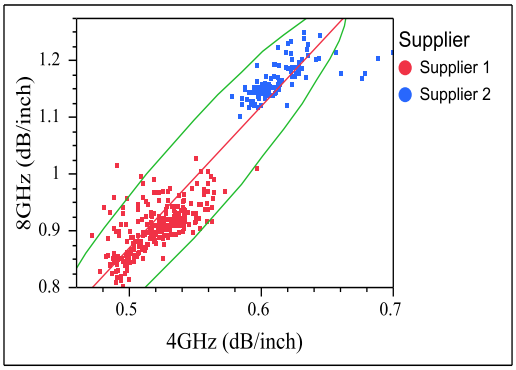

Figure 11. PCB insertion loss relationship between 4 GHz and 8 GHz on layer 1 of Product 1.

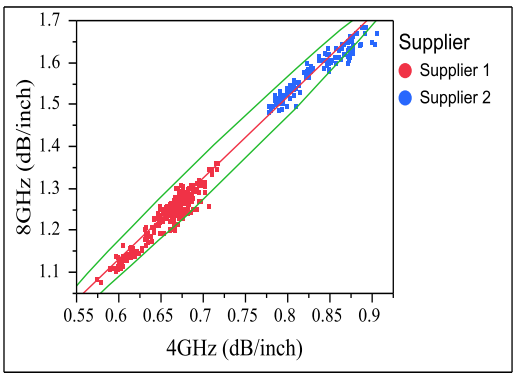

Figure 12. PCB insertion loss relationship between 4 GHz and 8 GHz on layer 3 of Product 1.

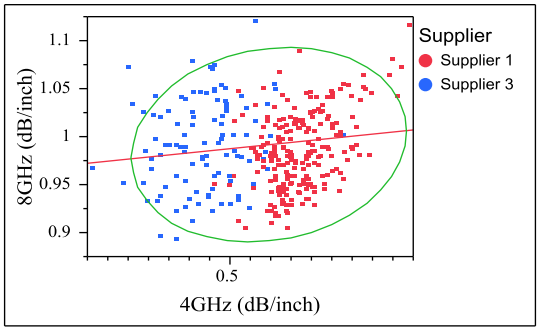

Figure 13. PCB insertion loss relationship between 4 GHz and 8 GHz on layer 1 of Product 2.

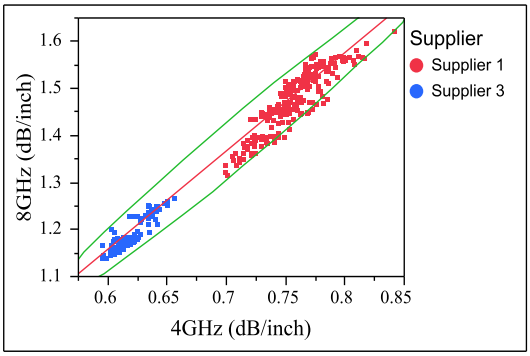

Figure 14. PCB insertion loss relationship between 4 GHz and 8 GHz on layer 3 of Product 2.

5.8. Impedance and Insertion Loss Relationship

Impedance and insertion loss relationship of Product 1 on one outer layer (layer 1) and Product 2 on one inner layer (layer 3) at 4GHz are shown in Figures 15 and 16 below. No consistent relationship can be found, nor is expected, between them. The same results held true when 4GHz data from the other layers of Products 1 and 2 were plotted. We also collected data at 8GHz on both Product 1 and 2 and no consistent relationship between impedance and insertion loss across products and layers existed.

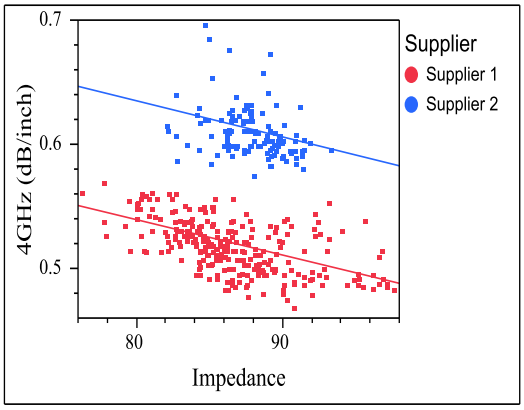

Figure 15. Impedance and insertion loss relationship of Product 1 layer 1 at 4GHz.

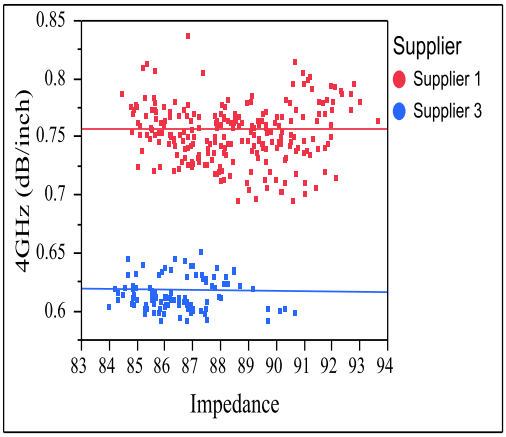

Figure 16. Impedance and insertion loss relationship of Product 2 layer 3 at 4GHz.

Conclusions

The following conclusions can be made from the experimental results:

1) The lower cost SET2DIL metrology is capable of measuring PCB insertion loss and can be used to monitor compliance in HVM PCB environments. Its P/T ratio was less than 10% in the Gauge R&R study.
2) Some PCB constructions met the PCB insertion loss requirements whereas others did not, even though all met impedance specifications. Raw material type was a key factor in determining the acceptance of a PCB construction. The number of acceptable raw materials was reduced due to insertion loss requirements.
3) About ±0.05 dB/inch variations in PCB insertion loss was observed from lot-to-lot of the same board. It was significantly less than that of impedance ranging ±10 to 15Ω. As a result, lot-to-lot compliance checking is not necessary in HVM PCB environments. Although it is not mandatory for PCB suppliers to measure loss on a lot-to-lot basis, it is recommended for them to implement a loss metrology in order to understand material and process interaction for future new boards.
4) A PCB insertion loss compliance determination should be a part of material selection in qualifying and locking down a PCB construction. The check must be performed again if raw material or process changes occur.
5) A consistent relationship in PCB insertion loss between two different frequencies, 4 GHz and 8 GHz, existed on all layers of one product tested but could not be consistently established on outer layers of the other product. Thus we need to measure at both frequencies for insertion loss compliance checking.
6) There was no consistent relationship between impedance and insertion loss across the products and layers. As a result, impedance alone can't be used to predict the acceptance of insertion loss.

A study in the variations of low loss board material PCB constructions and their comparison with these mid loss ones will be needed as the specification of PCB insertion loss becomes more stringent for future generations of server products.

Three HVM PCB suppliers were involved in this study. Expanding the study to include more HVM and quick turn suppliers is needed to gain a more comprehensive industry wide understanding of insertion loss variation in PCB manufacturing.

We also plan to perform a study establishing temperature and humidity impact on PCB insertion loss for specific PCB constructions used for server products.

Acknowledgments

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We would also like to offer special thanks to Brian Butler and his staff at Introbotix Corporation for diligently performing all of the coupon measurements for this study.

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A Study of PCB Insertion Loss Variation in Manufacturing Using a New Low Cost Metrology

Intel Corporation

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Agenda

- Background
- SET2DIL methodology
- Study summary
- Data analyses
- Conclusion

Background

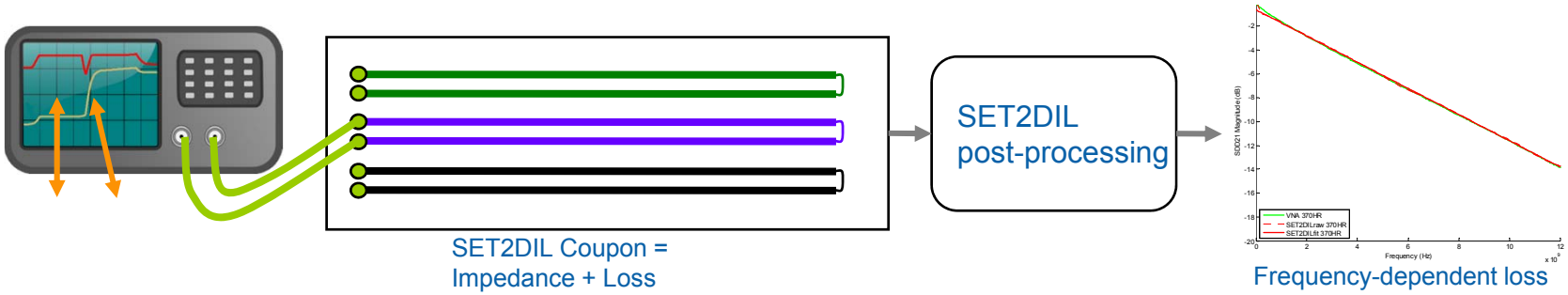
- PCB insertion loss becomes a critical performance attribute in typical server platforms
  - The data rate approaches ~ 10 gigabits per second on traces with routing lengths often > 12 inches
- How to determine loss compliance in manufacturing?
  - Where and how loss measurements should be done?
  - Most PCB fabricators do not have a good understanding of the impact of raw materials, process and metrology capability
- Traditional method of measuring differential insertion loss (4-port VNA) is difficult to adopt in manufacturing environments
  - Expensive equipment with highly trained technicians
  - Very slow throughput time, suitable for laboratory use

Need a lower cost, easier to use method for loss measurement

SET2DIL Methodology

(Single-Ended Time domain To Differential Insertion Loss)

- Use ubiquitous impedance coupon and associated 2-port TDR/TDT hardware
- Add a thin loopback to the end of each differential pair
- Extract differential loss (SDD21) and impedance from the TDR/TDT signals using post-processing algorithm



Less expensive 2-port TDR/TDT equipment and software

Study Objectives

- Determine if SET2DIL methodology is capable of measuring insertion loss
  - Use a formal Gauge repeatability/reproducibility study
- Understand variations of PCB insertion loss in HVM (High Volume Manufacturing)
  - Determine loss compliance tracking strategy
  - Make data driven decision in implementation details

Study Overview

- Select two 8-layer (4 signal layers) production boards
  - Product 1: 62 mil thick; Product 2: 93 mil thick
  - Each board produced at two different HVM PCB suppliers
  - Each unique FR4 raw material used for each board-supplier combination

	Product 1	**Product 2**
Supplier 1	Material 1	Material 2
Supplier 2	Material 3	None
Supplier 3	None	Material 4

- Adopt SET2DIL coupon for compliance measurement
  - Matching coupon Gerber files for the respective stack-up were created
  - PCB suppliers added coupons on the working panels of production runs
  - PCB suppliers followed the sampling plan to ship 15 coupons from each lot since August 2010
  - Coupons vacuum packaged containing desiccant in the bag during shipment
- Enable a third party to perform measurements @ 4 & 8 GHz
  - Each coupon pre-conditioned, baked at 105-120C for 6 hours with a ramp down to ambient of 30-60 minutes, before the measurement
- Collect data from over 800 coupons in 46 different manufacturing lots at three HVM suppliers over 6 months

Study Assumptions

- Humidity effect eliminated
  - All coupons pre-conditioned to eliminate moisture before measurements
- Lot variation in raw material
  - PCB suppliers built with multiple lots of raw material with random combinations of core and prepreg
- SET2DIL measurements made with standard GGB dual probe on a probing station
  - Three other commonly used probe types, included the handheld PicoProbe, not tested in this study

Note: "PCB Construction," a term used throughout this presentation, refers to the following *unique* set:

{stack up, materials, process, specific PCB supplier factory}

Data Analyses

Metrology Capability

Insertion Loss Measurement	Repeat ability (dB/in)	Precision (P) (dB/in)	P/T Ratio	P/6σ within lot
Outer layers 4 GHz	.00699	.0220	8.78% T=.25	21.2% 6σ=.102
Inner layers 4 GHz	.00681	.0240	8.27% T=.29	26.5% 6σ=.0904
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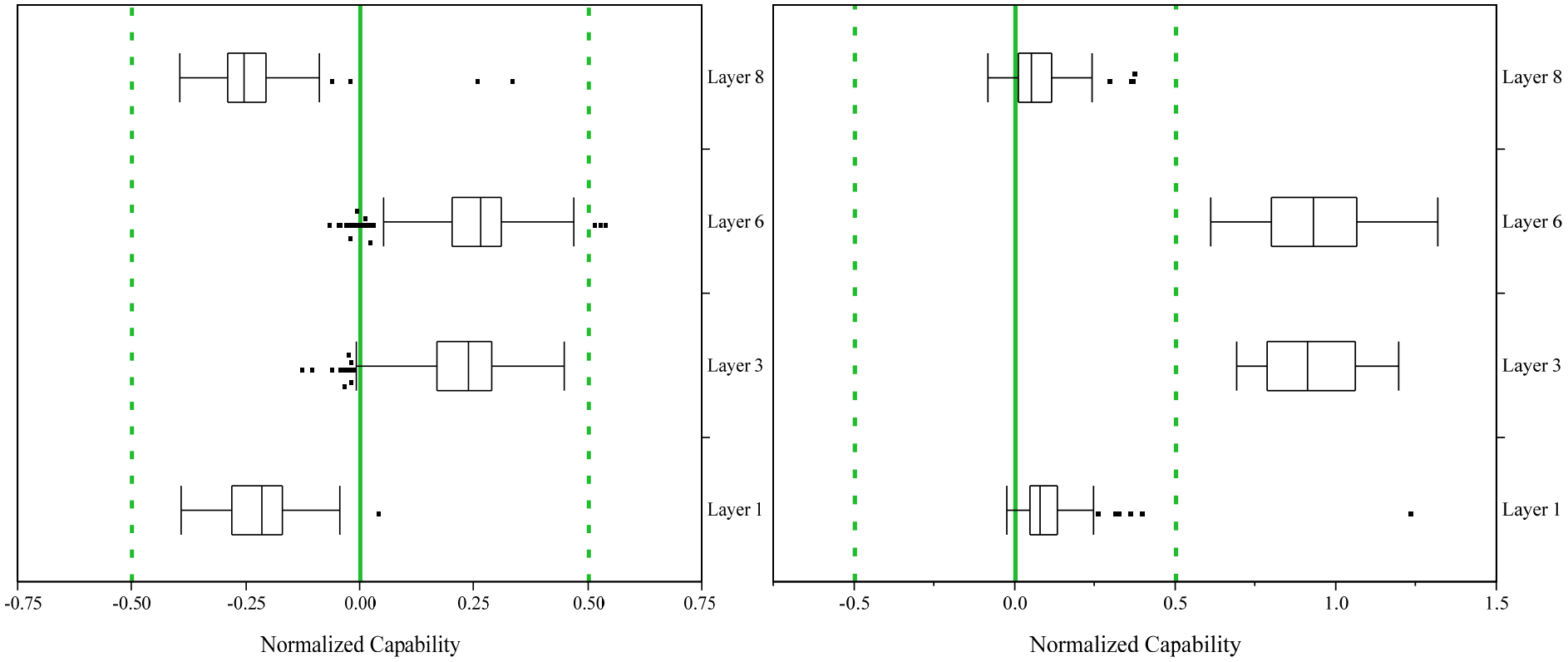
Inner layers 8 GHz	.00139	.0371	6.29% T=.58	24.1% 6σ=.154

Metrology is capable: P/T<10%

PCB Construction Capability

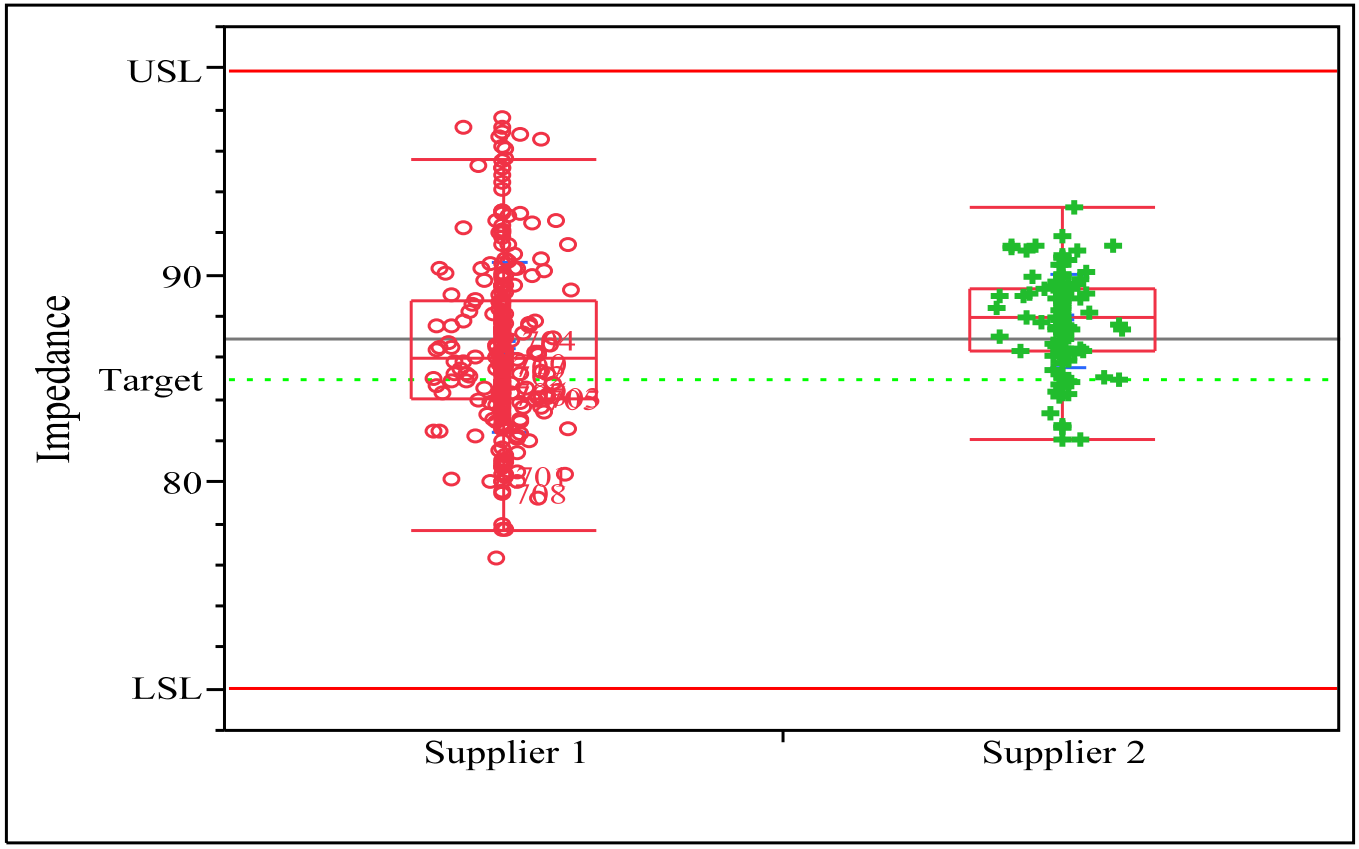


Supplier 1 on Product 1

Supplier 2 on Product 1

Not all PCB constructions are capable

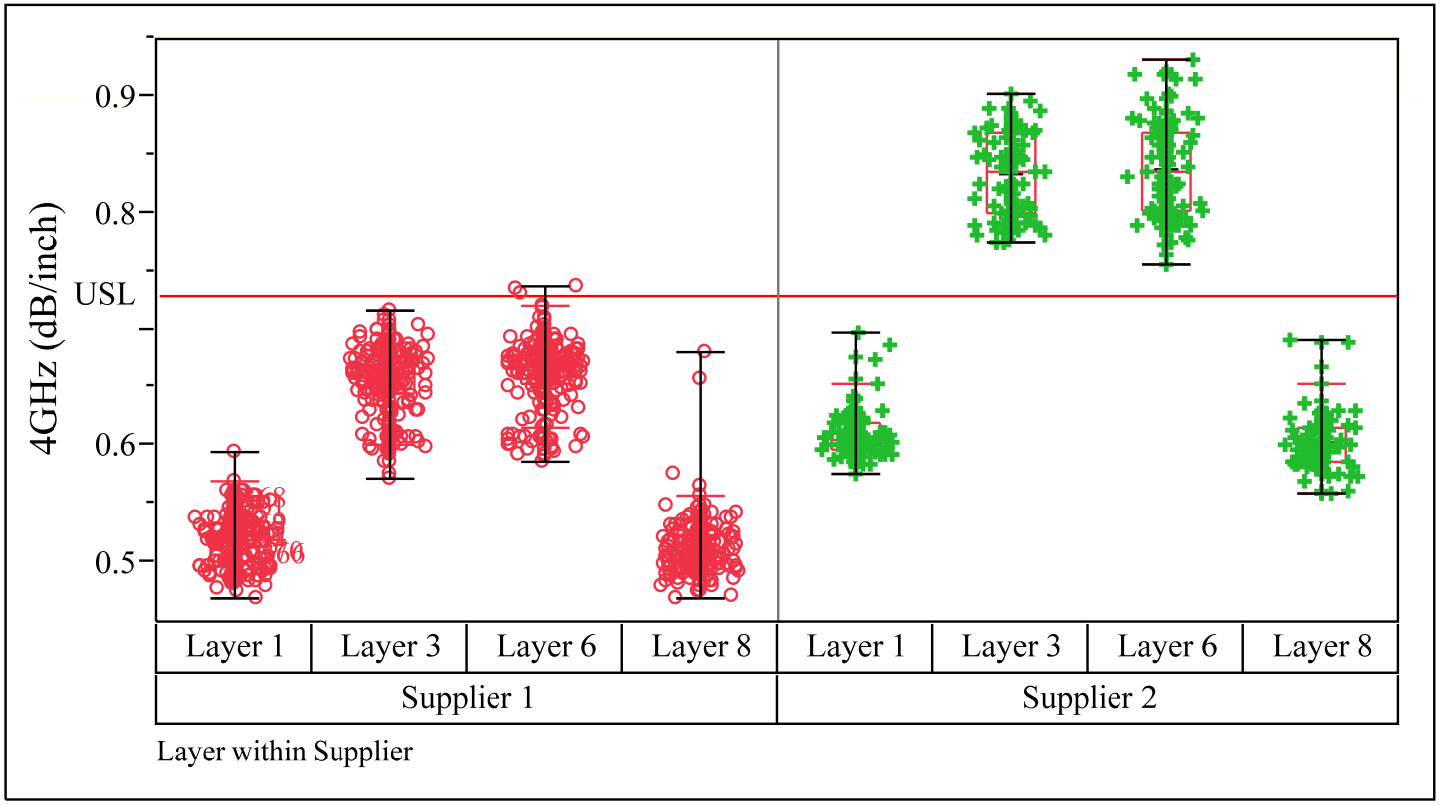
Impedance



Spec: 85 Ohm +/- 17.5% (***Product 1, Layer 1***)

Matched historical data at both suppliers (as expected)

PCB Insertion Loss

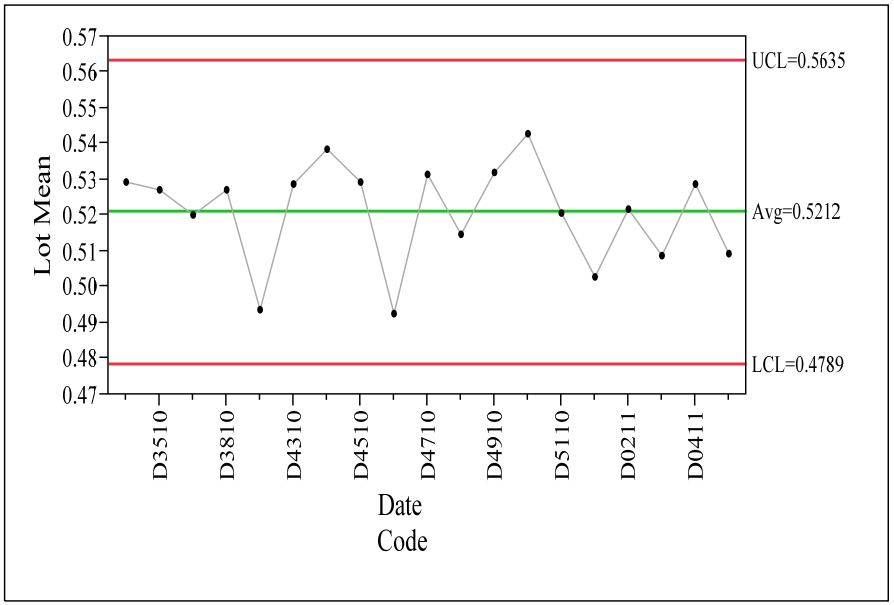


Product 1 @4 GHz

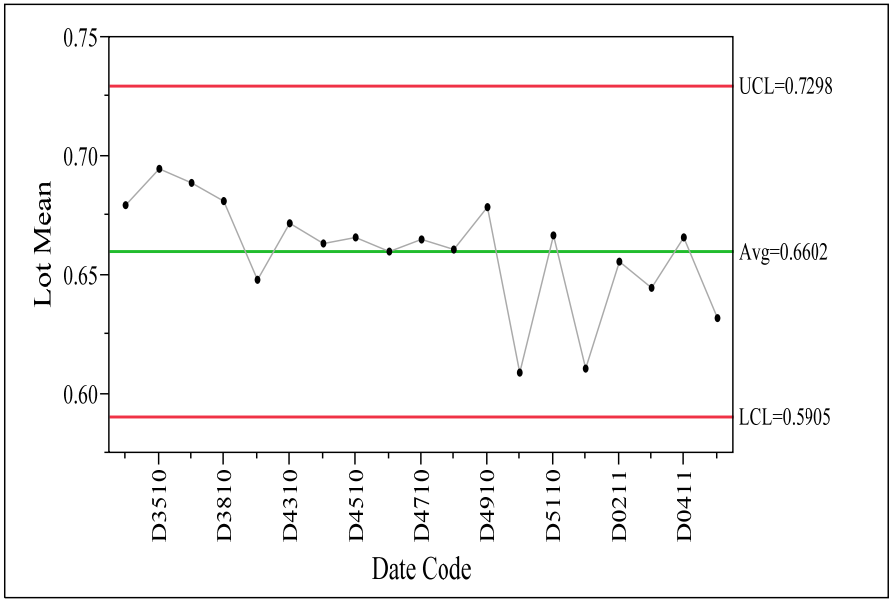
Not matched across suppliers/layers

Matched on inner and outer layers of a given PCB construction

Insertion Loss Lot Mean Distribution



Product 1 on layer 1 @4 GHz

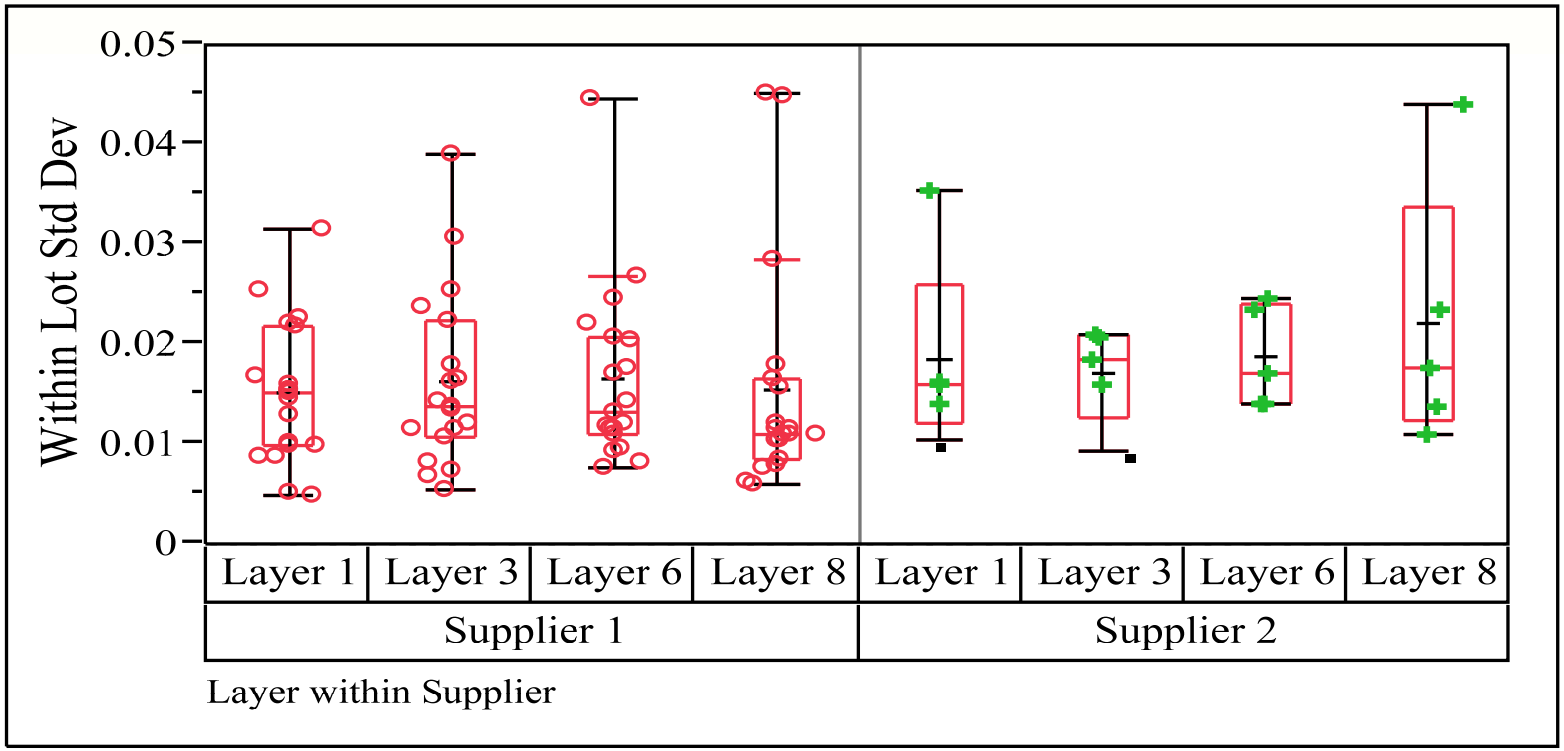


Product 1 on layer 3 @4 GHz

Insertion Loss is stable

(about ±0.05 dB/inch variation from lot-to-lot)

Coupon to Coupon Variation

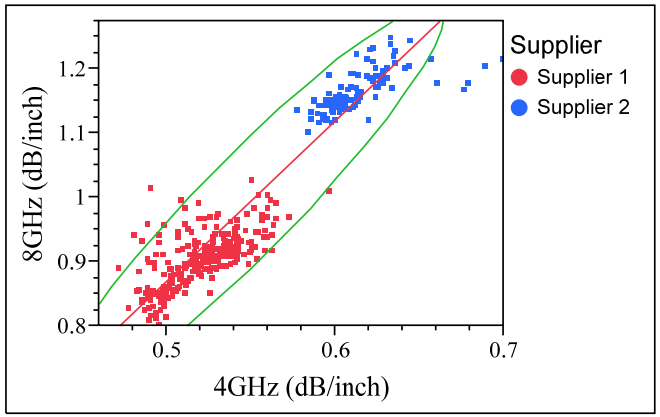


Product 1 @4 GHz

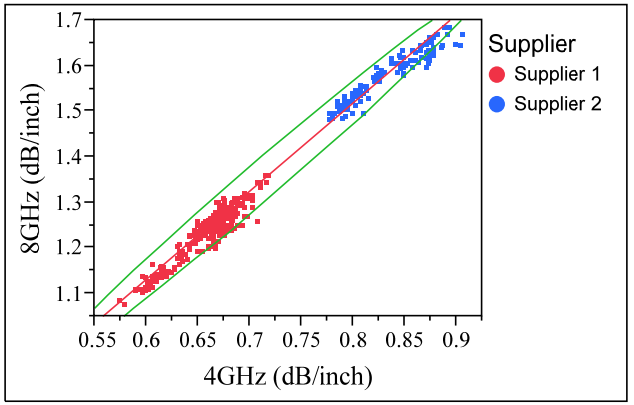
Within the Lot Variation Consistent

Loss Relationship between Frequencies

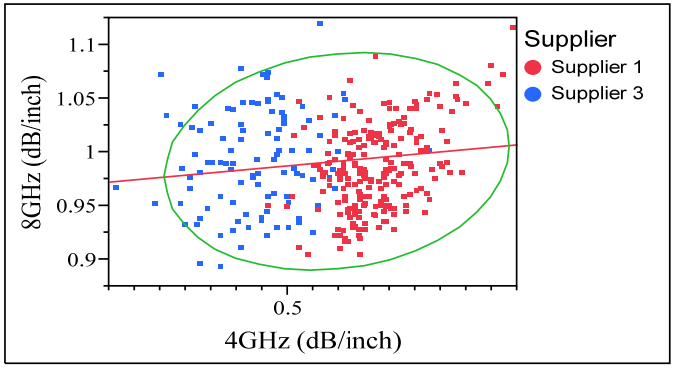
Product 1 Layer 1



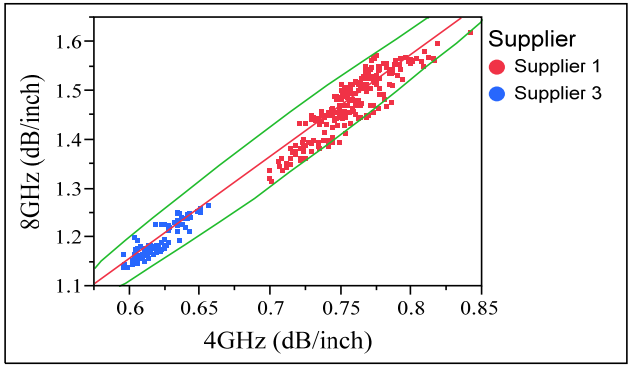
Product 1 Layer 3



Product 2 Layer 1

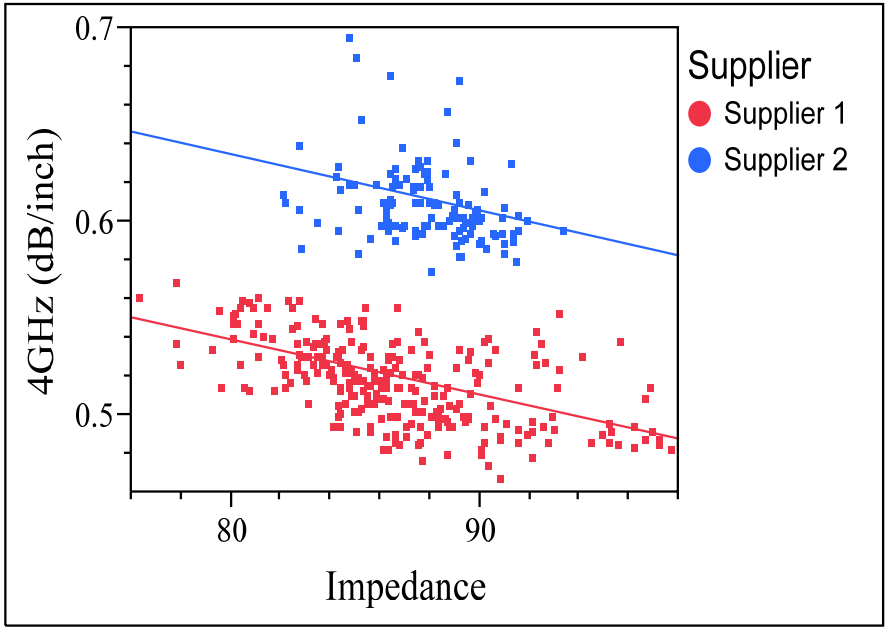


Product 2 Layer 3

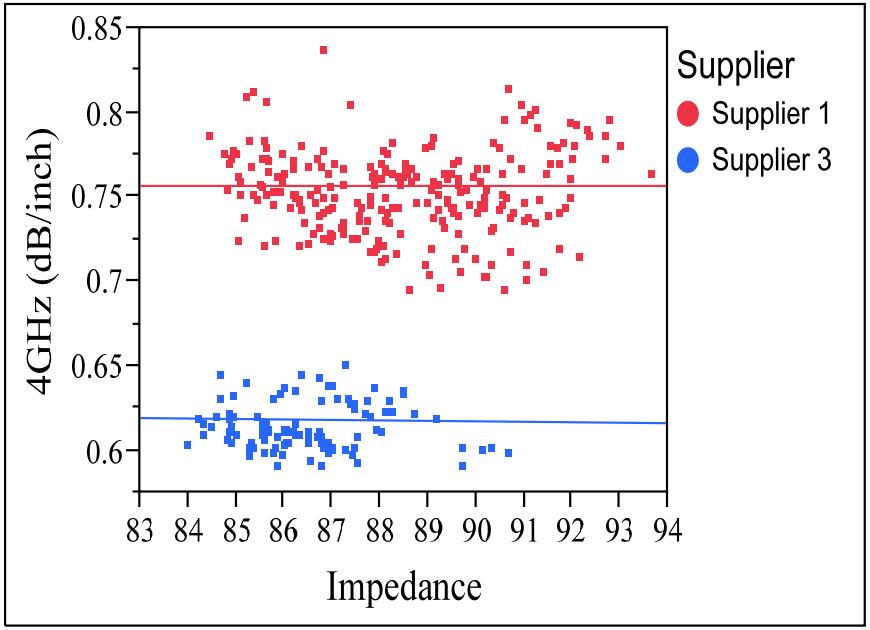


Not consistent between 4GhZ and 8GHz
(Need to measure both)

Impedance and Insertion Loss Relationship



Product 1 layer 1 @4 GHz



Product 2 layer 3 @4 GHz

Not consistent across products/layers
(Can't use impedance as only metric)

Conclusion

1) SET2DIL metrology for PCB insertion loss measurements is capable and can be used to monitor insertion loss compliance.
2) Some PCB constructions met the PCB insertion loss specification whereas others did not.
   - Raw material type is a primary factor.
3) About ±0.05dB/in variation in PCB insertion loss was observed from lot-to-lot of the same board and supplier.
4) PCB insertion loss compliance check should be a part of material selection in qualifying and locking down a PCB construction.
5) A consistent relationship in PCB insertion loss between two different frequencies, 4 GHz and 8 GHz, existed on all layers of one product but not on outer layers of the other product.
6) There was no consistent relationship between impedance and insertion loss across the products and layers.