Flip Chip Package Qualification of RF-IC Packages

Mumtaz Y. Bora
Peregrine Semiconductor
San Diego, Ca. 92121
mbora@psemi.com

Abstract
Quad Flat Pack No Leads (QFNs) are thermally enhanced plastic packages that use conventional copper leadframe with wire bonded interconnects. . These leadless components provide an advanced packaging solution that reduces board real estate, with improved electrical and thermal performance over traditional leaded packages. The move towards finer pitch is resulting in using flip chip bumps as interconnects on an interposer substrate and packaging as QFN. [1]

The QFN devices commonly known as BTC (bottom terminated components) are attractive due to their low cost per I/O, performance and low profile; they are also a challenge for assembly due to their low to zero standoff height. Successful assembly yields and solder joint reliability requires careful selection of substrate materials, fluxes, component plating finishes, controlled reflow processes and flatness of package and PWB. [2]

This challenge is enhanced with the transition to lead free reflow as the higher peak reflow temperatures results in more thermal and CTE mismatch between package and PWB. Wire bonded leadframe packages are typically plated with 100% Matte tin or NiPdgold on the solderable terminations. Interposer substrate is typically plated with Electroless nickel /gold for solderability of terminations. War page characteristics of interposer substrates have to be evaluated to minimize stress on the flip chip bumps.

Reflowing packages with flip chip bump interconnects requires a good balance of substrate /package material sets and controlled reflow profiles to ensure proper melt of the bump interconnects and solder joint reliability thru subsequent reflow processes at assembly facilities.

The paper reviews the qualification efforts for solder interconnects on interposer substrates, X-ray and X-sectional analysis of packages and process optimization efforts to improve reliability of the interconnects

Introduction
Flip chip interconnects are in demand for consumer electronics as these packages shorten the signals , reduce inductance and improve functionality of these packages as compared to the wire bonded packages. These packages are commonly known as LGA (Land Grid Array) packages. To ensure reliability of these packages in high volume SMT assembly production requires careful selection of critical commodities like IC Packages and PWBs. SMT assembly yields depend on good quality components, solder paste print processes and oven reflow profiles. This has become more critical in lead free reflow due to higher peak reflow temp. And narrow process windows. Proper storage and handling controls of components and process controls in production are necessary for good yields and reliability.

The paper summarizes the qualification of solder and copper interconnects. Package construction analysis was conducted to assess integrity of die attach, molding and plating processes. X-section and SEM/EDX analysis, and reliability test results for thermal cycling tests are presented including continuous improvement efforts at subcontract locations.

Substrate Selection and Design
The substrates used for interposer packages are typically 2 layers thin laminate approximately 150- 200 micron thick BT resin with 100 micron drilled visa for layer interconnects. The typical pad pitch is 200 microns with the option of having solder mask defined or non-solder mask de fined pads. Figure 1 shows the bottom side of the substrate pads with the terminations that solder to the board. Figure 2 shows an X-Ray image of a typical leadframe wire bonded package.

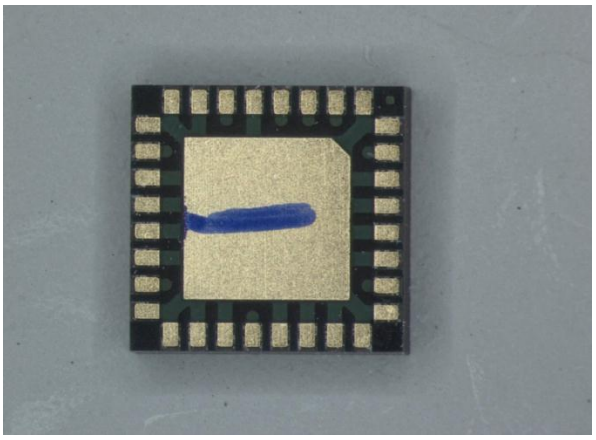


Figure 1. Subtrate bottom side terminations

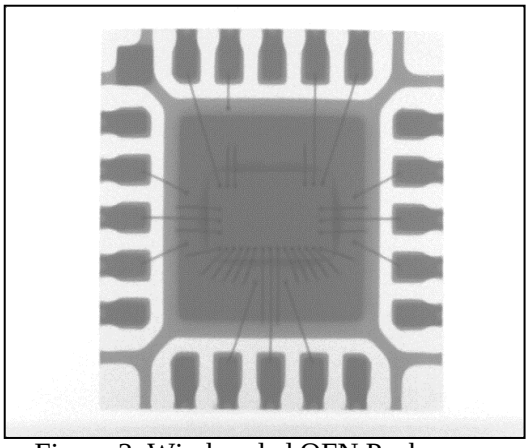


Figure 2. Wirebonded QFN Package

Flip Chip Bump Options

The bumping options require evaluation as there are many different metallurgies that can be used for flip chip bumping depending on the application and use environement for commercial products, Hi-Reliability products etc. The most common bump material used is eutectic or lead free solder. Other materials used are copper bumps or pillars with solder cap to attach to the
substrate pad or gold stud bumps for some hi-reliability applications.

The early process development work was done using daisy chain dies with lead free solder bumps.followed by product. Figure 3 shows a X-section of solder bump and Figure 4 shows an example of Copper bump in X-section.

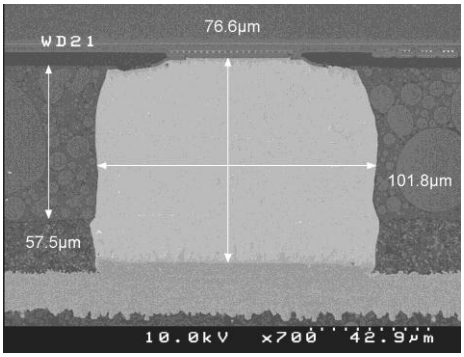


Figure 3 - Solder Bump

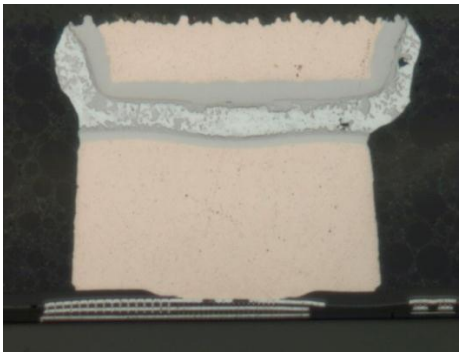


Figure 4 –Copper Bump

Assembly Process

The assembly process requires proper optimization of die placement on the interposer pads to get an optimized solder profile. Die placement is done using automated placement equipment. A tacky flux is sprayed on the substrate to facilitate the wetting of the solder bump. In some cases, the bottom one third of the bumps are dipped in flux and then placed on the substrate for reflow. Flux spray process on the substrate appears to give more uniformity and facilitates wetting of the bump.

X-Ray Inspection

Inspection after placement is done using X-Ray to ensure that thebump is aligned to the pad . A first article inspection is conducted using X-Ray , prior to die placement on the balance of the lot and the necessary adjustments are made to align the die.

Reflow Profile

Package was reflowed using a lead free solder profile for both solder bump and copper bump using a peak reflow temp of 250C . Multiple reflow profiles were evaluated until the heating and the cooling rate was sufficiently controlled to get an optimum bump profile post reflow. Profiles that are not optimized can result in open bumps post reflow or post thermal shock. X-Ray of the reflowed bumps is also conducted toensure proper melt of the bumps. Figure 5 shows the X-Ray image post reflow.

Post Reflow – X-sectioning was conducted to understand the solder joint profile, alignment, presence or absence of voids also to evaluate the grain structure of the solder joint. Voids can get trapped at the bump to substrate interface and cause assembly issues. Generally acceptable criteria for voids is less than 30% of the bump diameter.
Figure 6 shows X-section of a reflowed package

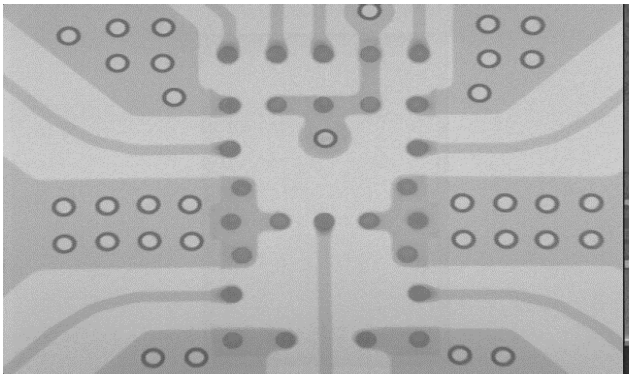


Figure 5- X-Ray image Post-Reflow

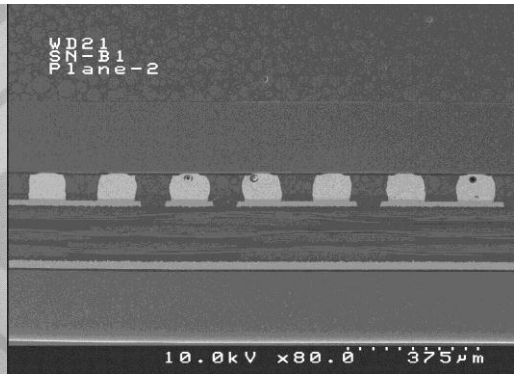


Figure 6- X-section of a reflowed solder bump

Reflow profile evaluations were also conducted on the copper bump to optimize the reflow profile and minimizes stress on the reflowed bump. Open bumps can occur on the reflowed side or at the die to bump interface due to coefficient of thermal expansion (CTE) mismatch and substrate warpage during reflow. Figure 7 shows the X-section of the copper bump post reflow

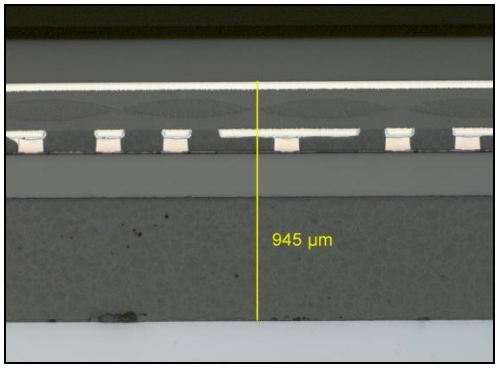


Figure 7- Copper bump Post Reflow

Overmolding:

Package is overmolded with a mold compound and post mold cured at 175C for 6 hours. Proper selection of molding materials is essenttial to minimize impact on electrical properties. Multiple runs were conducted to optimize the cure profile, mold pressure, cure time , temp. etc. Figure 8 shows the X-section of an overmolded package

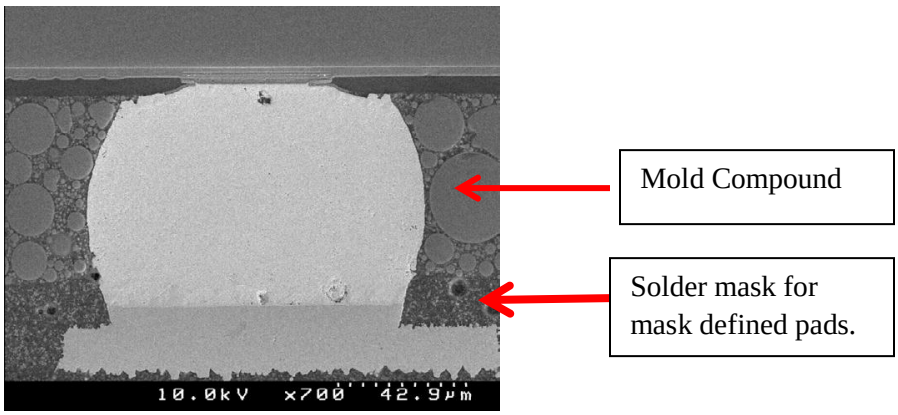


Figure 8 X-section of overmolded package

Reliability Testing

A prerequisite to package reliability testing is moisture pre-conditioning to classify package MSL class and ensure that it survives reliability test post moisture soak.

The package delamination testing was done using Pre/Post CSAM testing (Scanning Acoustic Microscopy). Packages were subjected to MSL-3 pre conditioning at 60C/30% RH for 192hours followed by 3X reflows at 260C. Both Pre-CSAM and post CSAM images showed no delamination in the packages as shown in Figure 9. The packages were classified MSL-3.per J-STD-020D.1 [3] as laminate based substrates cannot achieve MSL -1 (unlimited floor life). Figure 10 shows the CSAM image post- preconditioning showing no delamination. The reliability tests are summarized in Table 1. Solder bumps were characterized using JEDEC JEP154-Guideline for characterizing solder bump under constant current and temp. Stress. [4]

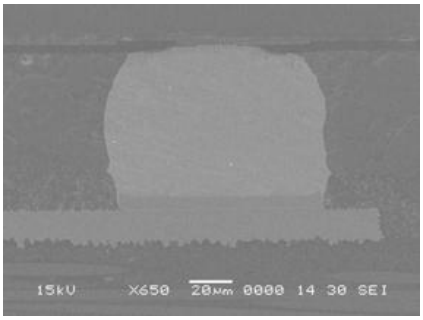


Figure 9 – X-section post preconditioning

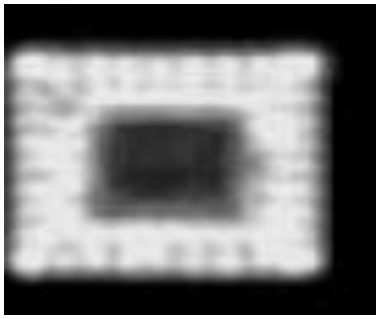


Figure 10—CSAM Image post preconditioning

Reliability Test	Condition	Acceptance
High Temp. Storage Life	150C-1000 hours	Pass electrical/visual
Autoclave Test	121C,100% RH 15Psig-96 hours	Pass electrical/decap
Thermal Cycling	-65C to +150C 500hours	Pass electrical /X-section

The initial evaluations at thermal cycling reliability test did show some cracking of bumps at the substrate bump interface. Figure 11 shows the X-section post thermal shock .

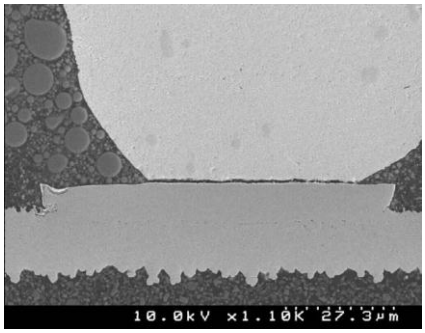


Figure 11—Bump Interface cracks post thermal shock.

This condiiton was eliminated by optimization of the reflow profile and controlling the heating and cooling rate during bump reflow.

The solder bumped package passed reliability tests, except some bump voids were observed at various stages of testing as shown in Figure 12.

.

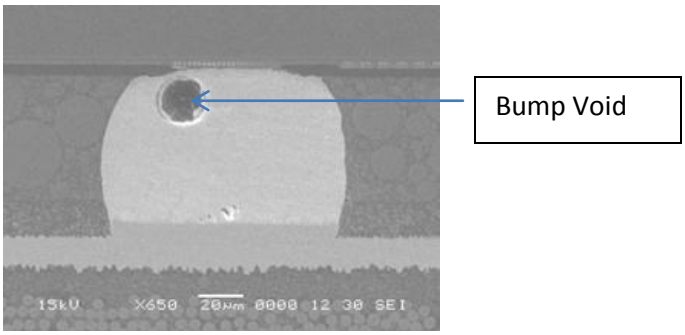


Figure 12- Bump void

Conclusion:

Bumped interconnects are a reliable form of interconnect if reflow process, mold material sets, substrate pads and solder mask are optimized. This will minimize CTE mismatch failures, dewetting of the bump and cracks at the bump to substrate interface. Solder bumps have the ability to self centre during reflow which minimizes failure due to misplacement. Package integrity can be maintained by proper control of processes.

References:

1.Leadfree solder Flip chip Assemblyon Laminate and Reliability .Zhen Wei Yu ,Erin Yaeger etal.

2.IPC-7093- Design and Assembly guideline for soldering of Bottom Terminated Components.

3. J-STD-020D.1 – Moisture refllow Sensitivity Classification of Non HermeticSolid State Devices

4. JEDEC JEP154-Guideline for characterizing solder bump under constant current and temp. stress.

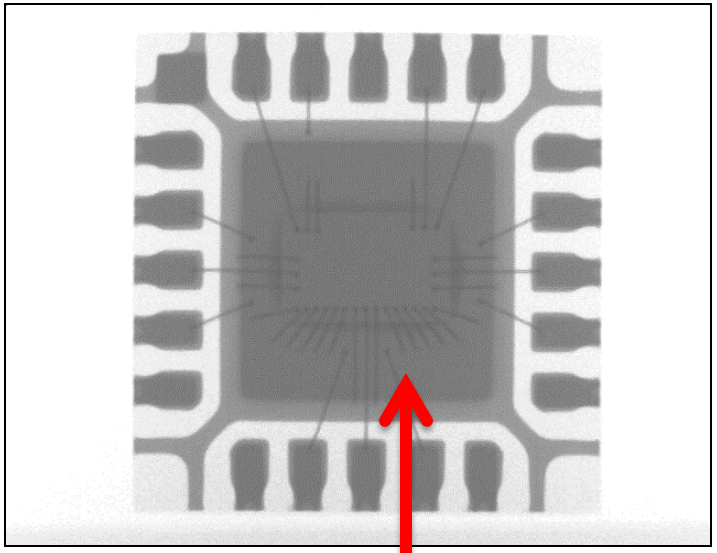
Flip Chip Package Qualification of RF-ICs

Mumtaz Y. Bora
Peregrine Semiconductor
San Diego, CA

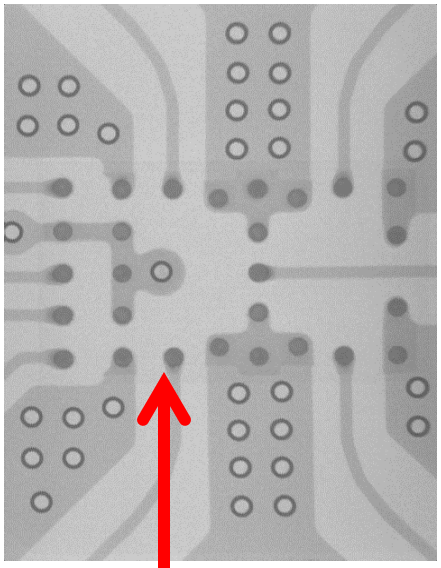
Overview

- Flip Chip vs. Wire bond Package
- Substrate Selection and Design
- Bump Technology Options
- Assembly Process
- Reliability Testing
- X-section/CSAM Analysis
- Future Outlook

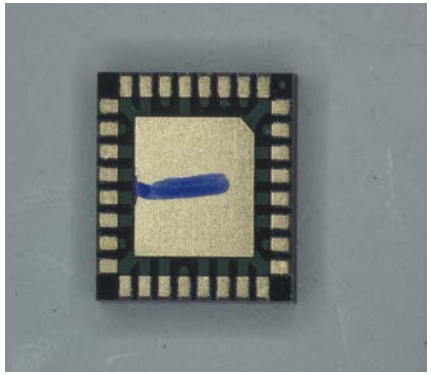
Flip chip vs. wire bond package



Wire Bonds



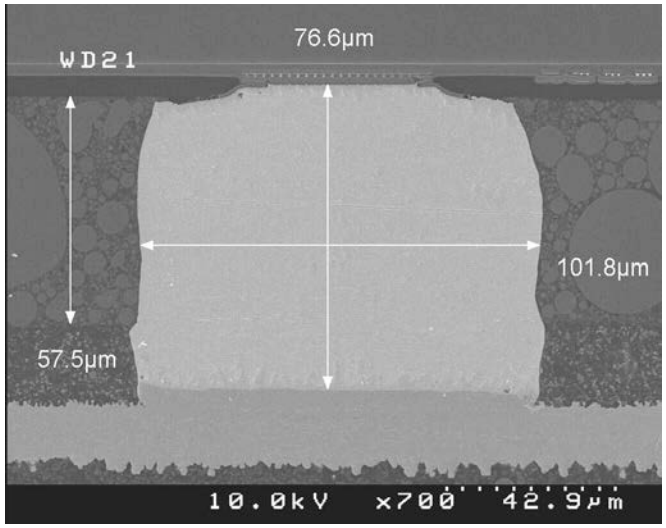
Solder bumps



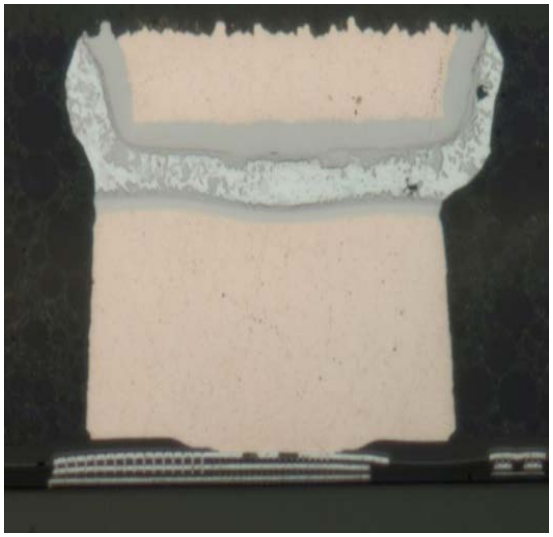
Package

Flip chip advantage-shortens the signals

Bump Options



Solder Bump
Collapse after reflow
Eutectic or lead Free



Copper Bump
Maintains standoff

- Other options, 10/90 high temp. bump, gold stud bumps

Substrate Selection

- Substrate
  - 2-4 Layer Interposer
  - BT resin
  - LTCC
  - Leadframe
  - Solder Mask Defined/Etch Defined Pads
  - 150-200 micron thick
  - Via 100 micron diameter
  - Trace Width >40 micron

Laminate Substrates

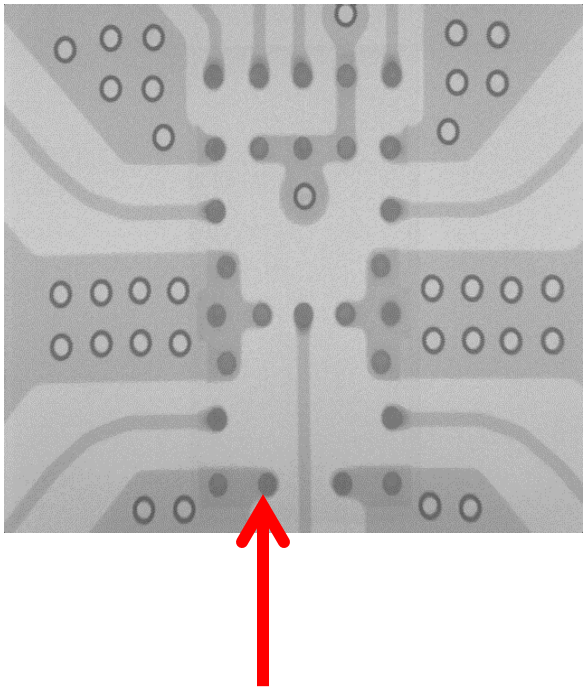
- Tg -Range –160C-220C
- Td - >300C
- CTE -Z- axis -below Tg/ above Tg
- Dk/Df- @1GHz, 5GHz, 10GHz
- Moisture Absorption
- Thermal Conductivity
- Peel strength of Copper
- % Filler
- Halogen Content

LTCC Substrate

- Used for High frequency Applications
  - Thermal Conductivity ~2-3W/mK
  - Dk values at 60GHz~ 5-8
  - Df values at 60GHz~ 25- 35 X10^{-}4
  - CTE-- 8-12 10^{-}6/K
  - Flexural Strength – 170-280 MPa
  - Modulus of Elasticity -72-100 GPa
  - Vias- Ag or Cu filled

Assembly Process

- Flux Application
  - Spray on substrate
  - Flux Dip Die
- Die Placement
  - Alignment of bump to pad
  - X-Ray Inspection
- Reflow Process
  - Lead free/Eutectic
  - Control Ramp Rate



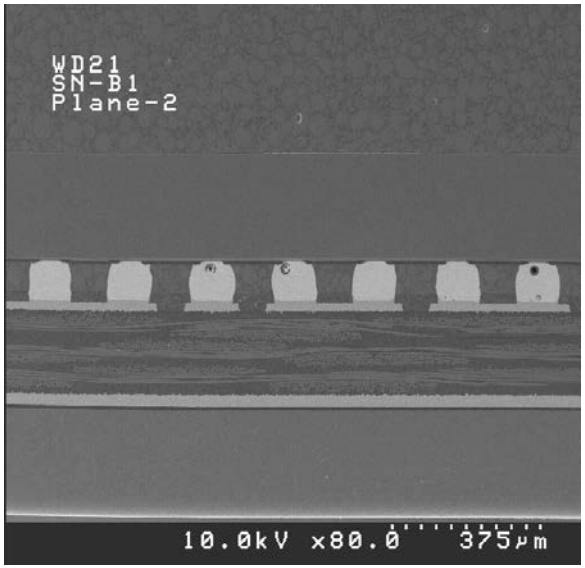
Bump Alignment

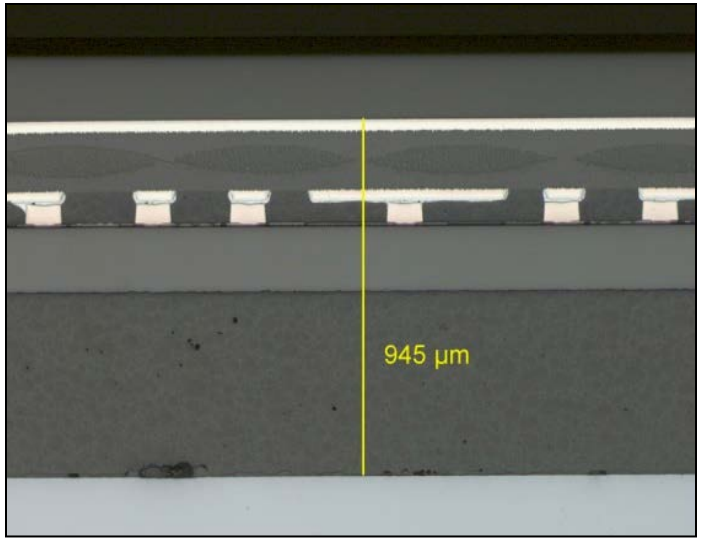
Assembly Process- Reflow

- Typically 250-260C for lead free bumps
- Optimized Reflow Profile
- Controlled Heating and Cooling Rate
- Typical Defects
  - Cracks
  - Voids
  - Opens
  - Delamination

Voids

Solder bump vs. Copper pillar



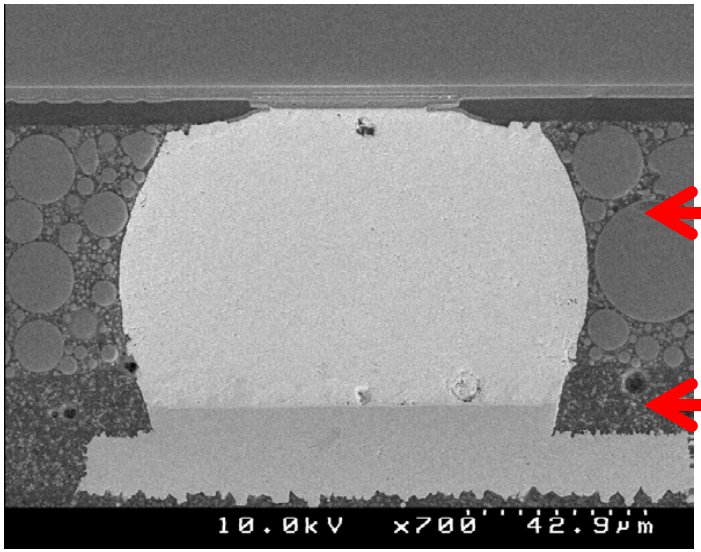


Bump collapse post reflow

Bump stand off post reflow

Package Thickness is 0.8-0.95 mm

Over molding



Mold Compound

Solder Mask

Type of mold compound, cure profile, cure time needs optimization. It can impact electrical properties.

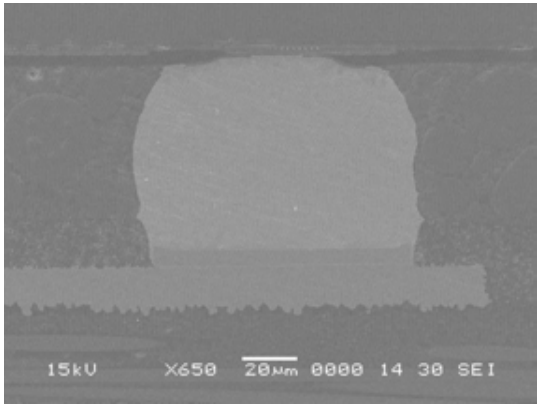
Some packages do use underfill post reflow.

Moisture Classification Test

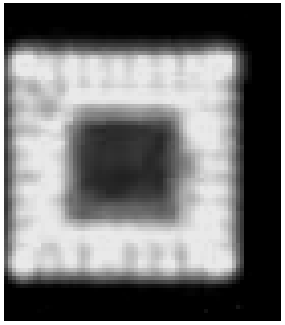
- All packages need to be tested for MSL Class per J-STD 020D.1
- Conduct Pre- CSAM(Scanning Acoustic Microscopy)

- Preconditioned at 60C/30% RH for 192 hours for MSL Class 3.
- 3X Reflow at 260C

- Post-CSAM
- Evaluate for die to mold compound or die to laminate delamination and electrical test



Cross-section Post Pre-conditioning



Post-CSAM Image-No Delamination

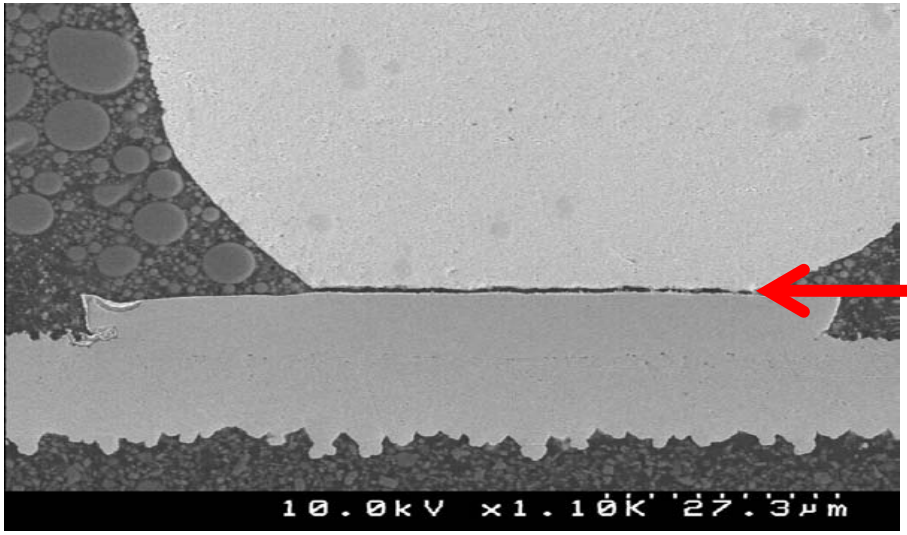
Post-CSAM Inspection

- Acceptance Criteria
  - No delamination on die surface
  - No delamination change>10% along mold/laminate interface and die/mold interface
  - No delamination change>10% solder mask/laminate interface
  - No delamination change>10% within the laminate
  - No delamination cracking>10% through the die attach region
  - No delamination between underfills/die and underfills/laminate

Reliability Test

Reliability Test	Condition	Acceptance
High Temp. Storage Life	150C-1000 hours	Pass electrical/visual
Autoclave Test (Preconditioned)	121C,100% RH 15Psig 96 hours	Pass electrical/decap
Thermal Cycling (preconditioned)	-65C to +150C 500hours	Pass electrical/X-section

Failure Evaluation



Crack at bump to substrate -500 thermal cycles

Optimized solder mask application on laminate and improved reflow profile to eliminate this condition