iNEMI

International Electronics Manufacturing Initiative

iNEMI HFR-Free (Halogen-Free) Session

Apex 2012
February 29, 2012

Advancing manufacturing technology

Presenter/Committee Chair(s):

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- Dr. Robert Pfahl, iNEMI
- John Davignon, PCB TD Manager, Intel Corporation
- Stephen Tisdale, Technology Development Mgr, Intel Corporation
- Lameck Banda Ph.D., Core R&D, Materials Science, Dow Chemical USA
- Stephen Hall, Sr. Staff Engineer, Intel Corporation
- David Senk, Manager, PCB Technology Group, Cisco Systems, Inc.
- Gary Long, PCB Technology Development, Intel Corporation

An Investigation to Identify Technology Readiness, Supply Capability, and Standards Development Opportunities for High Reliability "HFR-Free" Applications

•Stephen Tisdale, Intel Corporation

BFR-Free High Reliability Project

Project Leader

Stephen Tisdale,
Intel Corporation

BFR-Free High Reliability PCB Project

Project Members

Agilent Technologies

DELL

Celestica™

CISCO

DOOSAN Doosan Corporation Electro-Materials

EMC ELITE MATERIAL CO., LTD.

hp invent

intel

iST INTEGRATED SERVICE TECHNOLOGY

ITEQ

NAN YA

ROHM AND HAAS

Sun microsystems

iNEMI BFR-Free High Reliability PCB Project

IS / IS NOT

This Project IS:	This Project IS NOT:
Technical evaluation of key electrical and mechanical properties	An EHS assessment
Focused on those attributes which are of most value to supply chain	Biased towards specific laminate suppliers, geographies, or market segments
Build on learning from prior investigations	Repeat of prior work
Focused on completely HF SMT and Wave Solder Assembly & Rework Capability	Focused on standard processing
Focused on circuit board materials in LF assembly and LF solder joint reliability – Board / Component Interaction	Focused only on materials characterization

iNEMI BFR-Free High Reliability PCB Project

Phase 1: Design

Goal: *Review prior work and make recommendations for testing needed. Investigation should take into account the needs of electronic product sectors represented by iNEMI membership*

- **Identify market segment requirements**
- **Identify candidate materials**
- **Identify key performance characteristics and test criteria**
- **Design test vehicle(s) and test methodologies, leverage standards where possible**
  - Identify Components to be used in this project to evaluate SJR / board reliability

iNEMI BFR-Free High Reliability PCB Project

Phase 2: Test

Goal: *Develop, manage, and execute performance testing*

- **Develop evaluation schedule**
- **Procure parts and test vehicles**
- **Assign teams to carry out completion of the testing in a standardized fashion**

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- **Perform mechanical and reliability testing on test vehicles.**

iNEMI BFR-Free High Reliability PCB Project

Phase 3: Results

Goal: *Compile results, assess significance, make recommendations, and publish report*

- **Assess performance relative to market segment requirements**
- **Assess technology readiness / identify gaps**
- **Assess manufacturing capability and supply capacity**
- **Publish results**

iNEMI BFR-Free High Reliability PCB Project

Anticipated Outcomes

- Validate electrical and mechanical properties
  - Loss tangent and Dk modeling over required range of signal speed
  - Mechanical performance validation for lead free assembly and rework (delamination)
  - Critical Test Parameter Evaluation (CAF, IST, flex, etc.)

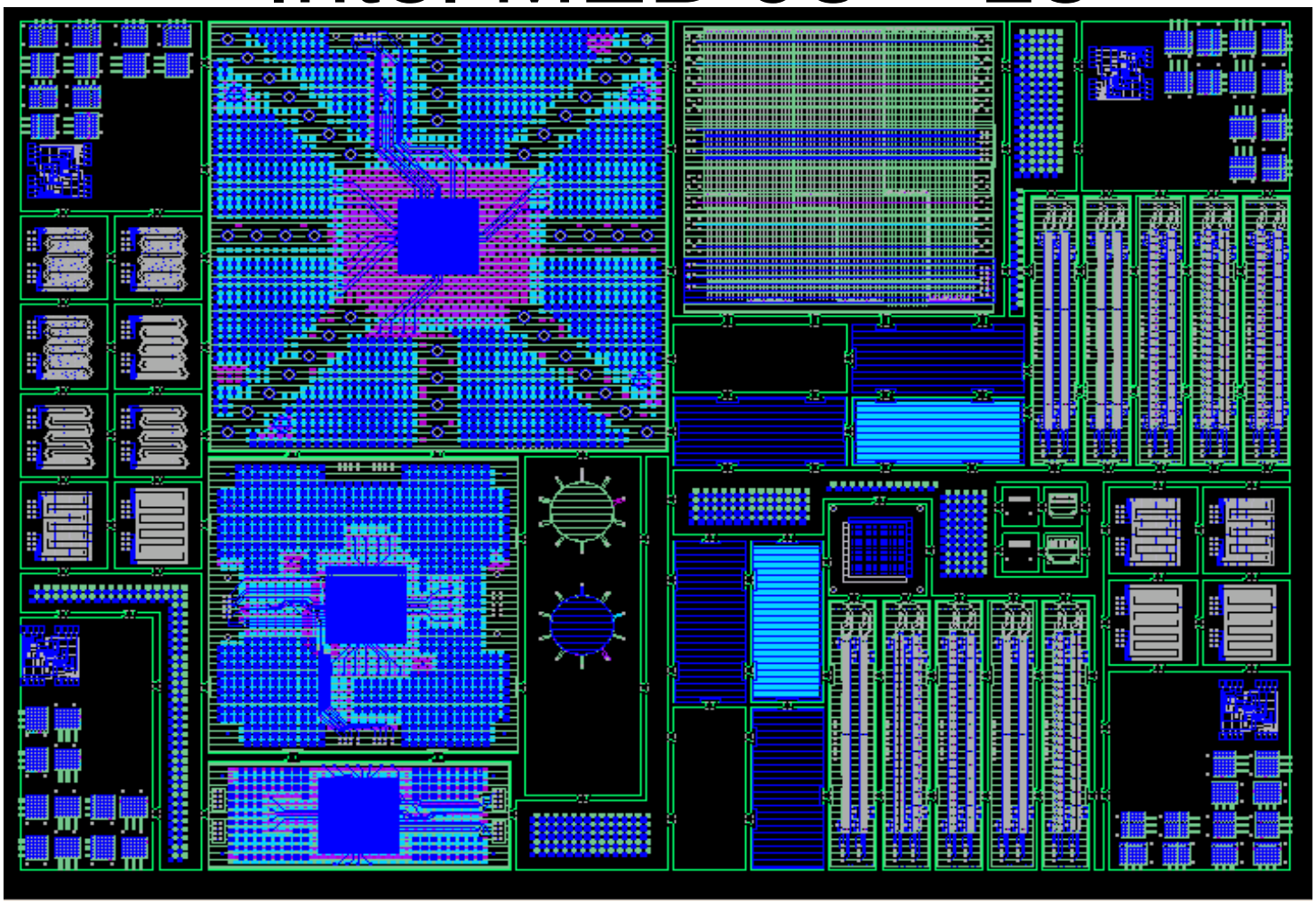
- Validate Board Level Reliability Capability
  - PCB Modulus / Thickness Impact on Mechanical Capability
  - HF Board Level Assy / Rework Process Characterization
  - Mechanical Characteristics (Pad Crater / Ball Pull etc)
  - CTE Characteristics
  - SJR (Shock / TC etc)
  - HF Component / HF PCB

iNEMI HFR-Free High Reliability PCB Project

- Focus is on Hi-Rel (Server) Market Segment Application Space
- PCB and PCBA components are HFR-free (Low-Halogen)
- Board Thicknesses are 0.093" & 0.125" (MEB's) & 0.116" (Agilent)
- PCB Material should be LF compatible, low / med loss and HVM capable
  - 8 BFR-free Materials Identified with 1 Halogenated Material as Control
- All TV's have been completed and are being tested (estimated completion is end of Q4'11)

	MEB III	MEB III	Agilent
Layer Count / Thickness	18 Layer / 0.093"	24 Layer / 0.125"	20 Layer / 0.116
Drill Sizes	8mil / 10mil / 12mil	10mil / 12mil / 14 mil	12 mil
Pitch	0.8mm / 1.0mm	0.8mm / 1.0mm	0.8 mm
Reflow Temps	245C & 260C	245C	245
# Reflows	6x & 10x	6x & 10x	6x

Intel MEB 93 – 18



- 22.25” X 15.75” in size
- Modular in design
- MEB125 – 24 Layer same footprint

Stack-ups

MEB 125 Stackup

	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu	S	1.6	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 2	Unplated 1 oz Cu	P	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 3	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 4	Unplated 1 oz Cu	P	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 5	Unplated 1 oz Cu	S	1.4	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 6	Unplated 1 oz Cu	P	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 7	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 8	Unplated 2 oz Cu	P	2.6	mils
	Core		4	mil core - 1 ply 2116
Layer 9	Unplated 2 oz Cu	P	2.6	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 10	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 11	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 12	Unplated 2 oz Cu	P	2.6	mils
	Core		4	mil core - 1 ply 2116
Layer 13	Unplated 2 oz Cu	P	2.6	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 14	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 15	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 16	Unplated 2 oz Cu	P	2.6	mils
	Core		4	mil core - 1 ply 2116
Layer 17	Unplated 2 oz Cu	P	2.6	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 18	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 19	Unplated 1 oz Cu	P	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 20	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 21	Unplated 1 oz Cu	P	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 22	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 23	Unplated 1 oz Cu	P	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 24	Plated 1/2 oz Cu	S	1.6	mils

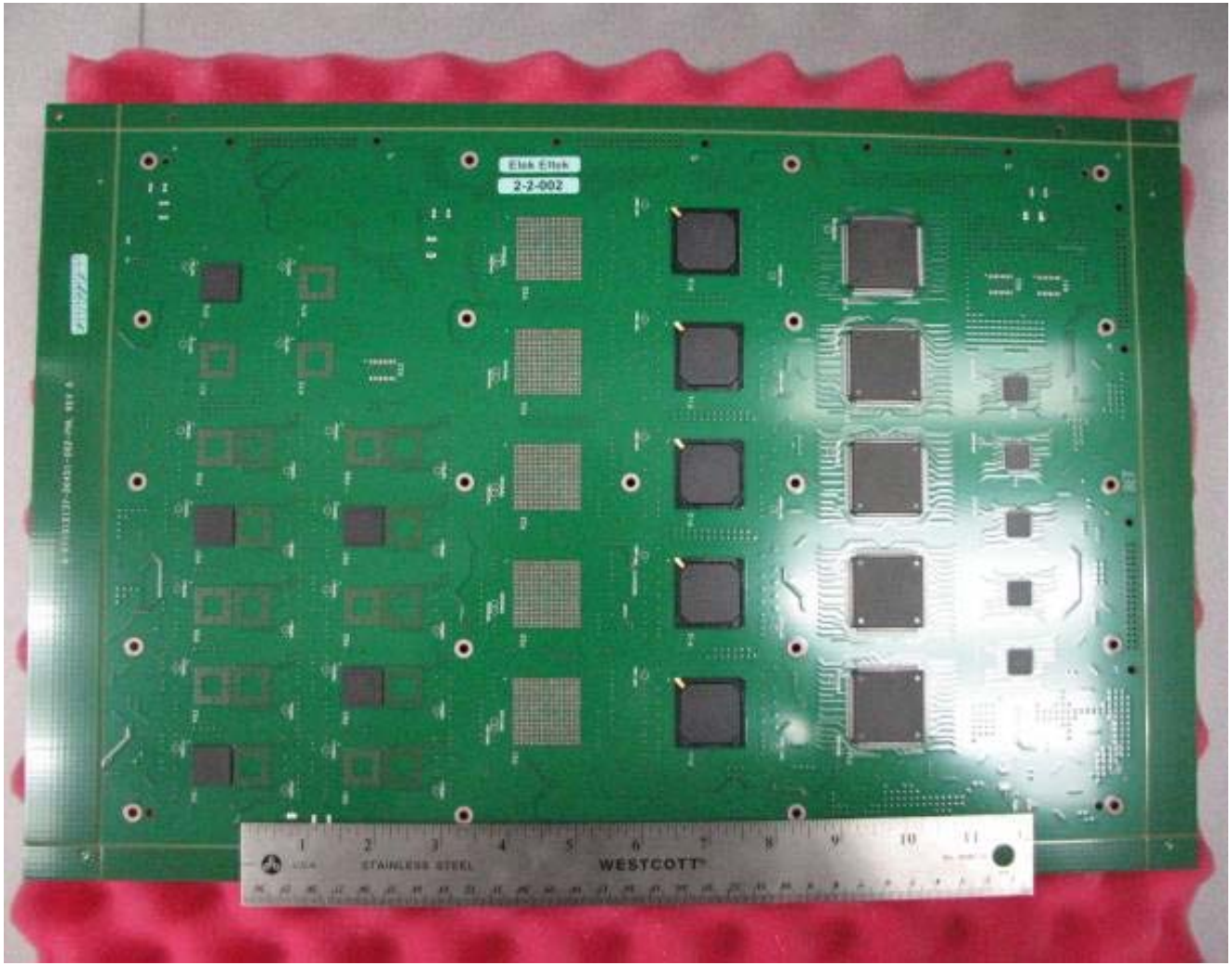
131.7

MEB 93 Stackup

	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu	S	1.6	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 2	Unplated 1 oz Cu	P	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 3	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 4	Unplated 1 oz Cu	P	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 5	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 6	Unplated 1 oz Cu	P	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 7	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 8	Unplated 2 oz Cu	P	2.6	mils
	Core		4	mils - 1 ply 2116
Layer 9	Unplated 2 oz Cu	P	2.6	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 10	Unplated 2 oz Cu	P	2.6	mils
	Core		4	mils - 1 ply 2116
Layer 11	Unplated 2 oz Cu	P	2.6	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 12	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 13	Unplated 1 oz Cu	P	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 14	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 15	Unplated 1 oz Cu	P	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 16	Unplated 1 oz Cu	S	1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 17	Unplated 1 oz Cu	P	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 18	Plated 1/2 oz Cu	S	1.6	mils

95.7

Agilent Test Board



Components	Quantity
BGA388T1.0C-DC264D	5
BGA208T.8C-DC170D	5
QFP120T30T3.2-DE-D	5
MLF68T.5-T-DE-D	5

Stencil Information

Thickness: 5 mils
Type: Laser Cut
Aperture Size:
BGA208 – Round 15.000 mil
BGA388 – Round 20.000 mil
QFP120 – Rectangle 15.000 mil x 75.000 mil
QFN 68 – Oblong 9.000 mil x 37.000 mil

Paste

OM338PT (Type 3)

Agilent Stack-up

Agilent Stackup

	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu	S	1.6	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 2	Unplated 1 oz Cu	S	1.3	mils
	Core		5	mil core - 1 ply 2116
Layer 3	Unplated 1 oz Cu	P	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 4	Unplated 1 oz Cu	S	1.3	mils
	Core		5	mil core - 1 ply 2116
Layer 5	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 6	Unplated 2 oz Cu	P	2.6	mils
	Core		5	mil core - 1 ply 2116
Layer 7	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 8	Unplated 1 oz Cu	P	1.3	mils
	Core		5	mil core - 1 ply 2116
Layer 9	Unplated 2 oz Cu	P	2.6	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 10	Unplated 1 oz Cu	S	1.3	mils
	Core		5	mil core - 1 ply 2116
Layer 11	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 12	Unplated 2 oz Cu	P	2.6	mils
	Core		5	mil core - 1 ply 2116
Layer 13	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 14	Unplated 1 oz Cu	S	1.3	mils
	Core		5	mil core - 1 ply 2116
Layer 15	Unplated 2 oz Cu	P	2.6	mils
	Prepreg		4.5	mils - 2 ply 1080
Layer 16	Unplated 1 oz Cu	S	1.3	mils
	Core		5	mil core - 1 ply 2116
Layer 17	Unplated 1 oz Cu	S	1.3	Mils
	Core		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 18	Unplated 1 oz Cu	P	1.3	mils
	Core		5	mil core - 1 ply 2116
Layer 19	Unplated 1 oz Cu	S	1.3	mils
	Prepreg		3.5	mils - 1 ply 2113 or 3313 or 2112
Layer 20	Plated 1/2 oz Cu	S	1.6	mils

115.8

iNEMI BFR-Free High Reliability PCB Project - TV Assembly Status

Materials Chosen For Evaluation	MEB 0.093”	MEB 0.125”	Agilent TV
A	Complete	Complete	Complete
B	Complete	Complete	Complete
C	Complete	Complete	Complete
D	Complete	Complete	Complete
E	Complete	Complete	Complete
F	Complete	Complete	Complete
G	Complete	Complete	Complete
H (Control)	Complete	Complete	Complete
I	Complete	Complete	Complete

Assembly Conditions at Celestica

18 layer 0.093” MEB:
- 6 panels @ 245C 6X
- 6 panels @ 245C 10X
- 6 panels @ 260C 6X
- 6 panels @ 260C 10X
- 6 panels – no reflow conditioning

24 layer 0.125” MEB:
- 6 panels @ 245C 6X
- 6 panels @ 245C 10X
- 18 panels – no reflow conditioning

20 layer 0.116” Agilent:
- 8 panels assembled with components @ 245C
- 5 panels bare @ 245C 6X
- 5 panels no reflow conditioning

iNEMI BFR-Free High Reliability PCB Project
MEB Test Status

Material / Stackup	A		B		C		D		E		F		G		I		H (Control)	
	.093	.125	.093	.125	.093	.125	.093	.125	.093	.125	.093	.125	.093	.125	.093	.125	.093	.125
IST - Intel	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
CAF – Doosan/Intel	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
Flex Mod - Doosan	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
Tg / z- CTE - Doosan	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
Solder Float - ITEQ	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
Dk & Total Loss up to 30GHz - Intel	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
Moisture Diffusivity Insertion Loss - Intel	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1	3/1
Drill Reg - Intel	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
HATS - IBM	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
Board Side Ball Pull - Intel	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Not started

In Process

Complete

Moisture Diffusivity testing to complete in March by Intel

iNEMI BFR-Free High Reliability PCB Project
MEB Test Parameters

IST – IPC TM-650-2.6.26, 10% resistance change cycled RT to 150C to a maximum cycle count of 1000.

CAF – IPC-TM-650-2.5.25.1

1) Stabilize samples for 24 hours at 23C and 50%RH
2) Perform initial measurements
3) Precondition samples for 96 hours at test temp and humidity
4) Apply bias and perform Insulation Resistance (IR) measurements for 1000 hrs

Test Site	Test Temp	Test Humidity	Test Voltage
Doosan	85C	85%	100V DC
Intel	85C	85%	80V DC

The testing differences at Doosan and Intel were as follows:

Flex Modulus – ASTM D790 procedure. Test samples in X and Y direction

Instrument: Instron 4202
Specimen dimension: 75 mm X 32 mm
Fixture: 3 point bending
Span: 38.4mm
Crosshead speed: 0.45mm/min

iNEMI BFR-Free High Reliability PCB Project
MEB Test Parameters

Tg/ Z-CTE – IPC-TM-650-2.4.24

- **Instrument: TMA 2940**
- **Specimen dimension: 6.35mm X 6.35mm**
- **Mode: Expansion**
- **Preconditioning: for 2hrs at 105℃**
- **Program: Ramp 10℃/min to 200℃, isothermal 5min, and ramp 5℃/min to 280℃**

Solder Float – IPC TM-650-2.6.8 Test Condition A (288C for 10 sec) repeat to 6X

Dk and Total Loss – S parameter extraction

- **Instrument: Agilent E8364B Performance Network Analyzer**
- **Specimen dimension: 5 mil nominal trace, 5 inches long**
- **Test structures: Microstrip (Layer 1 to 2, no soldermask), Microstrip (Layer 1 to 2, soldermask), and Stripline (Layer 2 to 1 and 3)**
- **Frequency Range: 10MHz to 50GHz**

Moisture Diffusivity – S parameter extraction

- **Instruments: Espec ECL 2CA Temperature Humidity chamber and HP 8510C VNA**
- **Test structures: 5 mil nominal trace as microstrip and embedded microstrip every layer**
- **Frequency Range: 10MHz to 20GHz**
- **Test Conditions: 1) initial readings, 2) soak at 35C/85% RH until readings reach asymptotic state, 3) dry bake at 105C/0%RH until readings reach asymptotic state, 4) soak at 85C/85%RH until readings reach asymptotic state, and 5) dry bake at 105C/0%RH until readings reach asymptotic state.**

iNEMI BFR-Free High Reliability PCB Project
MEB Test Parameters

Drill Registration – Electrical test Beep test coupon by layer

HATS – Modified IPC TM-650-2.6.7, 10% resistance change cycled -45C to 145C to a maximum cycle count of 500.

- **Instrument: ITRS HATS Tester**
- **Specimen: In-line and offset 10 mil via daisy chains at 18 and 22 mil via to via spacing**

Ball Pull – IPC 9708 Test Standard (Ball Pull Method).

- **Instrument: Dage 4000 with 5Kg Ball Pull cartridge and 750um jaw**
- **Specimen: 20 mil SAC 405 Ball on 16 mil nominal diameter PCB pad**
- **Test Parameters: 23psi clamp pressure, 1 sec jaw closing time, 5mm/sec pull speed**

iNEMI BFR-Free High Reliability PCB Project – Agilent Bd

MATERIAL	A	B	C	D	E	F	G	I	H (Control)
Monotonic Bend and FA – IST	Complete	Complete	Complete	Complete	Complete	Complete	Complete	Complete	Complete
HALT and FA - HP	Update	Update	Update	Update	Update	Update	Update	Update	Update
Aging - HP	Complete	Complete	Complete	Complete	Complete	Complete	Complete	Complete	Complete

HALT testing & FA update: Intel shipped 1 of each material type (aged board) to HP for initial testing week of Feb 20th. Completion Date TBD.

Aging for the Agilent RTV boards was performed at HP with the following equipment / conditions :

- **Equipment:** Thermotron Environmental Test Chamber
- **Model:** SMX-64-705-705
- **Capacity:** 64 ft^3
- **Capability:** -87° C - 190° C; 20% - 95% RH

Aging conditions: Isothermal @ 85° C w/humidity @85%RH, stressed for 496 hours (20.7 days)

iNEMI BFR-Free High Reliability PCB Project – Agilent Bd Testing Procedures

Monotonic Bend : Modified IPC 9702 Test Standard (Bare Board Test)

- **Equipment: Load Frame**
- **Strain Gauge: KYOWA KFG-02-120-C1-11L3M2R**
- **Gauge Specifics: Factor – 2.18 ± 1%, Resistance - 119.6±0.4 Ω**
- **Test Conditions:**
  - **Global PWB strain-rate:5000μstrain/sec**
  - **Load Span:100 mm**
  - **Support Span: 200 mm**
- **Monitor resistance of nets 1 and 4 for failure (open circuit)**

HALT Testing Profile Conditions:

1. **Ambient temp and no vibration (starting point) – 25C**
2. **Vibration ramp step with dwell – each step 2.4 GRMS increase with 5 minute dwell**
3. **Cold ramp step with dwell – each step -3C decrease with 15 minute dwell**
4. **Hot ramp step with dwell – each step 3C increase with 15 min dwell**
5. **Return to ambient ramp with no dwell**
6. **Repeat steps 2 through 5 for 25 steps to 60 GMRS, -50C, and 100C endpoint. Monitor package/ PCB daisy chains for failure.**

Project Timeline

Milestone	Date
• Complete all remaining MEB testing	March 2012
• Complete testing on Agilent Board	Addendum
• Write Final report	April, 2012
• iNEMI Webinar	May, 2012

An Investigation to Identify Technology Limitations Involved in Transitioning to HFR-Free PCB Materials

- John Davignon,
- Intel Corporation

iNEMI HFR-Free Signal Integrity Project: *An Investigation to Identify Degradation of Electrical Signals in HFR-Free PCB Materials*

Stephen Tisdale (Intel)
Stephen Hall (Intel)
Mike Leddige (Intel)
John Davignon (Intel)

David Senk (Cisco)
Scott Hinaga (Cisco)

January, 2012

Agenda

- iNEMI Halogen Free Consortium
- Drivers
- SI Overview
- WG Strategy
- Conclusions

Problem

- To meet market demands for “Green technology”, the electronics industry are removing halogenated flame retardants (HFRs) from FR4 based printed circuit boards (PCBs).

- Unfortunately, the thermo/mechanical & electrical properties of HFR-free PCBs tend to be meaningfully different to FR4 counterparts leading to …
    - Reduced electrical performance
    - Reduced thermo/mechanical performance
    - Supply chain and cost problems

To address these problems, the iNEMI HFR-free Leadership Project was initiated in early 2009

iNEMI Consortium

- The iNEMI HFR-free Leadership Project was initiated in February 2009 to align the industry on strategy to mitigate problems with designing client platforms using HFR-free PCBs.

iNEMI is a non-profit R&D consortium with wide membership from electronic industry

Mission: Forecast & accelerate improvements in the electronics manufacturing industry

Stephen Tisdale-Chair HFR-Free Leadership Program

HFR-Free PCB Materials (John Davignon)

Thermo/Mechanical properties

HFR-Free Signal Integrity (Stephen Hall / David Senk)

Electrical performance

This presentation focuses on the Signal Integrity WG

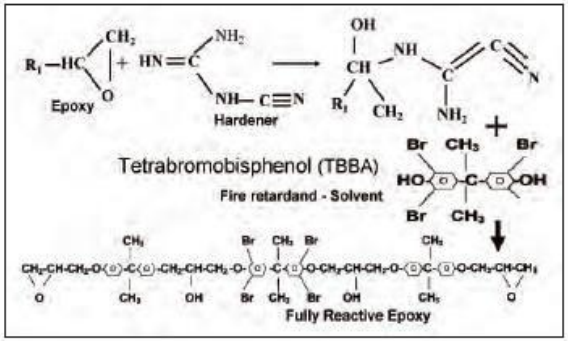
Signal Integrity WG: 16 Participating Members

"Critical Mass" of OEMs & Laminate manufactures was achieved to influence the industry

DRIVERS

Halogenated-Flame Retardants (HFRs) in PCBs

The Good: The addition of HFR's in FR4 are low cost & effective Flame retardant



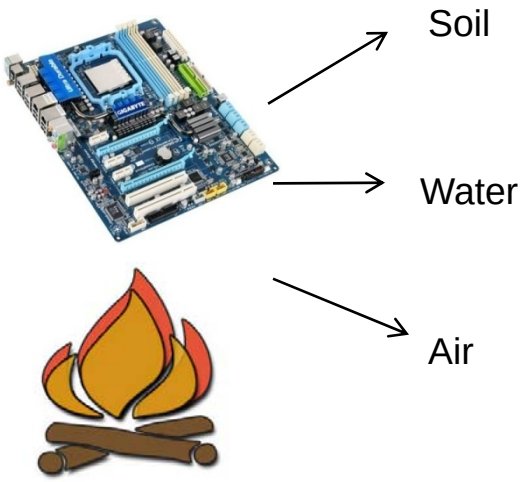
Tetrabromobisphenol-A (TBBA) is the flame retardant used in FR4

- TBBA Volatilizes at burning temperatures & blankets the fire, excluding oxygen

The Bad: HFRs are an environmental health hazard when disposed of improperly

- Yearly 20–50 million tons of E-wastes generated worldwide – Most contain HFRs
- Dioxins are released during improper EOL burning / recycling

Pollution in:



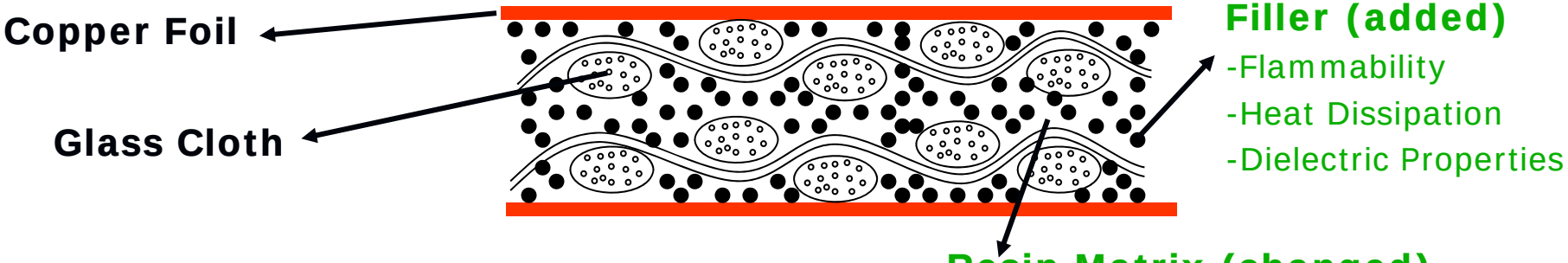
The Ugly: FR4 is a cornerstone of the electronic industry.

- Changes could impact performance, supply chain & cost

Drivers to eliminate HFRs:

- Global Environmental Responsibility
- Threat of legislation (Not likely but still possible)
- Pressure from Non-Governmental Organizations

Halogen-free PCB - What is different?



3-major types of HFR-free Flame Retardants in PCBs

- ✓ **Organophosphates** – Forms a carbonized layer to cover surface
- ✓ **Nitrogen Compounds** - Generates incombustible gas
- ✓ **Metal Hydroxides** - Releases water at high temperature

Each manufacturer has its own "recipe" for HFR-free PCB

- ✓ No standardization which complicates design
- ✓ Each recipe has unique properties

Wide variety of recipes leads to a dependency on specific materials from a few manufactures

SIGNAL INTEGRITY ON HFR-FREE PCBs

Problem

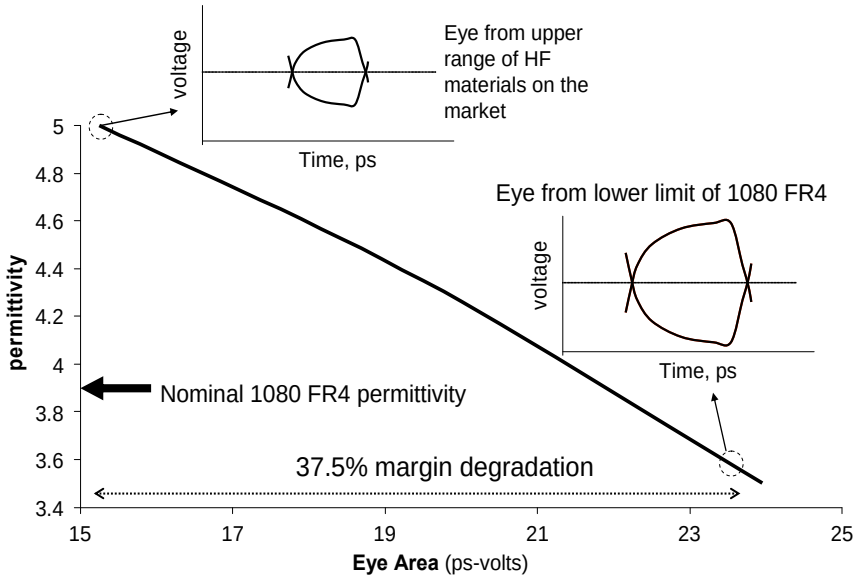
The critical electrical properties of many available HFR-free dielectrics make high-speed bus design problematic without increasing the cost of the system

WG Goal

Align the industry on a common strategy to eliminate any roadblocks to high-speed bus design using HFR-free PCBs

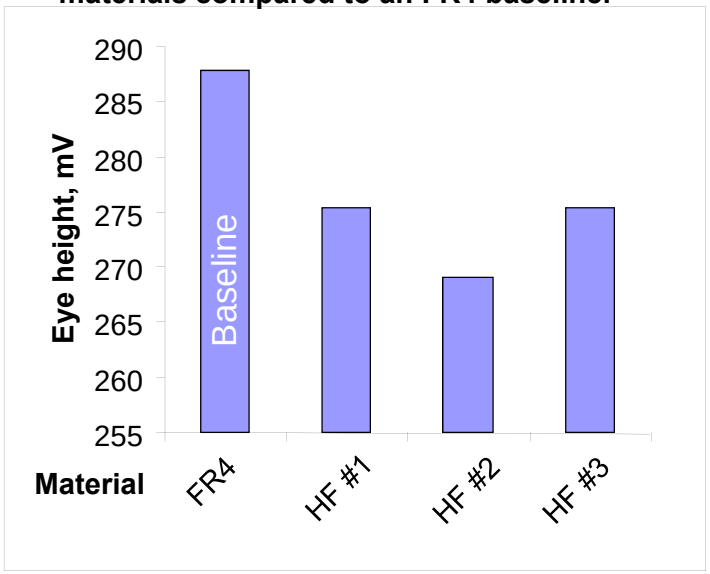
Performance of HFR-free PCB vs FR4

- ✓ **HFR-free PCB materials on the market tend to have higher permittivity values than FR4**
  - ✓ HFR-free Dk ~ 4.2 – 5.0 (1080)
  - ✓ FR4 Dk ~ 3.6-3.9 (1080)



Simulation of 1DPC DDR Bus

Measured DDR3 margin degradation caused by 3 HFR-free materials compared to an FR4 baseline.



- ✓ **Higher permittivity reduces bus performance**
  - Thicker layers at same Z_0 increases crosstalk
  - High crosstalk drives increased trace separation & more layers
  - PCB cost increase per layer ~ proportional to increased area (~50% 4L→6L)

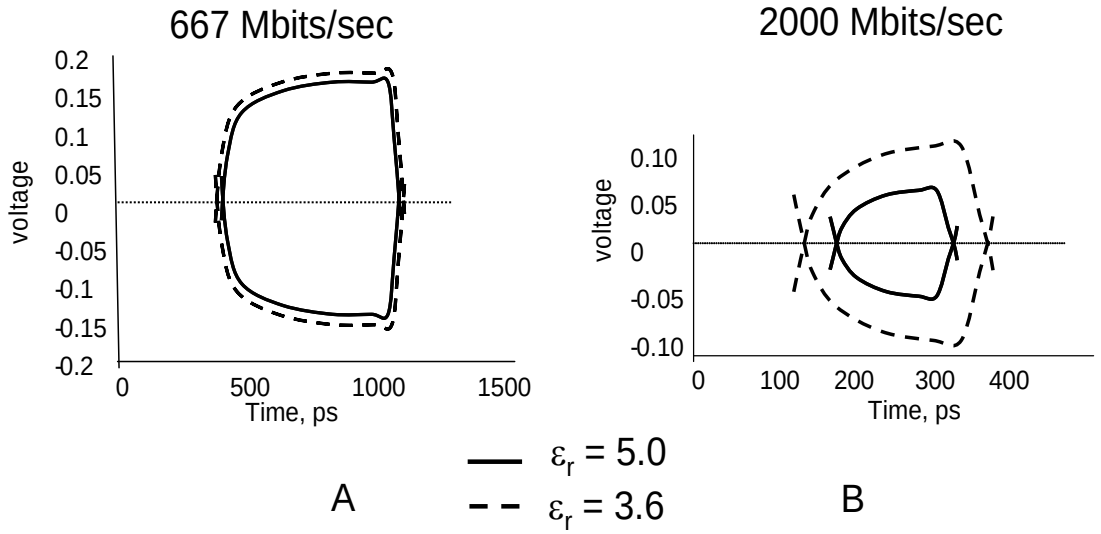
HFR-free PCBs can pose challenges to high speed bus design

Scaling HFR-free bus speeds

- ✓ **Margin reduction gets *worse* for faster buses**
  - HFR-free materials with high permittivity are adequate for lower speed buses, but are problematic at higher speeds

High permittivity values may be adequate for low-speed bus designs, but substantially degrade high-speed bus performance

Example: Simulation of simplified DDR 1DPC bus over extreme HF/FR4 permittivity range



HFR-free PCBs can make it difficult for buses to scale with Moore's Law

Solving the problem – 4-tier approach

1. Identify common critical electrical parameters
2. Define common performance limits
3. HFR-free design data base
4. Communicate industry needs to laminate suppliers

- ✓ **Not an "industry standard" or "spec" approach**
  - No consensus for spec development
- ✓ **Requires "*critical mass*" of industry heavy hitters**
- ✓ **Tell the laminate manufactures what "*we*" want as an industry so "*they*" will build it**

Approach designed to "voluntarily" get industry on the HFR-bandwagon before legislation forces it

iNEMI HF Signal Integrity WG Strategy

1. Identify common critical electrical parameters

Parameter	Other names	Design influences
Permittivity	Dk, ε_r, dielectric constant	Characteristic impedance, Propagation velocity, crosstalk
Loss tangent	Df, tanδ, dissipation factor	Signal attenuation
Moisture absorption	Environmental effects, humidity	When dielectric materials absorb water, Dk & Df increase.

Industry agreement on critical parameters gives us a set of metrics to make material choices

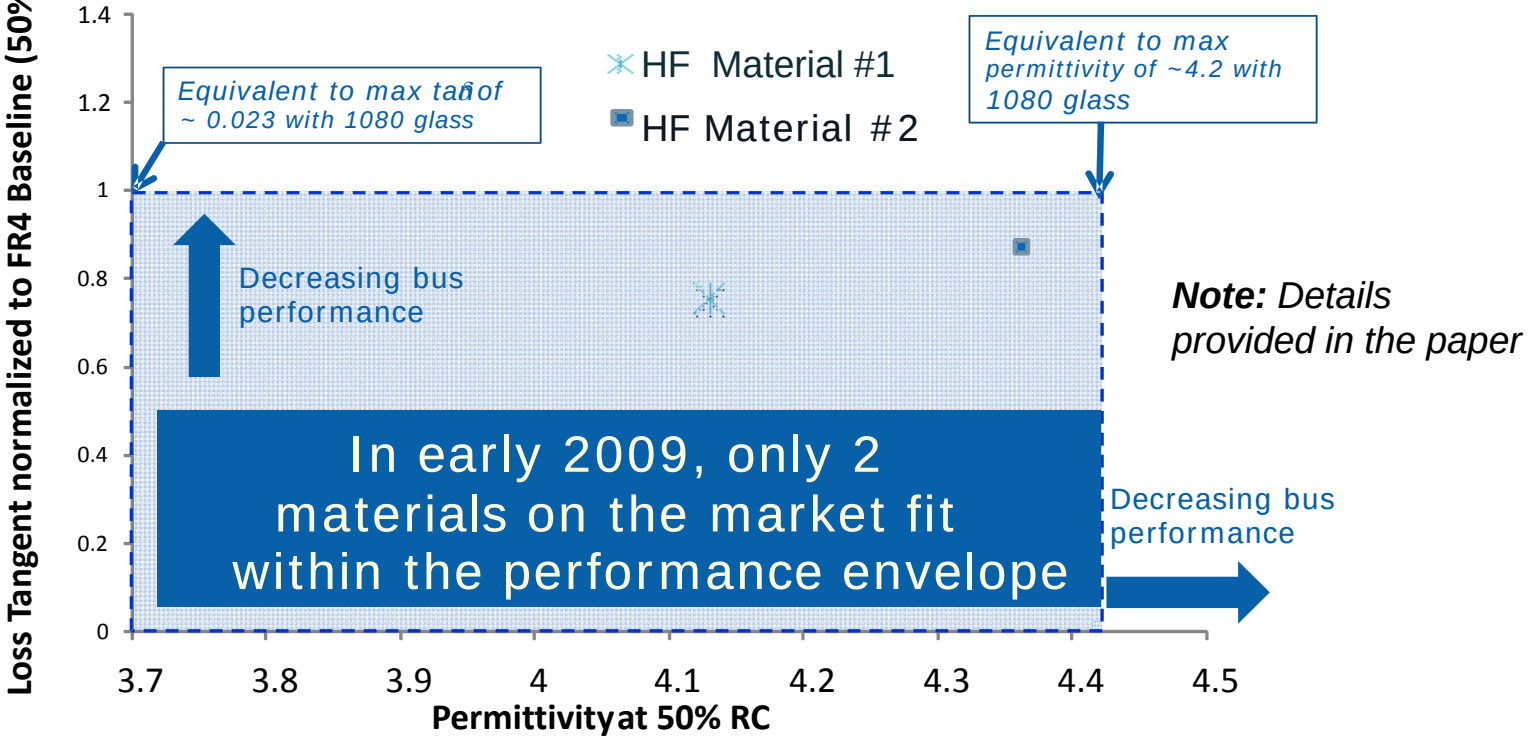
iNEMI HF Signal Integrity WG Strategy

2. Define common performance limits

For performance ≥ FR4, what are the electrical limits? →
Focus on high-speed buses

Example: HFR-free PCB Performance Limits

***(50% Resin Content**, 95% RH, 95°F, Normalized loss of 1.0 = average loss tangent of 3 FR4 baseline samples)*



***Note:** Details provided in the paper*

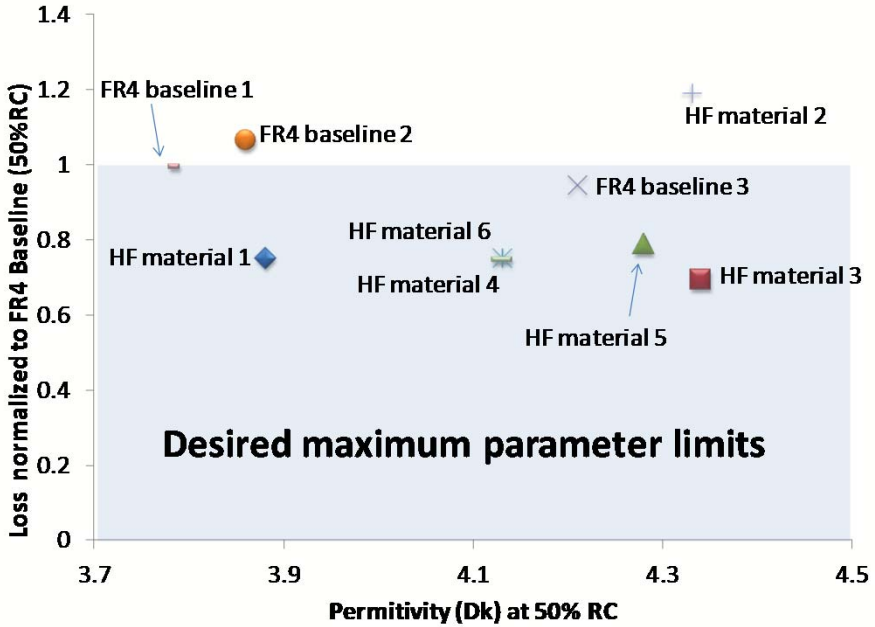
WG aligned on performance limits, providing requirements to laminators

iNEMI HF Signal Integrity WG Strategy

3. HFR-free design data base

Database helps members choose adequate materials

Test board measurements extrapolated to 50% Resin Content (RC) & mapped onto the desired properties;



Helps cements minimum performance message to laminate companies

- ✓ 7 member labs provided measurements
- ✓ 6 member laminate manufactures provided test boards

Note: *Values Reported at 50% RH, 21oC, 5 GHz, each data point is average of 15-25 data points from 3-5 samples at 5 separate labs*

Number of high-speed HF materials identified increased from 2 to 5

iNEMI HF Signal Integrity WG Strategy

4. Communicate industry needs to laminate suppliers

If a critical mass says “we want it” then “they will build it” → **increases supply & reduces cost**

Most important step → seeds the supply chain

- ✓Formally delivered “electrical requirements” to member laminators
- ✓Provided compliance test method for electrical requirements (*members only*)
- ✓Number of *compliant* materials increased from 2 to 5

The WG helped achieve industry momentum to ensure high performance HFR-free materials will continue to be developed

Summary

- ✓ **The WG has united a "critical mass" of the industry on …**
  1) the problems with designing high-speed buses with HFR-free PCB's
  2) a unified approach to mitigate the challenges
- ✓ **Established desired performance limits to remove signaling roadblocks from buses designed on HFR-free PCBs**
- ✓ **Delivered a design database & methodology to facilitate design choices between HFR-free materials**
  1. Helps member companies choose HFR-free materials
  2. Reinforces the limits needed by the industry to member laminators

The WG has paved the way for the industry to produce Environmentally Friendly Products with HFR-free Materials

An Investigation to Identify Degradation of Electrical Signals in HFR-Free PCB Materials

•Stephen Hall, Intel Corporation

An Investigation to Identify Technology Limitations Involved in Transitioning to HFR-Free PCB Materials

iNEMI HFR-Free Leadership Program

Program Manager: Stephen Tisdale, Intel

HFR-Free PCB Materials

Chair: John Davignon, Intel

Presented at APEX 2012, Feb 29, 2012

Agenda

- ***Introduction/Objectives***
- ***Strategy/Industry Concerns***
- ***Test Suite Methodology***
- ***Test Method Results (9 laminates)***
- ***Suppliers Capacity***
- ***Summary /Conclusions***

Introduction

The Industry is transitioning towards environmentally responsible designs and the elimination of Halogenated Flame Retardants (HFR-Free) from their Printed Circuit Board (PCB)

Although there is no pending legislation to ban all Brominated Flame Retardants, NGO pressure continues (Green Meter etc)

The iNEMI HFR-Free Leadership WG has spent the last 2 years investigating Low Halogen laminates for the Client space.

This presentation outlines the results of the investigation for 6 HFR-Free and 3 Halogenated (BFR) laminates.

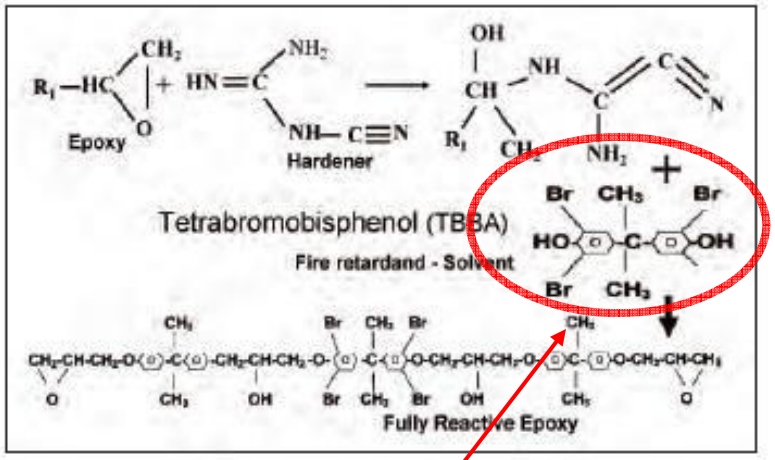
Consortium Objective & Goals

Identify the technology readiness, supply chain capability, and reliability characteristics for "HFR-Free" alternatives to conventional printed circuit board materials and assemblies (electrical and mechanical properties)

- **Define technology limits for HFR-Free materials across all market segments with initial focus on client platforms (desktop, notebook) in 2011 timeframe**
- **Define and implement quantifiable data into the HFR-Free Laminate Suppliers Datasheets that will assist in material selection by users**
- **Define a "Test Suite Methodology" which meets the quality and reliability requirements of the chosen market segments**
- **Ensure the Industry Laminate Suppliers have the capability and capacity to support the industry HFR-Free laminate requirements**

HFR-Free - What Changed in the Transition?

Low-Halogen changes the flame retardant used for epoxy laminate (FR4) materials



Phosphorous Compound	Nitrogen Compound	Inorganic Fillers (metal hydroxide)
Formation of carbonized layer to cover surface	Generating incombustible gas	Releasing water at high temperature
Additive type: Phosphorous compound Reactive type: Phosphate	Reactive type	Additive

Tetrabromo bisphenol-A (TBBPA) is the current halogenated flame retardant for all laminate epoxy systems

New non-Halogenated flame retardants are varied in both material types and percentages

HFR-Free PCB laminates contain reactive and additive components

iNEMI HFR-Free PCB Materials WG Strategy

1. Define Initial Areas of Concern (27 areas generated)
2. Define Metrologies & Test Methods to quantify these Material Properties at Laminate Supplier
3. Design Test Structures and Test Suite Construction/Lay up
4. Test and Evaluate Coupon design, metrology and performance (POC)
5. Build TV's with the 9 chosen laminates, test and evaluate performance
6. Incorporate "Tech Suite Methodology" into laminate datasheets
7. Work with Supply Chain to verify Capacity of Laminate Supply
8. Deliver the Test Suite and Test Methods to the Industry

PCB Materials Industry 27 Areas of Concerns

	Basic Materials Properties	*Rating*
1	Micro and macro hardness	
2	Glass transition temperature (Tg)	
3	Decomposition temperature (Td)	
4	Moisture absorption	
5	Fracture Toughness of Resin / Resin Cohesive Strength	
6	Stiffness	
7	Dk & Df	
8	Coefficient of thermal expansion (z-axis and x-, y-axes)	
9	Flexural strength	
	Thermo-Mechanical Performance	
10	Pad Cratering (brittle fracture)	
11	Shock & Vibe and Drop test data	
12	Transient Bend	
13	Copper Pad Adhesion (CBP/Hot Pin Pull/ Shear or Tensile)	
14	CAF resistance	
15	Long term life prediction, such as IST or thermal shock test.	
16	Plastic and elastic deformation characteristics	
17	Co-Planarity Warpage characteristics	
18	Delamination characteristics under stress conditions	
	Process/Manufacturing	
19	PCB fabrication process, drill wear, lamination & desmear	
20	Punchability/Scoring/Breakoff Performance	
	Assembly Process	
21	Lead Free Reflow Test	
22	Rework (Pad Peeling)	
	Other Concerns	
23	Resin system dependency/hardening/curing agents	
24	Affect of Fillers	
25	UL Fire ratings (V0-V1)	
26	Electrical Properties (UL CTI rating)	
27	MOT Maximum Operating Temperature	

Low	
Medium	
High	

27 Areas of Concern were defined and ranked according to Risk and / or Priority of the Concern by a broad section of the PCB Industry

iNEMI Test Suite Methodology (TSM)

Test Suite Methodology

- A single test method was chosen that related to one or more industry concerns and could give quantifiable values
- The test structures/coupons needed to complete the test method were designed
- A representative test board construction for the market segment under evaluation was developed (Notebook/Desktop)
- Testing was completed at several sites (2-3) and the data was combined

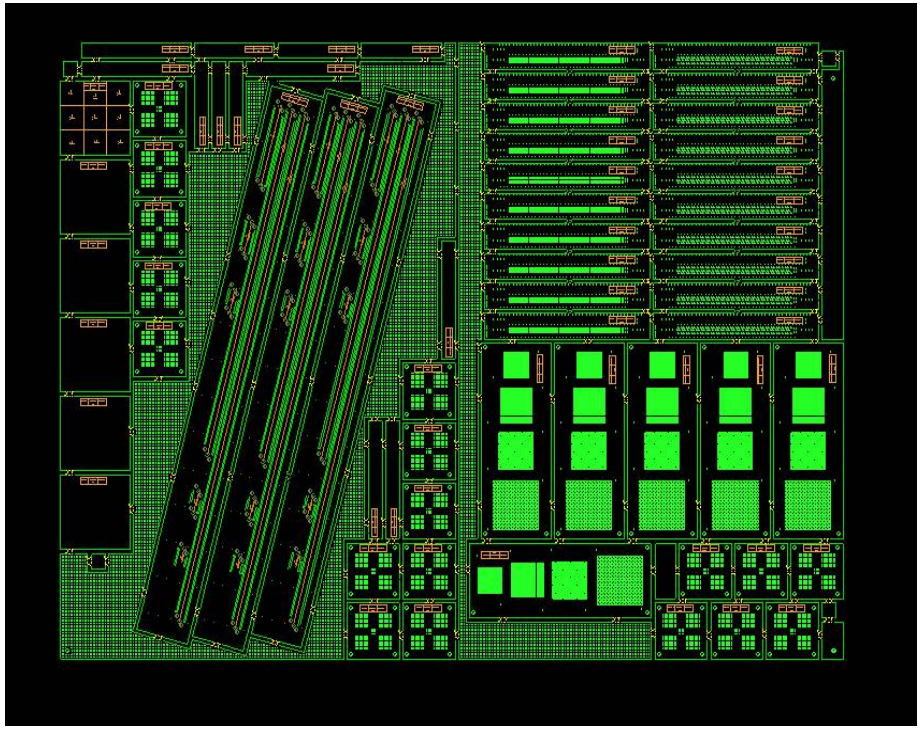
Test Methods Under Evaluation		
Glass Transition Temperature (Tg)		Stiffness/Flexural Strength
Decomposition Temperature (Td)		Rework (Pad Peeling)
Coefficient of Thermal Expansion (x,y,z)		Interconnect Stress Test (IST)
Moisture absorption		Conductive Anodic Filament (CAF)
Pad Adhesion (CBP/Hot Pin Pull)		Lead Free Reflow Test: Delamination
Permittivity (Dk)		Charpy Impact Test
Total Loss (Df)		Simulated Reflow Test

Test Suite Methodology

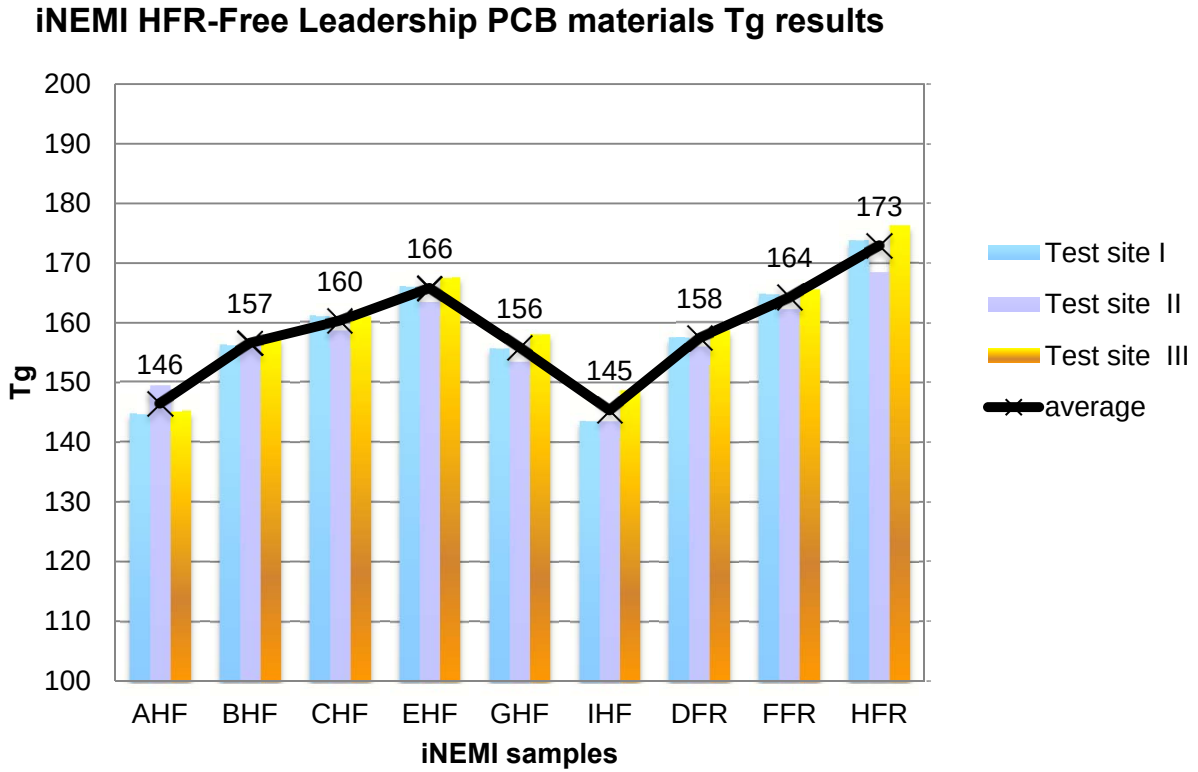
Stack up and test board layout

10 Layer Mobile Stack-up

	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu		1.6	mils
	Prepreg		3	mils - 1 ply 1080
Layer 2	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 3	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 4	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 5	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 6	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 7	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 8	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 9	Unplated 1 oz Cu		1.3	mils
	Prepreg		3	mils - 1 ply 1080
Layer 10	Plated 1/2 oz Cu		1.6	mils
			48.2	

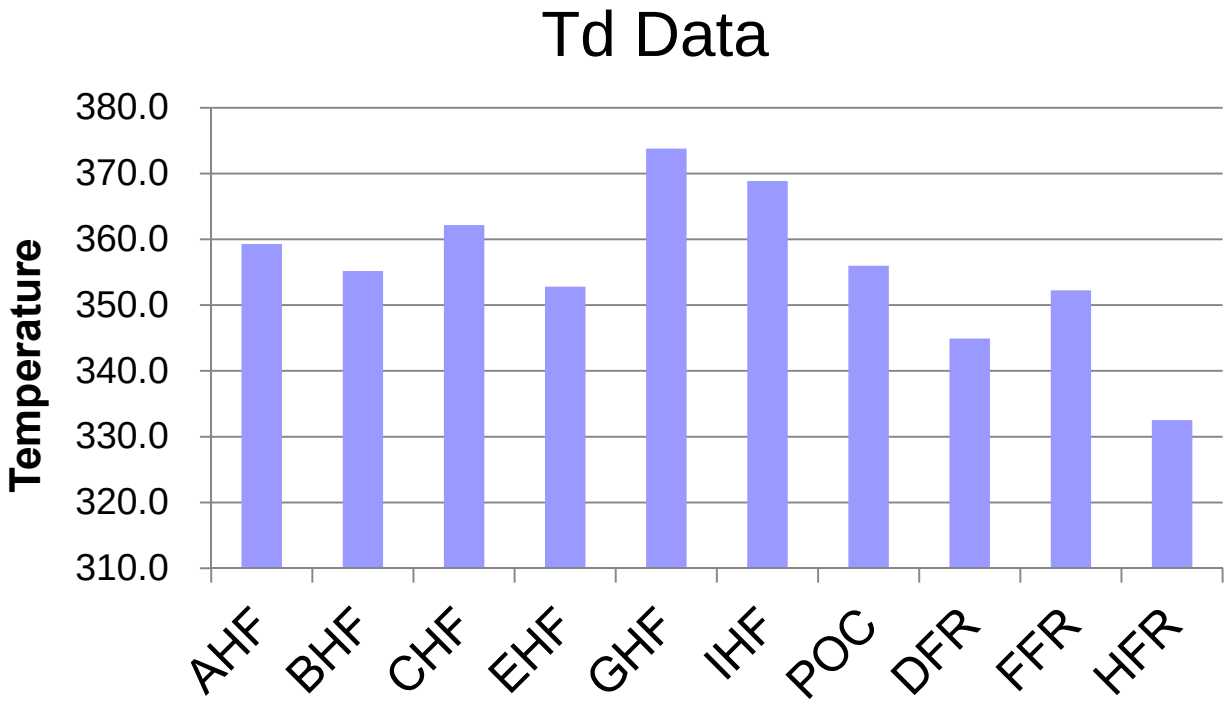


Test Methods Results for 9 Laminates
6 HFR-Free
3 BFR Baseline



Conclusions

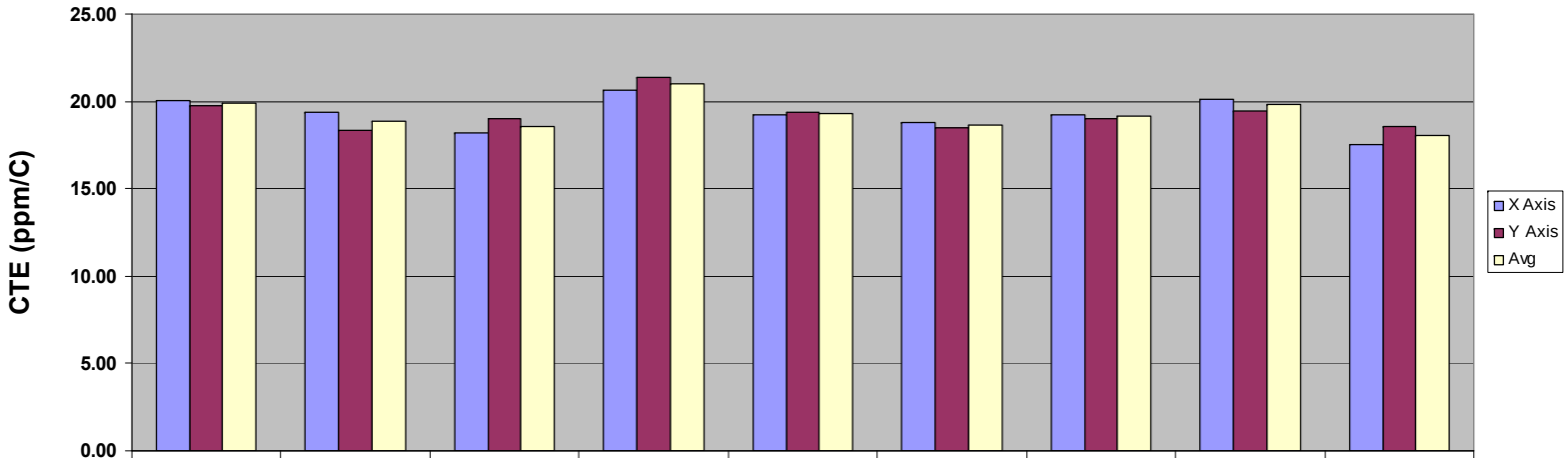
- The Tg of the laminates were within the acceptable range for the Client space (mid Tg). Tg is market sector dependent
- There is no indication that Tg is directly dependent on the Flame Retardant use in the polymer.



Conclusions

- **The Td values of HFR-Free material are significantly higher than those of the Halogenated laminates, reflecting the differences in chemistry between the two material classes**
- **HFR-Free materials are thermally more stable than the Halogenated materials**

CTE (X & Y Axis)



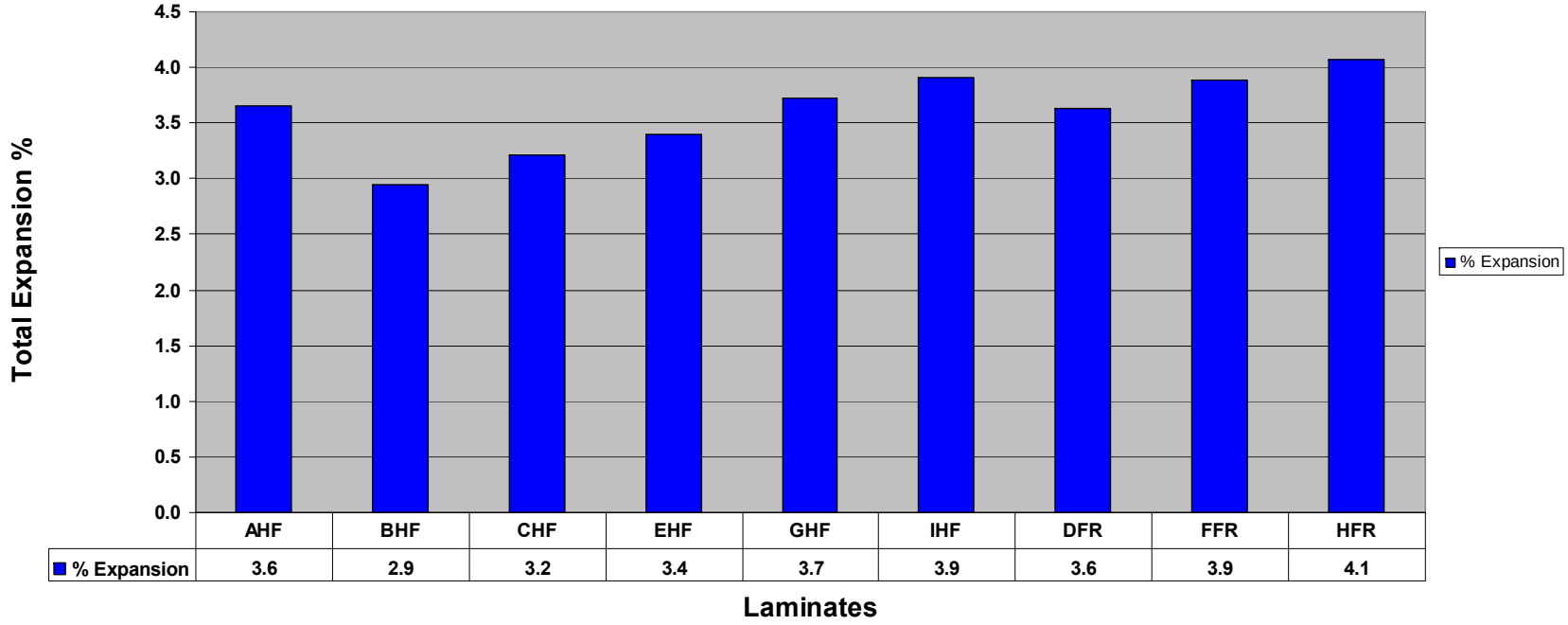
	AHF	BHF	CHF	EHF	GHF	IHF	DFR	FFR	HFR
X Axis	20.03	19.38	18.17	20.60	19.22	18.82	19.24	20.12	17.50
Y Axis	19.78	18.31	18.98	21.37	19.35	18.51	19.02	19.46	18.58
Avg	19.9	18.8	18.6	21.0	19.3	18.7	19.1	19.8	18.0

Laminates

Conclusions:

- **Average CTE measurements for HFR-Free materials are not significantly different from brominated FR4 materials**
- **CTE is most probably driven by the glass style used rather than resin class**

CTE Z Axis

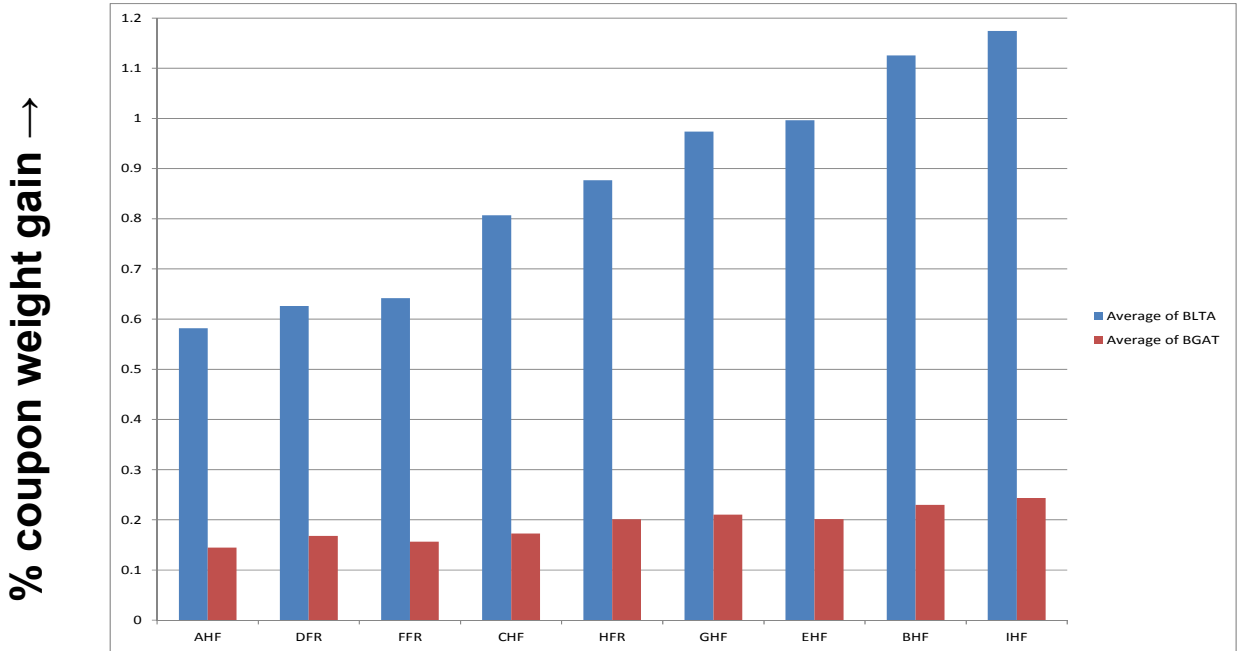


	AHF	BHF	CHF	EHF	GHF	IHF	DFR	FFR	HFR
% Expansion	3.6	2.9	3.2	3.4	3.7	3.9	3.6	3.9	4.1

Conclusions:

- **Average Z-axis total expansion is approximately 10% less for HFR-Free materials when compared with Brominated FR4.**
- **This lower CTE is attributed to the higher volume & types of fillers in HFR than FR4**
- **The overall average Z-axis HFR-Free CTE <Tg is 62 ppm/°C compared to 73 for FR4**
- **The overall average Z-axis HFR-Free CTE >Tg is 253 ppm/°C compared to 284 for FR4**

Average Total-Absorbed Moisture



	Bare Lam Total	Bare Lam Bonded	BGA Total	BGA Bonded
Max %	1.403	0.221	0.288	0.111
Min%	0.571	0.023	0.134	0.015

Conclusions:

- **HFR-Free has higher moisture absorption than FR4. (Testing did not go to saturation)**
- **Total absorbed moisture between HFR-Free & FR4 is significantly different**
- **Bonded moisture between bare HFR-Free & FR laminates is significantly different**

Initial 16 mil Pad Adhesion

Comparisons for all pairs using Tukey-Kramer HSD		
Level	Mean	Std-Dev
DFR	1412	89
CHF	1239	118
IHF	1184	99
HFR	1142	76
GHF	1129	55
FFR	1050	105
BHF	1048	84
AHF	929	90
EHF	900	117

Initial Vs. Reflow Delta

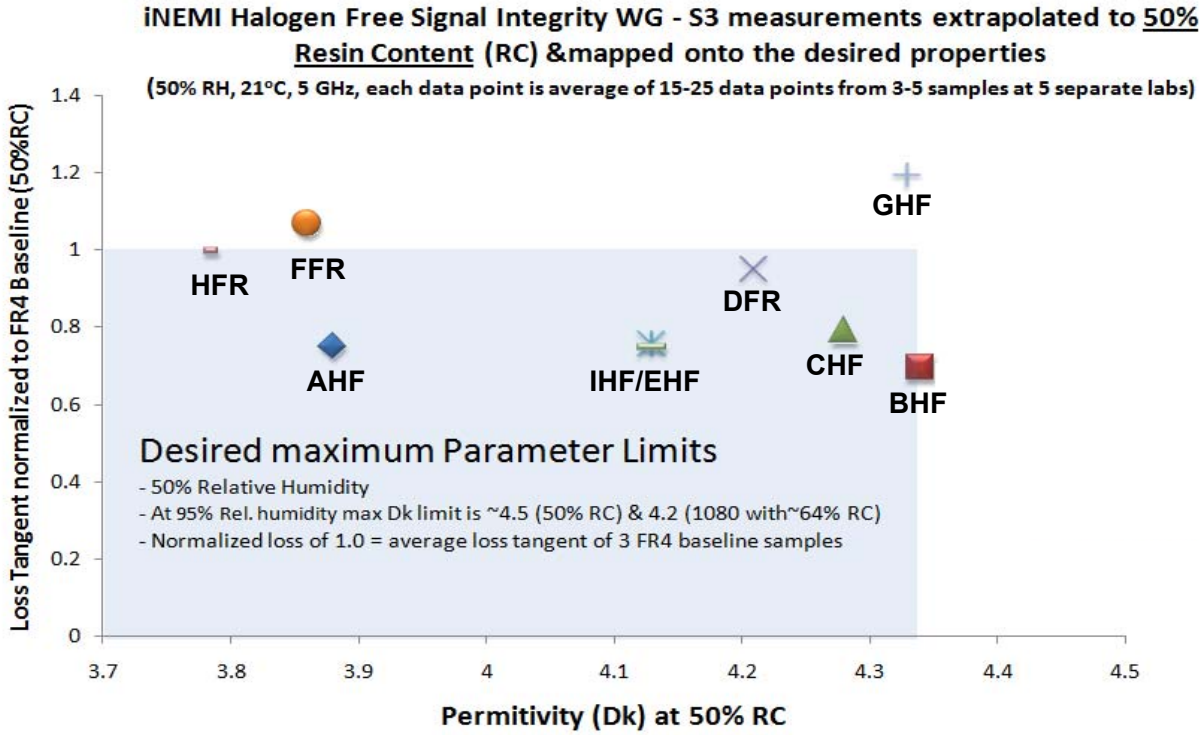
Level	Pull force Delta (PA-RWK)
DFR	118
CHF	136
IHF	167
HFR	28
GHF	71
FFR	34
BHF	2
AHF	49
EHF	92

After 6 x LF reflows

Comparisons for all pairs using Tukey-Kramer HSD		
Level	Mean	Std-Dev
DFR	1293	128
HFR	1170	73
CHF	1103	86
GHF	1058	100
BHF	1051	137
IHF	1017	111
FFR	1016	117
AHF	880	65
EHF	808	96

Conclusions:

- **The Cold Ball Pull Method (CBP) does differentiate materials but not material class. i.e. HFR-Free vs. FR4.**
- **Multiple reflows can slightly degrade the CBP force, but does not significantly alter the ranking of the materials.**
- **Cold Ball Pull method is very dependent upon the Ball Attach method and technique**



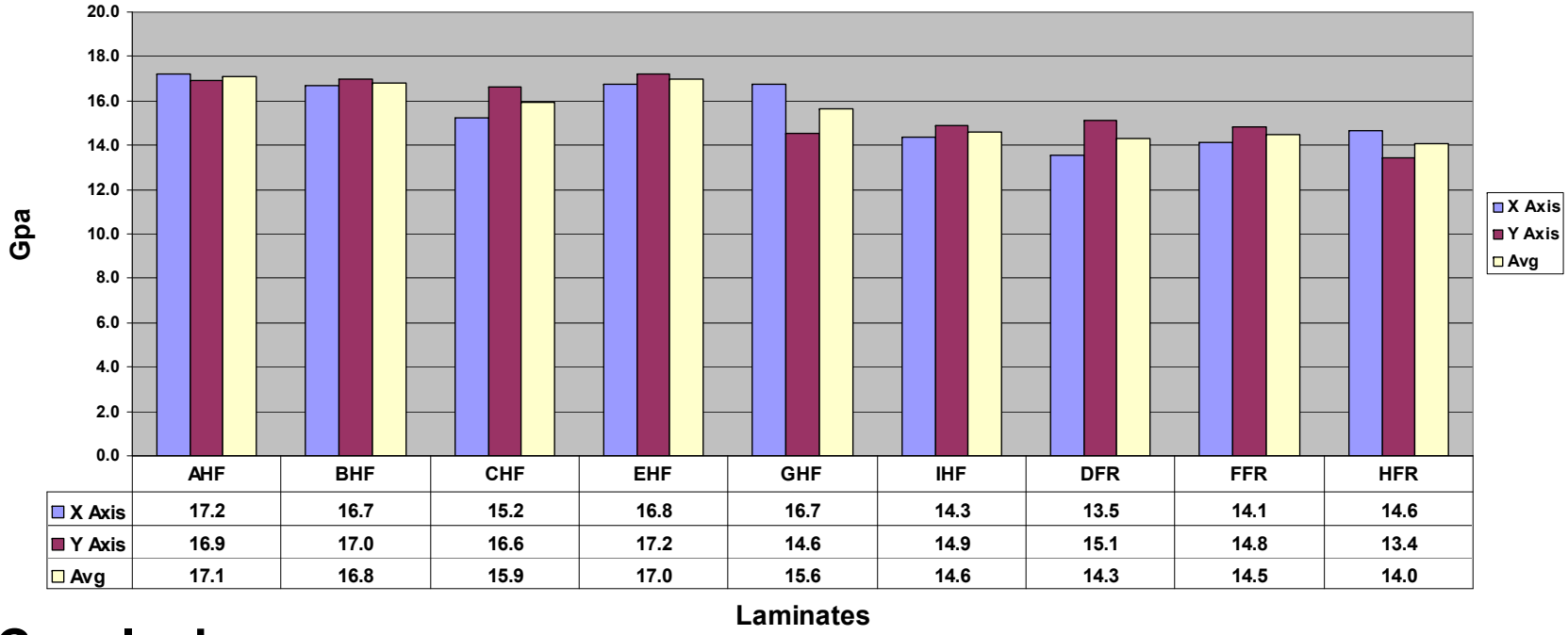
Consortium Dk/Df limits

- **Dk<4.35 at 50% resin content (RC) & 50% relative humidity (RH)**
- **Dk<4.35 at 50% RC & 95% RH**
- **Losses =< FR4 baseline at 50% RC & 50% RH**

Conclusions:

- **HFR-Free Laminates tend have increased permittivity (Dk) over FR4**
- **HFR-Free Laminates tend have decreased loss (Df) over FR4**
- **2011 Client Platforms simulation and preliminary validation suggests the defined envelope will meet the platform requirements with 5 out of 6 HFR-Free laminates tested**

Flex Modulus



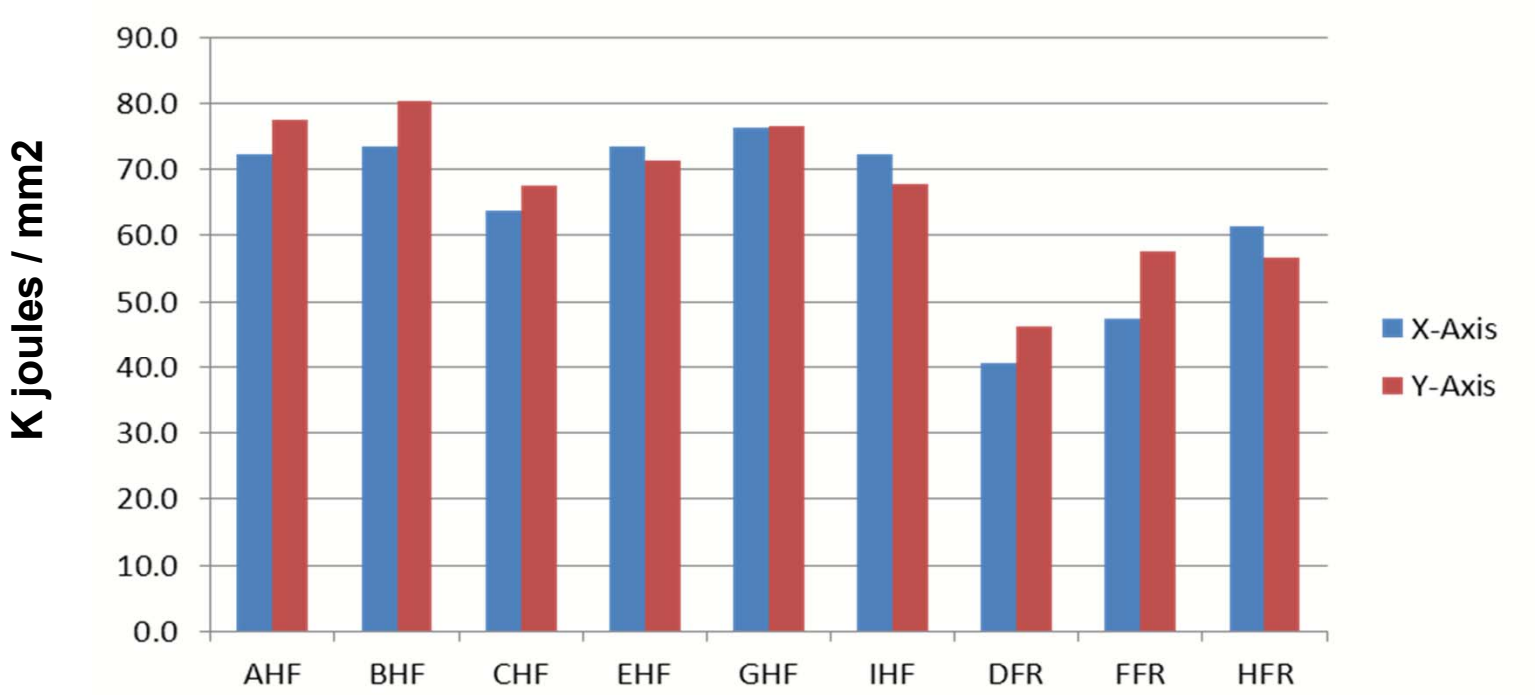
	AHF	BHF	CHF	EHF	GHF	IHF	DFR	FFR	HFR
X Axis	17.2	16.7	15.2	16.8	16.7	14.3	13.5	14.1	14.6
Y Axis	16.9	17.0	16.6	17.2	14.6	14.9	15.1	14.8	13.4
Avg	17.1	16.8	15.9	17.0	15.6	14.6	14.3	14.5	14.0

Laminates

Conclusions:

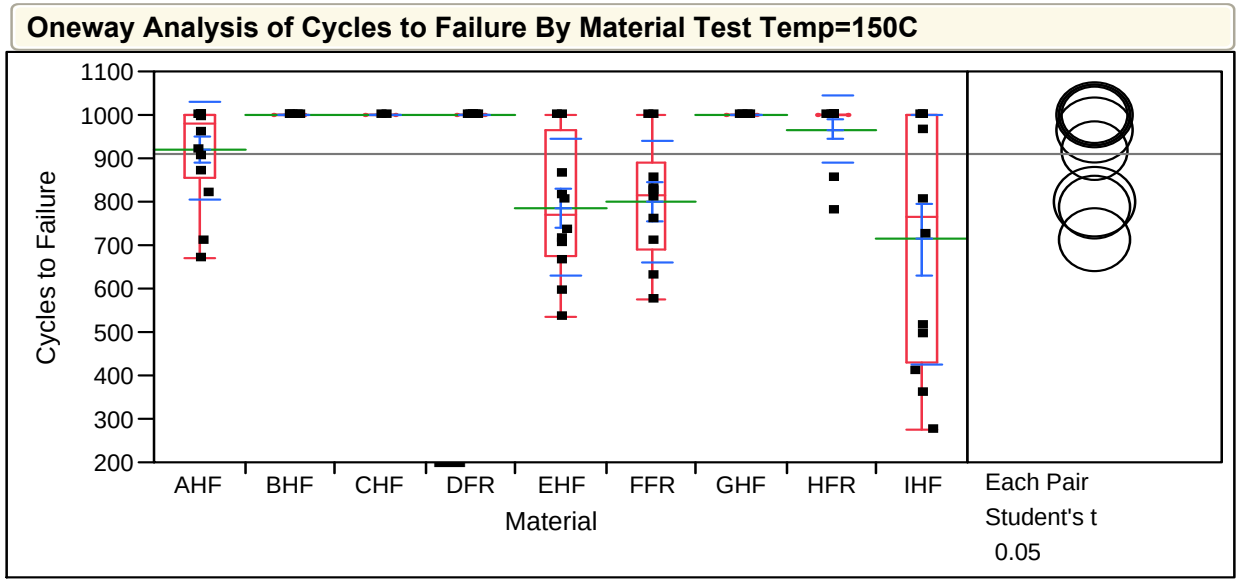
- **HFR-Free Flexural modulus values are statistically different and slightly higher than the FR4**
- **The higher modulus of the HFR-Free materials is attributed to the higher loading of in-organic fillers**
- **Flexural modulus values doesn't significantly differ in X & Y directions**

Charpy Impact Test



Conclusions:

- HFR-Free materials exhibit higher impact strength than FR4 material
- The higher impact strength of the HFR-Free materials is attributed to the higher loading of in-organic fillers
- The test method appears to be able to differentiate between materials

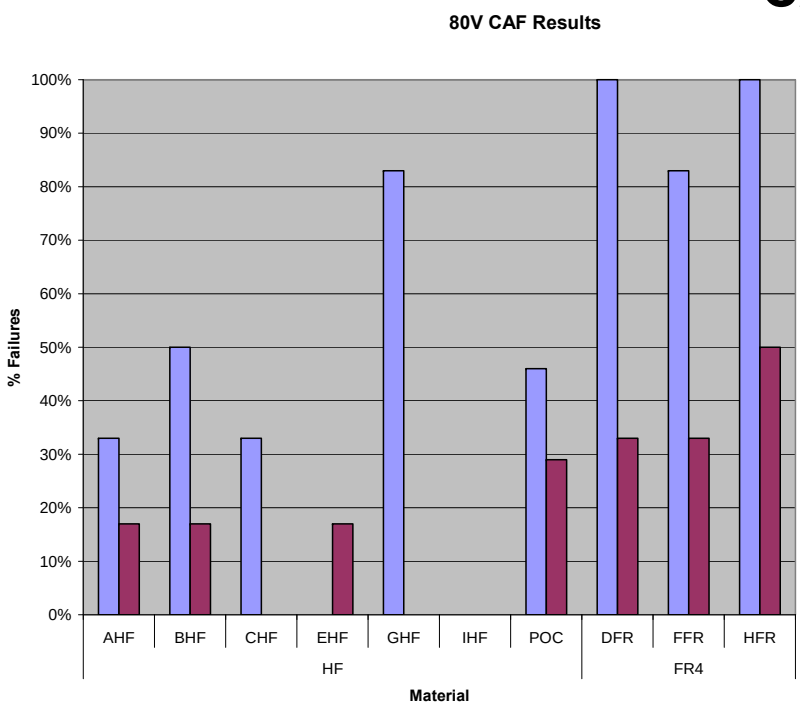


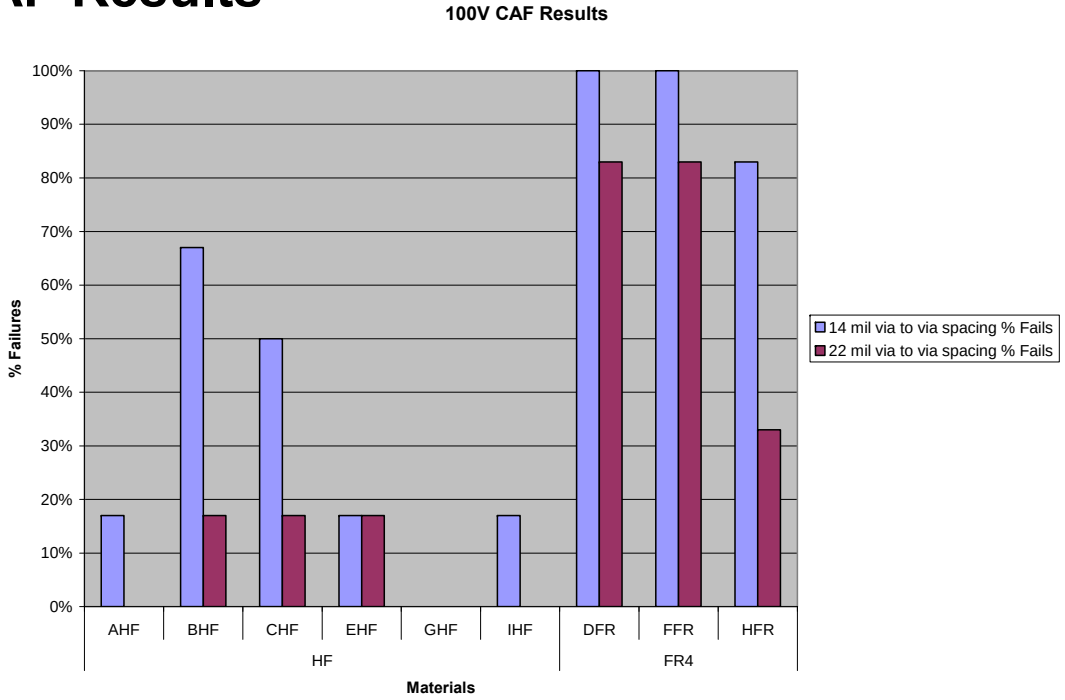
Excluded Rows 6

Conclusions:

- All materials showed acceptable via reliability performance for Client type product designs (>500 cycle average)
- Test temp of 150C unable to adequately differentiate between materials after 1000 cycles of test
- Expected failure modes seen in all materials with failures (barrel cracks)

CAF Results





Conclusions:

- HFR-Free materials outperformed their brominated FR4 counterparts for both bias levels (80 vs. 100 volts).
- 22 mil via to via spacing outperformed 14 mil via to via spacing as expected.
- 80V 14 mil via to via spacing data for GHF appears to be an outlier.

Suppliers HFR-Free Laminate Capacity (2008 -2011)

HFR-Free laminate materials shipped have doubled in the past 3 Years

Total % of HFR-Free/FR4 Laminates shipped				
Year	2008	2009	2010	2011 (Q1-3)
HFR-Free shipped as a % of Total Laminates MM²	8%	10%	15%	17%

Summary/Conclusions

Conclusion: HFR-Free Transition Readiness

The iNEMI HFR-Free Leadership WG believes that HFR-Free Laminates are ready for the Client space transition

Reliability:

- Due in part from the emphasis of this consortia, the laminate suppliers have modified there initial HFR-Free offerings and the laminates in the study now have properties that equal or exceed the BFR version.

Capacity:

- The growth of HFR-Free laminates has increased over the past several years with WG laminate members doubling (2X) their capacity

Commitment:

- Each Laminate Supplier in the WG has committed to supplying the TSM data for HFR-Free Laminates upon request.

- The iNEMI High Reliability WG is extending HFR-Free alternatives for other high end market sectors

Conclusion: Test Suite Methodology

- The Test Suite Methodology (TSM) has been successful in allowing direct quantifiable comparison of desired laminate properties
- The TSM has added non-traditional performance data to the Laminate suppliers data sheets
- Several of the new Test Methods will require more evaluation before full acceptance by the Industry
- Some TSM structures and the stack-up/construction would have to change to accommodate higher layer count/thicker PCB

Firms Participating in the Program

Special Acknowledgment

- Brian Gray & DW Chen, Celestica
- Scott Hinaga, Cisco
- Steve Ethridge, Wallace Ables & Aamir Kazi, Dell
- Ray Fairchild, Delphi
- Tim Lee, Doosan Electro-Materials
- Martin Bayes, DOW
- Ka Wai Chan, Elec & Eltek, PIC
- Dongji Xie, Flextronics
- Rich Barnett & Rocky Shih, Hewlett Packard
- Gary B Long & Deassy Novita, Intel Corporation
- Mike Leddige & Louis Armenta, Intel Corporation
- Satish Parupalli & Steve Hall, Intel Corporation
- Graver Chang & Michael Peng, IST
- Tadashi Kosuga, Frank Chan, Lenovo
- Louis Lin, Nan Ya Plastics
- Scarlet Wang, SYTECH
- Jeffrey Liao, Elite Materials Co.
- Jason Zhang, Foxconn
- Bill Weng & Anderson Chen, ITEQ
- Yu Xi, Quanta
- Bill Birch, PWB Interconnects
- Jim Arnold & David Godlewski, iNEMI

Questions?

Next iNEMI Activities in PWB Technology

Improving UL Certification of Laminates and Printed Circuit Boards

- Co-Chairs:
- Valerie St. Cyr (Teradyne)
- Greg Monty (UL),
- Jackie Adams(IBM)

Improving UL Certification of Laminates and PCBs

- Problem
  - Technology advancements in PCB materials and densities have progressed at a very rapid rate
    - Low Halogen laminates; HDI materials; inks and pastes to embed functions or connection structures
  - The existing UL certification requirements need to be updated and streamlined to support the rapid TTM requirements of new PCB designs.

- Goals
  - Clear and defined recommendations on improvements for the present UL materials and PCB standards. This may include: number of samples; types of samples; test suites; test methodologies, techniques or procedures based upon scientific evidence.
  - A review of the possibility of newer existing tests or the development of new tests, to complement or replace the existing tests.
  - Potential reduction in the present time to acquire UL certification.

Project Formation Participants

IBM

UL

生益科技 SHENGYI SCI. TECH

MULTEK

VIASYSTEMS.

TERADYNE

TERADYNE

intel

Current Status of Initiative

- Project formation Group has Completed Satement of Work (SOW) and Project Statement (PS)
- Technical Committee will review SOW & PS on Friday
- Anticipate a call for Project Signup will occur next week
- See iNEMI Website for latest information

Other Proposed PWB and PWA Consortia Initiatives

- Material Evaluation for Low-Loss High Reliability Applications Thick board rework
- Surface finish evaluations by market segment
- Molding Compounds for packages
- Underfill Materials
- Side to side registration of PCBs
- Delamination and Pad Cratering of PWBs

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