iNEMI HFR-Free Signal Integrity Project: An Investigation to Identify Degradation of Electrical Signals in HFR-Free PCB Materials

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Abstract:
Recent environmental concerns over the safety of the halogenated flame retardants (HFR) used in commonplace FR4 printed circuit boards (PCB) have prompted market demand for HFR-free computer systems. Unfortunately, the critical electrical properties of most HFR-free dielectrics on the market in 2009 made high-speed bus designs such as DDR3 & PCIe3 problematic without increasing the cost of the system. The iNEMI HFR-Free Signal Integrity Working Group was established in early 2009 with membership from 16 OEM, ODM and laminate supplier companies to address these industry concerns. This effort has helped pave the way for member companies to produce "green" HFR-free product lines by: 1) Uniting a large portion of the industry on the problems associated with high-speed bus design on HFR-free PCB's, 2) Defining a common approach to mitigate the signal integrity challenges and 3) Communicating a unified set of desired electrical properties to the major laminate manufacturers to produce higher volumes and lower cost HFR-free dielectric materials suitable for high-speed bus design.

Membership:

Cisco, Intel, Dell, Doosan Electro-Materials, Dow Chemical, Elec & Eltek, Elite Material Co., Flextronics, Foxconn, Hewlett-Packard, IBIDEN, ITEQ, Lenovo, NanYa Plastics, Quanta Computer, Shengyi Technology.

Problem:

FR4 epoxy has been used in the construction of PCBs for decades. Consequently, its electrical properties, which are influenced by brominated flame retardants integrated into the molecular structure of the resin, have been studied extensively. As an environmentally friendly alternative to the halogenated flame retardants present in FR4 PCB dielectric materials, several new non-halogenated formulations were developed by different material suppliers. Unfortunately, each new formulation has a unique electrical performance that differs from FR4. This leads to the current problem: The critical electrical properties of most HFR-free dielectrics currently on the market make high-speed bus designs such as DDR3 and PCIe problematic without increasing the cost of the system.

The most apparent problem lies with the increased permittivity of the HFR-free dielectric materials compared to FR4. Measurements show that most HFR-free PCB materials on the market have permittivity values at 1 GHz in the 4.5-5.5 range, while FR4 built with 1080 glass has permittivity values in the upper 3's [1]. Increased permittivity requires thicker dielectric layers to achieve equivalent impedance compared to FR4. Thicker dielectric layers lead to an increase in crosstalk in microstrip lines which will reduce bus performance. Figure 1 demonstrates the margin reduction using three 10-inch long coupled microstrip transmission lines with routing guidelines consistent with a DDR3 bus. If the trace-to-trace spacing and line widths remain constant (consequently board area consumed remains constant), and the dielectric thickness is adjusted to maintain constant characteristic impedance (50 ohms in this case), the eye area is substantially reduced for high permittivity values. Since smaller eyes equate to lower bus performance, many HFR-free materials will challenge high speed bus design.

Conventional means of reducing crosstalk is to isolate traces by increasing spacing as much as practical to reduce the electromagnetic coupling of energy. Unfortunately, modern motherboard designs are already area constrained requiring extra layers (and therefore cost) to provide additional real-estate for crosstalk compensation when using high permittivity dielectrics.

Bus speed scaling

As bus speeds increase, the negative impact of the higher permittivity values (compared to 1080 FR4) associated with many HFR-free materials is exacerbated. Figure 2 demonstrates the degradation of the signal eyes at 667 Mbits/second and 2000 Mbits per second, which roughly correspond to end-of-life DDR2 and DDR3 bus speeds respectively. Note that at 667 Mbits/sec, the higher permittivity has very little impact (Figure 2-A). However, if the same topology is driven at 2000 Mbits/sec, the signal degradation is more dramatic (Figure 2-B). The degradation at higher bus speeds exemplifies the signal integrity problems associated with higher permittivity. Performance can be reclaimed by increasing signal spacing, which consumes more board real-estate, or by designing with glass styles thinner than 1080, such as 106, but each of these options increases platform costs.

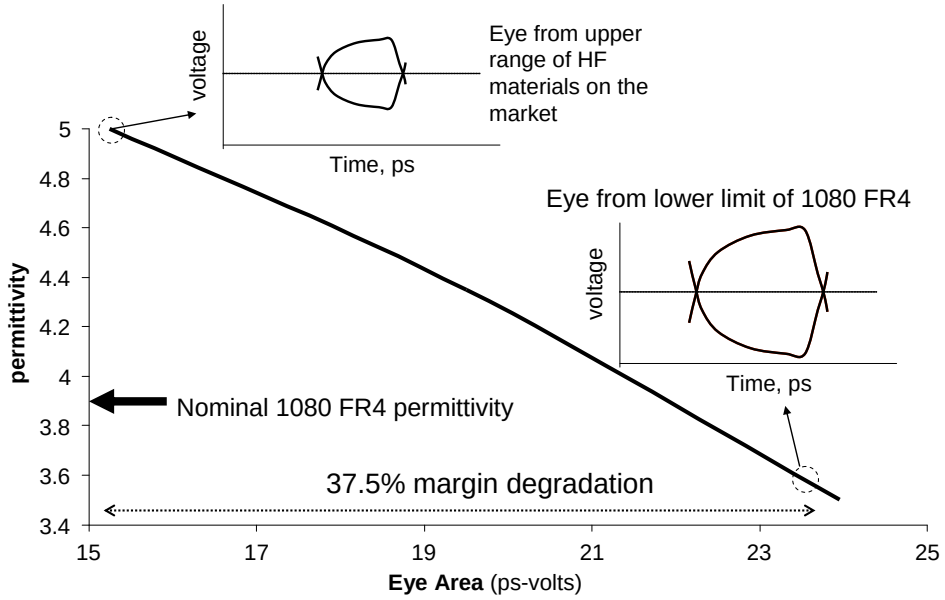

Figure 1: Example of margin reduction due to high permittivity values; three 10-inch coupled microstrips; trace to trace spacing is constant; dielectric thickness adjusted to maintain constant 50 ohm characteristic impedance for all permittivity values

Mitigation

The most cost effective strategy for mitigating the negative effects of HFR-free materials is to place bounds on the electrical material properties so that signal integrity will not be degraded. Based on the high-speed signaling needs required by each product, the limits of each parameter can be identified. Samples of HFR-Free materials can then be evaluated and the results mapped into the requirements envelope providing a design data base that can be used to select adequate materials for products. An example of this performance requirement envelope is shown in Figure 3, where limits on the loss tangent and the permittivity have been determined for a class of high-speed buses. It is important that the specific glass style, resin ratio and the environmental conditions are properly accounted for in the performance envelope. Simulations on DDR3 and PCIe2/3 buses were used to derive the envelope listed in Figure 3 and two HFR-materials were found to fit within the envelope (materials 4 and 5).

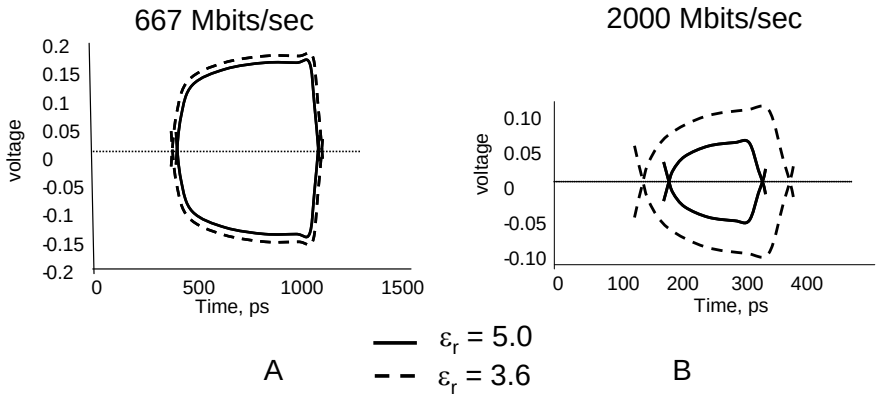

Figure 2: High permittivity values may be adequate for low-speed bus designs, but substantially degrade high-speed bus performance (Simulation of the 10-inch microstrips used to create figure 1)

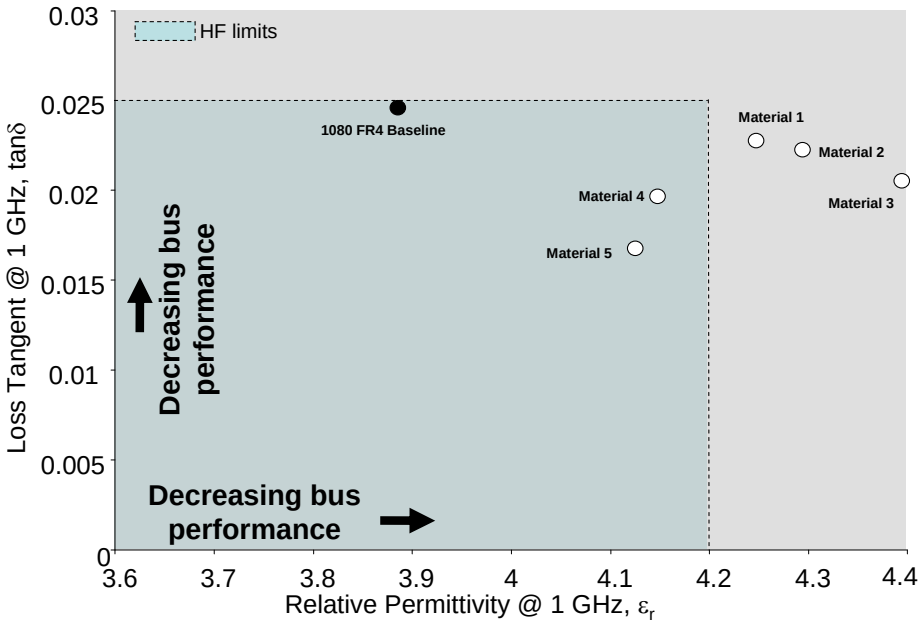

Figure 3: HFR-free dielectric electrical envelope with 2 plies of 1080 glass; humid conditions; 95°F and 95% RH

Since the permittivity of materials 4 and 5 is higher than the 1080-FR4, crosstalk was increased when the materials were used as a "drop in" for the 1080-FR4. However, the degradation in performance compared to the FR4 baseline was small enough to be acceptable to the platform designers. Note that the degradation will increase with bus speeds and will eventually become unacceptable. This means that at some speed bin, the materials cannot be a "drop-in" replacement for FR4 with the same glass style due to the increased permittivity. Figure 4 shows measured results of identical DDR3 buses built with FR4 and HFR-free PCB materials. The designs were optimized for FR4 materials, and then built with HFR-free materials 4 and 5 from Figure 3. In order to achieve the same impedance values, the stackups where adjusted appropriately by the PCB vendors. Note that both HFR-free materials have lower margins as expected due to the higher permittivity, thicker layers (to achieve the same impedance as the FR4 design) and increased crosstalk.

Critical Electrical Parameters

In addition to the permittivity, the work group has identified 2 additional critical electrical parameters. Table 1 provides details on how each of the critical variables affects bus design. Each of these parameters must be assessed for all new HFR-free dielectric materials to ensure they remain within acceptable bounds. Note that a materials affinity to absorb moisture from the environment must also be understood. Water is a large, polar molecule and therefore even a small amount of absorbed water can have a large impact on the electrical properties of a dielectric. Even if a particular dielectric exhibits excellent electrical properties at nominal relative humidity (RH) levels, if significant water is absorbed, the properties quickly degrade.

Table 1: Critical dielectric design parameters

Parameter	Other names	Design influences
Permittivity	Dk, ε_r, dielectric constant	Characteristic impedance, Propagation velocity, crosstalk
Loss tangent	Df, tanδ, dissipation factor	Signal attenuation
Moisture absorption	Environmental effects, humidity	When dielectric materials absorb water, Dk & Df increase.

Test Boards

The critical electrical parameters detailed in Table 1 were measured and extracted using transmission line structures [2]. Lateral slots were cut through the board between and parallel to the striplines to allow humidity from an environmental chamber to permeate into the dielectric material so the electrical properties can be evaluated at different environmental conditions.

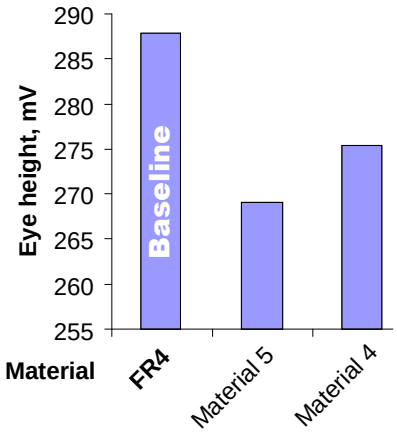

Figure 4: Measured DDR3 margin degradation caused by the HF materials that fell within the performance envelope in figure 3 compared to an FR4 baseline.

Unfortunately, it is very difficult to extract accurate Df (loss tangent) values from transmission line structures because there is no unique way to mathematically separate the extra losses caused by the finite surface roughness of the copper. Inevitably, surface roughness losses contaminate the extracted Df values resulting in errors. One method to circumvent this problem is to create all test boards using the same copper type, glass style and cross section geometry to force the errors due to the surface roughness to be approximately equal for each sample. Then total power loss can be measured with a vector network analyzer (VNA) as shown in equation (1a)**,** where the asterisk signifies the complex conjugate and the term $\frac{P_{dissapted}}{P_{incident}}$ is the percentage power (when multiplied by 100) dissipated by the transmission line under test.

$$\frac{P_{dissapated}}{P_{incident}} = 1 - \left(S_{11}S_{11}^{*} + S_{21}S_{21}^{*}\right) \tag{1a}$$

If reasonable efforts are made to ensure the stackup and copper type are identical, the differences in total loss can be used to make relative comparisons of dielectric losses.

Dk can easily be calculated by measuring the phase of the insertion loss (S_{21}) with a vector network analyzer (VNA) as shown in equation (1b) through (1d),

$$\theta_{S_{21}} = \arctan\frac{\mathrm{Im}(S_{21})}{\mathrm{Re}(S_{21})} \tag{1b}$$

$$\tau_p = \frac{\theta_{S_{21}}}{360^0 f} \tag{1c}$$

$$Dk = \left(c \cdot \tau_p\right)^2 \tag{1d}$$

where c= the speed of light in a vacuum ($3x10^8$ meters/sec).

Test Conditions

Since the ambient environmental conditions significantly affect the measured values of the permittivity (Dk) and the loss tangent (Df), relative humidity and temperature standards were used when characterizing materials. The values of the permittivity (Dk), loss tangent (Df) and total loss should be measured on the test boards after conditioning in an environmental chamber with the following setup:

Pre-conditioning *(drive the moisture out of the board)*
Duration: 3 days

Relative humidity: 10%
Temperature: 212°F

Conditioning (*nominal* environmental corner)
Duration: >~14 days
Relative humidity: 50%
Temperature: 70°F
Parameters to be measured: S_{11}, S_{21}
Parameters to be extracted: permittivity, total loss

Conditioning (*wet* environmental corner)
Duration: >~14 days
Relative humidity: 95%
Temperature: 95°F
Parameters to be measured: S_{11}, S_{21}
Parameters to be extracted: permittivity, total loss

Note that the duration of conditioning should be long enough to ensure full saturation of moisture from the atmosphere. This can be determined by conditioning the test board in an environmental chamber and periodically measuring the insertion loss (S_{21}) at daily (or weekly) intervals. When the insertion loss has stabilized, the dielectric material has saturated and will no longer absorb ambient moisture from the atmosphere. A similar procedure was performed in [4]. The duration of 14 days is as estimate based on data from [4] that indicate a buried microstrip would saturate in less than ~100 hours of conditioning in an environmental chamber. Although standard stripline structures with full copper cladding over the dielectric would take months to fully saturate [4], the lateral slots cut into the test boards should dramatically decrease the diffusion time for ambient moisture to fully saturate the dielectric material surrounding the strip.

Due to time and resource limitation, this working group only fully studied the electrical performance of the HFR-free dielectric materials at the nominal environmental corner.

Extrapolating to different resin/glass ratios

To properly compare the electrical properties of HFR-free dielectric materials it is necessary to choose a specific resin to glass ratio. If a non-standard resin/glass ratio is used to measure the dielectric properties, then the results will be dominated by relative properties of glass and resin and not the performance of the HFR-free PCB dielectric. Figure 7 is an example of how the permittivity (Dk) and loss tangent (tand or Df) changes as a function of the percentage resin content. From Figure 7, the permittivity (Dk) of glass is ~ 6.5 while the permittivity of resin (in this example) is approximately 3.2 while the permittivity of a 50% resin content dielectric material is ~ 4.3.

For the purposes of the workgroup, it was decided to report all permittivity (Dk) and loss tangent (Df) values at a 50% glass/resin ratio so the relative electrical performance of different dielectrics can be compared.

The test boards were constructed with balanced stripline transmission line structures using one ply of 2116 glass above and below the strip [2], as shown in Figure 8. The stackup resulted in a resin content of ~44.7%. Consequently, the measured data was adjusted to reflect the expected values at 50% resin content.

The measured permittivity (Dk) and loss tangent (Df) values were extrapolated to the equivalent value expected at a 50% resin content using the cross-section thickness and the number and type of glass plies are known using equation (2) [3]. The procedure is outlined here.

Step 1: Measure the permittivity (Dk) and the loss tangent (Df) using a test board with stripline structures similar to that described in [2].

Step 2: Determine the stripline structure height from the cross section. The test boards constructed for this project have a stripline height of approximately 4.0 + 4.2 =8.2 mils or 208 microns (see figure 8).

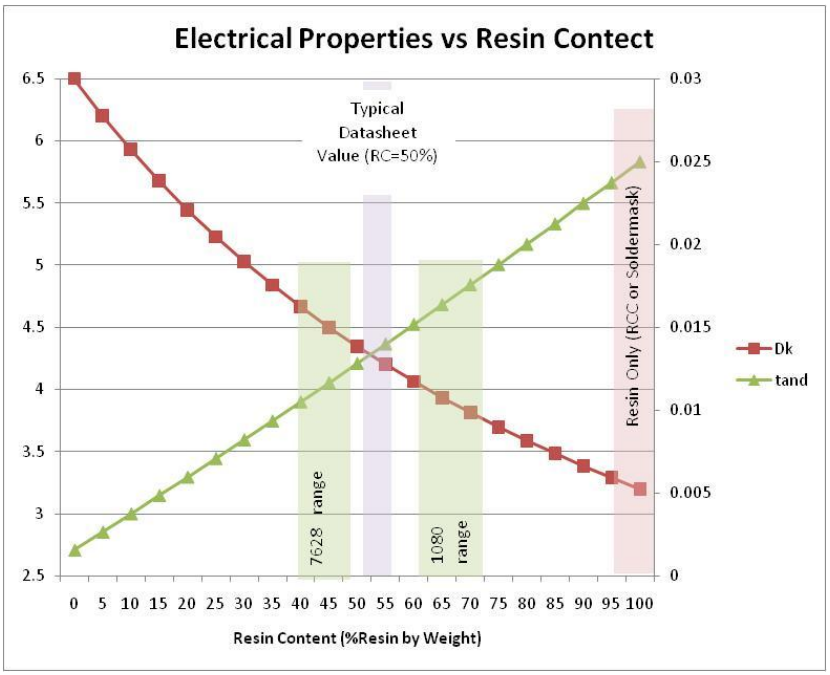

Figure 7: Example of how the electrical properties of a typical glass/resin composite dielectric change with percentage of resin content

Step 3: Calculate the resin content of the test board using equation (2). If it is not 50%, then proceed to step 4.

$$R_C = \frac{R_d(G_d H - W)}{G_d W + R_d(G_d H - W)} \tag{2}$$

where,

R_c = resin content between 0 and 1
R_d = Resin density (g/m^3)
G_d=Glass density (g/m^3)
H=dielectric height (m)
W=Glass Weight Basis (g/m^2)

The resin density is different for each material tested. The range of densities and t he glass properties for the dielectric materials characterized in the workgroup is listed in **table 3**.

Step 4: Calculate the resin volume ratio (V_r) of the S3 board using (3)

$$V_r = \frac{G_d R_C}{G_d R_C + R_d(1 - R_C)} \tag{3}$$

Step 5: Calculate the permittivity of the resin with (4)

$$\varepsilon'_{\text{resin}} = \frac{\varepsilon'_{\text{measured}} - \varepsilon'_{\text{glass}}(1 - V_r)}{V_r} \tag{4}$$

10 Layer Stack-up

	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu		1.6	mils
	Prepreg		3	mils - 1 ply 1080
Layer 2	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 3	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 4	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 5	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 6	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 7	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 8	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 9	Unplated 1 oz Cu		1.3	mils
	Prepreg		3	mils - 1 ply 1080
Layer 10	Plated 1/2 oz Cu		1.6	mils
			48.2	

Figure 8: Target stackup for the testboards. Stripline test structures were built on layers 3, 5 and 7.

Step 6: Calculate the resin volume needed for 50% resin content

$$V_{r\_50\%RC} = \frac{0.5G_d}{0.5G_d + R_d(1-0.5)} \tag{5}$$

Step 7: Calculate the permittivity (*Dk*) at 50% resin content

$$\varepsilon'_{\_50\%\mathrm{RC}} = Dk_{\_50\%} = \varepsilon'_{\mathrm{resin}} V_{r\_50\%RC} + \varepsilon'_{\mathrm{glass}} \left(1 - V_{\_50\%RC}\right) \tag{6}$$

Step 8: Calculate the imaginary portion of the permittivity from *Df* measured from the test boards with (7)

$$\varepsilon''_{measured} = Df \cdot Dk \tag{7}$$

Step 9: Calculate the imaginary portion of the resin permittivity

$$\varepsilon''_{\mathrm{resin}} = \frac{\varepsilon''_{\mathrm{measured}} - \varepsilon''_{\mathrm{glass}} \left(1 - V_r\right)}{V_r} \tag{8}$$

Step 10: Calculate the imaginary permittivity of the resin with (9)

$$\varepsilon''_{\_50\%\mathrm{RC}} = \varepsilon''_{\mathrm{resin}} V_{r\_50\%RC} + \varepsilon''_{\mathrm{glass}} \left(1 - V_{\_50\%RC}\right) \tag{9}$$

Step 11: Calculate the loss tangent (Df) at 50% resin content with equation (10)

$$Df_{50\%RC} = \frac{\varepsilon''_{50\%RC}}{Dk_{50\%RC}} \tag{10}$$

Although each manufacturer has specific glass and resin properties used in each product, ranges and typical values are shown in table 3.

Table 3: Typical resin and glass properties for the materials tested in the working group

Glass Density (G_d)	Resin Density (R_d)	Glass Weight Basis (W) *(Style:W)*	Glass Dk	Glass Df
2.54 g/cc	1.35-1.55 g/cc	2116: 105 g/m^2 1080: 50 g/m^2 106: 25 g/m^2 7628: 200 g/m^2 1500: 165 g/m^2 2313: 80 g/m^2	6.8	0.0007-0.0015

Choosing an HFR-free material:

The choice of an HFR-free dielectric material for a specific design is a compromise between performance and cost. Consequently, it is impossible to define universal requirements for HFR-free dielectrics that will be adequate for all products on the market. However, general trends for dielectric performance can easily be identified because they are based on the physics of signal propagation across an interconnect and are not specific to any design. Generally speaking, the dielectric materials used to design printed circuit boards (PCB's) with high-speed digital interfaces (such as DDR3 pr PCIe) require low permittivity (Dk) and low losses. Low permittivity tends to reduce crosstalk noise for given impedance and low loss tangents reduce signal attenuation.

In order to communicate meaningful requirements for the general electrical properties of HFR-free dielectrics to material manufacturing companies, reasonable limits must be chosen that are adequate for the majority of products that utilize high-speed digital buses. These requirements will help the material manufactures know what type of product the industry (as represented by the work group members) desires. Theoretically, if the industry communicates a single message of what is desired, the material manufacturing companies will allocate more resources to developing the most desirable products, leading to increased volume and decreased cost.

Common Electrical Limits

Although it is impossible to define electrical limits to universally select "good" materials versus "bad" materials, general limits can be chosen that will be "good enough" for many applications currently on the market. The team members were polled to determine the "generally preferred" electrical limits they desire for HFR-free dielectric materials. The electrical performance limits are shown in table 4.

Table 4: General limits of desired electrical performance of HFR-free dielectric materials to minimize signal integrity problems; determined by polling the companies in the workgroup;

	Limits
Permittivity (Dk)	<4.2 (1 ply 1080, RC~64%) <4.5 (RC50%) (any environmental condition)
Loss Tangent (Df)	<0.018 (1 ply 1080, RC~64%) <0.014 (1 ply 1080, RC50%) (measured at 50% RH & 75^{o}F)
Moisture Impact on loss	Df<0.024(1 ply 1080, RC~64%) Df<0.019(RC50%) (measured at 95% RH & 95^{o}F)

Table 4 is meant to communicate the general limits above which high-speed design becomes more difficult due to the phenomena discussed earlier in this document. It is possible than some designers may choose materials that fall outside these guidelines due to other favorable qualities such as cost or thermo-mechanical properties.

Design Data Base

If the dielectric properties of various HFR-free dielectric materials are measured and compared to the electric requirements detailed in Table 4, a design database can be constructed to help member companies make relative comparisons of materials. This methodology will streamline the process of choosing specific HFR-free PCB materials with adequate performance for a given design.

Test boards were constructed from 9 different PCB dielectric materials, including 6 HFR-free and 3 FR4 baseline samples. Multiple test boards constructed with each material were sent to six member companies for measurement. The average of all results for each material were calculated and plotted against the electrical performance limits as outlined in table 4. Figure 9 depicts the design data base constructed with this data where the measured results were mapped onto the desired electric limits.

As discussed previously, it is difficult to extract accurate loss tangent numbers using transmission lines unless the extra losses due to the copper roughness are carefully characterized. To circumvent this problem, all test boards were designed with identical cross sections using the same copper type so the extra losses due to the copper roughness will be approximately equal and the extracted loss tangents can be normalized against the average value of the three FR4 samples. Since the electrical limits on Df shown in table 4 correlate reasonably close to the loss tangent of standard FR4, normalizing the data to the average loss of the FR4 samples allows a simple way to make relative comparisons of dielectric materials compared to the desired performance limits. The normalized loss shown on the y-axis of figure 9 was calculated with equation (11),

$$\text{Normalized Loss} = \frac{P_{loss(HFR-free)}}{\frac{1}{3}\left(P_{loss(FR4-1)} + P_{loss(FR4-2)} + P_{loss(FR4-3)}\right)} \tag{11}$$

where the FR4 loss terms ($P_{loss(FR4)}$) are the measured results from the following three baseline FR4 materials. The loss terms can be evaluated using extracted values of Df or the total power dissipated as described in figure 1a.

Therefore, if a HFR-free material has a loss tangent (Df) lower than the FR4 baseline, then the normalized value is <1 and if the loss is higher, then the normalized value is >1.

Figure 9 shows there are several HFR-free materials that appear to have adequate electrical performance to satisfy the general requirements for high-speed digital bus design. Note that the figure does not guarantee the materials are suitable for thermo-mechanical requirements. The iNEMI HFR-free materials working group has performed a wide variety of thermo-mechanical tests in the same material set, which will be published in late 2011 [5].

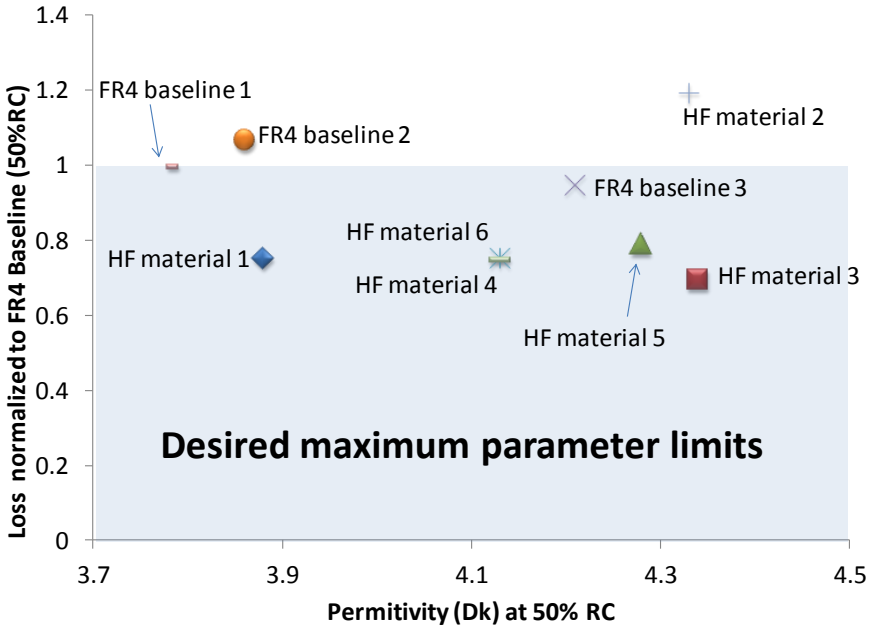

Figure 9: Test board measurements extrapolated to 50% Resin Content (RC) & mapped onto the desired properties; Reported at 50% RH, 21°C, 5 GHz, each data point is average of 15-25 data points from 3-5 samples at 5 separate labs; note that this is a different material set from figures 3 & 4

Conclusions:

At the onset of this working group, the critical electrical properties of most HFR-free dielectrics on the market made high-speed bus designs such as DDR3 and PCIe problematic without increasing the cost of the system. In order to circumvent this problem, the iNEMI HFR-free Signal Integrity Working group was formed with 16 member companies. The working group identified the critical electrical parameters that must be controlled to mitigate signal integrity problems, placed general limits on the critical electrical parameters to reduce signal integrity problems and communicated those limits to material manufacturers to facilitate an increase in volume and decrease in cost. Additionally, the working group identified 6 HFR-free materials for testing, and constructed a design data base by mapping the measured material properties onto the performance limits providing an easy methodology that consortium members can use to make relative comparisons of PCB materials for design purposes. Since the working group membership includes OEMs, ODMs and laminate suppliers, a significant portion of the industry is represented. The workgroup has been effective in 1) uniting a large portion of the industry on the problems associated with designing high-speed buses with HFR-free PCB's, 2) defining a unified approach to mitigate the signal integrity challenges and 3) paving the way for member companies to produce "green" HFR-free product lines.

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[2] Gary B Long, "iNEMI Consortium HFR-free Test Boards", 2010.
Contact Jim Arnold (jim.arnold@inemi.org) for a copy of the test board Gerbers as a reference design.

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[5] John Davignon, Gary Long, "Final Report – iNEMI HFR-free materials working group", to be published late 2011.
Contact Jim Arnold (jim.arnold@inemi.org)
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Agenda

- iNEMI Halogen Free Consortium
- Drivers
- SI Overview
- WG Strategy
- Conclusions

Problem

- To meet market demands for “Green technology”, the electronics industry are removing halogenated flame retardants (HFRs) from FR4 based printed circuit boards (PCBs).

- Unfortunately, the thermo/mechanical & electrical properties of HFR-free PCBs tend to be meaningfully different to FR4 counterparts leading to …
    - Reduced electrical performance
    - Reduced thermo/mechanical performance
    - Supply chain and cost problems

To address these problems, the iNEMI HFR-free Leadership Project was initiated in early 2009

iNEMI Consortium

The iNEMI HFR-free Leadership Project was initiated in February 2009 to align the industry on strategy to mitigate problems with designing client platforms using HFR-free PCBs.

iNEMI is a non-profit R&D consortium with wide membership from electronic industry

Mission: Forecast & accelerate improvements in the electronics manufacturing industry

iNEMI International Electronics Manufacturing Initiative

Stephen Tisdale-Chair HFR-Free Leadership Program

HFR-Free PCB Materials (John Davignon)

Thermo/Mechanical properties

HFR-Free Signal Integrity (Stephen Hall / David Senk)

Electrical performance

This presentation focuses on the Signal Integrity WG

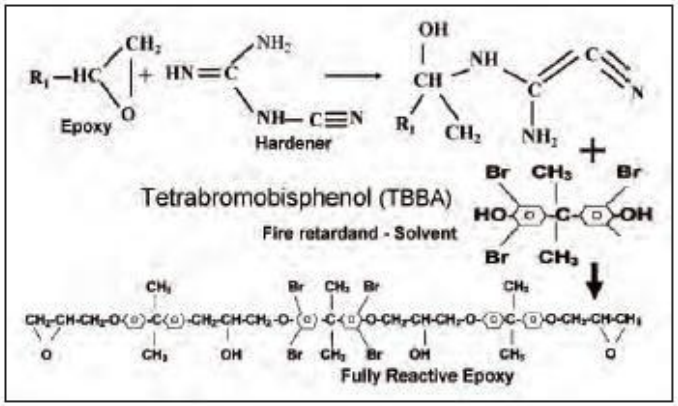
Signal Integrity WG: 16 Participating Members

“Critical Mass” of OEMs & Laminate manufactures was achieved to influence the industry

DRIVERS

Halogenated-Flame Retardants (HFRs) in PCBs

The Good: The addition of HFR's in FR4 are low cost & effective Flame retardant



Tetrabromobisphenol-A (TBBA) is the flame retardant used in FR4

- TBBA Volatilizes at burning temperatures & blankets the fire, excluding oxygen

The Bad: HFRs are an environmental health hazard when disposed of improperly

- Yearly 20–50 million tons of E-wastes generated worldwide – Most contain HFRs
- Dioxins are released during improper EOL burning / recycling

The Ugly: FR4 is a cornerstone of the electronic industry.

- Changes could have consequences in performance, supply chain & cost

Drivers to eliminate HFRs:

- Global Environmental Responsibility
- Threat of legislation (Not likely but still possible)
- Pressure from Non-Governmental Organizations

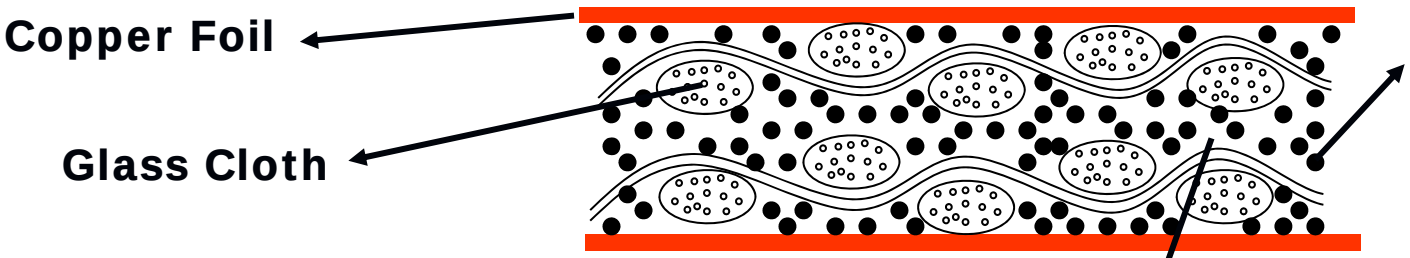
Pollution in:

Soil

Water

Air

Halogen-free PCB - What is different?



Filler (added)
- -Flammability
- -Heat Dissipation
- -Dielectric Properties

Resin Matrix (changed)
- -Heat Resistance
- -Bonding Strength
- -Flammability
- -Dielectric Properties
- -Water Absorption

3-major types of HFR-free Flame Retardants in PCBs

- ✓ **Organophosphates** – Forms a carbonized layer to cover surface
- ✓ **Nitrogen Compounds** – Generates incombustible gas
- ✓ **Metal Hydroxides** - Releases water at high temperature

Each manufacturer has its own "recipe" for HFR-free PCB

- ✓ No standardization which complicates design
- ✓ Each recipe has unique properties

Wide variety of recipes leads to a dependency on specific materials from a few manufactures

SIGNAL INTEGRITY ON HFR-FREE PCBs

Problem

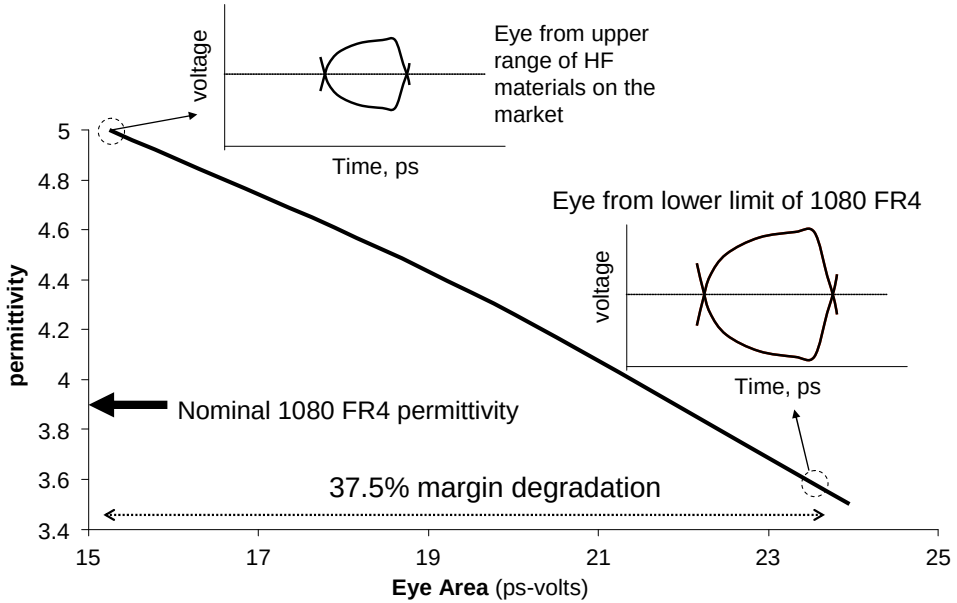
The critical electrical properties of many available HFR-free dielectrics make high-speed bus design problematic without increasing the cost of the system

WG Goal

Align the industry on a common strategy to eliminate any roadblocks to high-speed bus design using HFR-free PCBs

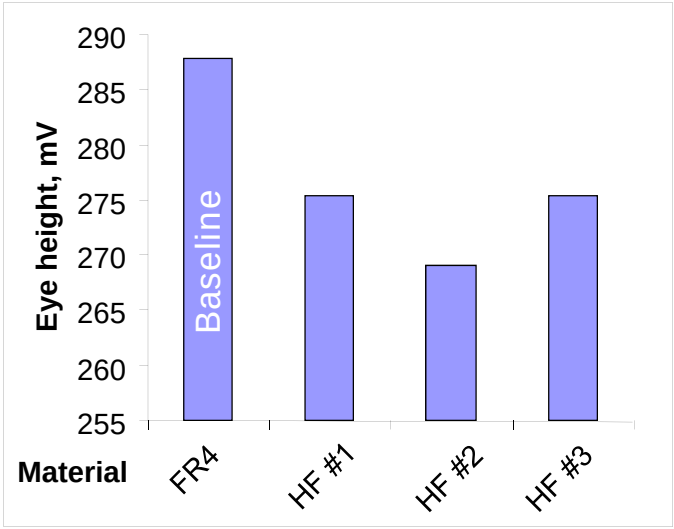
Performance of HFR-free PCB vs FR4

- ✓ **HFR-free PCB materials on the market tend to have higher permittivity values than FR4**
  - ✓ HFR-free Dk ~ 4.2 – 5.0 (1080)
  - ✓ FR4 Dk ~ 3.6-3.9 (1080)



Simulation of 1DPC DDR Bus

Measured DDR3 margin degradation caused by 3 HFR-free materials compared to an FR4 baseline.



- ✓ **Higher permittivity reduces bus performance**
  - Thicker layers at same Z_0 <u>increases crosstalk</u>
  - High crosstalk drives increased trace separation & more layers
  - PCB cost increase per layer ~ proportional to increased area (~50% 4L→6L)

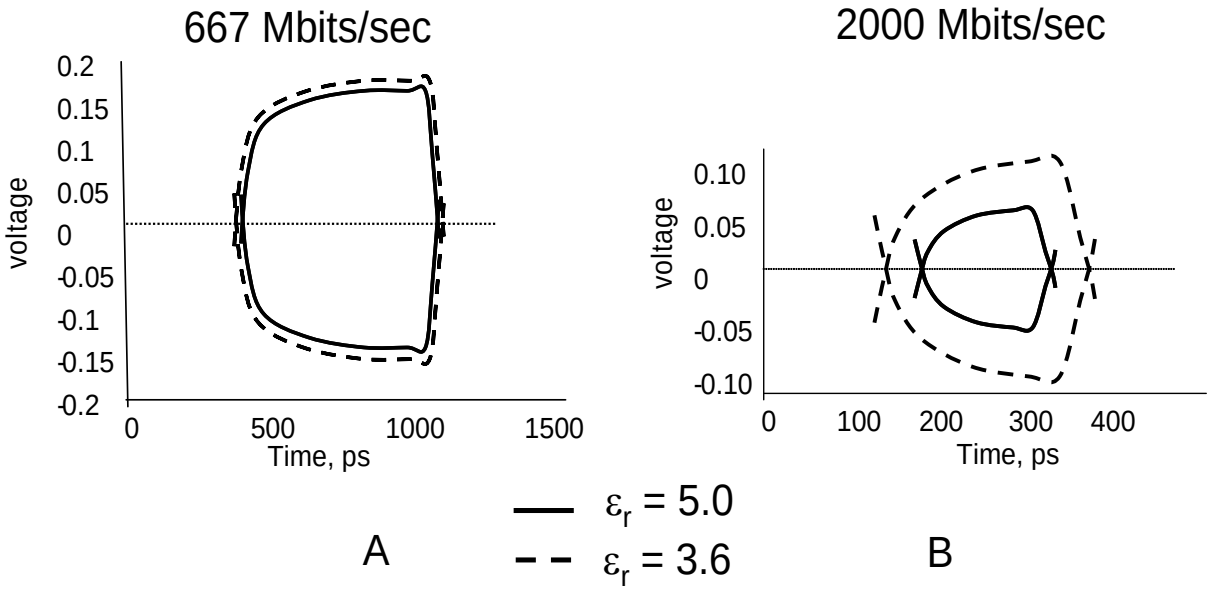
Compared to FR4, HFR-free PCBs can pose significant challenges to high speed bus design

Scaling HFR-free bus speeds

- ✓ **Margin reduction gets *worse* for faster buses**
  - HFR-free materials with high permittivity are adequate for lower speed buses, but are problematic at higher speeds

High permittivity values may be adequate for low-speed bus designs, but substantially degrade high-speed bus performance

Example: Simulation of simplified DDR 1DPC bus over extreme HF/FR4 permittivity range



HFR-free PCBs can make it difficult for buses to scale with Moore's Law

Solving the problem – 4-tier approach

1. Identify common critical electrical parameters
2. Define common performance limits
3. HFR-free design data base
4. Communicate industry needs to laminate suppliers

- ✓ **Not an "industry standard" or "spec" approach**
  - No consensus for spec development
- ✓ **Requires "*critical mass*" of industry heavy hitters**
- ✓ **Tell the laminate manufactures what "*we*" want as an industry so "*they*" will build it**

Approach designed to "voluntarily" get industry on the HFR-bandwagon before legislation forces it

iNEMI HF Signal Integrity WG Strategy

1. Identify common critical electrical parameters

Parameter	Other names	Design influences
Permittivity	Dk, ε_r, dielectric constant	Characteristic impedance, Propagation velocity, crosstalk
Loss tangent	Df, tanδ, dissipation factor	Signal attenuation
Moisture absorption	Environmental effects, humidity	When dielectric materials absorb water, Dk & Df increase.

Industry agreement on critical parameters gives us a set of metrics to make material choices

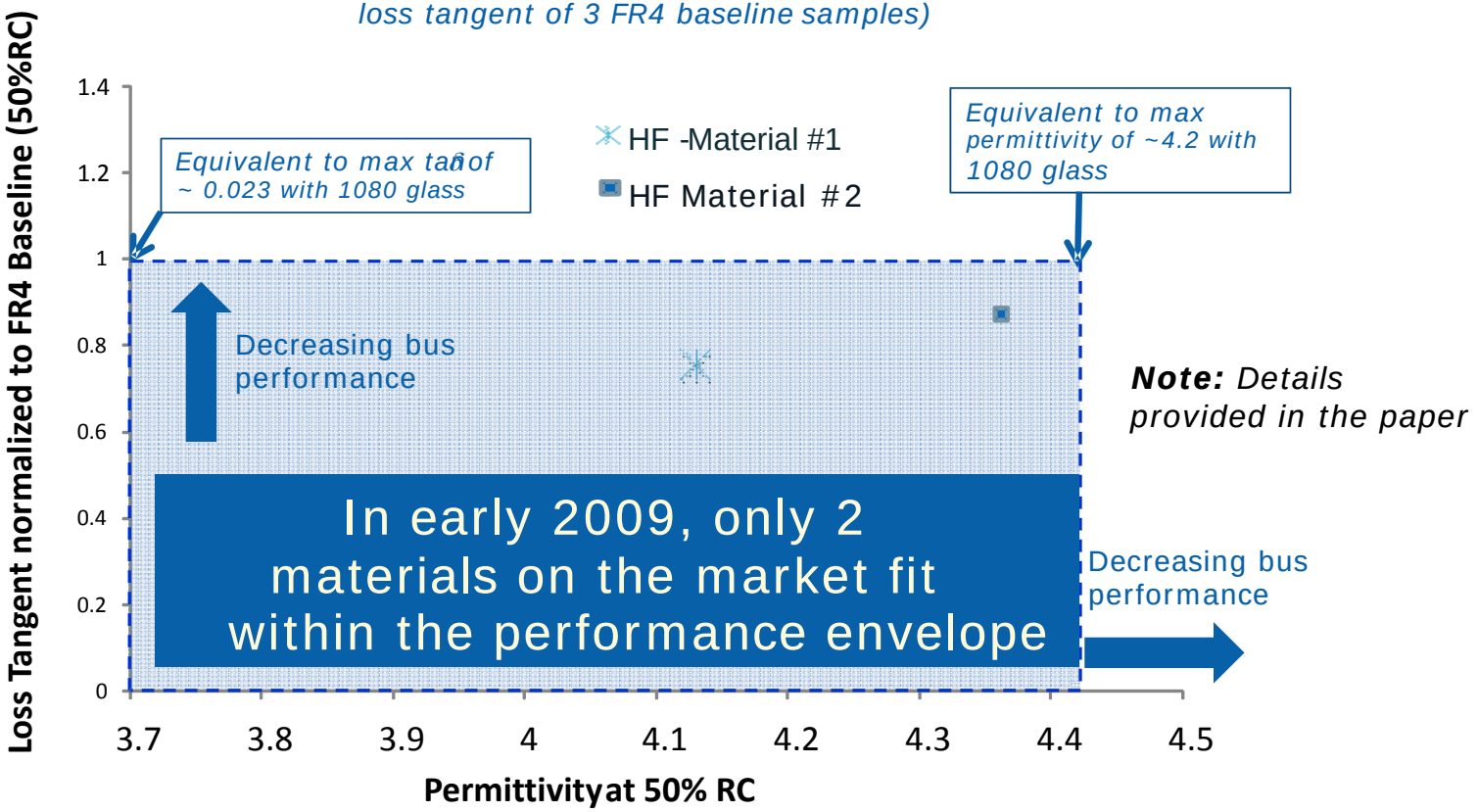
iNEMI HF Signal Integrity WG Strategy

2. Define common performance limits

For performance ≥ FR4, what are the electrical limits? → Focus on high-speed buses

Example: HFR-free PCB Performance Limits

***(50% Resin Content**, 95% RH, 95°F, Normalized loss of 1.0 = average loss tangent of 3 FR4 baseline samples)*



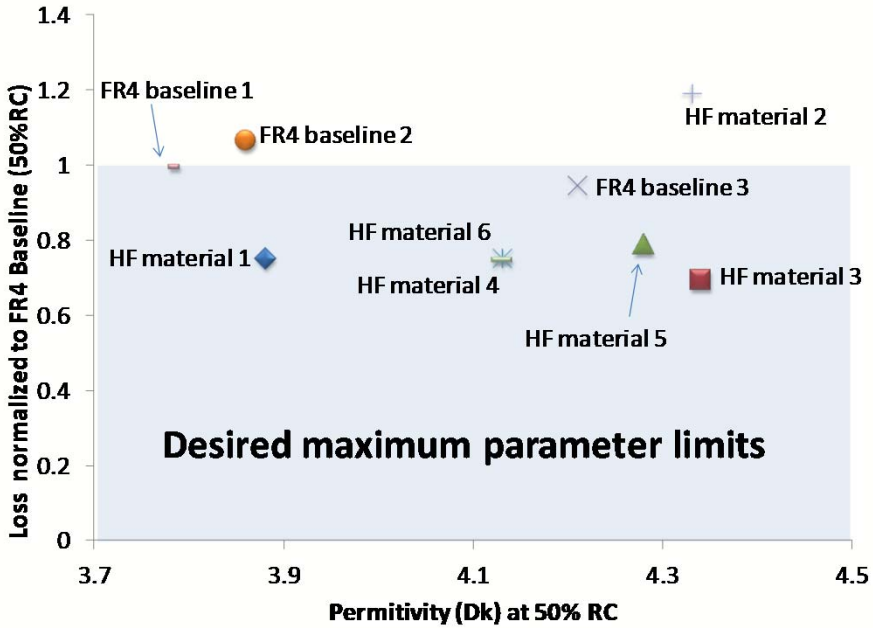
WG fully aligned on common performance envelope, providing requirements message to laminators

iNEMI HF Signal Integrity WG Strategy

3. HFR-free design data base

Database helps members choose adequate materials

Test board measurements extrapolated to 50% Resin Content (RC) & mapped onto the desired properties;



Helps cements minimum performance message to laminate companies

- ✓ 7 member labs provided measurements
- ✓ 6 member laminate manufactures provided test boards

Note: *Values Reported at 50% RH, 21oC, 5 GHz, each data point is average of 15-25 data points from 3-5 samples at 5 separate labs*

Number of high-speed HF materials identified by WG increased from 2 to 5

iNEMI HF Signal Integrity WG Strategy

4. Communicate industry needs to laminate suppliers

If a critical mass says "we want it" then "they will build it" → **increases supply & reduces cost**

Most important step → seeds the supply chain

- ✓Formally delivered "electrical requirements" to member laminators
- ✓Provided compliance test method for electrical requirements (*members only*)
- ✓Number of *compliant* materials increased from 2 to 5

The WG helped achieve industry momentum to ensure high performance HFR-free materials will continue to be developed

Summary

- ✓ **The WG has united a "critical mass" of the industry on …**
  1) the problems with designing high-speed buses with HFR-free PCB's
  2) a unified approach to mitigate the challenges
- ✓ **Established desired performance limits to remove signaling roadblocks from buses designed on HFR-free PCBs**
- ✓ **Delivered a design database & methodology to facilitate design choices between HFR-free materials**
  1. Helps member companies choose HFR-free materials
  2. Reinforces the limits needed by the industry to member laminators

The WG has paved the way for the industry to produce Environmentally Friendly Products with HFR-free Materials