Newest ED-Copper Foils for Low Loss / High Speed PCBs and for IC-Packaging Applications

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Abstract
The latest status of new ED copper foil developments is presented: ultra-flat profile for high speed digital boards and ultra-thin foil for finest pitch applications.

Copper surface roughness has become a significant factor influencing the losses in high speed PCBs, particularly as they move into the 10 GHz range and above. A new base foil has been developed which achieves very smooth surfaces.

The combination of the new base foil types and new fine pitch treatments increases the active surface between copper and resin, providing reliable bond strength to proprietary resin systems used for low loss applications.

Ultra-thin foils down to 2µ have been developed for modified semi-additive technology enabling the PCB producer to achieve finest pitch, down to L/S of 20µ/20µ as required in the latest IC-Packaging generation and for flexible printed circuits.

Combined with a proprietary primer resin coating, these new generations of ultra-low profile foils are designed for both, high speed applications and high density boards by increasing the bond strength on low loss and high TG resin systems.

Introduction
Since our planet gets more interconnected, the infrastructure needed to capture and work with the increasing amounts of data must respond and deliver faster results to more users. Numerous studies about the subject foresee that global IP traffic will again increase fourfold over the next 5 years. Between 2010 to 2015 a 32 percent growth rate is predicted [1].
In order to cope with an increased demand for improved resin systems with better electrical properties, many new dielectrics have already been introduced to the market and many others are at their final development stage.

BPA predicts for the period between 2009 and 2014 that laminates with loss factors Df @ 10 GHz of less than 0,005 may increase by 19% and with a Df @ 10 GHz between 0,010 and 0,005 by 57 % [2].

Several papers have shown that with increasing frequencies, overall transmission losses are becoming higher [3]. When the depth of penetration (so-called "skin depth") of the electromagnetic fields exceeds the root-mean-square roughness height, the influence of the roughness on the loss is minimal. With increasing frequency, the depth of penetration becomes smaller and currents flow near the surface, following the contour of that surface and thus resulting in an increased resistance because of the additional distance the currents must flow. At the highest frequencies, the depth of the penetration is much smaller than the roughness height and the additional loss caused by the roughness becomes almost independent of the frequency. At 10 GHz, the skin effect of copper is below 1µ.

The reduction of the foil's treatment profile has essential advantages since insertion loss and skin effect are widely improved and therefore allowing new opportunities in the antenna and high speed sector.

Methodology and Results
Typical ED copper foils prior to treatment have a typical roughness Rz ISO of ~7µ or around ~4µ for very low profile types. After treatment, such foils achieve a final roughness Rz ISO close to ~9µ for a regular matte side respectively ~6µ for a lower profile type.

For several years now, reverse treated foils are successfully used in some antenna applications and low noise amplifier boxes. Such foils achieve a final roughness of ~4µ.

In order to significantly reduce the foil's profile, a new ED copper foil type was developed. Prior treatment, such foils have a roughness Rz of ~1.5µ and less than 3µ after treatment:

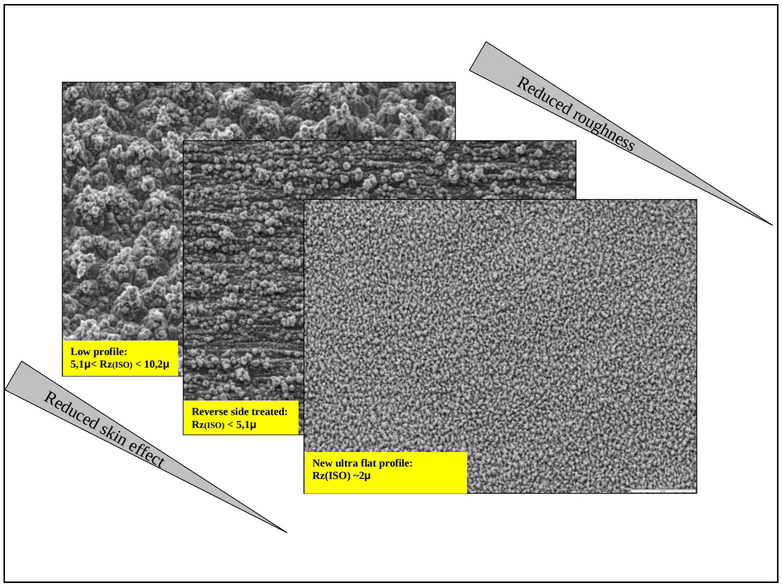

Figure 1 - Comparison of 3 different roughness profiles

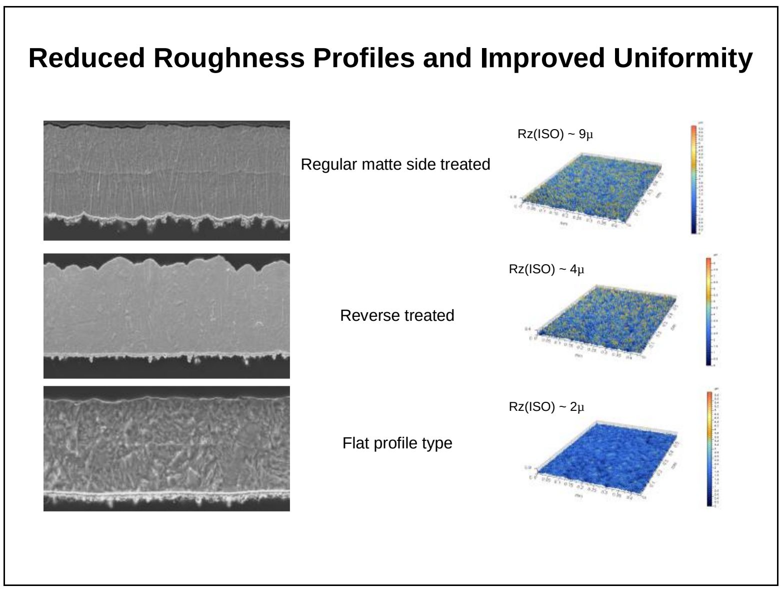

Figure 2 - Roughness profiles as cross sections and for uniformity

With an extremely dense and very uniform treatment, the new foil type offers a large contact area to the dielectric. This is illustrated by the treatment imprints after etching:

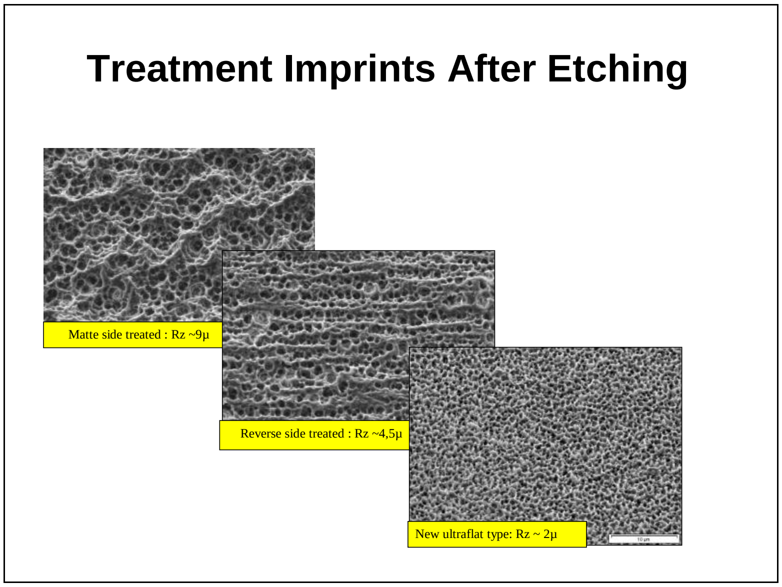

Figure 3 - Treatment imprints after etching

With several highly filled resin systems, mechanical anchorage of the treatment dendrites is the leading factor for bonding securely. With the new foil type, the reduced roughness profile compensates the mechanical anchorage by a much higher contact area. This is also improved because of a much higher uniformity of the fine dendritic treatment. Table 1 compares 4 different roughness profiles.

Table 1 - Comparison for the roughness profiles

Roughness of major foil types	**Rz ISO**	**Rz JIS**	**Rq = RMS**
Treated sides	**values in µm**		
Regular mat side treated foil type	~9	~7,5	~2
Mat side treated very low profile type	~5	~4	~1
Reverse treated foil type	~4	~3,5	~0,8
Flat profile type	~2,5	~2	~0,2

For a number of applications, the adhesion of the flat profile foil might be sufficient. Additional bonding strength is achieved by coating the same ultra flat profile foils with a thin layer of a primer coating. A 4µ layer of a proprietary resin system provides nearly identical bonding strength than high profile copper foils on the same resin systems. Table 2 illustrates the gain in bond strength on various resin systems.

Table 2 – Gain in peel strength with a 4µm primer layer

<table>
<tr><td colspan="2" rowspan="3">All values in lb/inch</td><td>Halogen free</td><td colspan="5">Low Loss Resin Systems</td></tr>
<tr><td>CCL 1</td><td>CCL 2</td><td>CCL 3</td><td>CCL 4</td><td>CCL 5</td><td>CCL 6</td></tr>
<tr><td>FR4</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="2">Df @ 10 GHz</td><td>> 0.010</td><td colspan="2">0.007–0.010</td><td>0.005–0.007</td><td colspan="2">< 0.005</td></tr>
<tr><td rowspan="2">12µ</td><td>as received</td><td>5.5–6.5</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>with Primer</td><td>7.5–8.0</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">18µ</td><td>as received</td><td></td><td>3.0–3.5</td><td>3.5–4.0</td><td>3.0–3.5</td><td colspan="2">3.0–4.0</td></tr>
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<tr><td rowspan="2">35µ</td><td>as received</td><td></td><td></td><td></td><td></td><td></td><td>3.5–4.0</td></tr>
<tr><td>with Primer</td><td></td><td></td><td></td><td></td><td></td><td>4.0–4.5</td></tr>
</table>

The rather new concept of using ultra flat profile copper foils with a primer coating opens new opportunities in high speed/low loss applications since the skin depth is much lower and the reduced bonding strength is more than compensated on many of the new resin systems.

Analysis
The influence of different roughness profiles was compared by extracting the overall loss of micro strips realized on dedicated test boards. The same study also investigated the impact of the thin Primer coating. The method used here was based on the Multiline TRL calibration algorithm, which makes it possible to extract the propagation constant and thus the loss of the interconnect, while removing all external and parasitic influences, as well as probe and contact pad disturbances. The study compared the extracted overall loss for various foil types on 2 different laminate materials over a frequency range from 0,1 GHz to 40 GHz. In total, 4 types of copper foil profiles have been studied: all with zinc free and arsenic free treatments; one ultra-flat profile foil type also had a primer coating. (Table 3).

Table 3 – Foil type for the study

Foil description	Rz JIS	Rq = RMS	Primer coating
Regular matte side treated low profile type	~ 4,6 µ	~ 1,1 µ	without
Regular shiny side treated very low profile type	~ 2,9 µ	~ 0,5 µ	without
New ultra flat profile type	~ 0,9 µ	~ 0,2 µ	without
New ultra flat profile type	~ 0,9 µ	~ 0,2 µ	with

2 types of low loss resin systems from 2 distinct Df groups have been selected: CCL A and CCL B.

Table 4 - Test vehicle build-up

CCL A		**CCL B**
0.009	Df @ 10 GHz	0.0065
1oz	Copper	1oz
2 x 106	Prepreg	2 x 1037
½ oz	Cu	½ oz
150µ	Core	200µ
½ oz	Cu	½ oz
2 x 106	PP	2 x 1037
1oz	Copper	1oz

Per roughness profile and laminate material, two test boards have been fully measured. In total, five sets of Multiline-TRL test structures on the top and bottom side of each test board, leading to 20 extracted propagation constants per roughness profile and laminate material have been generated.

Results and Discussion
Since two distinctly different materials have been selected (Df~0,009 vs. 0,0065 according to the data sheets), it is obvious that the overall loss for the material A is slightly higher than for the material B.

Irrespective the frequency range, the foil type having the highest roughness (regular matte side treated foil type) has also the highest loss. On both materials, the smoothest roughness profile has also the lowest loss. This is valid at high frequencies up to 40 GHz and for both resin systems: Figures 4 and 5.

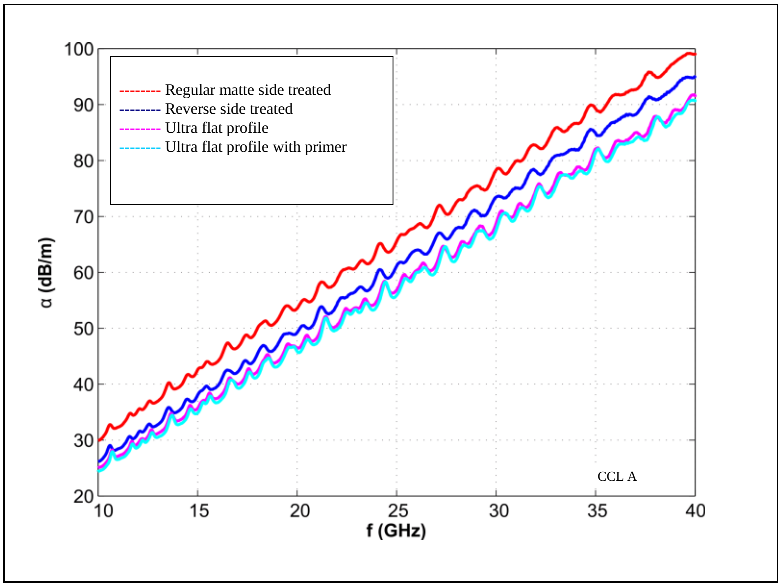


Figure 4 - High frequency range

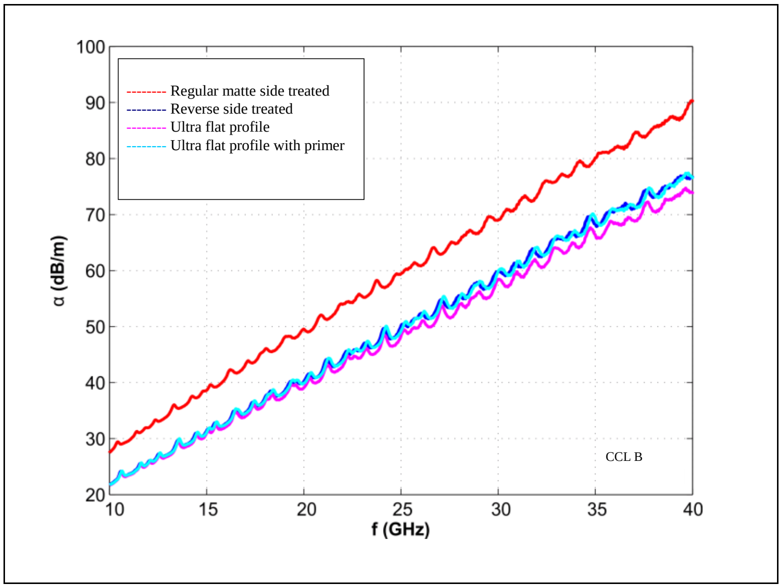


Figure 5 - High frequency range

Primer coating on the ultra-flat topography did not deteriorate the high frequency loss. On both materials and for frequencies up to 40 GHz, they showed very similar or better results.

Ultra-thin foils for finest pitch and IC-Packaging applications

Ultra-thin copper foils are typically ranging from 2µ up to 9µ and are plated on copper carrier foils that are most of time ½ oz. or 1 oz or 2 oz foils. Foils like 5µ or 9µ have gained larger usage in fine line applications. The protection from the carrier foil until it is peeled off the functional foil after lamination preserves a cosmetically perfect surface. Such thin copper layers may be obtained by starting with a 12µ foil that is „half etched"down to ~5µ. However, such a process does not allow to obtain the necessary uniformity in thickness; differences over the surface of the panel and variations between top and bottom are very common.

Using the same approach for obtaining copper foils with less than 5µ carries high risks but applications in chip scale packaging do require foils with 2 or 3µ functional layers. Such foils enable definitions of L/S down to 20/20µ.

For obtaining such finest line densities, ultra-thin foils have been developed with a special fine pitch treatment. Such functional foils have a very uniform and minute treatment with a roughness of less than 2µ Rz (ISO) and enabling flash etching through a modified semi-additive process (See Figures 6 and 7).

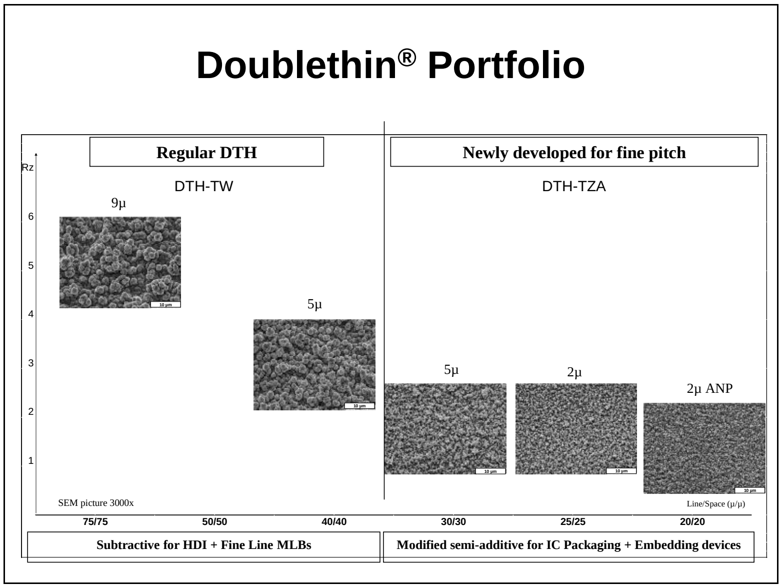


Figure 6 – Comparison of existing ultra thin Cu Foils

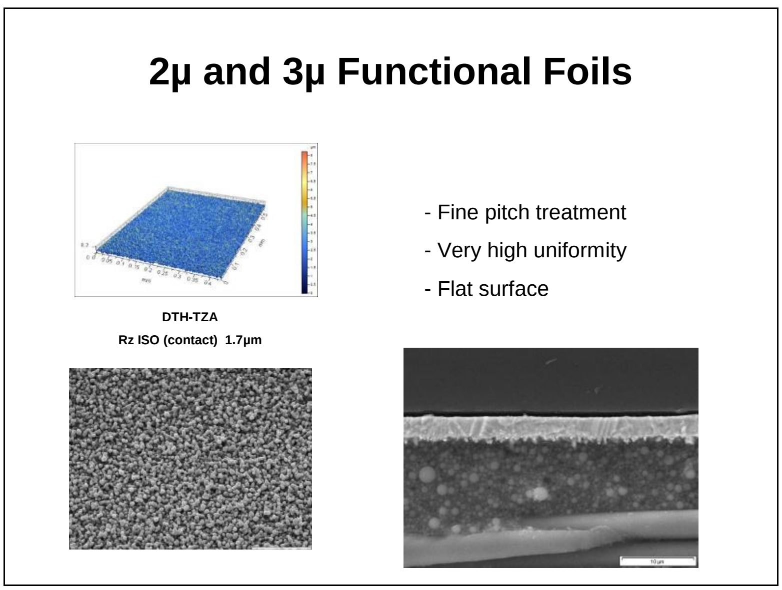


Figure 7 – Ultra Thin Foils with the new fine pitch treatment

The new types of carrier supported functional foils are used on resin systems like BT-resin systems that require high lamination temperatures. The easy to peel copper carrier allows a separation from the functional foil without inducing any kind of stress to the thin laminate construction. This enables also their utilization on thin flex laminates.

Despite the ultra flat treatment profile, the bond strength on various kinds of high TG resins is secure and can be further improved by using the version with a primer coating:

Table 5 – Peel Strength on BT resin systems

All values in N/mm (lb/inch)	Peel Strength of 2µ Functional Foils (3 mm tracks after 20µm build-up)					
	Values in N/mm					
	BT style 1		BT style 2		BT style 3	
	As received	After PCT	As received	After PCT	As received	After PCT
DTH-TZA	0.65 (3.70)	0.60 (3.40)	0.67 (3.80)	0.60 (3.70)	0.68 (3.90)	0.63 (3.60)
DTH-TZA + Primer	0.93 (5.30)	0.83 (4.70)	0.86 (4.90)	0.76 (4.30)	0.90 (5.10)	0.89 (5.10)
Lab press Pressure Cooker Test (PCT) @ 121°C for 1h						

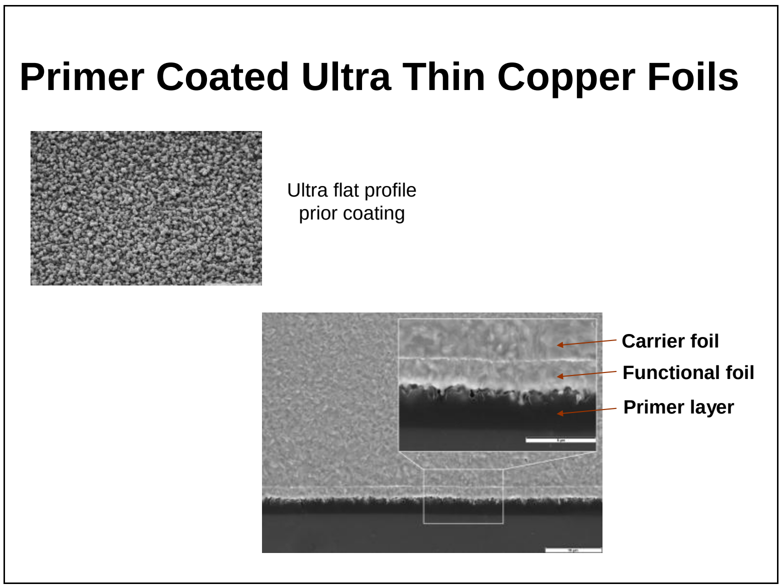


Figure 8 – Ultra Thin Foils with Primer

Embedding passive and active devices is a more recent approach for microelectronic component packaging where the highest levels of functional density, mechanical and thermal reliability and performance are demanded. Several techniques are now very close to market introduction including the European HERMES[4]. project. Embedding a bare die into the printed circuit board allows a very dense interconnection and a 3D integration. A single layer of embedded chips provides already room for passives or other SMD components on top, a multilevel embedding of components creates real 3D packages (Figure 9).

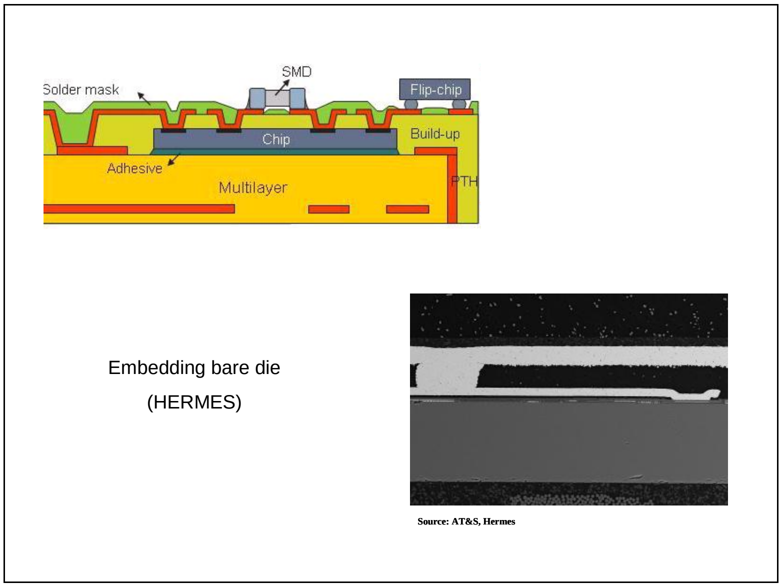


Figure 9 - Cross-section of a printed circuit board with an embedded silicon die

Outlook

Future foil profiles may further decrease towards so-called “almost no profile” types with roughness Rz of less than 1µ.

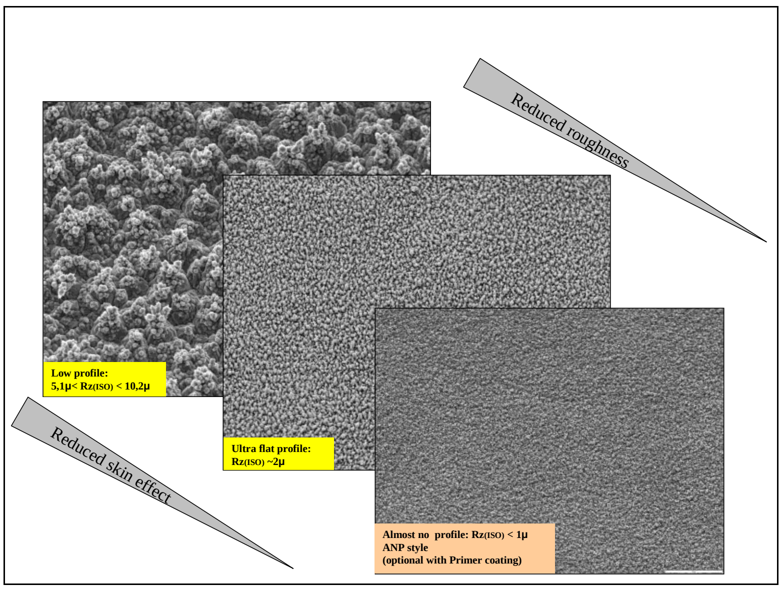


Figure 10 - Future trend: almost no profile treatments

It is obvious, that such foils will mainly work with appropriate primer coatings that could compensate the lower bond strength.

Summary and Conclusions

A new approach for high speed/low loss copper foils has been discussed. The reduced treatment profile improves the electrical properties of the copper clad laminate. Despite a flat profile, bonding strength is sufficient on most resin systems. It has been shown that the combination of the flat profile copper and a proprietary primer coating exhibits a secure bonding to most of the low loss resin systems and that the thin primer coating does not affect the electrical performance up to 40 GHz.

For IC packaging and very dense fine line boards, a newly developed family of ultra thin foils from 2µ to 5µ with reduced foil profiles was presented. The very uniform treatment allows extreme fine pitch down to L/S of 20µ/20µ.

The same foils with primer coating are advantageously used in CSP applications and embedded chip technologies.

References

[1].Cisco® VNI global IP traffic forecast: http://www.cisco.com
[2].BPA Report 921: http://www.bpaconsulting.com
[3].A. F. Horn , III, J. W. Reynolds, P. A. LaFrance, and J. C. Rautio, ‘‘Effect of conductor profile on the insertion loss, phase constant, and dispersion in thin high frequency transmission lines’’, DesignCon2010, Santa Clara, February 2010.
[4] HERMES: http://www.hermes-ect.net

APEX EXPO IPC 2012

Newest ED-Copper Foils for High Speed PCBs and for IC-Packaging Applications

Raymond GALES

CIRCUIT FOIL

APEX EXPO IPC San Diego, February 28, 2012 – March 1, 2012

Agenda

- High Speed & Low Loss CCL
  - New requirements for ED copper foils
    - Minimalist effects for up to 40 GHz
- Ultra thin foils
  - Trends and Realizations
  - Primer coated version as viable concept
- Outlook and Conclusions

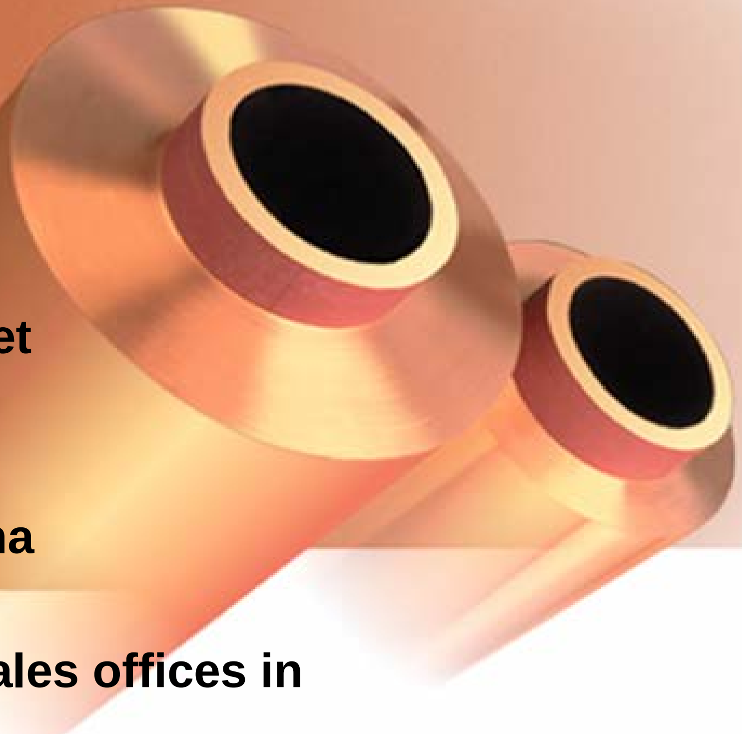
Circuit Foil: Global Presence

- Corporate of CF Group
- Total capacity of:

  ~ 41 Mio m²/year
- Sheeting & Tooling for European PCB market

Slitting + Sheeting Centers in

Granby / Canada and Shanghai / China



Sales offices in

Philadelphia / USA and Hong-Kong

Dedicated to Quality

Agenda

- **High Speed & Low Loss CCL**
  - **New requirements for ED copper foils**
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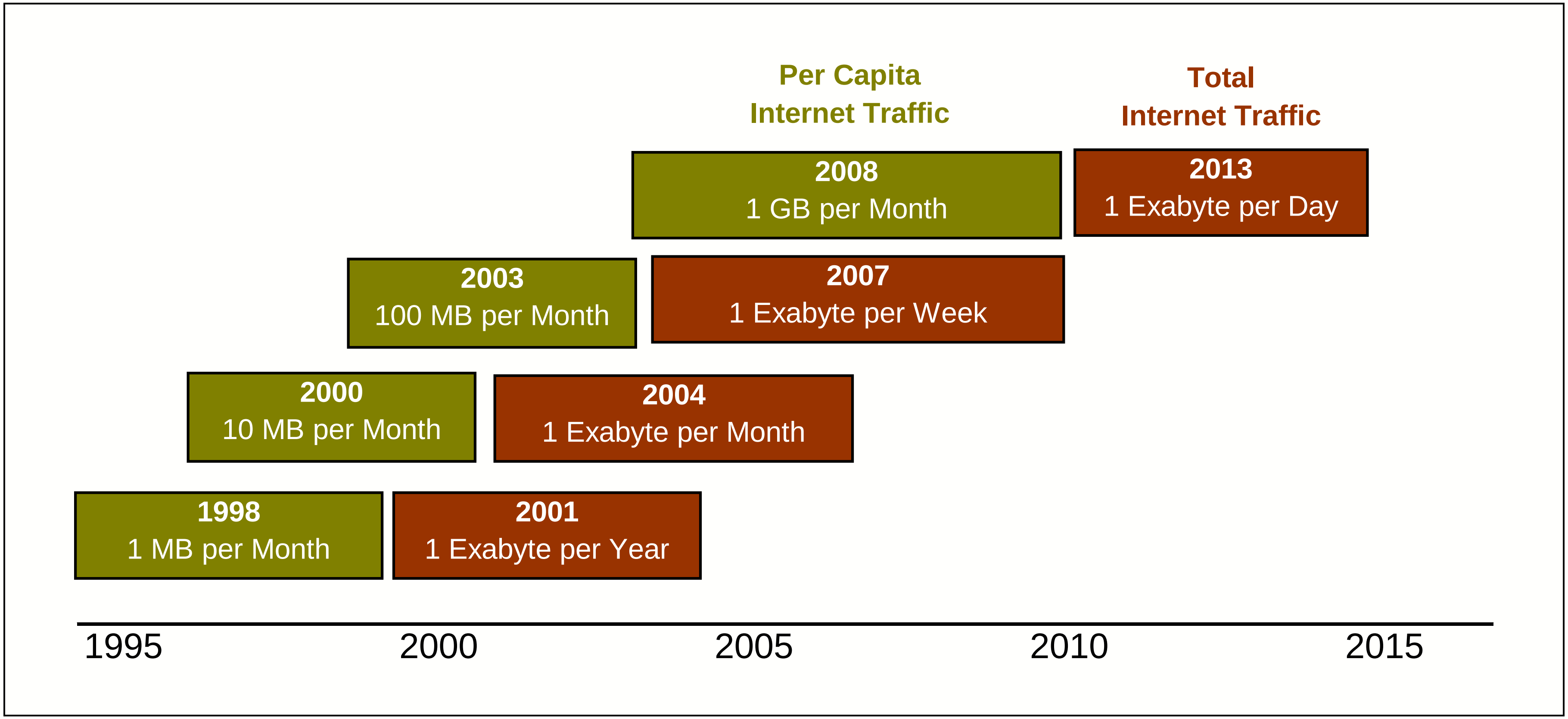
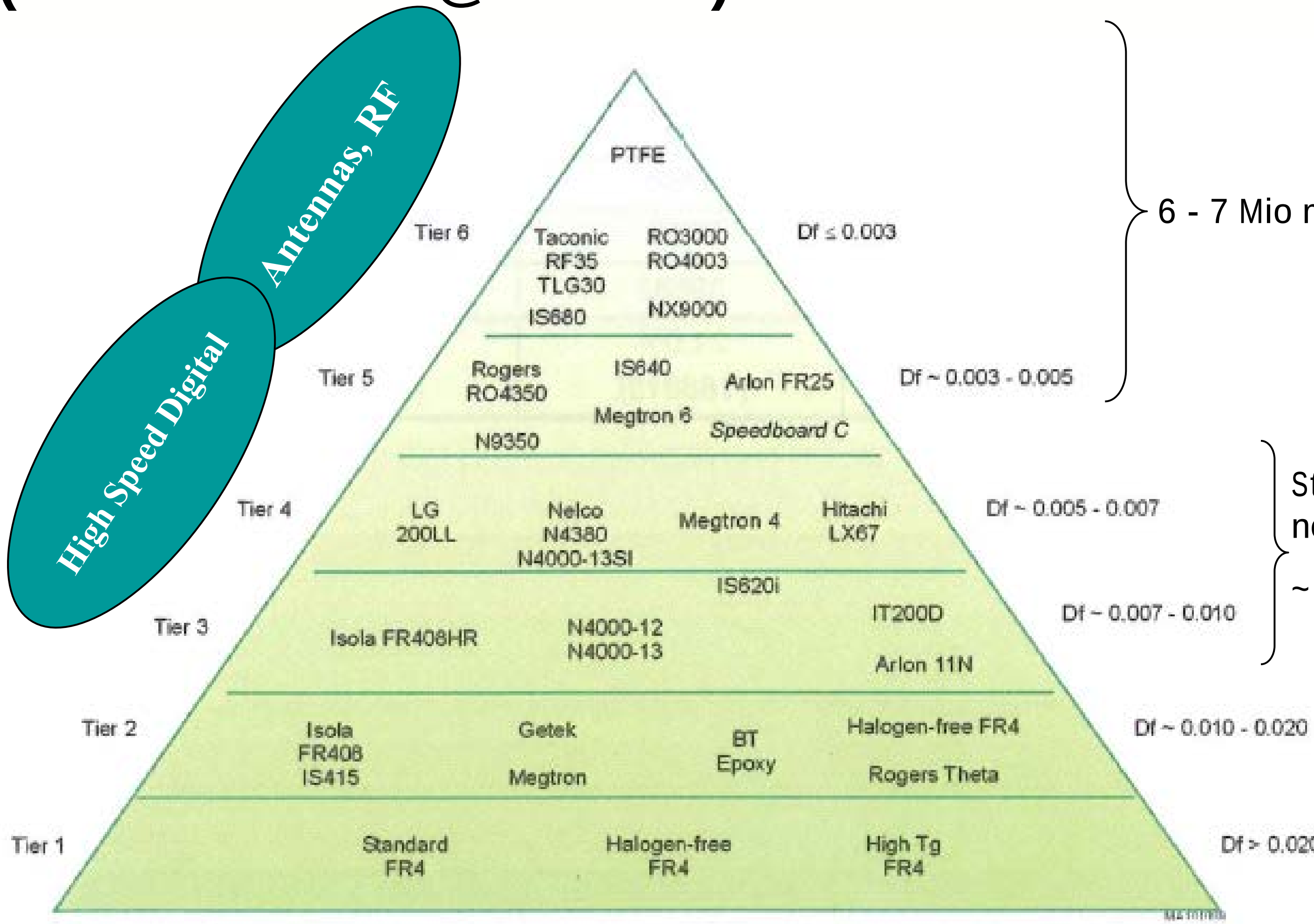
Traffic Forecast



Source: CISCO VNI, 2011

Low Loss Laminate Market

(Loss factor Df @ 10 GHz)



6 - 7 Mio m²

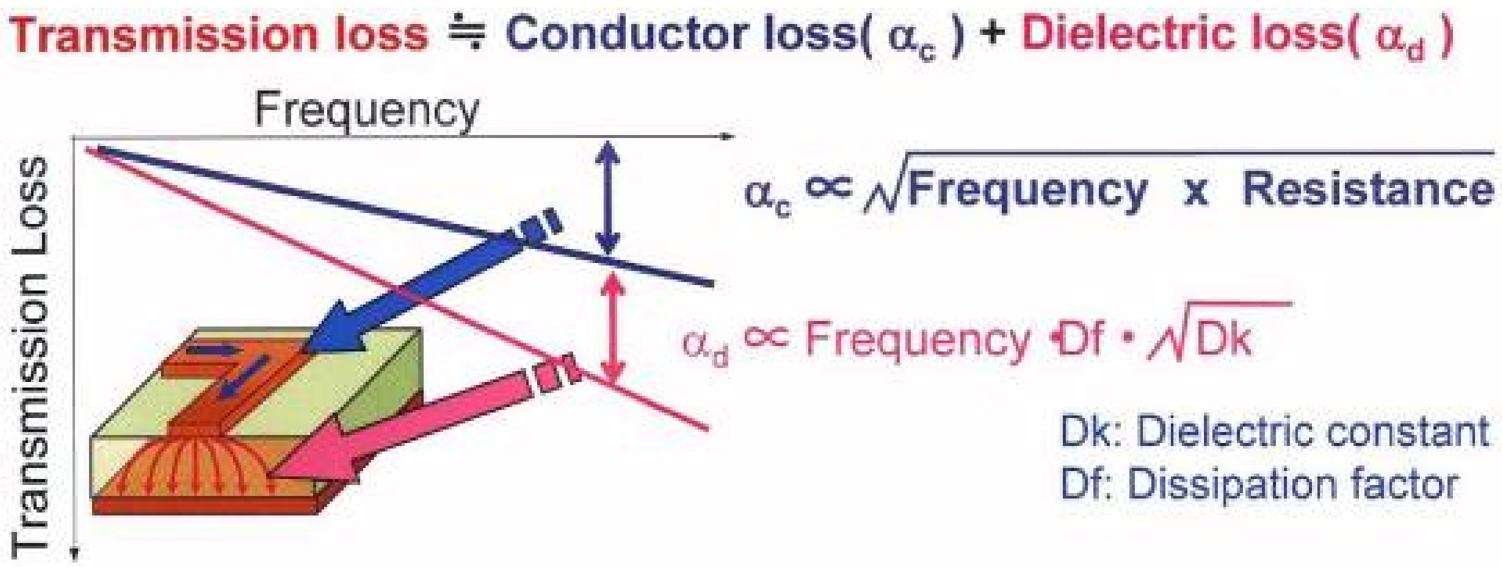
Strongest increase over next years:

~ 14-16 Mio m²

Source: BPA

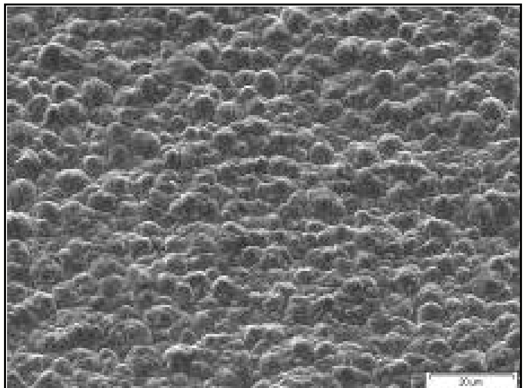
Main Driving Factors

- With increasing frequencies, overall transmission losses are becoming higher and losses linked to skin effect will add up
  - above 5 Gb/sec, dielectric losses start dominating over skin effect losses

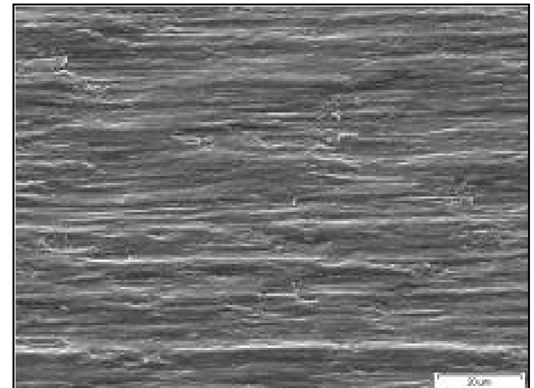


Source: Hitachi Chemical

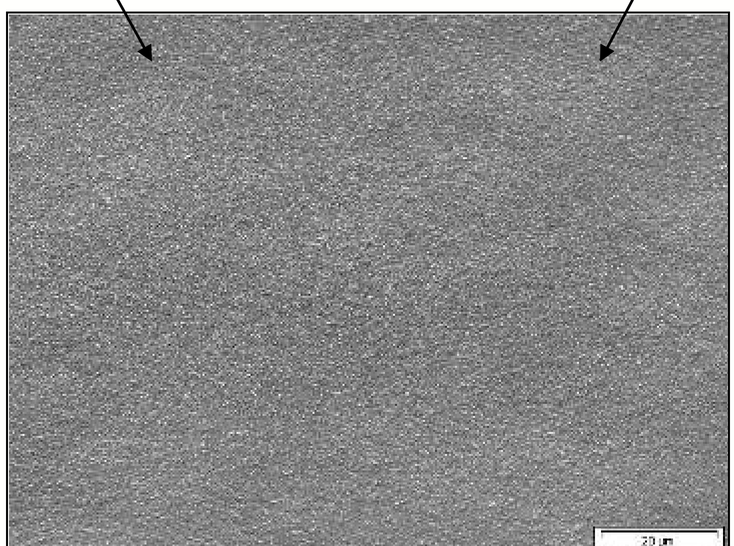
Comparison prior Treatment



Matte side treated :
Rz ~7µ

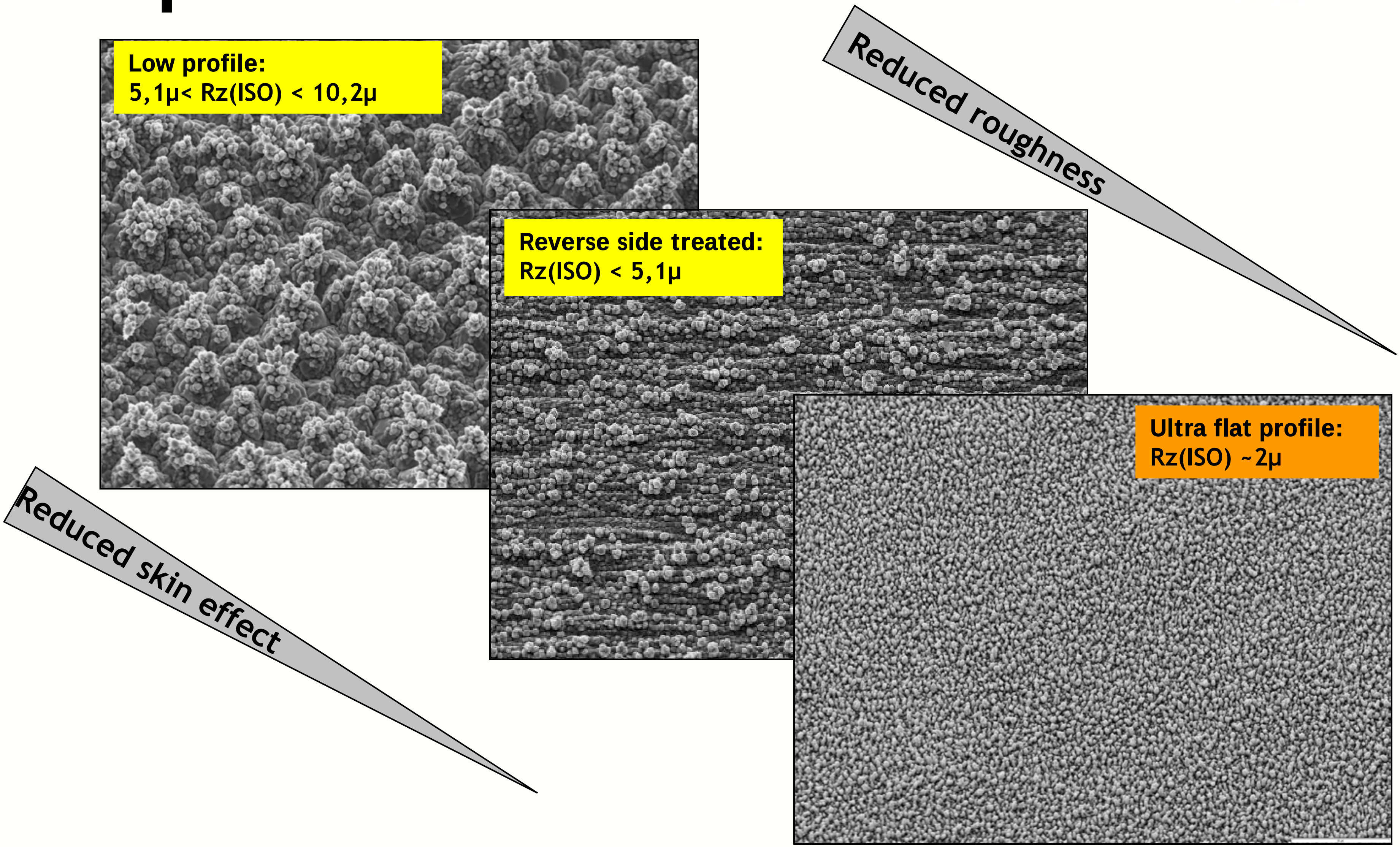


Reverse side treated:
Rz ~2,5µ

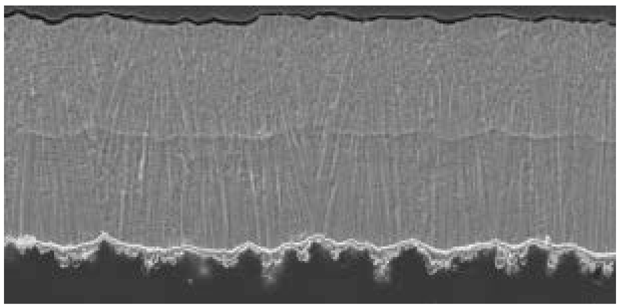


New ultraflat type:
Rz ~ 1µ

Comparison after Treatment

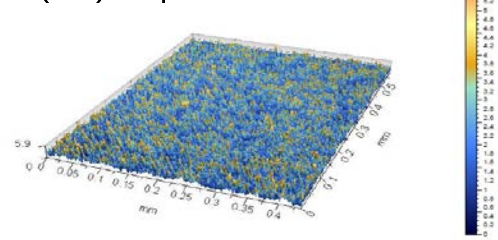


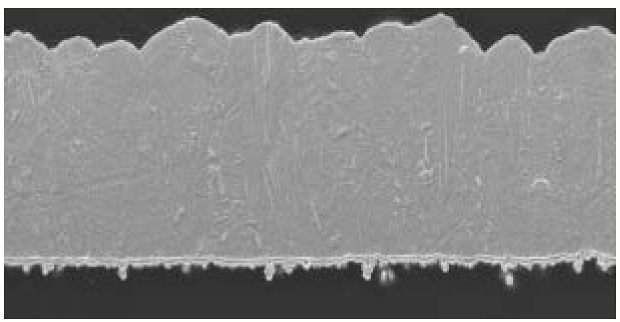
Reduced Roughness Profiles



Regular matte side treated

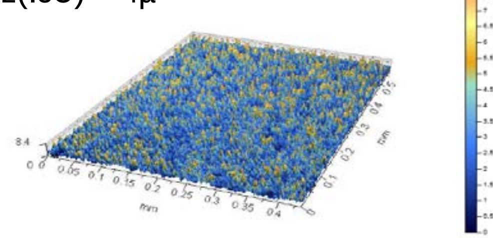
Rz(ISO) ~ 9µ

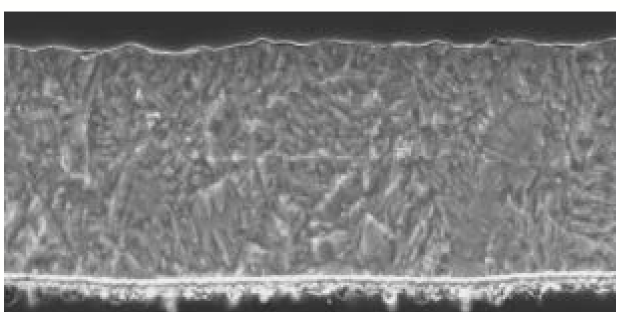




Reverse treated

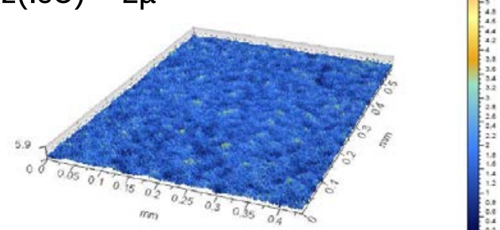
Rz(ISO) ~ 4µ



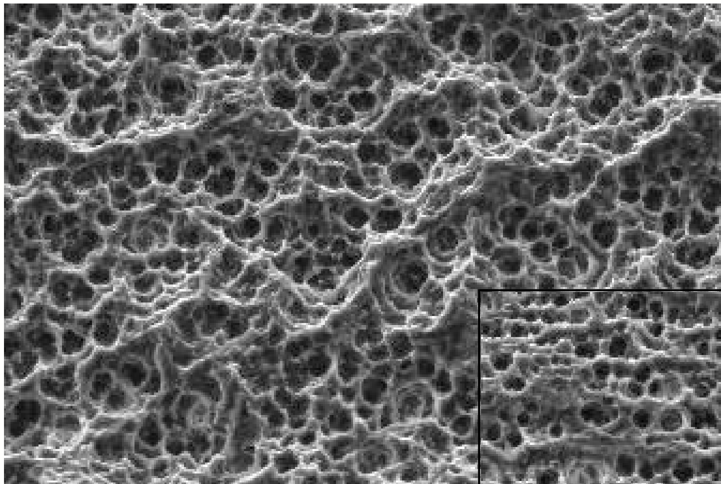


Ultra flat profile type

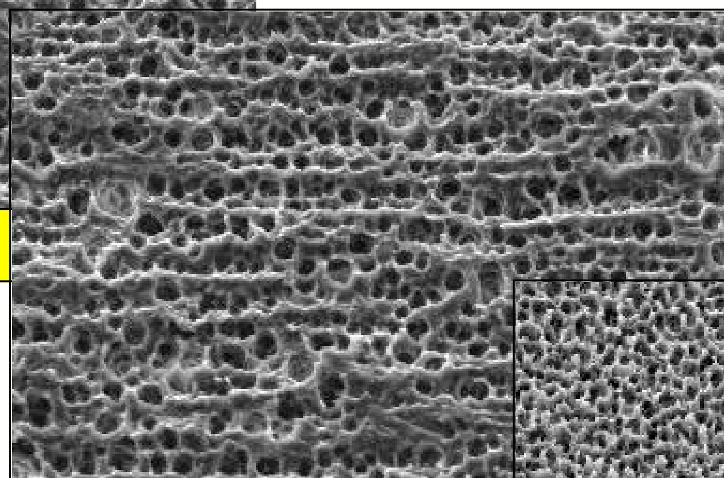
Rz(ISO) ~ 2µ



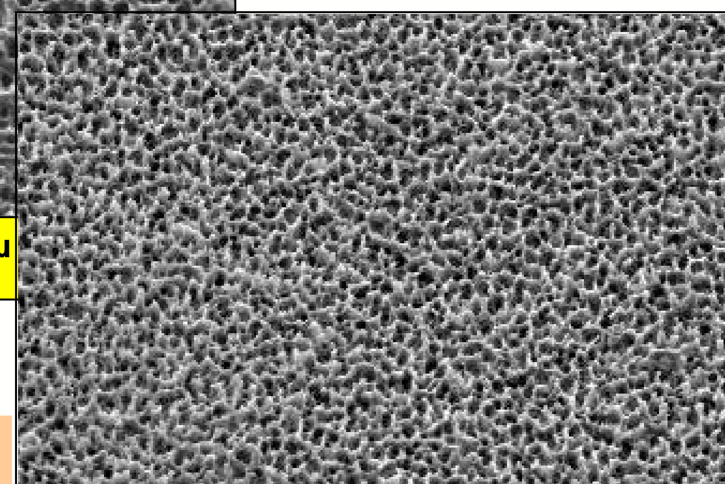
Treatment Imprints After Etching



Matte side treated : Rz ~9µ



Reverse side treated : Rz ~4,5µ



Ultra flat type: Rz ~ 2µ

high active surface
much higher uniformity

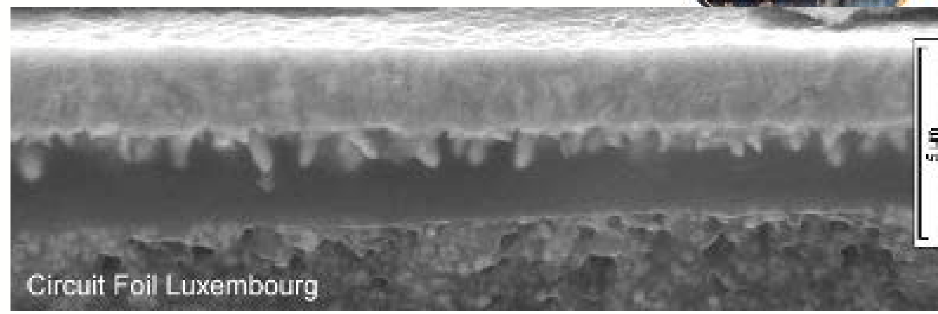
Peel Strength

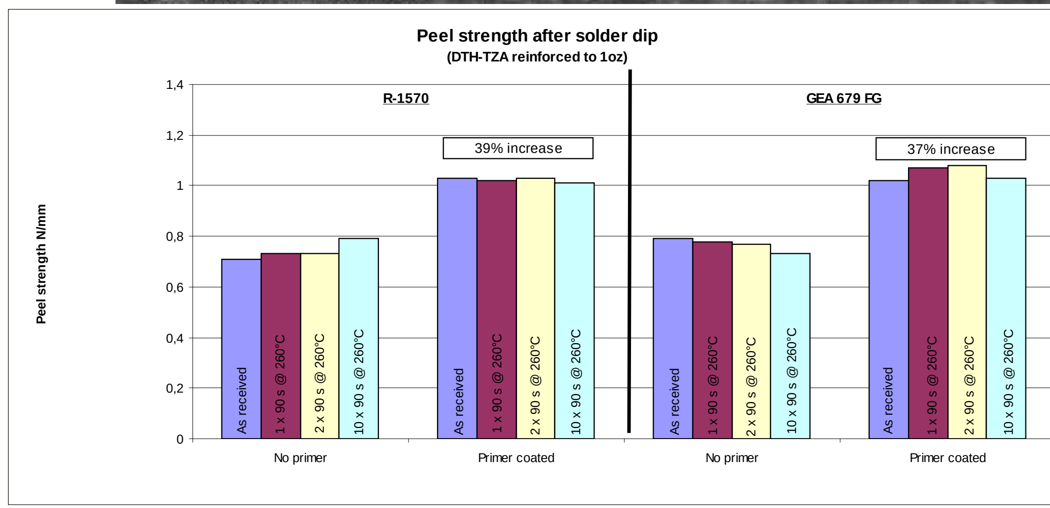
		Halogen free	**Low Loss Resin Systems**				
		CCL 1	**CCL 2**	**CCL 3**	**CCL 4**	**CCL 5**	**CCL 6**
All values in lb/inch		FR4					
Df @ 10 GHz		> 0.010	**0.007-0.010**		**0.005-0.007**	**< 0.005**	
12µ	as received (not reinforced)	5.5-6.5					
18µ	as received (not reinforced)		**3.0-3.5**	**3.5-4.0**	**3.0-3.5**	**3.0-4.0**	
35µ	as received						**3.5-4.0**

Ultra flat profile Cu has secure Peel Strength on many resin systems

Primer Coating

- Main Goal:
  - Peel Strength increase by >30% on most low loss resins without degradation of other properties
- Major Properties:
  - Thin layer of 3µm:
  - TG ~150° C (DSC)
  - Halogen Free: <900ppm
  - High Thermal Resistance
    - No degradation after multiple solder dips
    - Late thermal degradation
      - 5% after >1 hr @ >340° C
  - High Chemical resistance
    - No additional losses in desmear chemistries





Weight Loss of	At Temperature ° C	After minutes
1%	~313	~72
5%	~346	~78
10%	~363	~82

Improved Peel Strength

All values in lb/inch		Halogen free	Low Loss Resin Systems				
		CCL 1	**CCL 2**	**CCL 3**	**CCL 4**	**CCL 5**	**CCL 6**
		FR4					
Df @ 10 GHz		> 0.010	**0.007-0.010**		**0.005-0.007**	**< 0.005**	
12µ	as received (not reinforced)	5.5-6.5					
	with Primer (not reinforced)	***7.5-8.0***					
18µ	as received (not reinforced)		**3.0-3.5**	**3.5-4.0**	**3.0-3.5**	**3.0-4.0**	
	with Primer (not reinforced)		***5.0-5.5***	***6.0-6.5***	***5.0-5.5***	***5.0-5.5***	
35µ	as received						**3.5-4.0**
	with Primer						***4.0-4.5***

Primer Coated version can increase Peel Strength on many low loss resin systems

Independent Study

- 4 roughness profiles have been compared

RMS-RQ

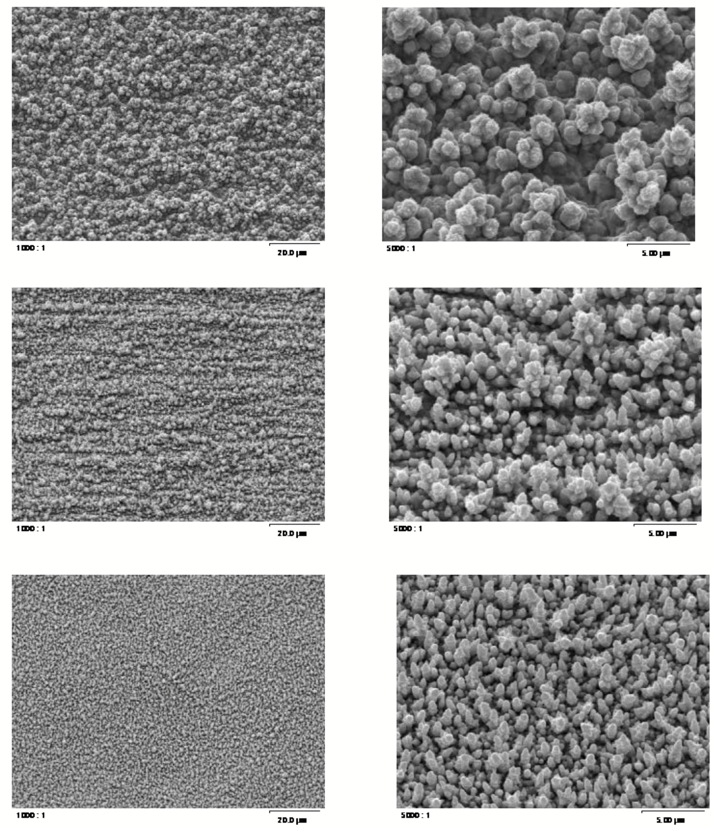
Treated side

- Low profile, matte side treated: Rz JIS ~4.6µ
  HFI-LP: zinc free — ~1.1µ

- Low profile, reverse side treated: Rz JIS ~2.9µ
  HFZ-B: zinc + arsenic free — ~0.5µ

- Flat profile, matte side treated: Rz JIS ~0.9µ
  BF-TZA: zinc + arsenic free

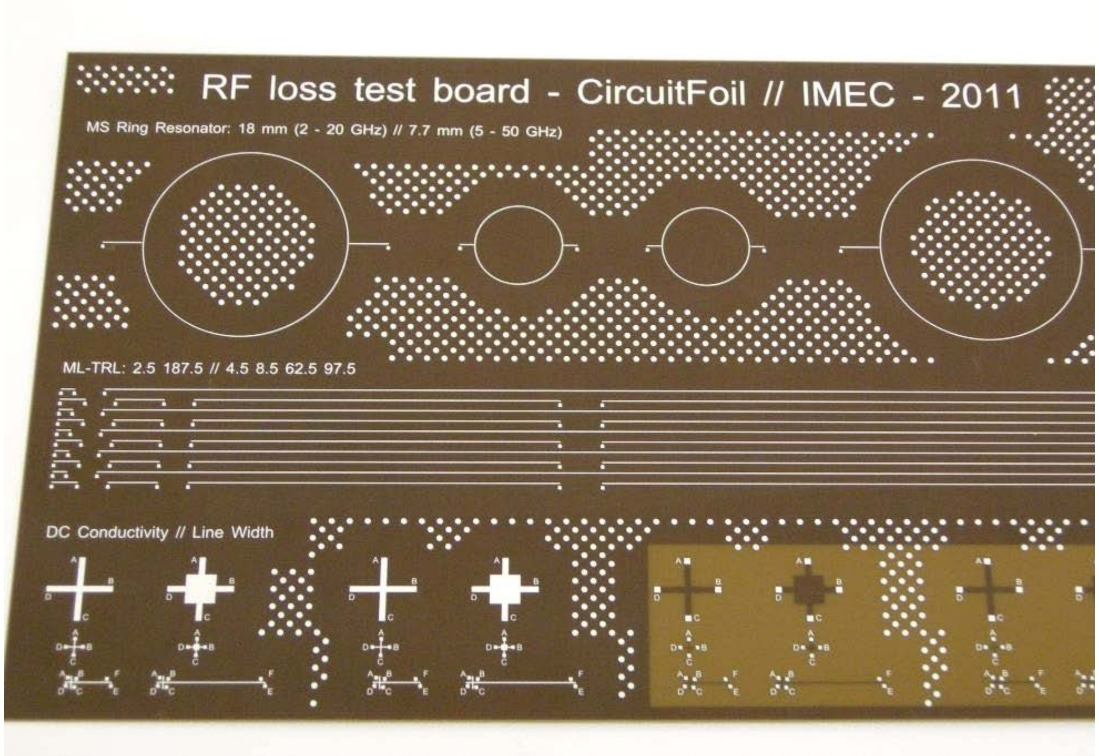
- Flat profile with Primer coating: Rz JIS ~0.9µ
  BF-TZA: zinc + arsenic free with Primer — ~0.2µ

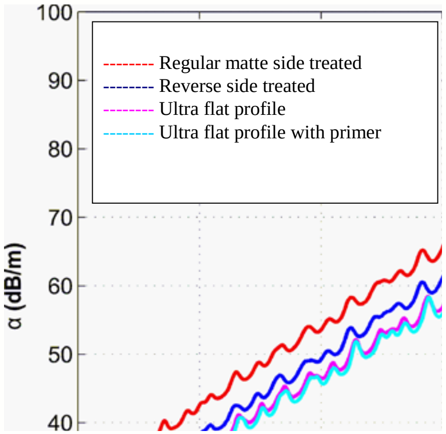


1000 x | 5000 x

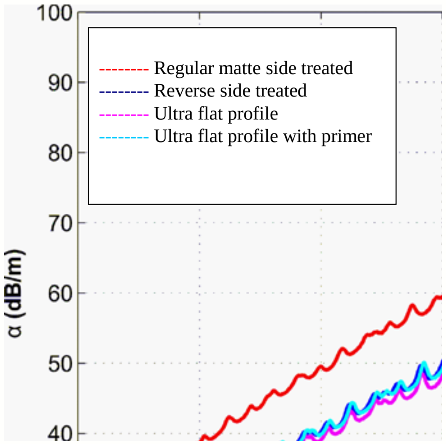
Test layout

- Microstrip lines [Multiline TRL (ML-TRL) calibration algorithm] and frequency up to 50 GHz





CCL A



CCL B

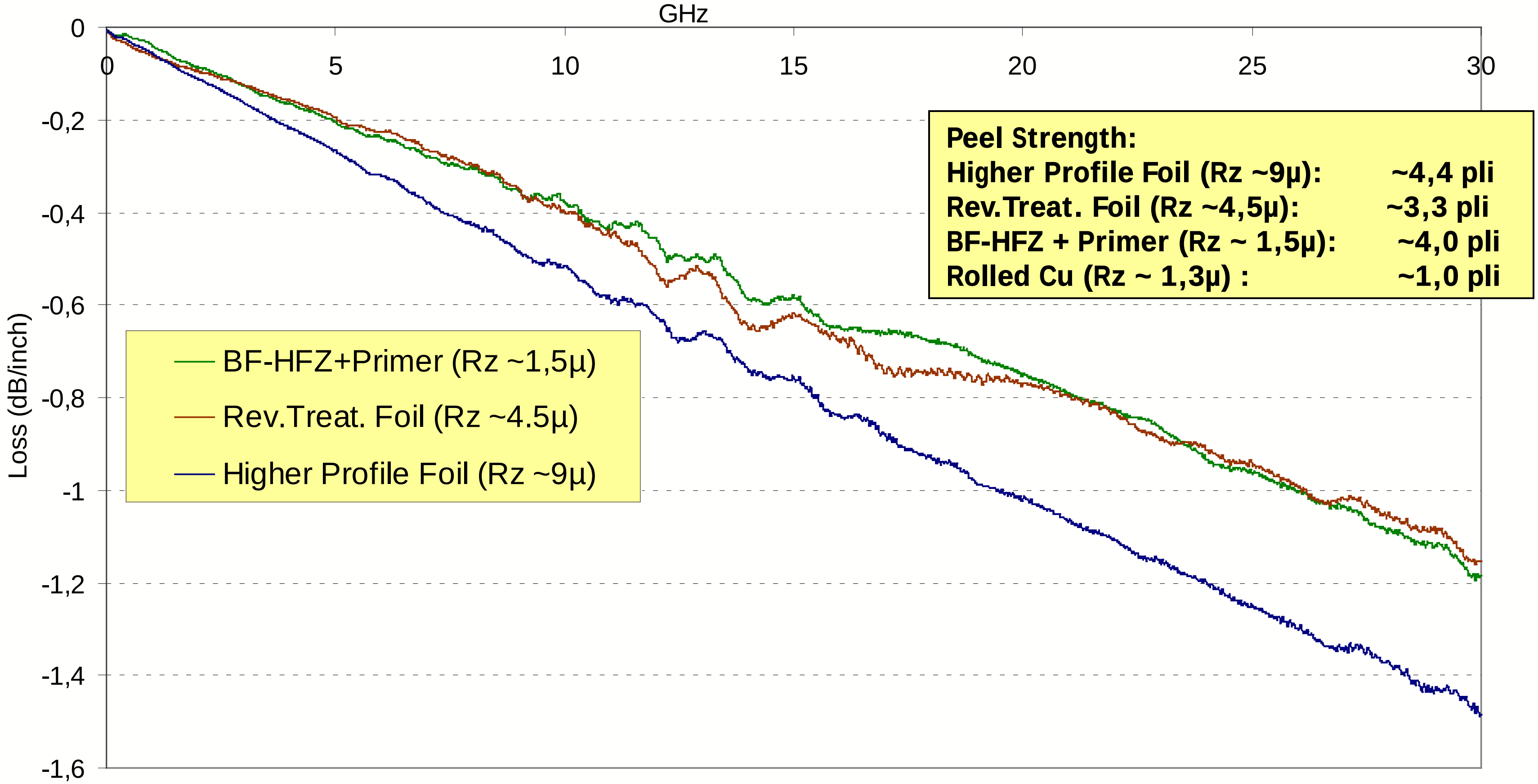
Df ~0.007-0.010 @ 10 GHz	Df ~0.005-0.007 @ 10 GHz
(Tier 3)	(Tier 4)

Ultra flat profile foils generate lower transmission losses

Primer Coated Ultra flat profile foils generate similar low transmission losses but they increase the Peel Strength

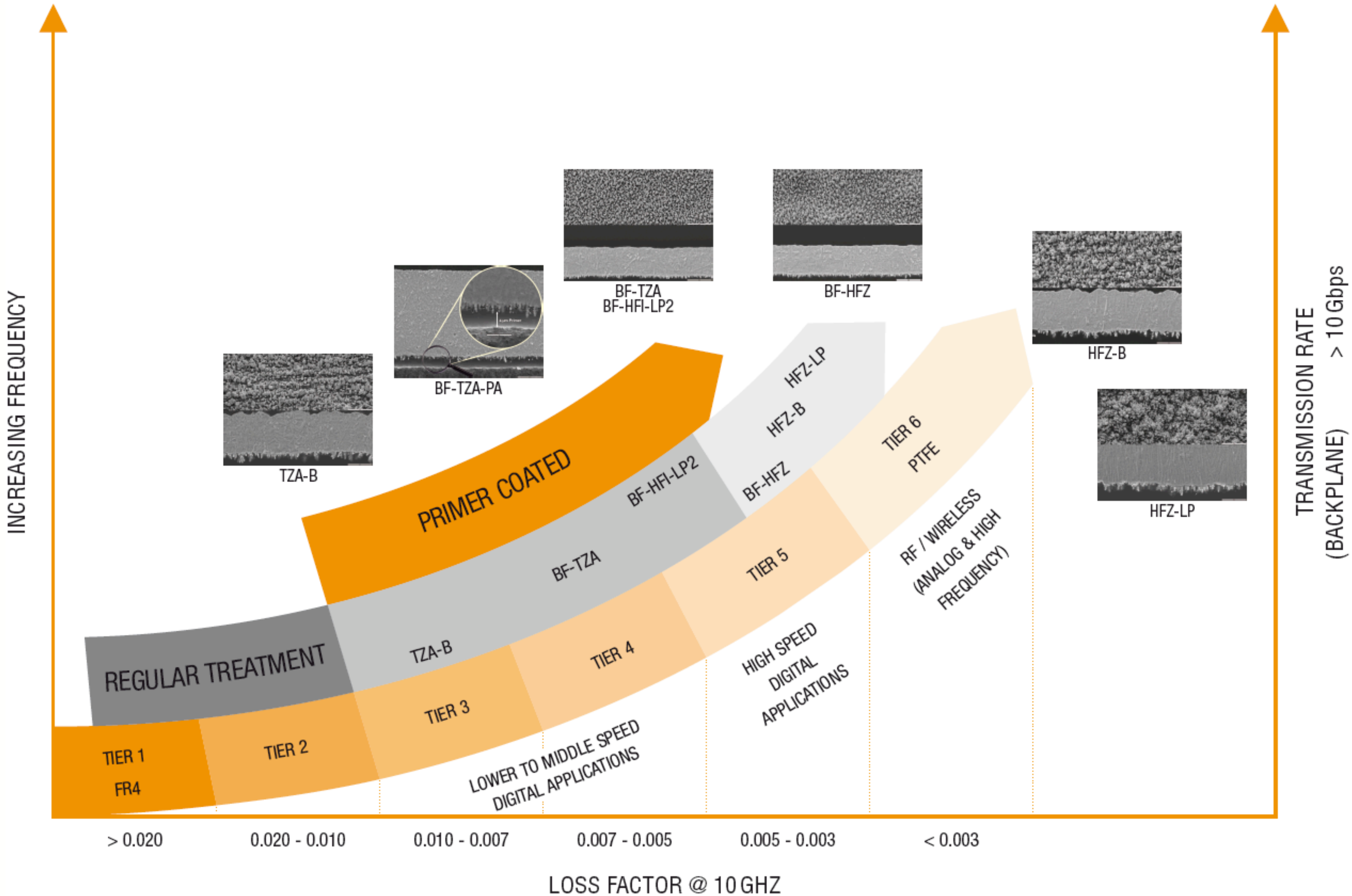
Microstrip Insertion Loss

Resin Type : Df ~0,0055 @ 10 GHz   1/2oz foils   50Ω

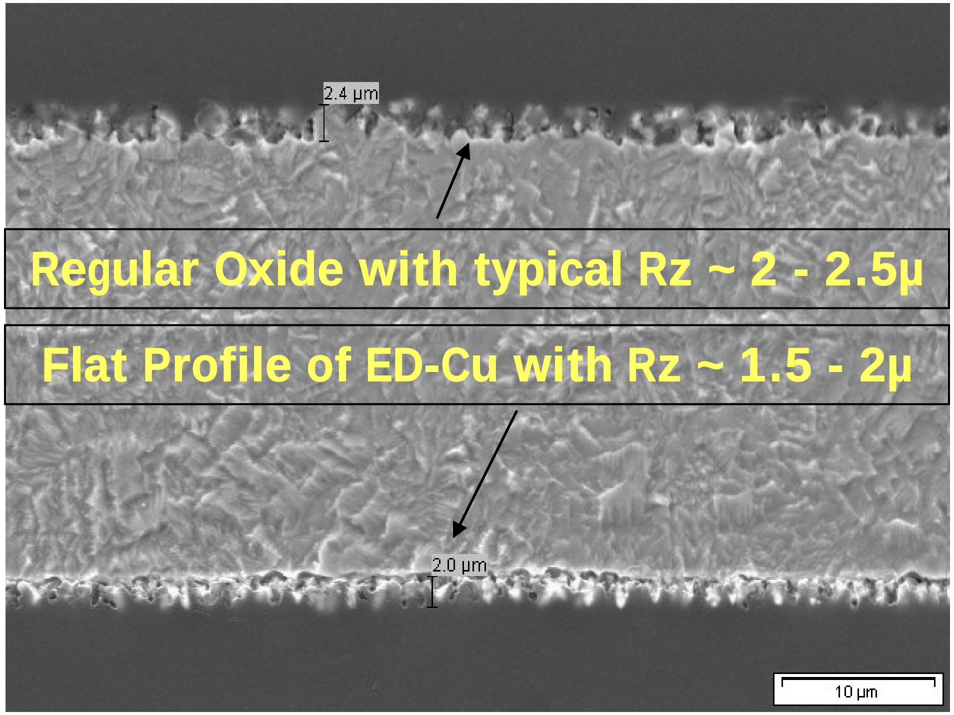


(Customer data)

Low Loss Systems



Further possible evolution



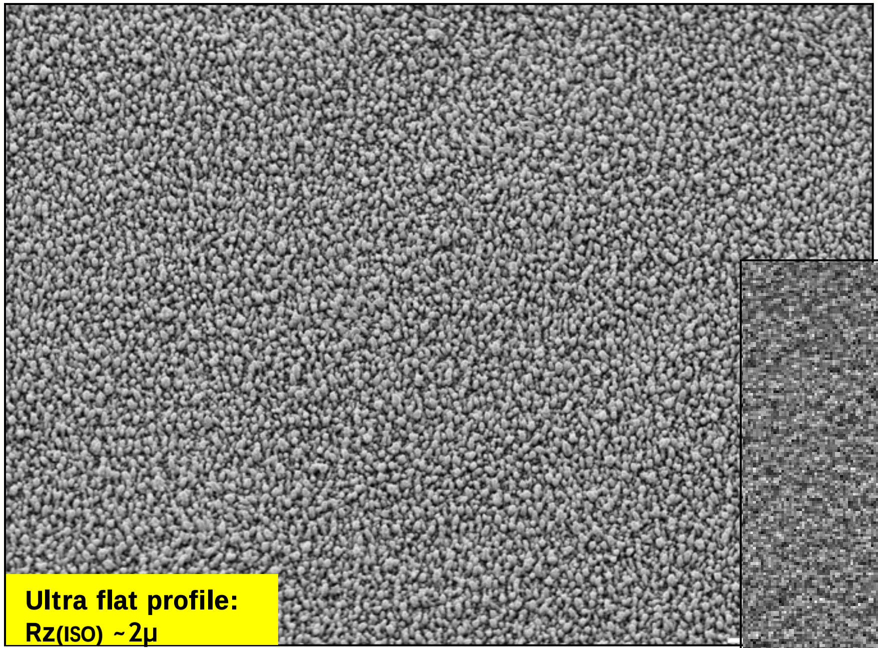
- Reduced profile of the innerlayer oxide

  → Non Etching Adhesion Promotor type

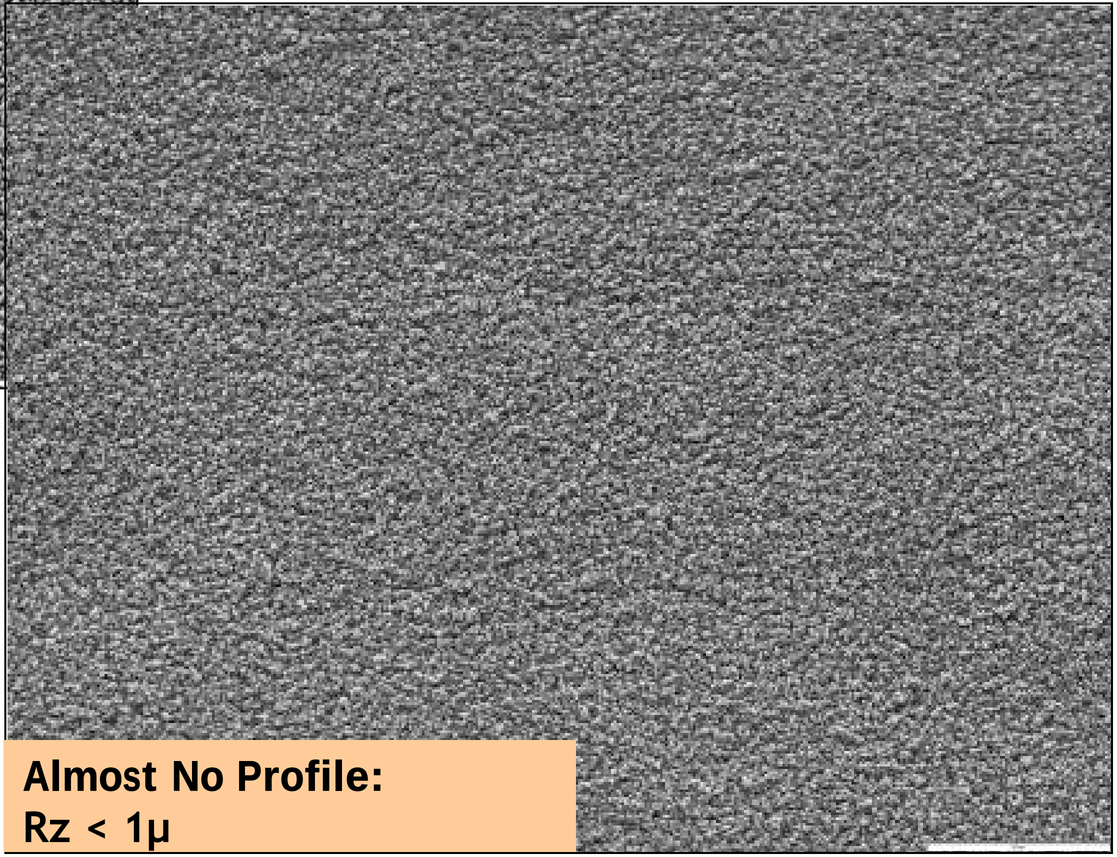
- Reduced profile of the foil's treatment

  → Almost No Profile

Outlook



Ultra flat profile:
Rz(ISO) ~2µ



Almost No Profile:
Rz < 1µ

Agenda

- High Speed & Low Loss CCL
  - New requirements for ED copper foils
    - Minimalist effects for up to 40 GHz
- **Ultra thin foils**
  - **Trends and Realizations**
  - **Primer coated version as viable concept**
- Outlook and Conclusions

General Design Rules

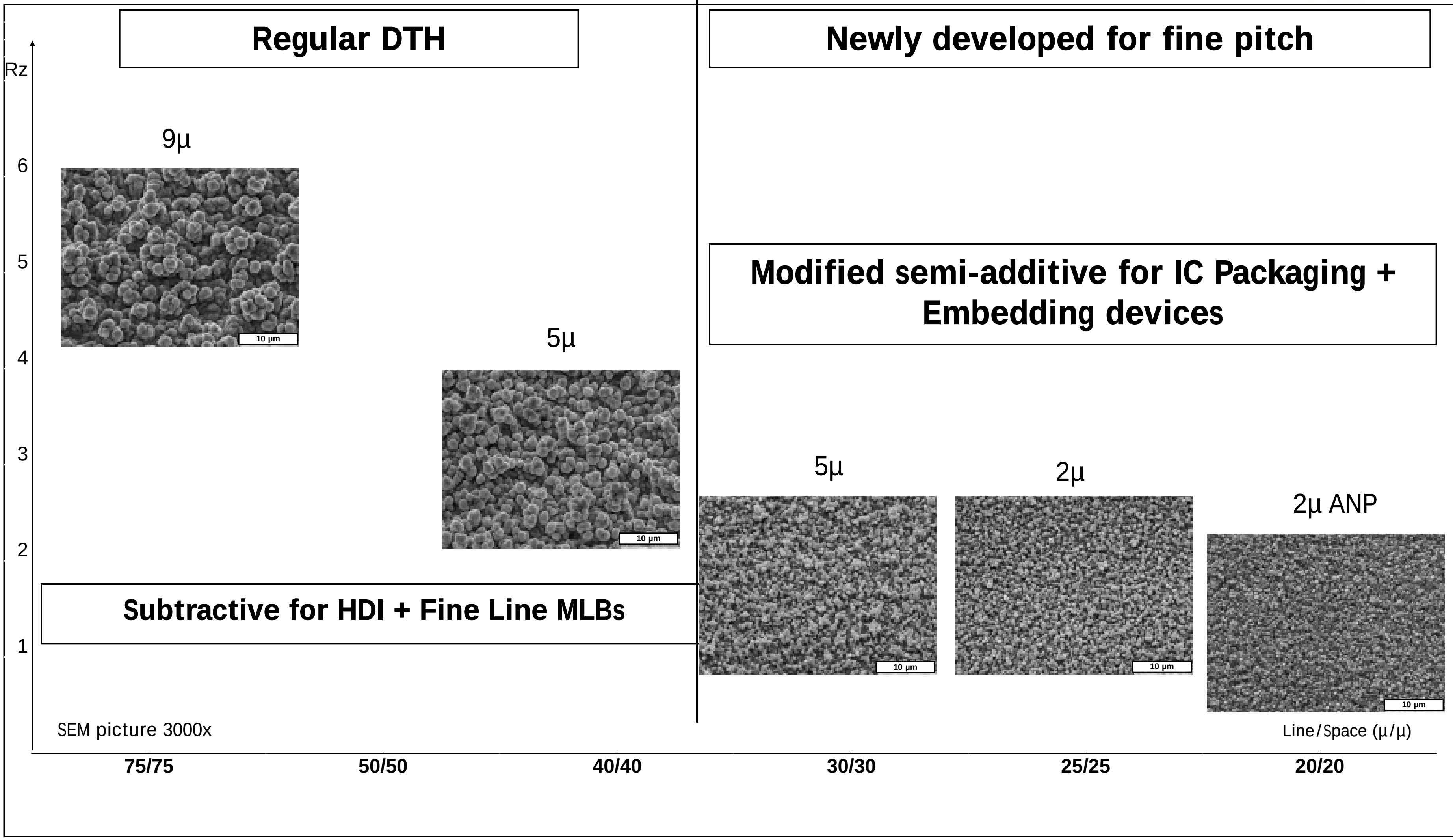
Motherboard:		Pad Pitch (mm)	Space width (µm)	Line width (µm)	Via diameter (µm)
FBGA (CSP)	1 line/via	0.30	50	50	75
		0.20	30	40	50
		0.15	**25**	**25**	**40**
		0.10	**18**	**18**	**30**

Substrates:		Pad Pitch (mm)	Space width (µm)	Line width (µm)	Via diameter (µm)
FC	2 lines/via	0.18	**18**	**18**	55
		0.15	**15**	**15**	**35**
		0.13	**15**	**15**	**25**
	3 lines/via	0.18	**10**	**10**	55
		0.15	**8**	**10**	**35**
		0.13	**8**	**10**	**25**

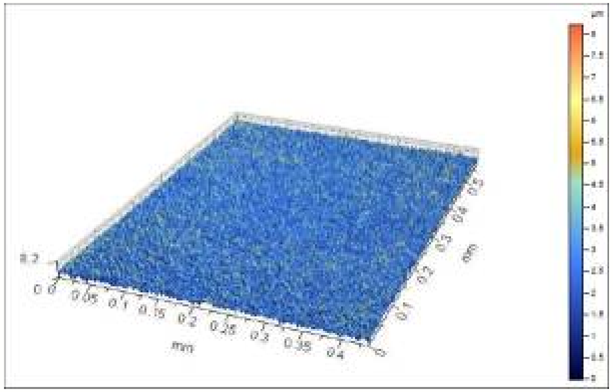
(Modified) Semi-additive Process MSAP

UV-Yag / Excimer Laser

Doublethin


Regular DTH
Newly developed for fine pitch
Rz
6
5
4
3
2
1
9µ
5µ
Modified semi-additive for IC Packaging + Embedding devices
5µ
2µ
2µ ANP
Subtractive for HDI + Fine Line MLBs
10 µm
SEM picture 3000x
Line/Space (µ/µ)
75/75
50/50
40/40
30/30
25/25
20/20

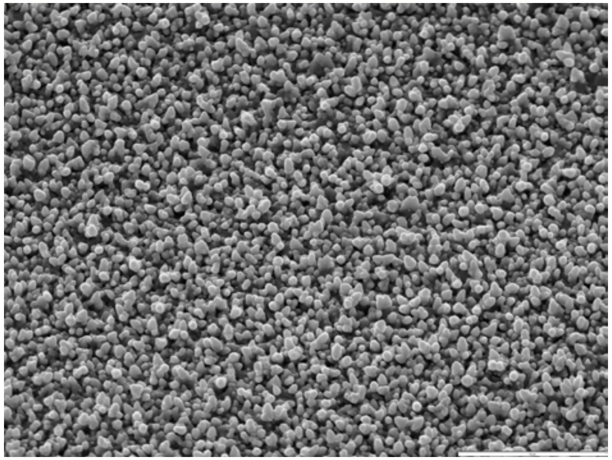
2µ and 3µ Functional Foils

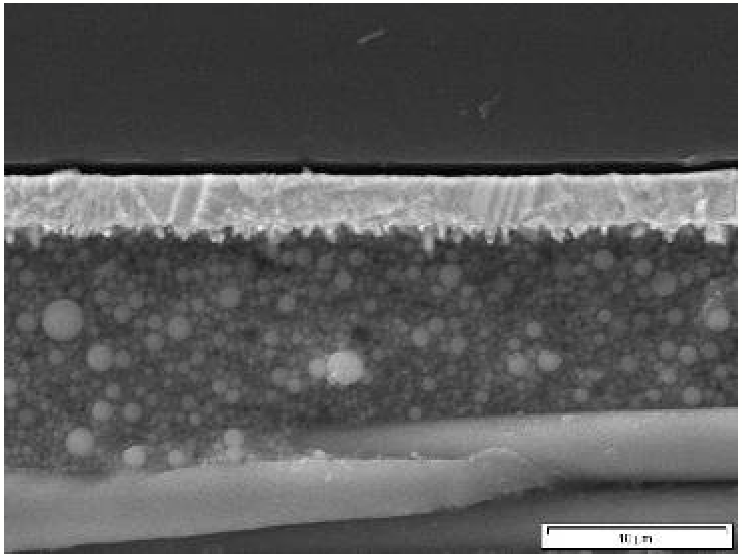


DTH-TZA

Rz ISO (contact) 1.7µm

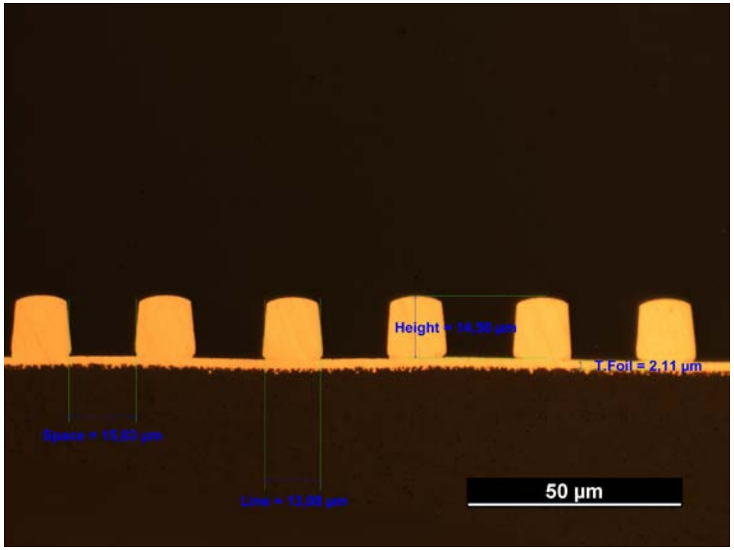
- Perfect protection and easy handling due to the Cu carrier
- Very accurate and uniform thickness of the functional foil
  - Much more precise than by half etching
- Fine pitch treatment
  - Arsenic free

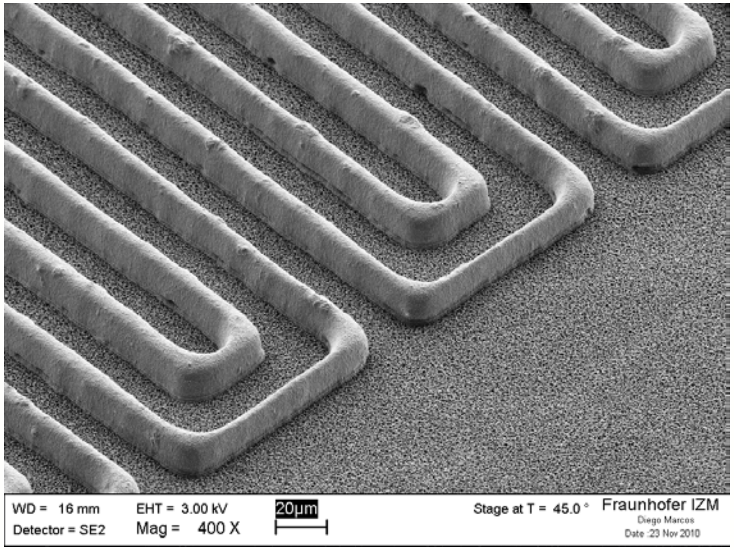




Fine Pitch Definition

- Modified semi-additive process (MSAP) and flash etching allows finest pitch, down to L/S of 15µ/15µ



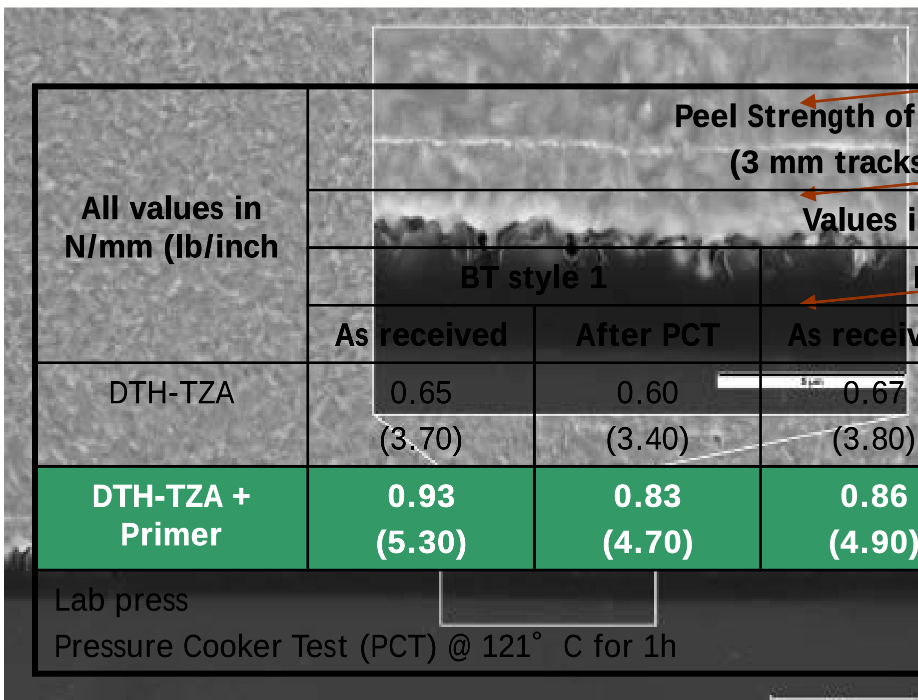


Source: Fraunhofer IZM

Peel Strength

All values in N/mm (lb/inch	Peel Strength of 2µ Functional Foils on BT (3 mm tracks after 20µm build-up)					
	Values in N/mm (lb/inch)					
	BT style 1		BT style 2		BT style 3	
	As received	After PCT	As received	After PCT	As received	After PCT
DTH-TZA	0.65 (3.70)	0.60 (3.40)	0.67 (3.80)	0.60 (3.40)	0.68 (3.90)	0.63 (3.60)
Lab press Pressure Cooker Test (PCT) @ 121° C for 1h						

Primer Coated Ultra Thin Copper Foils

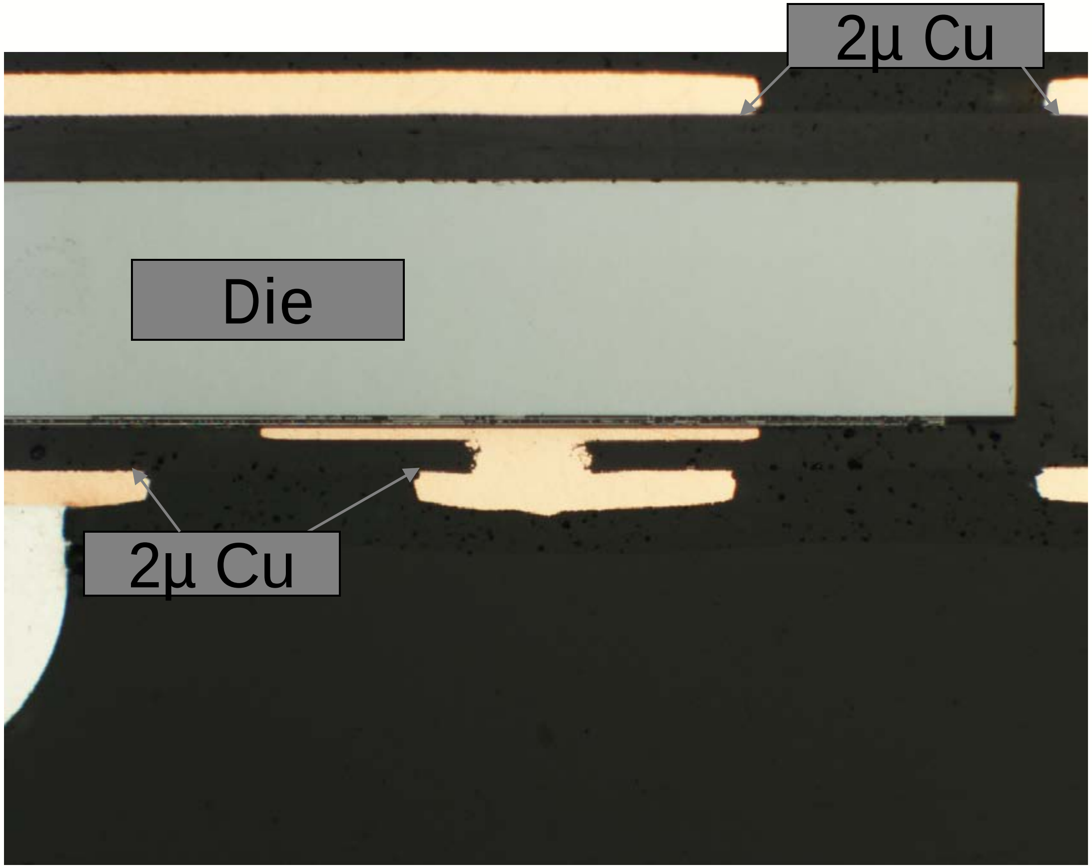


All values in N/mm (lb/inch	Peel Strength of 2µ Functional Foils on BT (3 mm tracks after 20µm build-up)					
	Values in N/mm (lb/inch)					
	BT style 1		BT style 2		BT style 3	
	As received	After PCT	As received	After PCT	As received	After PCT
DTH-TZA	0.65 (3.70)	0.60 (3.40)	0.67 (3.80)	0.60 (3.70)	0.68 (3.90)	0.63 (3.60)
DTH-TZA + Primer	**0.93 (5.30)**	**0.83 (4.70)**	**0.86 (4.90)**	**0.76 (4.30)**	**0.90 (5.10)**	**0.89 (5.10)**
Lab press Pressure Cooker Test (PCT) @ 121° C for 1h						

- **Significant increase on 3 different BT substrate systems**
- **Compatible with MSAP process**

Embedding Passive and Active Devices

- Major benefits for future miniaturisation requests
- Up to 40% reduction of x, y footprint
- Embedding bare die (European HERMES project)



Source: AT&S, HERMES

Conclusion

- Rapid trend to smoother tooth profile for high frequency/low loss PCBs and for fine pitch applications
- In the near future Primer coated versions may contribute to ensure secure bond for high reliability applications despite lowest roughness profiles

Thank you!

Visit us at booth #1807