A Designed Experiment for the Influence of Copper Foils on Impedance, DC Line Resistance and Insertion Loss

Alexander Ippich
Multek Inc.
Böblingen, Germany

Abstract
For the last couple of years, the main concerns regarding the electrical performance of blank PCB boards were impedance and ohmic resistance. Just recently, the need to reduce insertion loss came up in discussions with blank board customers.

One approach to alleviate the issue is the change to a lower loss dielectric material. Hence the percentage of boards that require a lower loss material is increasing significantly.
However, changing to a lower loss material influences PCB cost and in addition may affect the reliability of the boards.

The second way to reduce insertion loss is to minimize the conductor roughness. The roughness is influenced by two factors: the initial roughness of the copper foil (as received) and the treatment of the copper surface prior to lamination (a.k.a the oxide replacement).

Our first investigation, presented at Apex 2011, focused mainly on the influence of a wide variety of oxide replacements. The main focus of this follow on investigation is copper foil quality. Several very low profile and ultra low profile copper foils were investigated in a DOE, together with two types of oxide replacements.
The resulting electrical performance characteristics, like impedance, DC line resistance and insertion loss were evaluated in an ANOVA approach.

The paper describes the test vehicle and the testing methodology and discusses in detail the electrical performance characteristics. The influence of the independent variables on the performance characteristics is presented.
Finally the thermal reliability of the boards built applying different copper foils and oxide replacements was investigated.

Introduction
Compared with data processing and data transfer rates of just a decade ago, there is a significant increase of the required bandwidth. Concepts like cloud computing or video streaming are putting enormous requirements to the amount of information that needs to be transferred, both within a computer and over networking infrastructure.

To support these requirements, the insertion loss of a given data channel should be as low as possible, especially since the loss margin is decreasing continuously. Where an insertion loss of 0.78dB/inch at 4GHz was acceptable for PCIeIII just recently, there is already a push to reduce this spec limit to 0.48dB/inch.

There is a need in the industry for verification of the insertion loss on the real product. This may be testing of just a few sample boards in the measurement lab, but the trend is to require product testing at the back end of the line with methods like Intel's SET2DIL [1] or IBM's SPP [2].

To reduce insertion loss without changing the dielectric to a material with a lower dissipation factor, the roughness of the surface of the trace needs to be decreased [3, 4].
Two factors influence surface roughness of the traces: the as-received roughness of the copper foil and the oxide replacement.

The influence of various oxide replacements was presented in a paper at Apex 2011 [5]. The main conclusion was that some oxide replacements were able to reduce the loss significantly.
The downside is that changing the oxide replacement chemistry will affect all products using this manufacturing line, even if not needed for these products.

Changing the copper foil type, on the other hand, can be done on a part number basis, so the cost increase in using this is incremental. This is an exclusive solution for these part numbers only that need the loss reduction.

To quantify the reduction of insertion loss by using copper foils with reduced roughness, test boards were manufactured applying various foil qualities in combination with two oxide replacements covered in the Apex 2011 paper.

These test boards were measured for resistance, impedance and insertion loss. The measurement results were evaluated with a statistical approach (ANOVA) [6, 7]. Finally, the thermo-mechanical reliability was examined by repeated reflow and solder shock testing.

Description of the Test Vehicle and the Test Cells

An 8 layer stackup was used for the test vehicle. It contained two offset striplines, one on layer 3 (referencing to ground layers 2 and 4) and one on layer 6 (referencing to layers 5 and 7). The outermost layers were providing the landing patterns for probing.

The two stripline layers were identical in structures and stackup. Each featured 14" long striplines in 5 different line widths, going from 7.25mil to 8.25mil.

This test design was stepped 3 times on the panel, along with a small differential impedance test coupon.

A mid loss material was chosen for the DOE, as many designs in the 3.125 to 10Gbs range are using them. Similar glass styles and thicknesses were used for the cores and prepregs to get a relatively balanced stripline design.

Four different copper foil types and two oxide replacements have been used in the DOE. The copper foils were a matte side treated VLP [8] foil, a shiny side treated VLP foil and two matte side treated ultra low profile copper foils (see Figure 1).

As a result of our prior investigation into oxide replacements, a 'standard' and a surface preparation with reduced etching rate were chosen.

Since the DOE was run as a full-factorial, 8 test cells were evaluated.

Cu foils:

- matte side treated foil | very low profile (VLP) characteristics
- shiny-side treated foil (RTF) | very low profile (VLP) characteristics
- matte side treated foil | ultra low profile characteristics
- matte side treated foil | ultra low profile characteristics, with adhesion promoter

oxide replacements:

- 'standard' oxide replacement
- low etch oxide replacement

→ 4x2 = 8 test cells total

Figure 1
Oxide Replacements and Cu Foils tested

Unfortunately, the IPC standard for copper foils [8] is only defining maximum roughness values for LP and VLP foils. But copper foil suppliers are producing more advanced foils by now with names like H-VLP, ultra low profile, profile free, etc. To illustrate the differences of the copper foil roughness on the matte side for these foils, SEM pictures are shown in Figure 2.

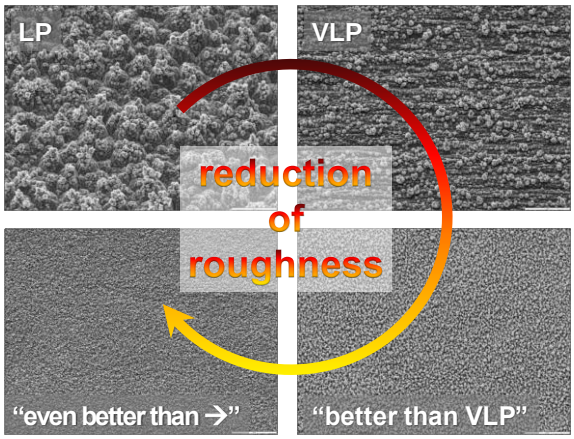


Figure 2
Differences in Surface Appearance

Results of Impedance and DC Line Resistance Testing

The impedance and DC line resistance testing was performed on standard production floor equipment. For impedance testing, a Polar Instruments CITS900s4 with handheld probes was used. The DC line resistance testing was done using an Agilent 34401A multimeter in 4-wire configuration; the measurement data was transferred to a computer via an IEEE488 interface.

The first test was on the differential impedance coupon. Since this coupon is on the edge of the test structure, the differential impedance coupon for PCB #1 is very close to the panel border compared to the coupons for PCB #2 and #3 (see Figure 3). At this location, the dielectric thickness of the prepregs tends to be slightly lower than on the other parts of the panel.

Figure 3
Location of Differential Impedance Coupon

Evaluating the differential impedance measurements with an Analysis of Variances (ANOVA) approach revealed a significant influence of the copper foil type. The influence of the oxide replacement is much smaller in comparison. The position on the panel was also a significant variable, but this is caused mainly by the fact, that the differential impedance coupon for PCB #1 is at the very edge of the panel, therefore seeing a reduced dielectric thickness (see Figure 4).

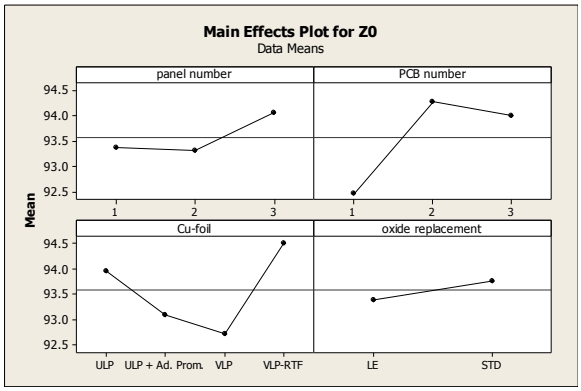


Figure 4
Main Effect Plot for Differential Impedance

The Analysis of Variances calculation was also performed for the DC line resistance in the same differential impedance coupon. Again, the copper foil type showed a significant influence. As a general trend, the reverse treated foil showed higher values for both impedance and ohmic resistance compared to the shiny-side treated foils.
The oxide replacement influences Rdc even more significant compared to impedance, with the low etch surface preparation showing lower values than the standard oxide replacement (see Figure 5).

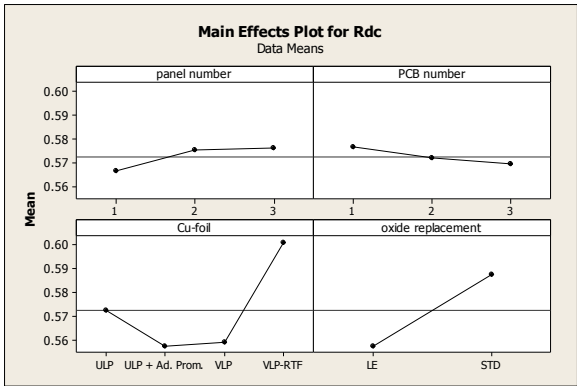


Figure 5
Main Effect Plot for DC Line Resistance
(Differential Impedance Coupon)

As a next step, the impedance and DC line resistance readings of the main coupon were evaluated. The main coupon, later to be used for the insertion loss testing, is designed as single ended traces. Each coupon contained traces in 5 different line widths.

The ANOVA evaluation shows for both values, impedance and DC line resistance, that the panel number has basically no influence. This is indicating a stable process.

The center coupon on the panel (PCB number 2) yielded higher impedance readings than the other 2 PCBs, whereas no change was detected for the DC line resistance. This can be explained by the fact, that the prepreg thickness in the center of the panel typically is higher compared to the panel edges. This is increasing impedance, but has no influence on Rdc.

As expected, both impedance and DC line resistance readings showed a monotonic drop for the line width going from 7.25mil to 8.25mil.

The copper foil shows a significant influence; again the RTF foil gives higher readings.

An interesting result is, that the impedance was higher for the low etch oxide replacement, but the DC line resistance was lower compared to the standard oxide replacement. The effect for Rdc may be explained easily by the fact, that an oxide replacement with reduced etching rate is able to retain a higher copper thickness for the traces. The complete overview of the influence of the independent variables can be seen in figures 6 and 7.

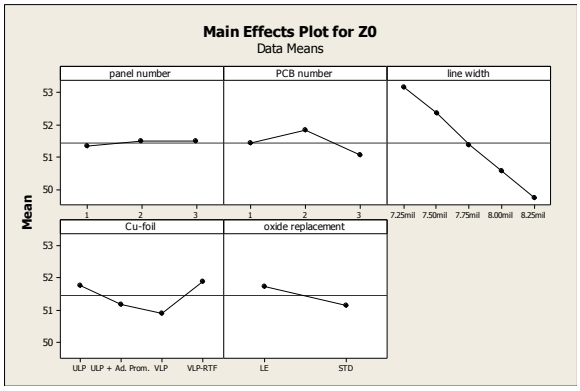


Figure 6
Main Effect Plot Single Ended Impedance

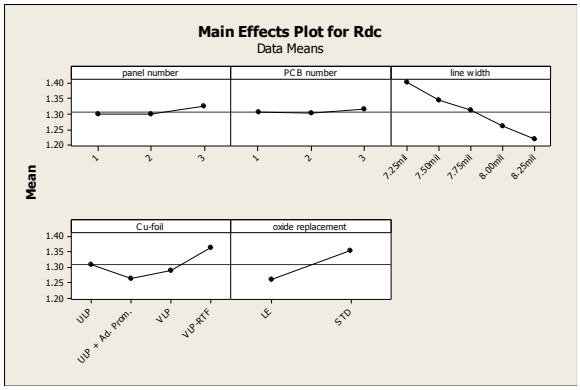


Figure 7
Main Effect Plot for DC Line Resistance
(Single Ended Impedance Coupon)

Measurement of Insertion Loss

For the insertion loss testing, an Agilent N5244A PNA-X [9] network analyzer was used. Although the instrument is capable of measuring differential insertion loss (4-port testing), for ease of probing, single ended insertion loss was determined.

The test boards were probed with GGB Industries Picoprobes (see Figure 8 + 9). A full 2-port SOLT calibration was performed at the tip of the probes with an appropriate calibration substrate.

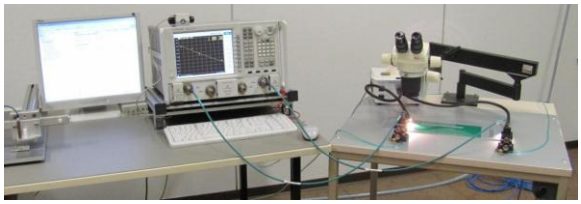


Figure 8
Measurement Setup for Insertion Loss Testing

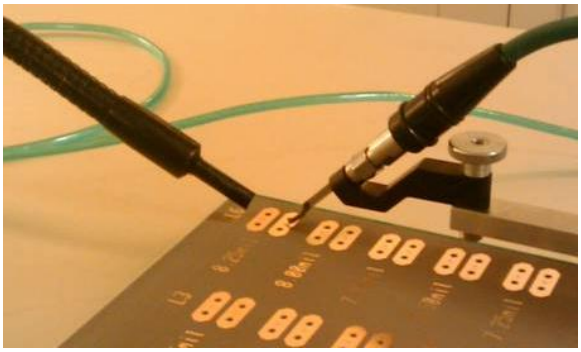


Figure 9
Probing of the Test Vehicle

After collecting the S-parameter over frequency data for all test boards, the data was transferred to a PC for further evaluation.

To check for any measurement traces with an unusual behavior, the S21 curves for all 5 line widths, both layers and all 3 panels were plotted into one chart for each test cell. An example can be found in Figure 10.

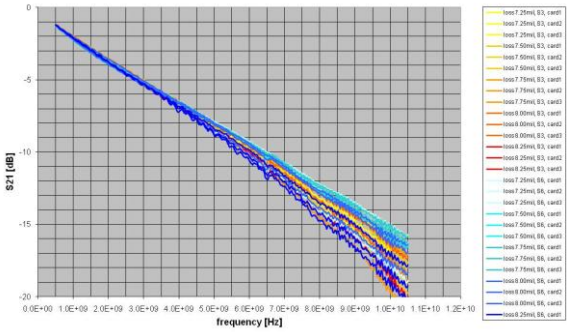


Figure 10
Spread of S21 Traces for one Test Cell

As a further check for unusual behavior, the traces were averaged over the 5 line widths and 3 panels to allow for a comparison of the data between layer3 and layer6. Up to approximately 6.5GHz, no difference between the two layers was found, see Figure 11.

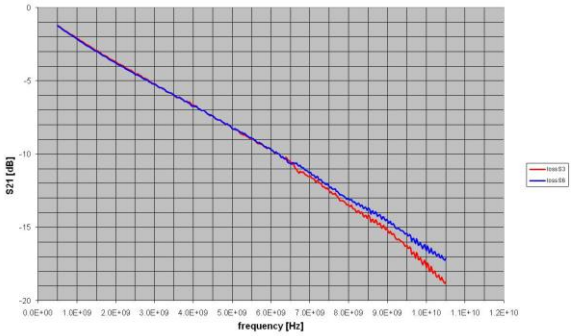


Figure 11
Difference off S21 between the two Layers

To visualize the effect of the various copper foils and the two oxide replacements on the insertion loss at 5GHz, the S21 data was plotted for each test cell of the DOE. The traces for each cell were calculated as an average of the 5 line widths, two layers and 3 panels. The total spread over the 8 test cells is 1.17dB at 5GHz (see Figure 12).

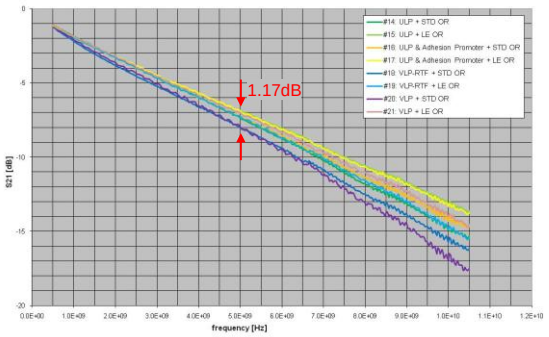


Figure 12
Spread of S21 Values

To get a better understanding of the effect of the various independent variables, an analysis of variances was performed. Since S21 data was available for a frequency range starting at 500MHz, a lower frequency of 750MHz was chosen as well as a second frequency of 5GHz, to estimate the influence on a 10Gbps system.

For the lower frequency of 750MHz, the ANOVA analysis showed only minor variation over the set of 3 panels. The influence of the line width was small and inconclusive. However, the oxide replacement influence was clearly observable. The test cell with the oxide replacement with reduced etching rate showed significantly lower insertion loss than standard oxide replacement. The main variable clearly is the copper foil type at this lower frequency. The ultra-low profile copper foils

outperform all other copper types in the test, with the RTF copper showing the worst insertion loss of all 4 foils (see Figure 13).

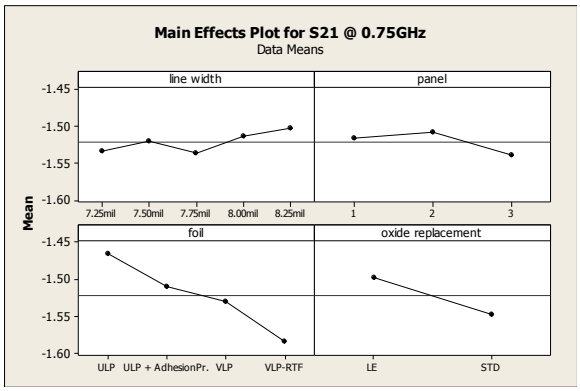


Figure 13
Main Effect Plot for S21 at 750MHz

The numerical output of the ANOVA analysis confirmed that line width and panel number have only a small influence with less than 1.5% and around 1.6% respectively. The oxide replacement accounted for roughly 6% of the variation and the copper foil was responsible for 17.5% of the variation (see Figure 14).

Analysis of Variance for S21 @ 0.75GHz, using Adjusted SS for Tests

Source	DF	Seq SS	Adj SS	Adj MS	F	P
foil	3	0.438365	0.438365	0.146122	21.67	0.000
oxide replacement	1	0.149110	0.149110	0.149110	22.11	0.000
line width	4	0.035666	0.035666	0.008916	1.32	0.262
panel	2	0.040515	0.040515	0.020258	3.00	0.052
Error	228	1.537558	1.537558	0.006744		
Total	239	2.498146				

S = 0.0821199 R-Sq = 38.45% R-Sq(adj) = 35.48%

Figure 14
Numerical ANOVA Results at 750MHz

At the main frequency of interest of 5GHz for the DOE the ANOVA plots showed similar characteristics as for the lower frequency. Again, line width and panel number had a very small influence. The copper foil showed a strong influence, with the ultra-low profile foils again outperforming the VLP foils and the RTF foil showed the worst results.
In case of the higher frequency, the oxide replacement influence is stronger in comparison to the lower frequency analysis. But again, the low-etch oxide replacement performed by far better than the standard oxide replacement (see Figure 15).

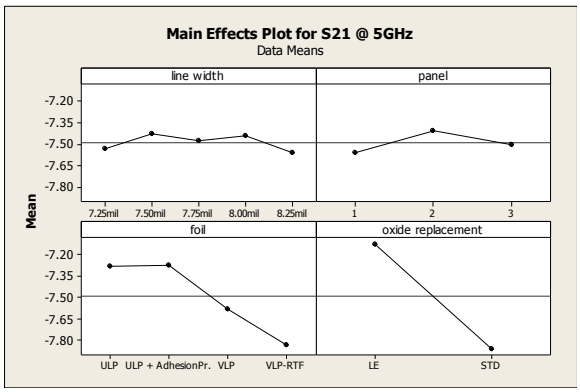


Figure 15
Main Effect Plot for S21 at 5GHz

The calculated sum-of-square values confirmed the ANOVA main effect plot. Line width and panel number show no significant contribution (<1% and ~1.3%). The copper foil is confirmed as a main influencing factor with 17% of the variation and the oxide replacement had the biggest contribution with around 42% of the variation (see Figure 16).

Analysis of Variance for S21 @ 5GHz, using Adjusted SS for Tests

Source	DF	Seq SS	Adj SS	Adj MS	F	P
foil	3	13.0978	13.0978	4.3659	37.31	0.000
oxide replacement	1	32.4591	32.4591	32.4591	277.38	0.000
line width	4	0.6387	0.6387	0.1597	1.36	0.247
panel	2	0.9754	0.9754	0.4877	4.17	0.017
Error	228	26.6810	26.6810	0.1170		
Total	239	77.3533				

S = 0.342085 R-Sq = 65.51% R-Sq(adj) = 63.84%

Figure 16
Numerical ANOVA Results at 5GHz

Comparing insertion loss at 5GHz of the 8 cells of the DOE, the best performing combination of copper foil and oxide replacement showed a 1.31dB gain compared to combination performing worst. The two ultra-low profile foils showed very similar characteristics with the matte side treated VLP foil as the next best foil. The highest insertion loss was detected for the shiny side treated VLP copper foil.
All four copper foils showed a significant improvement in insertion loss in combination with the low-etch oxide replacement, when compared to the standard oxide replacement. The direct comparison can be found in Table 1 and Figure 17.

Table 1 – Improvement of Insertion Loss

oxide replacement / Cu Foil	standard	low etch
ultra low profile	7.55dB [0.58dB]	7.01dB [0.03dB]
ultra low profile + adhesion promoter	7.56dB [0.58dB]	6.98dB [ref]
very low profile	8.03dB [1.06dB]	7.13dB [0.15dB]
very low profile - RTF	8.28dB [1.31dB]	7.38dB [0.40dB]

S21 @ 5GHz: absolute [delta]

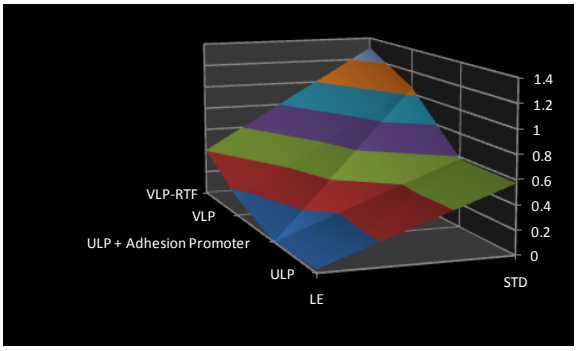


Figure 17
Improvement of Insertion Loss

Comparison of Geometrical Attributes
To better understand the differences between the 4 copper foils and two oxide replacements, cross sections were taken out of boards from each cell of the DOE. The sections clearly showed a difference in the micro roughness on the prepreg side between the standard and the low-etch oxide replacement.
Comparing the cross sections of the two ultra-low profile copper foils showed no observable difference, but far less roughness on the treatment side could be observed than for the VLP foil.
The cross section of the reverse treated VLP foil clearly explained the relatively high insertion loss. These samples showed a higher roughness compared to all other samples (Figure 18 & 19).

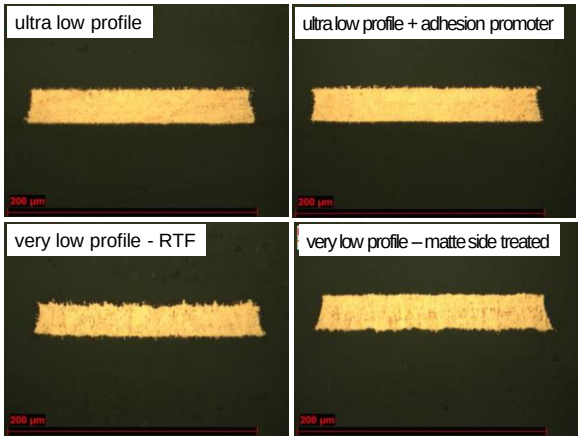


Figure 18
Cross Sections of the Samples with Standard Oxide Replacement

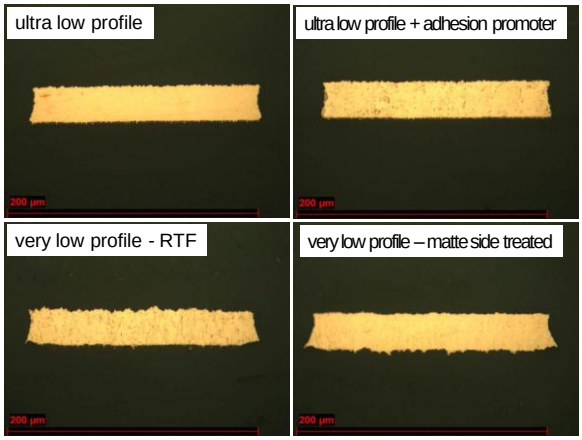


Figure 19
Cross Sections of the Samples with Low-Etch Oxide Replacement

Reliability

As the roughness of the copper foil decreases, it gets more and more difficult to achieve a sufficient adhesion between the copper and the resin system. This affects both, the copper-core and the copper-prepreg interface.

For matte-side treated materials, the height of the copper needles anchored into the core decrease from STD to LP, VLP and to ultra-low profile foils. So the copper-to-core interface after thermal stress was of particular interest for the investigated ultra-low profile foils.

The copper-to-prepreg interface is mainly influenced by the oxide replacement. Since a low-etch variant was used in half of the test cells and 3 of them were also having the shiny side of the copper facing the prepreg, these test cells were also considered the most interesting ones regarding thermal stress testing.

In the reliability testing, the samples were stressed with both solder shock and repeated reflow testing. Solder shock was performed 6 times at 288 deg C according to IPC-TM650 2.6.8, and reflow was repeated six times with a standard eutectic reflow profile with 230 deg C. peak temperature. The solder shocks were performed after preconditioning the samples for 4 hours at 150 deg C; repeated reflow was performed without any preconditioning.

After both, solder shock and repeated reflow, cross sectioning was used to check for any degradation.

Repeated reflow testing did not show any delaminations of the samples. All of them withstood 6 cycles without issues. Figure 20 shows one cross section of an ultra-low profile foil test cell as an example.

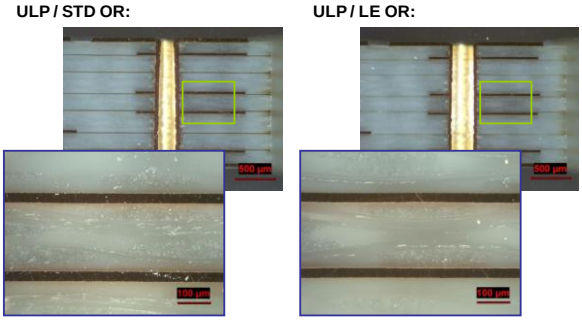


Figure 20
Cross Sections of ULP Samples after Repeated Reflow

The second test of thermo-mechanical robustness using solder shock testing also showed no irregularities on the samples. All 8 test cells survived 6x solder shock for 10 seconds at 288 deg C. The cross section results for the two ultra low profile foils can be found in Figure 21.

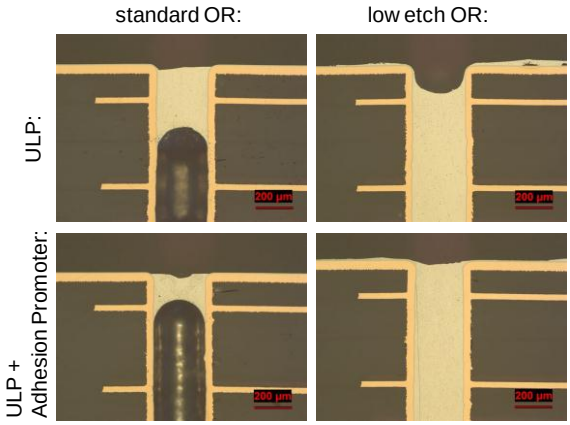


Figure 21
Cross Sections of the ULP Samples after Solder Shock Testing

Summary

As loss requirements on high performance printed circuit boards are getting more stringent, the influence of the roughness for the copper foils used can no longer be ignored. The investigation clearly shows the influence of various very low profile and ultra low profile copper foils on the insertion loss. It was shown that using a smooth copper foil in combination with a low etch oxide replacement is the best option to minimize the copper loss.

The investigation also demonstrated that designs using these options would be reliable enough to survive solder shock and repeated reflow testing.

References

1. Loyer, J. “SET2DIL: Method to Derive Differential Insertion Loss from Single-Ended TDR/TDT Measurements”, DesignCon 2010
2. IPC TM-650 2.5.5.12 “Test Methods to Determine the Amount of Signal Loss on Printed Boards”
3. Lee, B “The Impact of Innerlayer Copper Foil Roughness on Signal Integrity”, Printed Circuit Design and Fab, April 2007
4. Briest, G. and Hall, S. “Non-Classical Conductor Losses due to Copper Foil Roughness and Treatment”, IPC Printed Circuit Expo 2005
5. Ippich, A. “A Designed Experiment for the Influence of Copper Foils on Impedance, DC Line Resistance and Insertion Loss”, IPC APEX Expo 2010
6. Perez-Wilson, M. “The M/PCpS Methodology – Stage IV: Optimization”, ISBN 1-883237-05-X
7. Perez-Wilson, M. “AnovA – Analysis of Variance”, ISBN 1-883237-14-9
8. IPC-4562 “Metal Foil for Printed Wiring Applications”
9. Agilent User Manual “N5242A User’s and Service Guide”, N5242-90008

Influence of Copper Foils on Insertion Loss

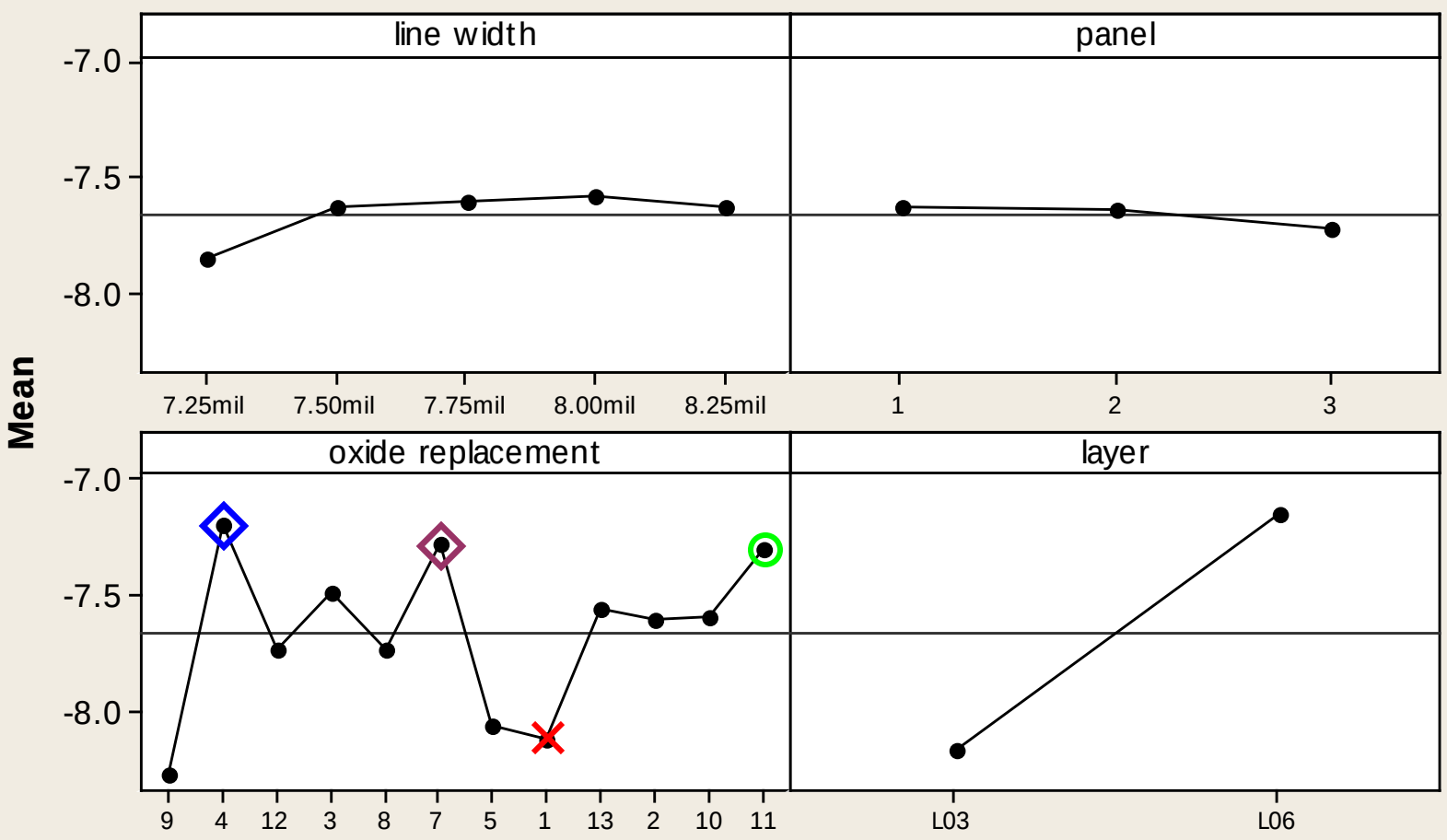
Alexander Ippich

Multek Inc.
Herrenberger Strasse 110
71034 Böblingen / Germany
email: alexander.ippich@de.multek.com

objective / link to Apex2011

- the objective of the investigation was to reduce insertion loss by reducing conductor roughness
- the first part, looking mainly into the influence of the oxide replacement, was presented at Apex 2011
- this second part is concentrating on the influence of the copper foil type, like ‘very low profile’ or ‘ultra low profile’

insertion loss at 5GHz

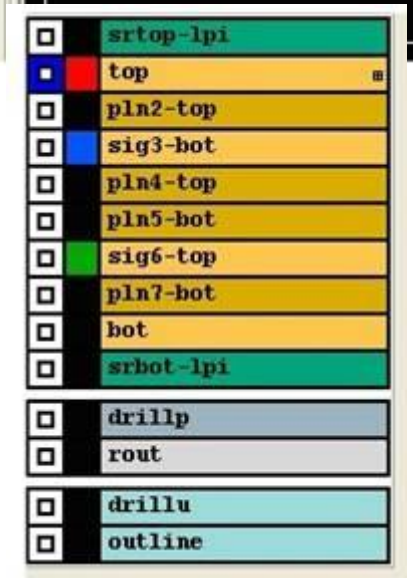


description of test vehicle and test cells

measured coupons

- coupon has 5 different line widths (7.25 - 8.25mil)
- coupon is routed on two layers (L3 & L6 – 35um Cu)
- coupon is 3x on each panel
- 3 panels produced per test cell
- 4 different copper foil types
- 2 different oxide replacements
- measured insertion loss, impedance and DC line resistance
- repeated reflow and solder shock testing

test design – single image



test design – panel design

stackup

Layer type	#	Layer description	For dielectric layers: Material selection, Multek Code For copper layers: copper utilization in %	Via Structure	Multek Material code	glass style	resin content [%]	dielectric constant @ 5 GHz	Thickness: nominal thickness. [um]	Thickness: after lamination [um]	Thickness: after lamination [mil]
Air						added copper thickness	4				
soldermask									10	10	0.4
Top	1	Primary Side Traces			17um foil, thinned to 7um + plated copper				105	105	4.1
prepreg			QI 5.52mil (2116)		P-QI001	2116	56%	3.46	140	135	5.3
pln	2		85%		1				31	35	1.4
core			QI 8mil 1/1 (2x2116)		C-QI036	2x2116		3.71	203	203	8.0
sig	3		15%		1				31	35	1.4
prepreg			QI 9.43mil (2116+2113)		P-QI001+P-QI005	2116+2113	57%	3.45	239	194	7.7
pln	4		85%		1				31	35	1.4
core			QI 8mil 1/1 (2x2116)		C-QI036	2x2116		3.71	203	203	8.0
pln	5		85%		1				31	35	1.4
prepreg			QI 9.43mil (2116+2113)		P-QI001+P-QI005	2116+2113	57%	3.45	239	194	7.7
sig	6		15%		1				31	35	1.4
core			QI 8mil 1/1 (2x2116)		C-QI036	2x2116		3.71	203	203	8.0
pln	7		85%		1				31	35	1.4
prepreg			QI 5.52mil (2116)		P-QI001	2116	56%	3.46	140	135	5.3
Bot	8	Secondary Side Traces			17um foil, thinned to 7um + plated copper				105	105	4.1
soldermask									10	10	0.4
Air											

- used different 1oz copper foils on the signal layers

overview of test cells

Cu foils:

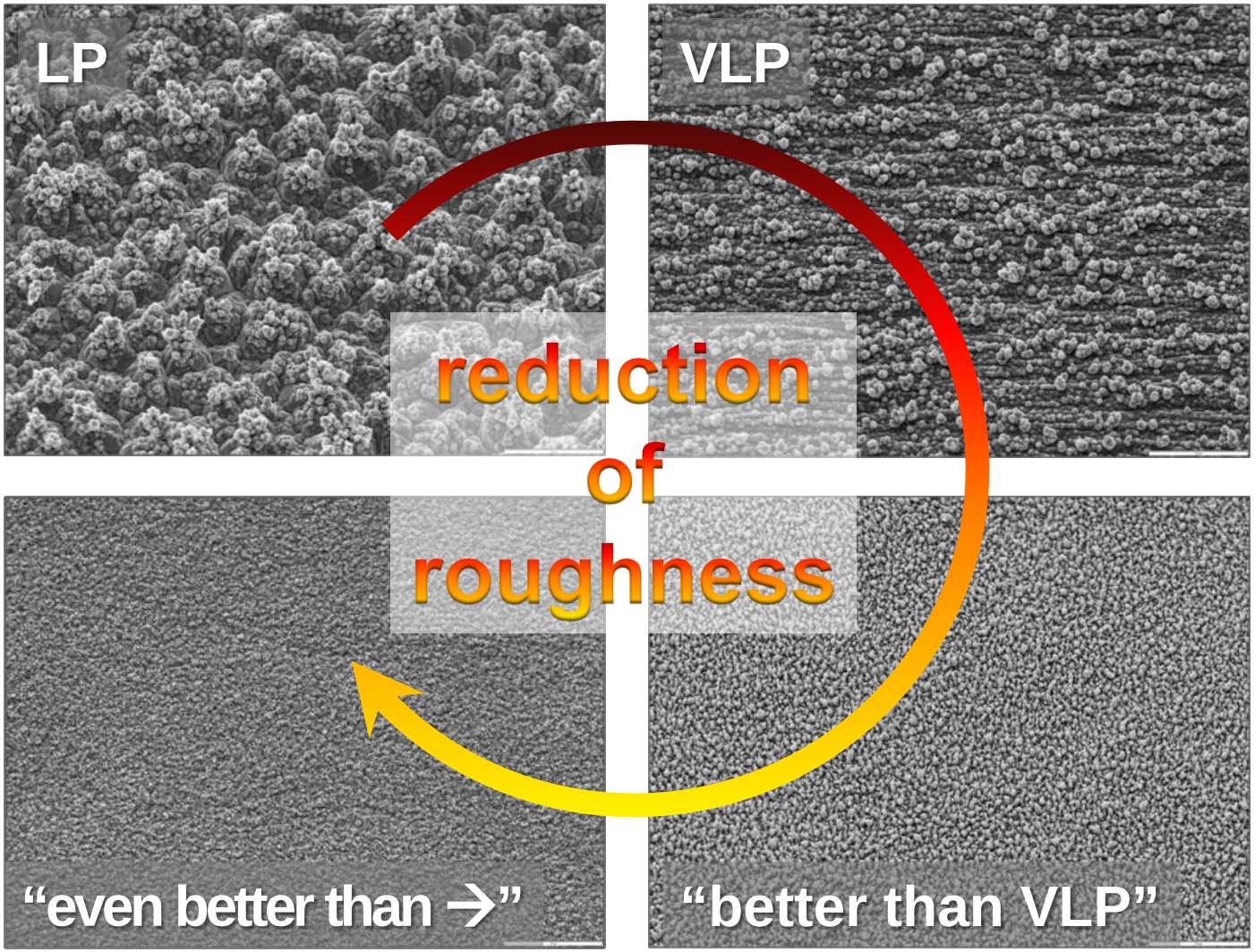
- matte side treated foil | very low profile (VLP) characteristics
- shiny-side treated foil (RTF) | very low profile (VLP) characteristics
- matte side treated foil | ultra low profile characteristics
- matte side treated foil | ultra low profile characteristics, with adhesion promoter

oxide replacements:

- ‘standard’ oxide replacement
- low etch oxide replacement

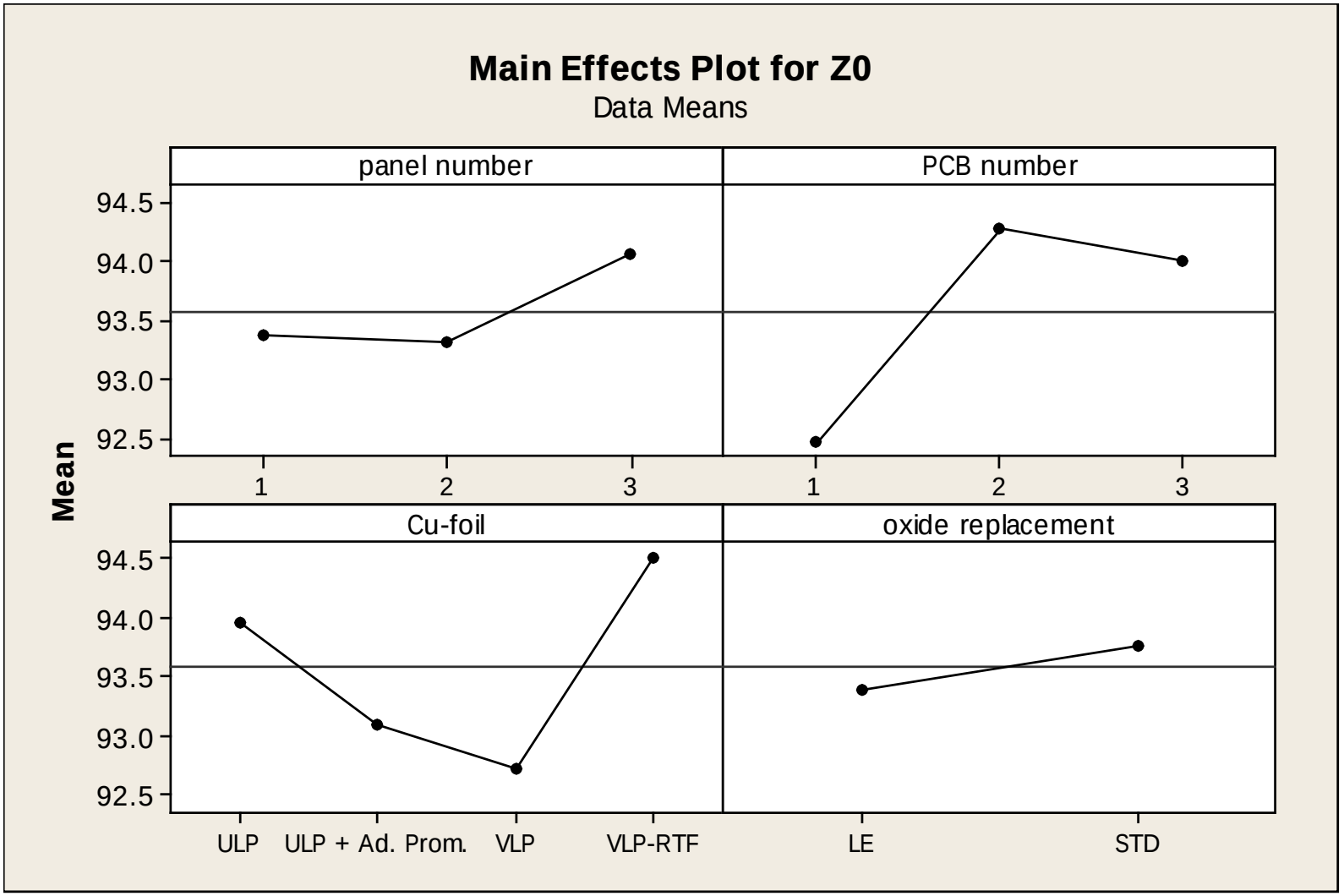
→ 4x2 = 8 test cells total

differences in Cu roughness

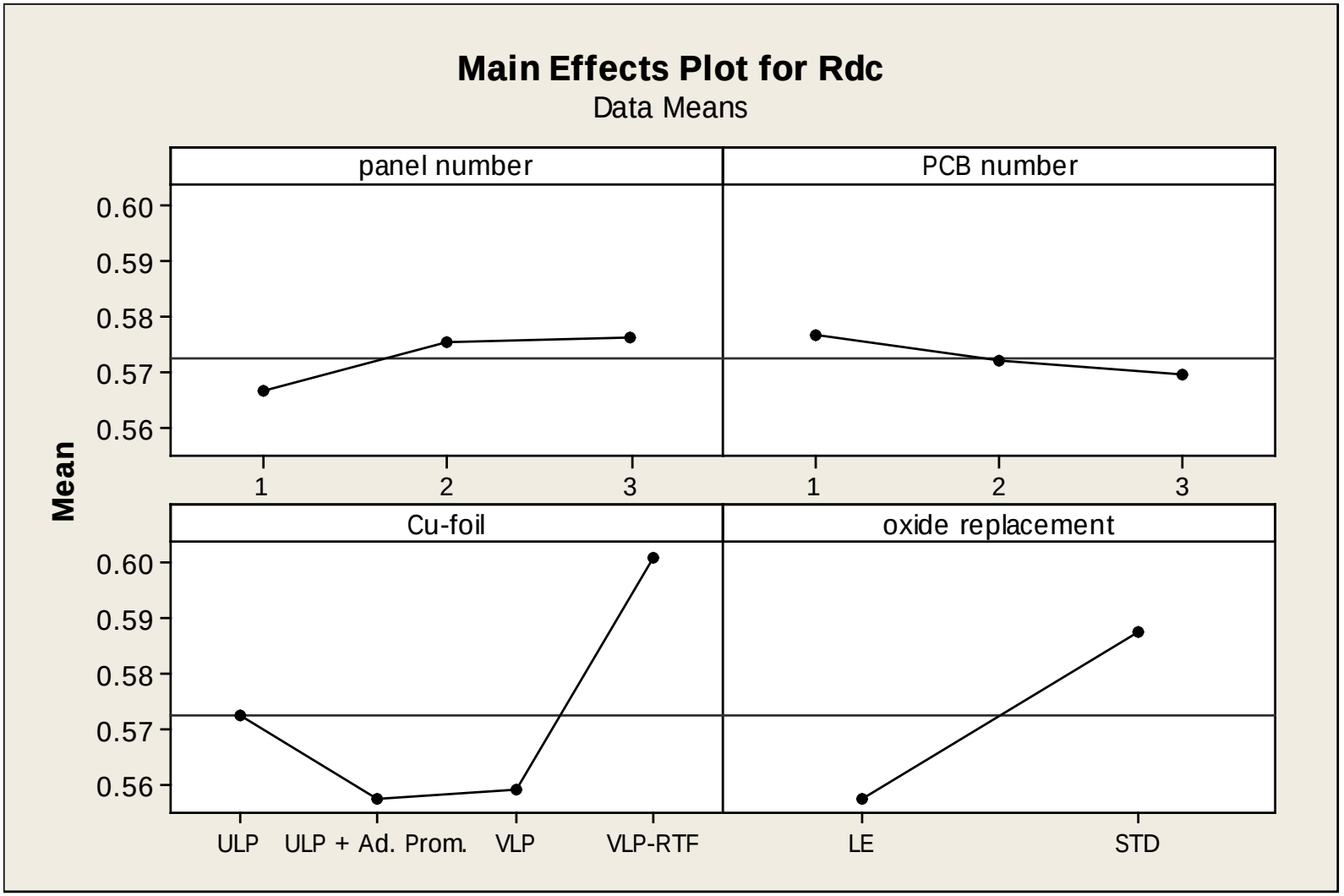


impedance and DC line resistance testing

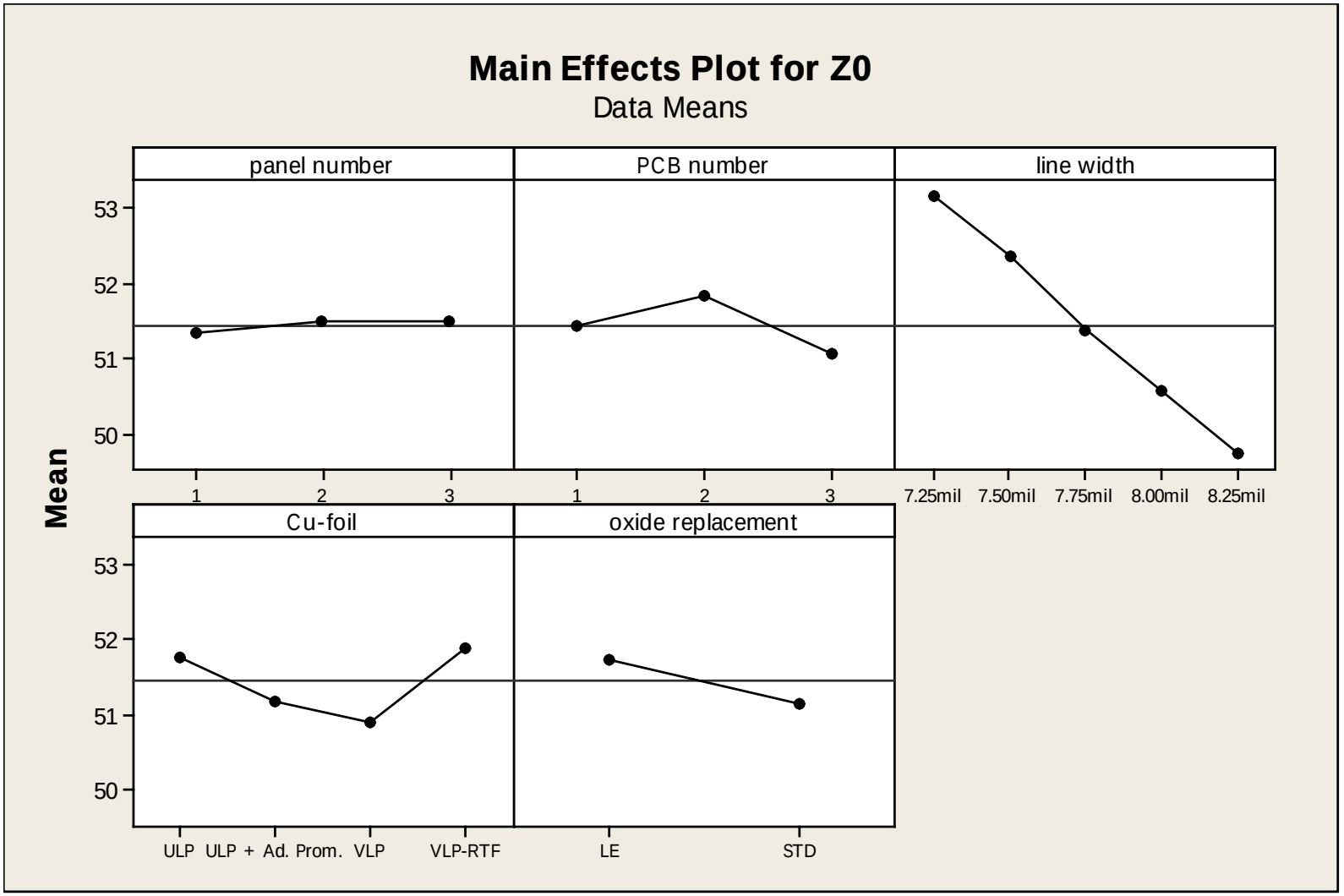
impedance (edge coupon)



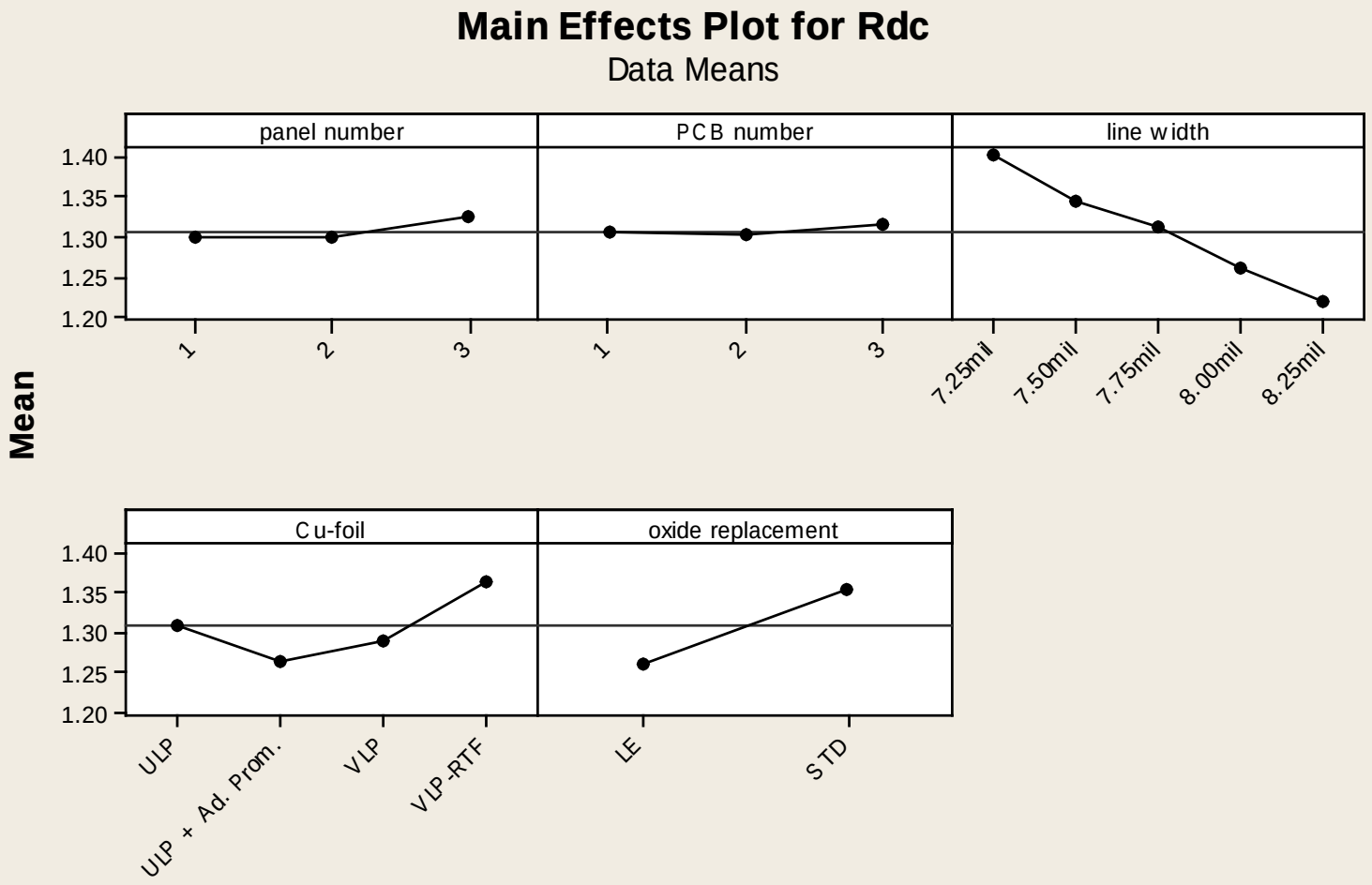
resistance (edge coupon)



impedance (loss coupon)



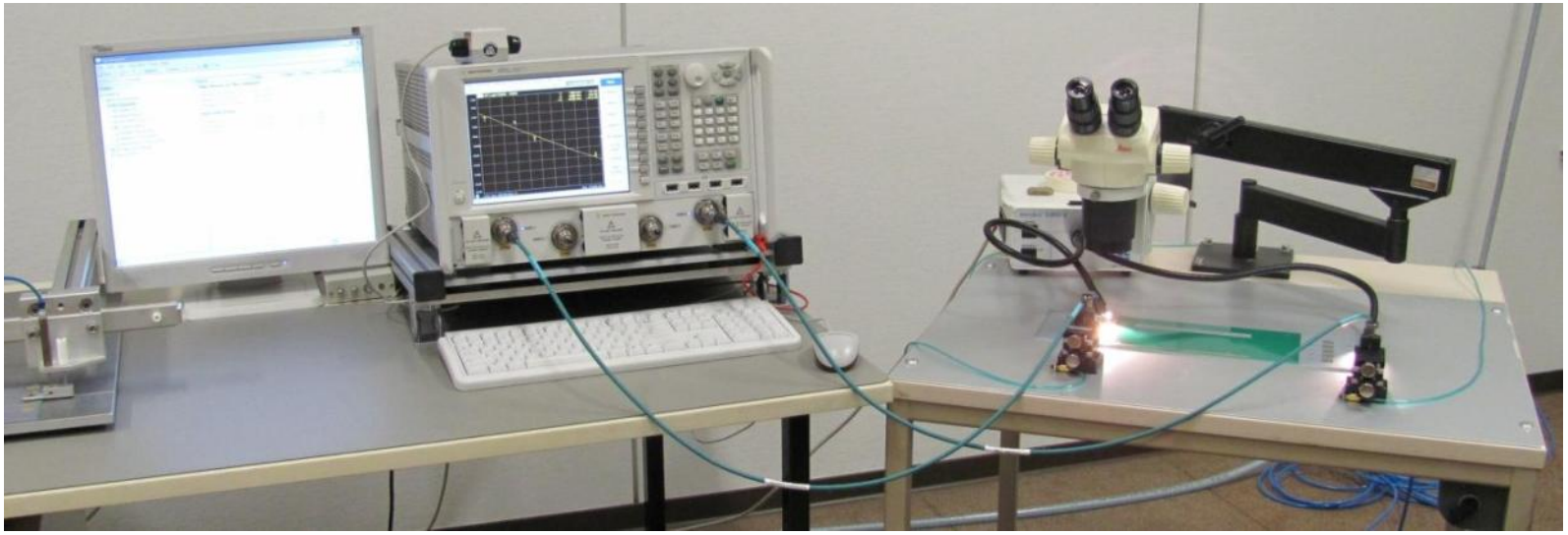
resistance (loss coupon)



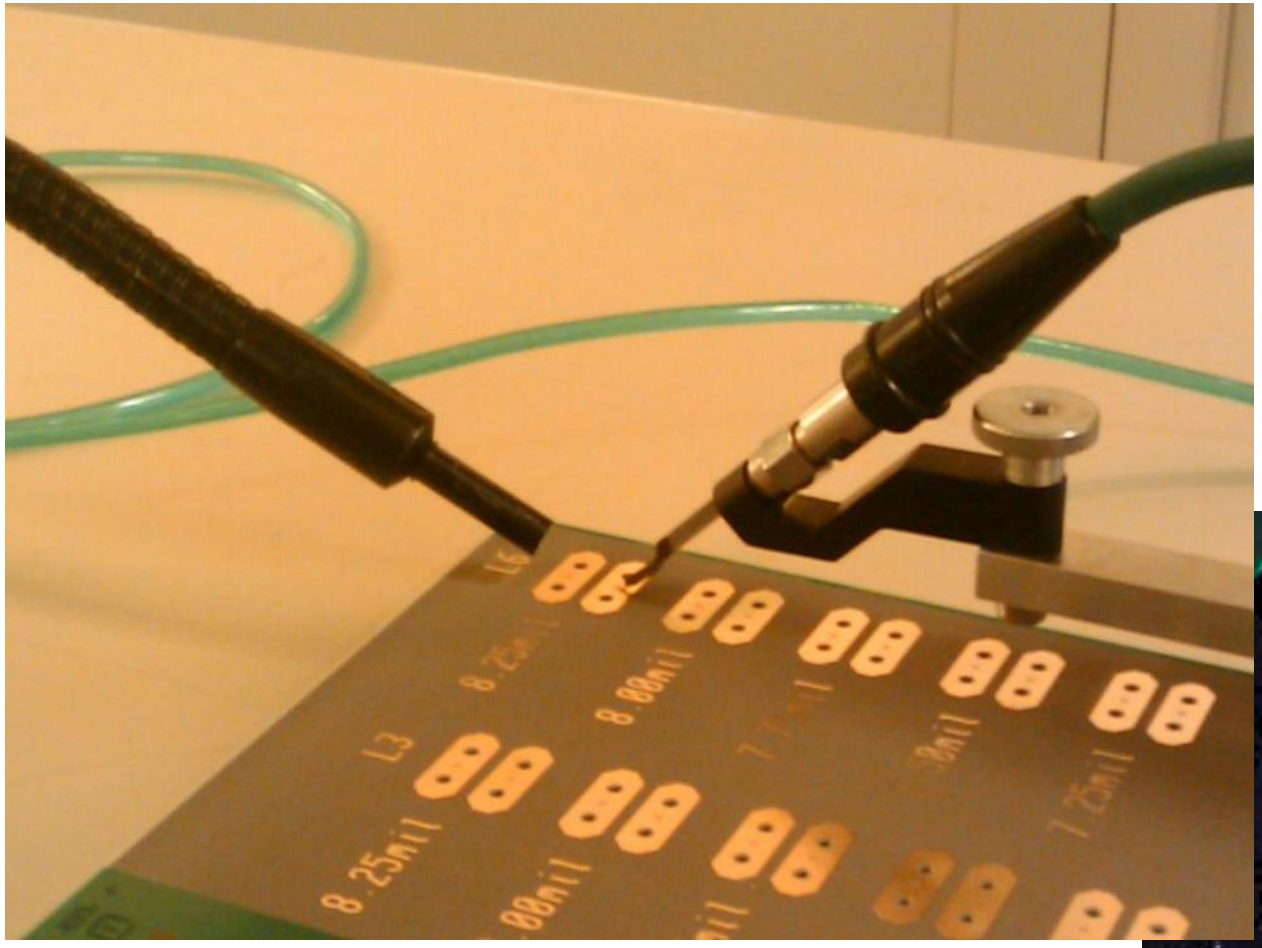
insertion loss testing

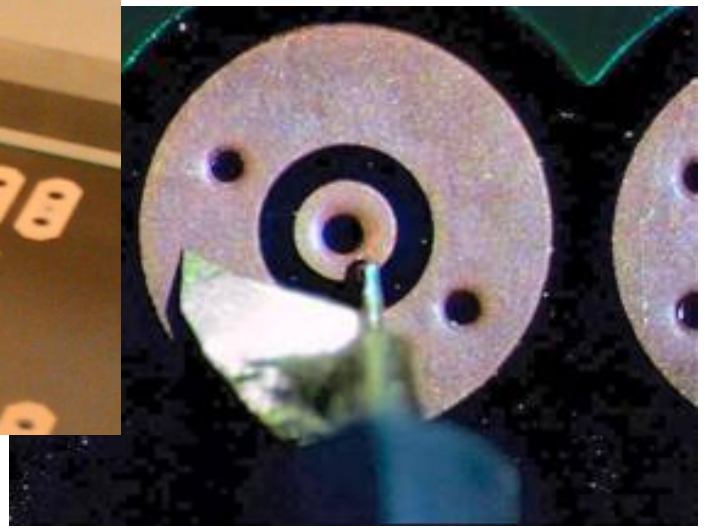
measurement system

- Agilent N5244A PNA-X vector network analyzer
- Agilent N4692A eCal module
- Rosenberger Microcoax Utiflex cables
- Quater Research XYZ500MIS probe positioner
- GGB Industries 40A-SG-1000-DS Picoprobe®
- GGB Industries CS-11 calibration substrate



probing detail

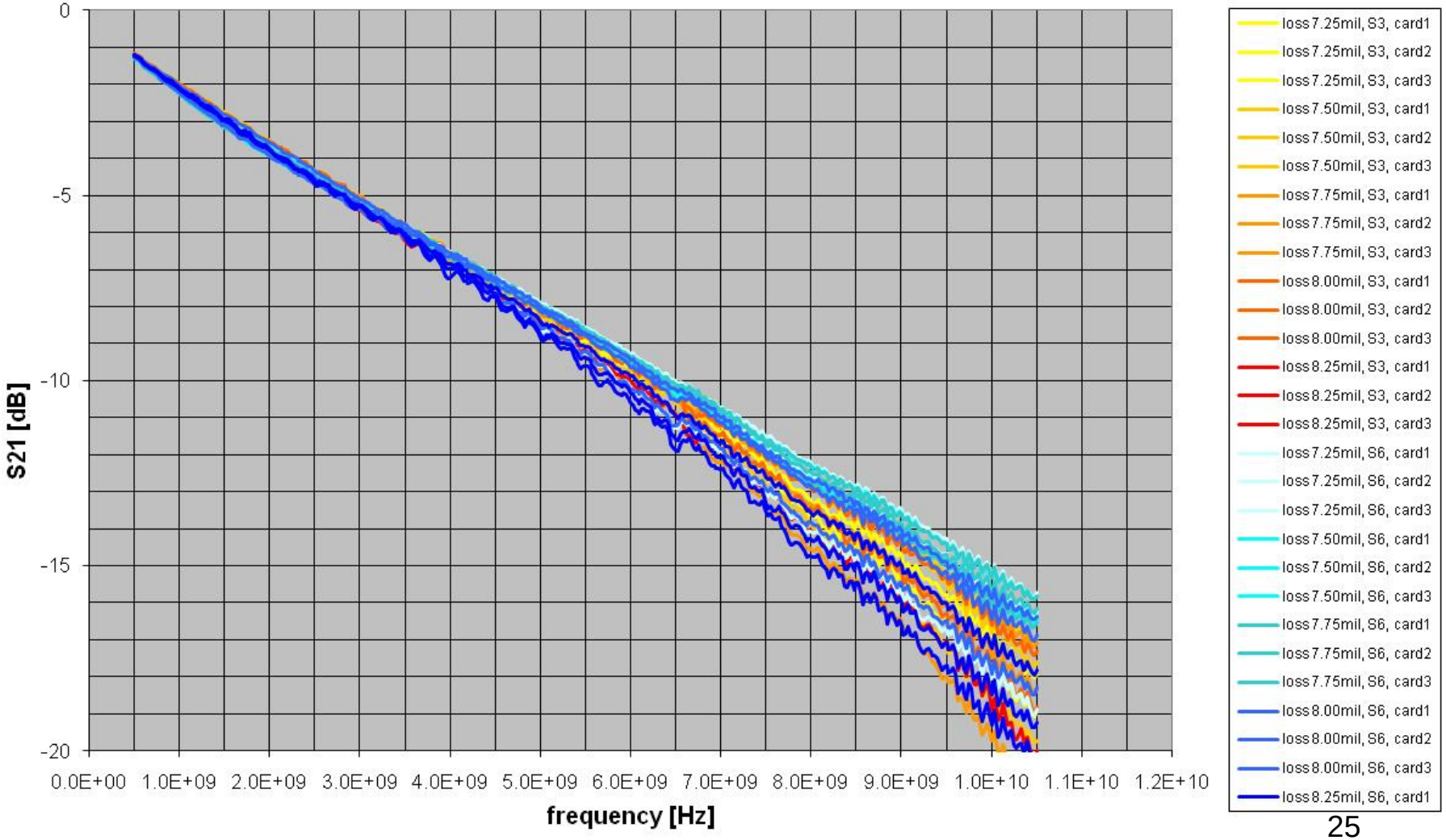




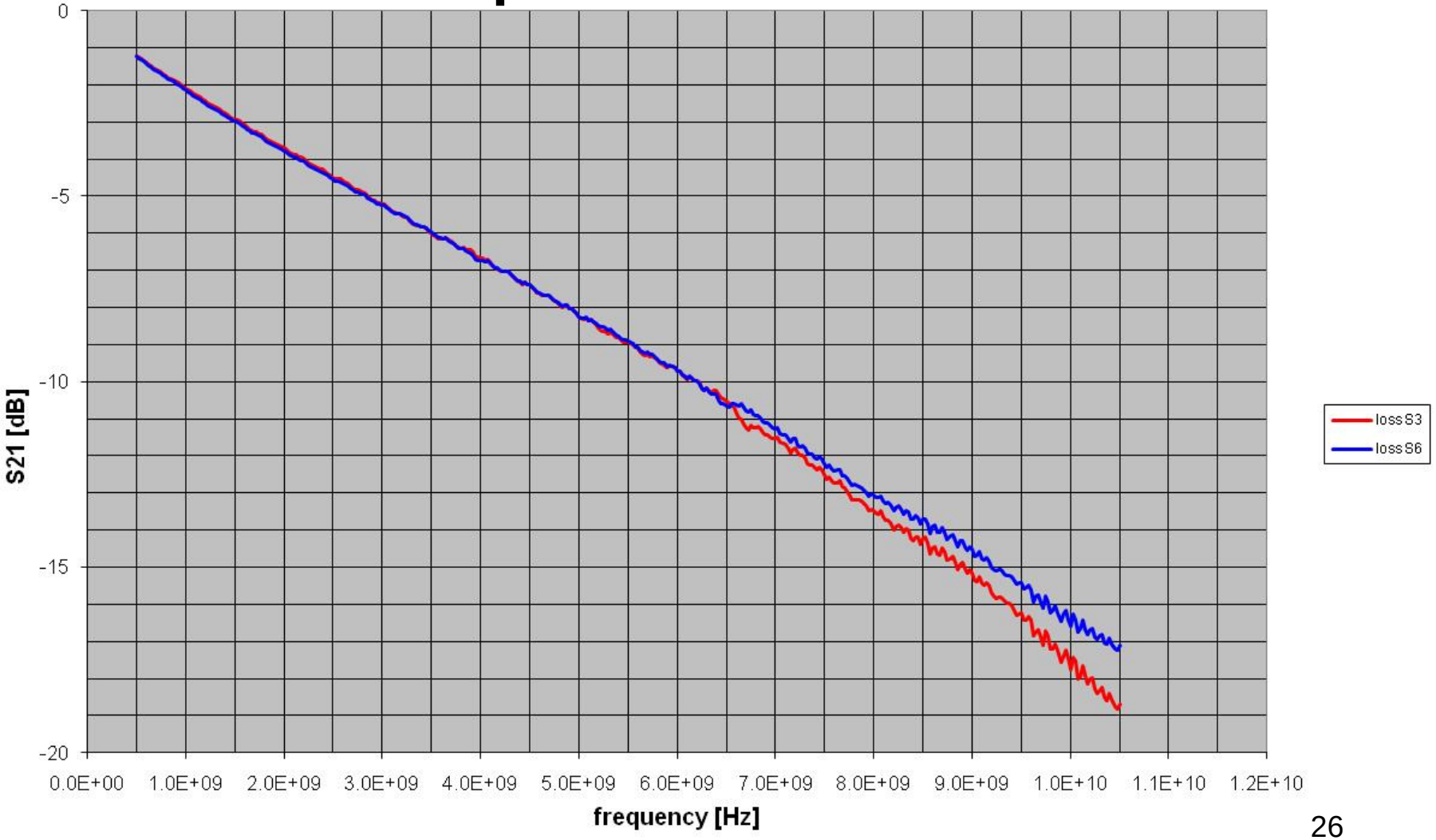
measurement procedure

- full two port calibration of PNA-X
  - warm up of minimum 2h
  - calibration with CS-11 calibration substrate at the tip of the Picoprobes
- measurement of S-parameters
  - probing with Picoprobes
  - transfer S-parameters to hard disc drive
- all further data processing in statistic software
  - charts of various parameters
  - ANOVA evaluation to find the ‘vital few’ parameters

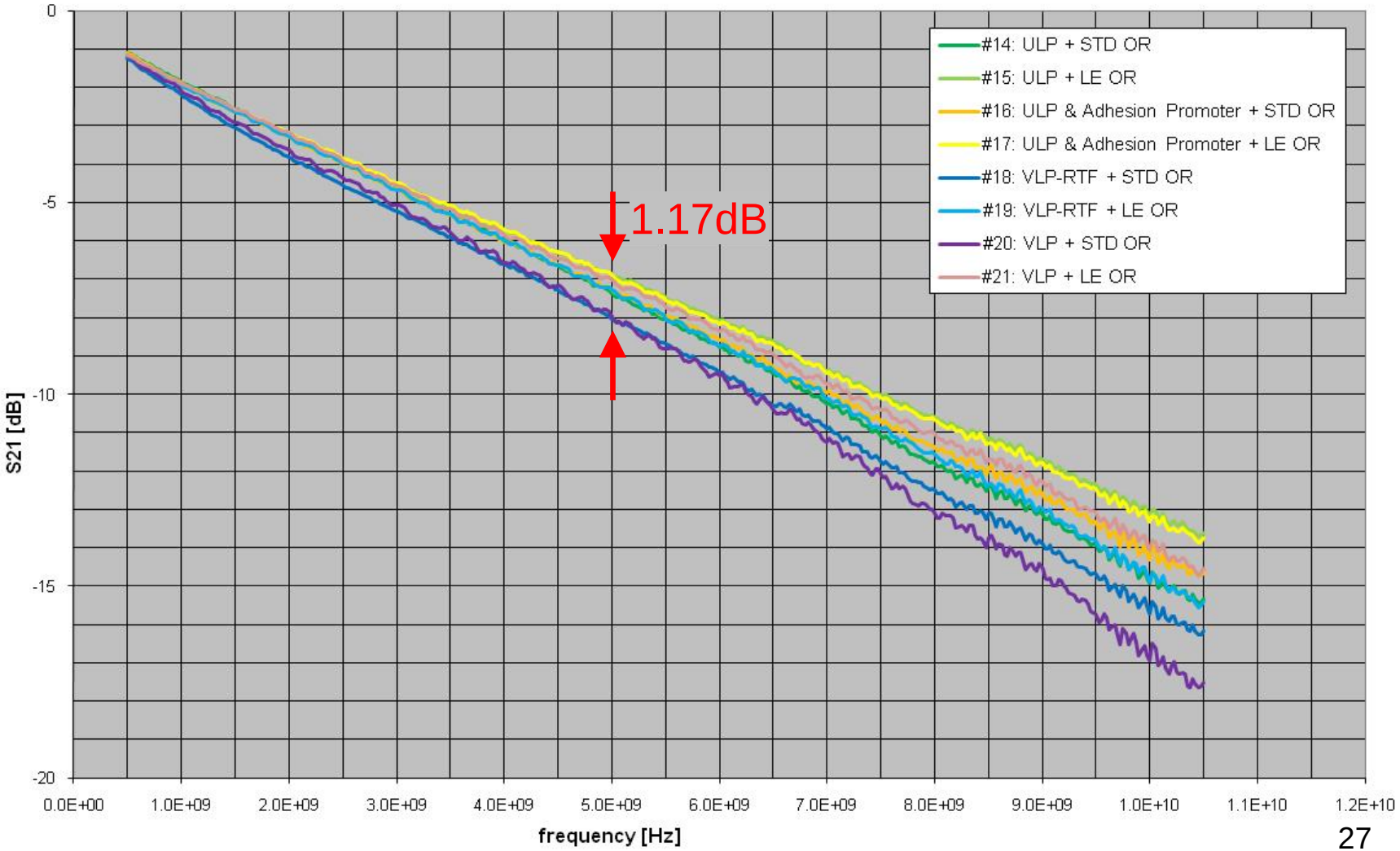
example of S21 curves



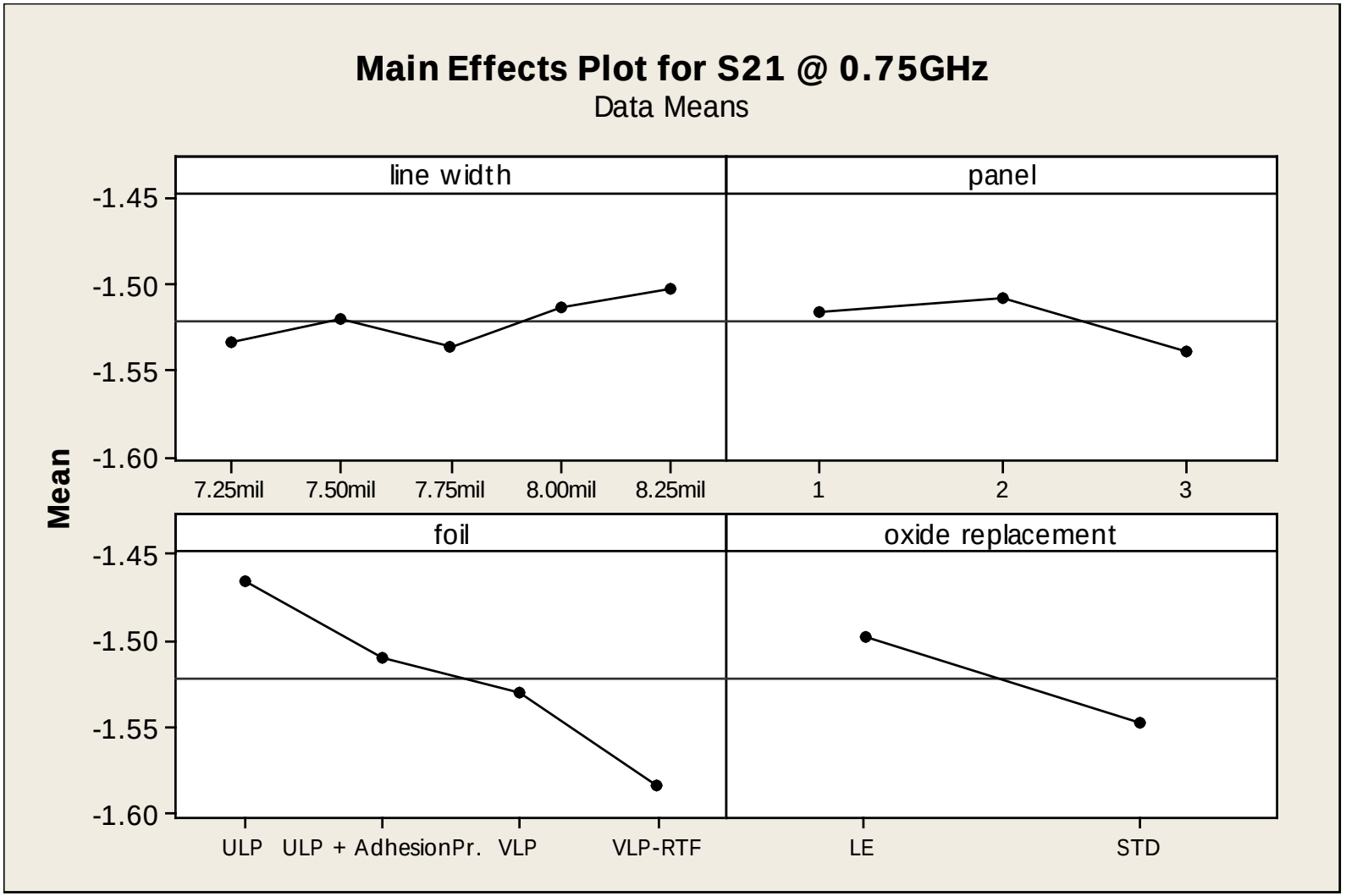
comparison S3 /S6



S21 delta @ 5 GHz



insertion loss at 0.75GHz



Anova results @ 0.75GHz

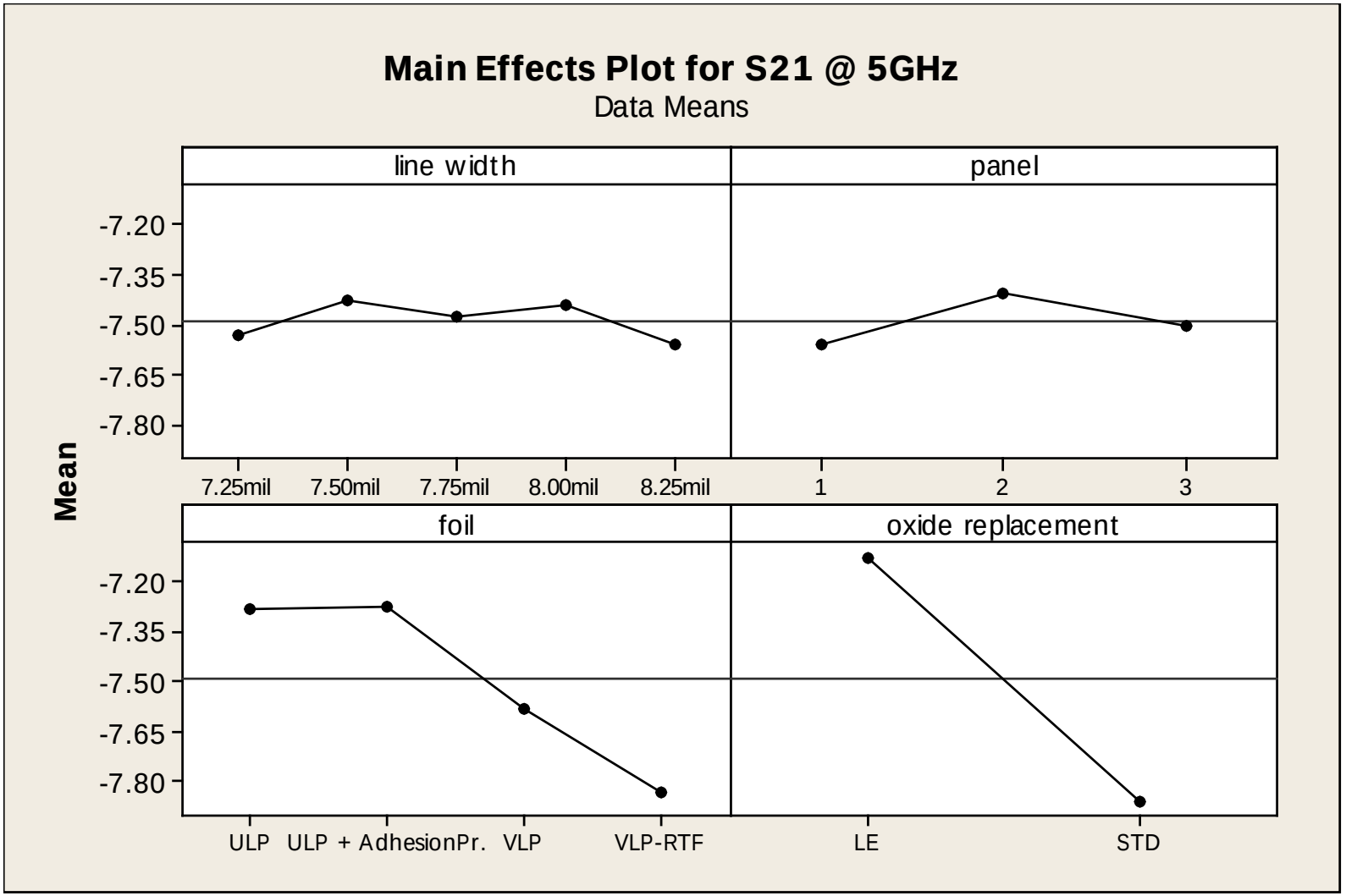
Analysis of Variance for S21 @ 0.75GHz, using Adjusted SS for Tests

Source	DF	Seq SS	Adj SS	Adj MS	F	P
foil	3	0.438365	0.438365	0.146122	21.67	0.000
oxide replacement	1	0.149110	0.149110	0.149110	22.11	0.000
line width	4	0.035666	0.035666	0.008916	1.32	0.262
panel	2	0.040515	0.040515	0.020258	3.00	0.052
Error	228	1.537558	1.537558	0.006744		
Total	239	2.498146				

S = 0.0821199 R-Sq = 38.45% R-Sq(adj) = 35.48%

- line width is accounting for less than 1.5% → non significant factor
- panel is accounting for ~1.6% → non significant factor
- oxide replacement is accounting ~6% of the variation → significant factor
- copper foil type is accounting for 17.5% of the variation → main influencing factor

insertion loss at 5GHz



Anova results @ 5GHz

Analysis of Variance for S21 @ 5GHz, using Adjusted SS for Tests

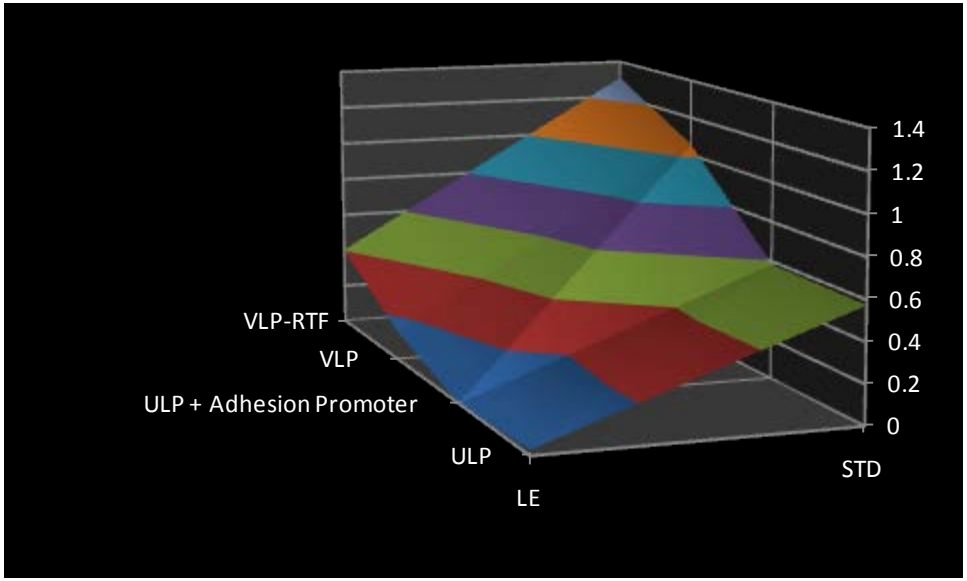
Source	DF	Seq SS	Adj SS	Adj MS	F	P
foil	3	13.0978	13.0978	4.3659	37.31	0.000
oxide replacement	1	32.4591	32.4591	32.4591	277.38	0.000
line width	4	0.6387	0.6387	0.1597	1.36	0.247
panel	2	0.9754	0.9754	0.4877	4.17	0.017
Error	228	26.6810	26.6810	0.1170		
Total	239	77.3533				

S = 0.342085 R-Sq = 65.51% R-Sq(adj) = 63.84%

- line width is accounting for <1% → non significant factor
- panel is accounting for ~1.3% → non significant factor
- oxide replacement is accounting for ~42% of the variation → main influencing factor
- copper foil type is accounting for ~17% of the variation → main influencing factor

summary / electrical results

oxide replacement / Cu Foil	standard	low etch
ultra low profile	7.55dB [0.58dB]	7.01dB [0.03dB]
ultra low profile + adhesion promoter	7.56dB [0.58dB]	6.98dB [ref]
very low profile	8.03dB [1.06dB]	7.13dB [0.15dB]
very low profile - RTF	8.28dB [1.31dB]	7.38dB [0.40dB]



S21 @ 5GHz: absolute [delta]

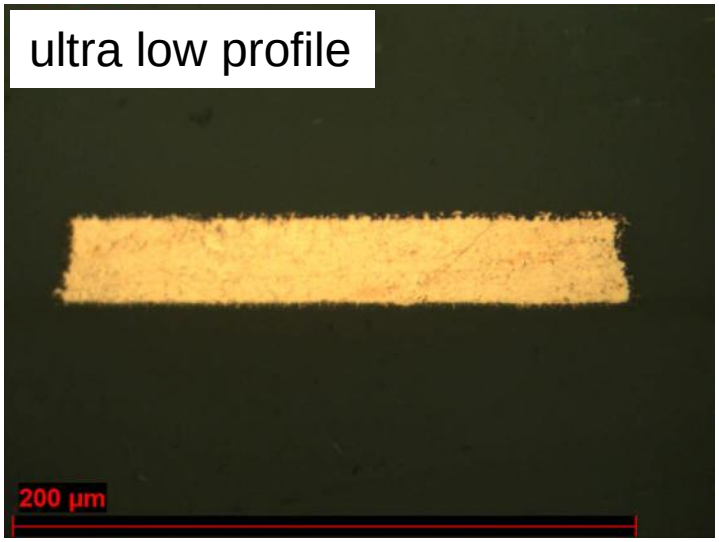
summary / electrical results

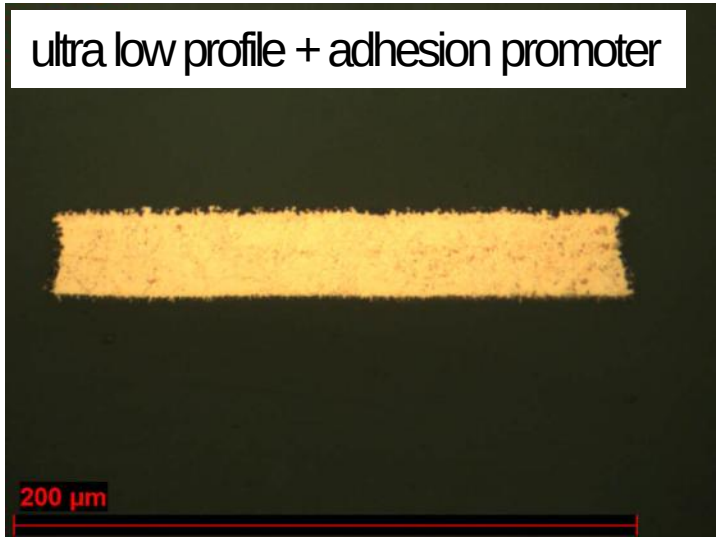
- there is a significant difference in insertion loss between matte side treated VLP and reverse treated VLP
- the insertion loss can be significantly reduced by going from VLP to ultra low profile type of foils
- the addition of an adhesion promoter for the ULP foil has no negative effect at 5 GHz

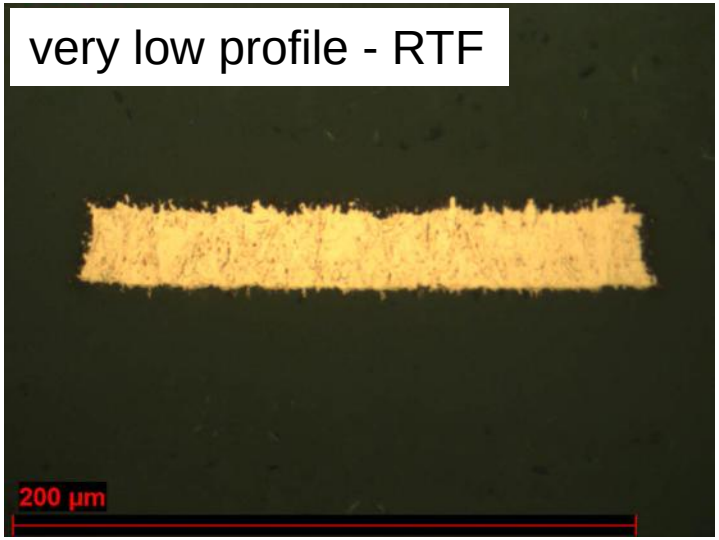
- usage of a low etch oxide replacement instead of a standard oxide replacement is beneficial regarding insertion loss
  - this is true for standard Cu foil (see presentation from Apex2011)
  - this is also true for lower profile copper foils

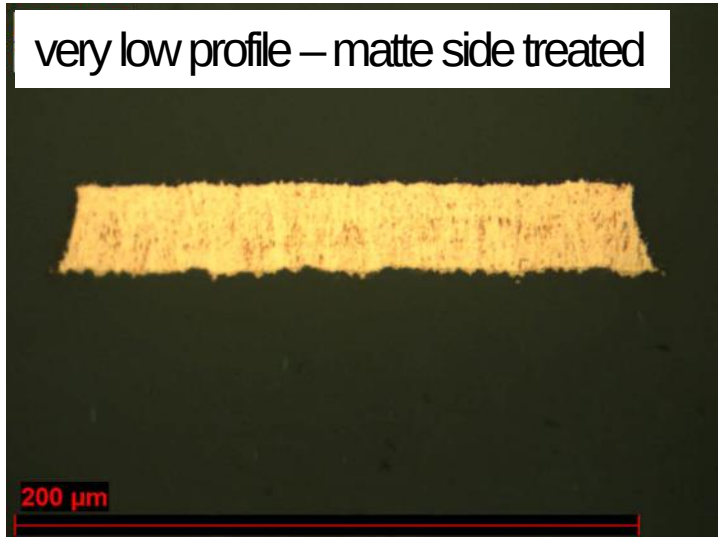
cross section pictures

standard oxide replacement

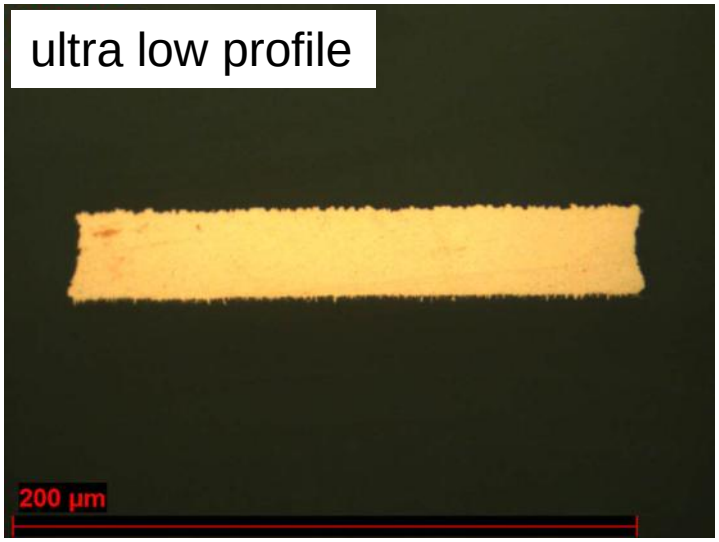


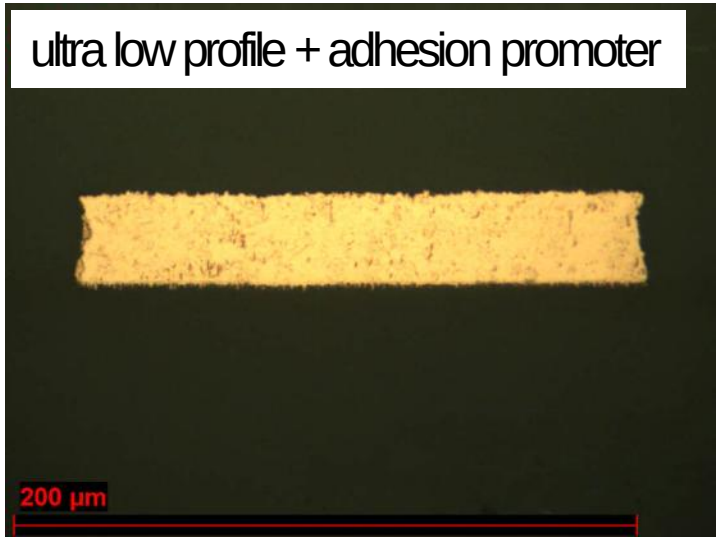


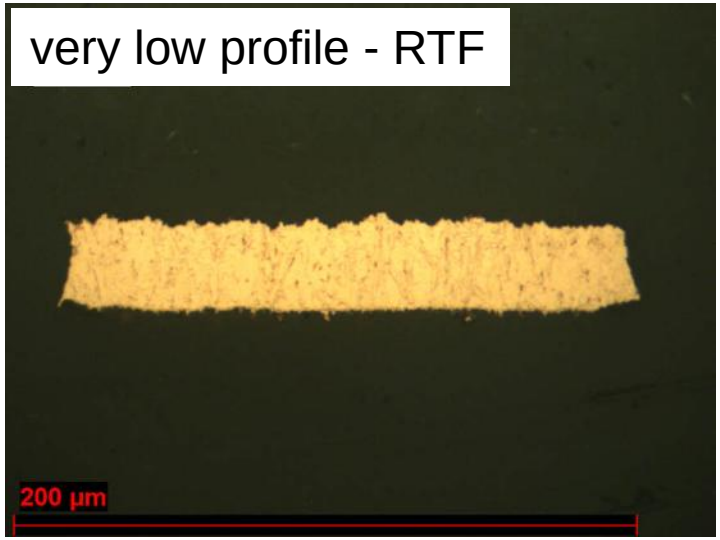


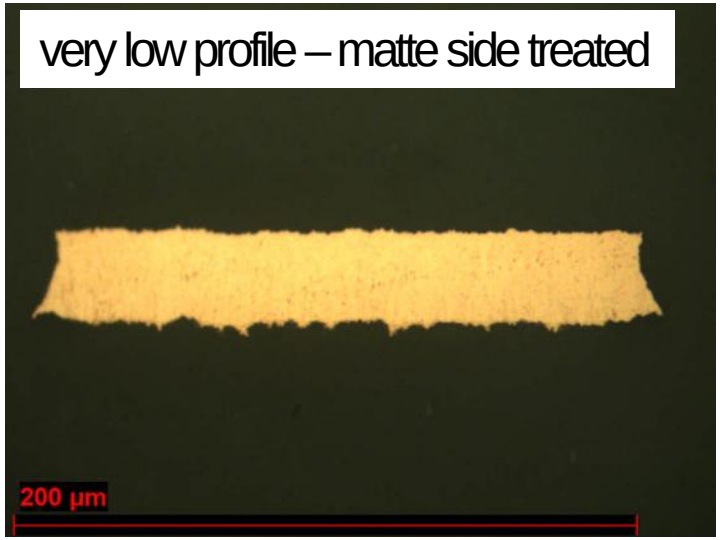


low etch oxide replacement









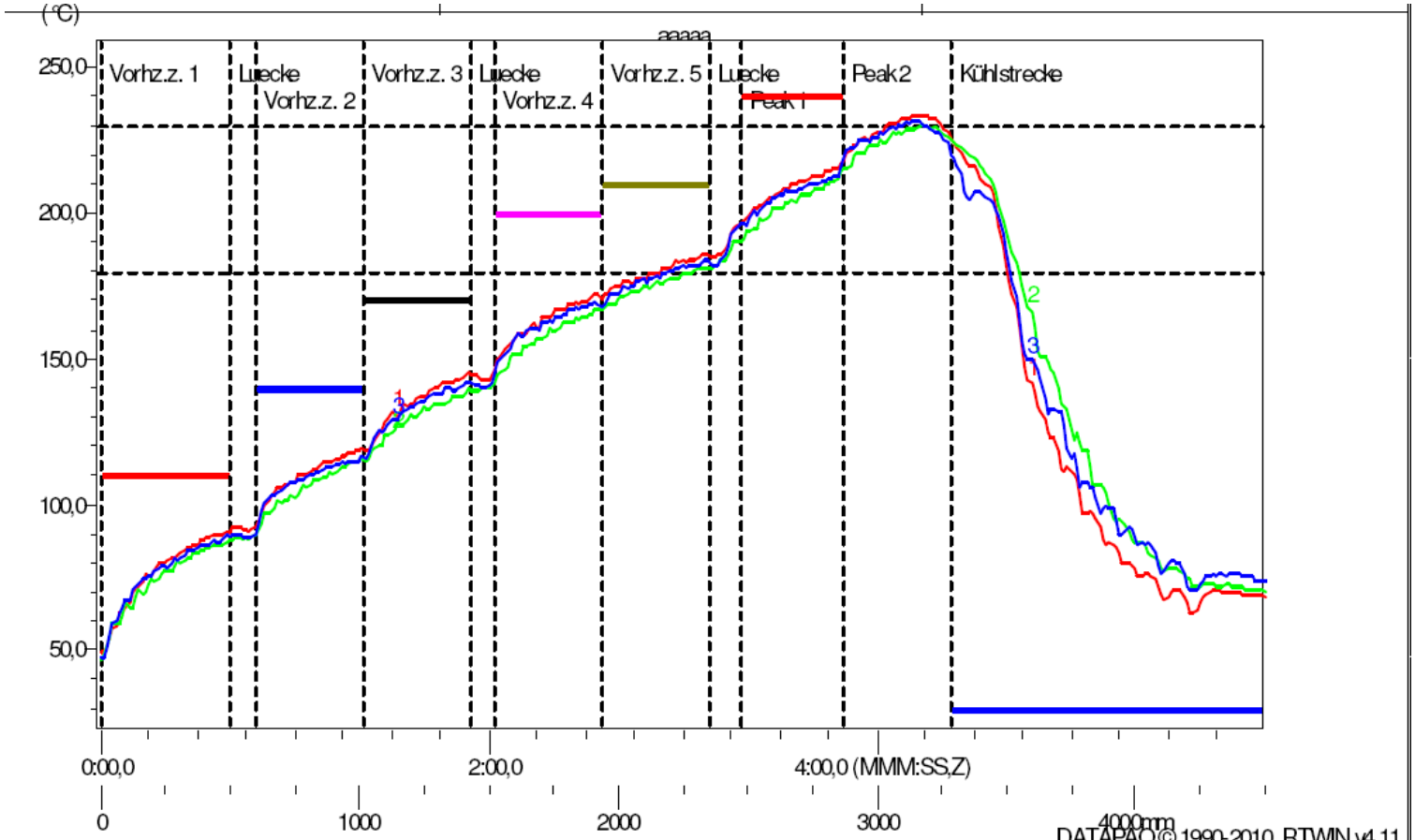
thermo mechanical reliability

performed tests

- repeated reflow 6x @ 230 deg C
  - as received
- solder float testing 3x 10 sec @ 288 deg C
  - after preconditioning 4h @ 150 deg C
- solder float testing 6x 10 sec @ 288 deg C
  - after preconditioning 4h @ 150 deg C

- cross section to check for degradation

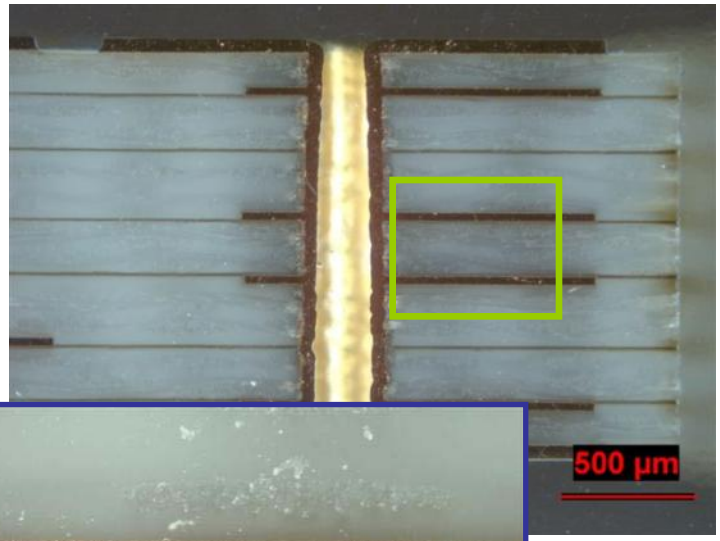
reflow profile

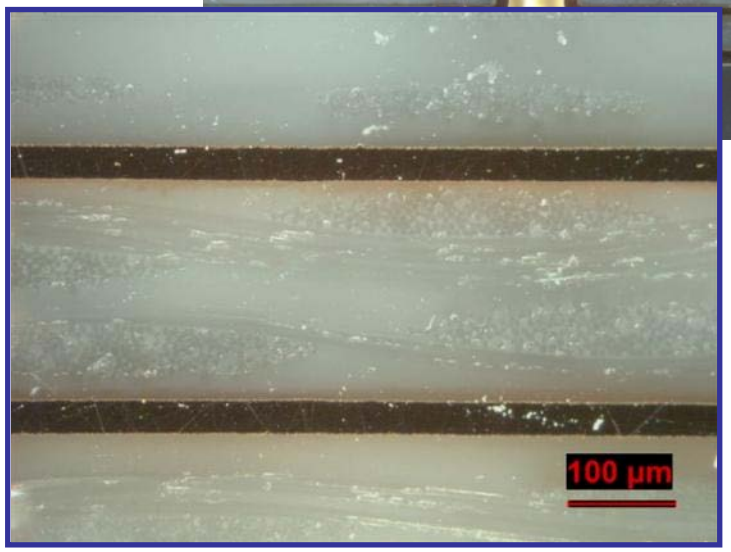


	Zone	xhz.z	uecke	xhz.z	xhz.z	uecke	xhz.z	xhz.z	uecke	Peak	Peak2	lstre
Geschwindigkeit	Oben	110	0	140	170	0	200	210	0	240	265	30
750,0 (mm/min)	Unten	0	0	0	0	0	0	0	0	240	265	0

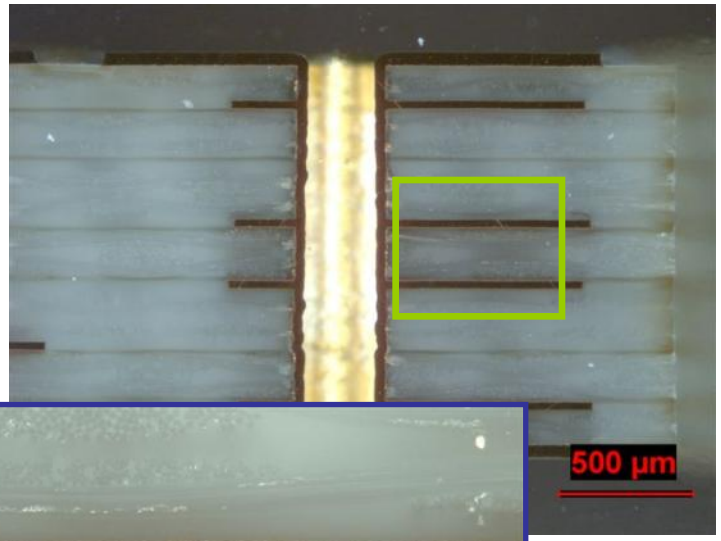
cross section after 6x reflow

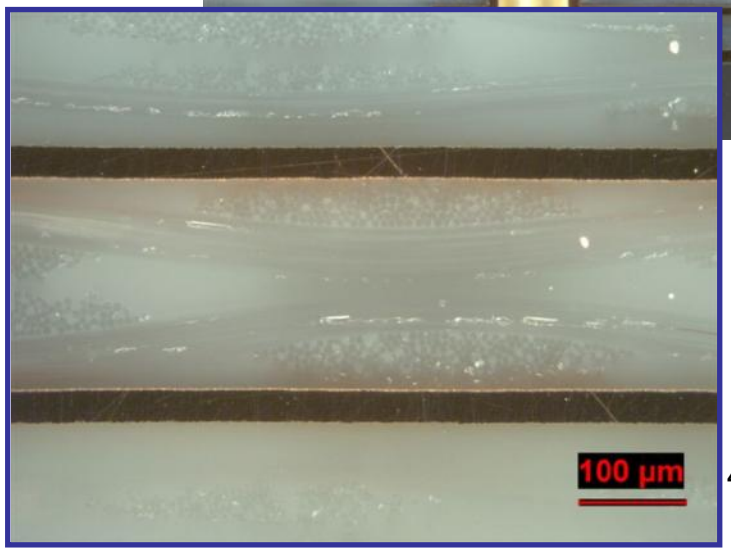
ULP / STD OR:





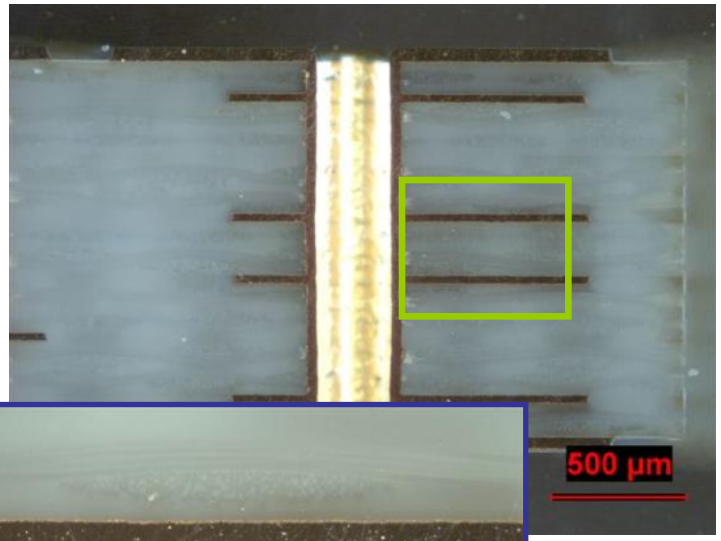
ULP / LE OR:

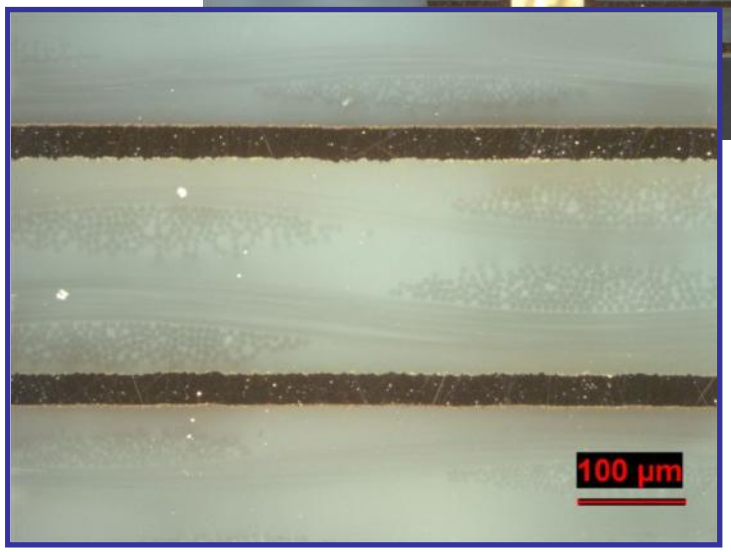




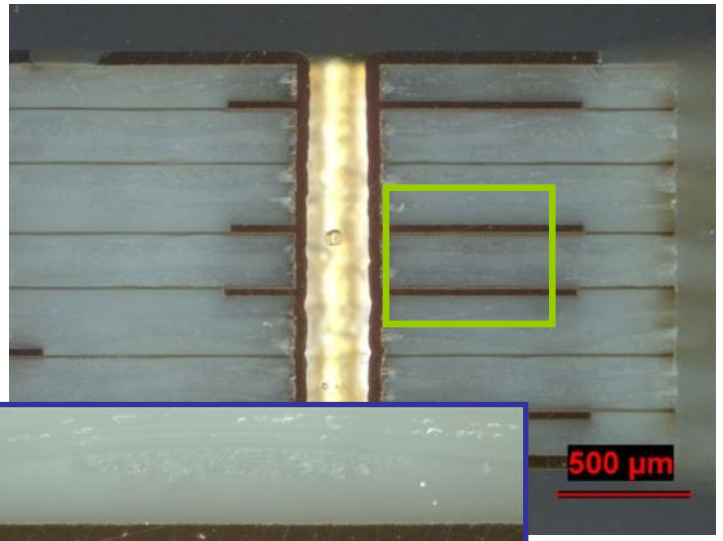
cross section after 6x reflow

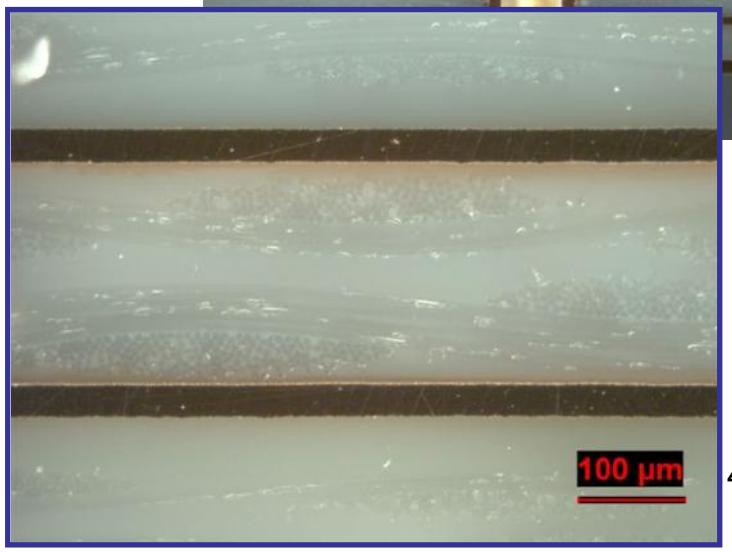
ULP + Adhesion Promoter / STD OR:





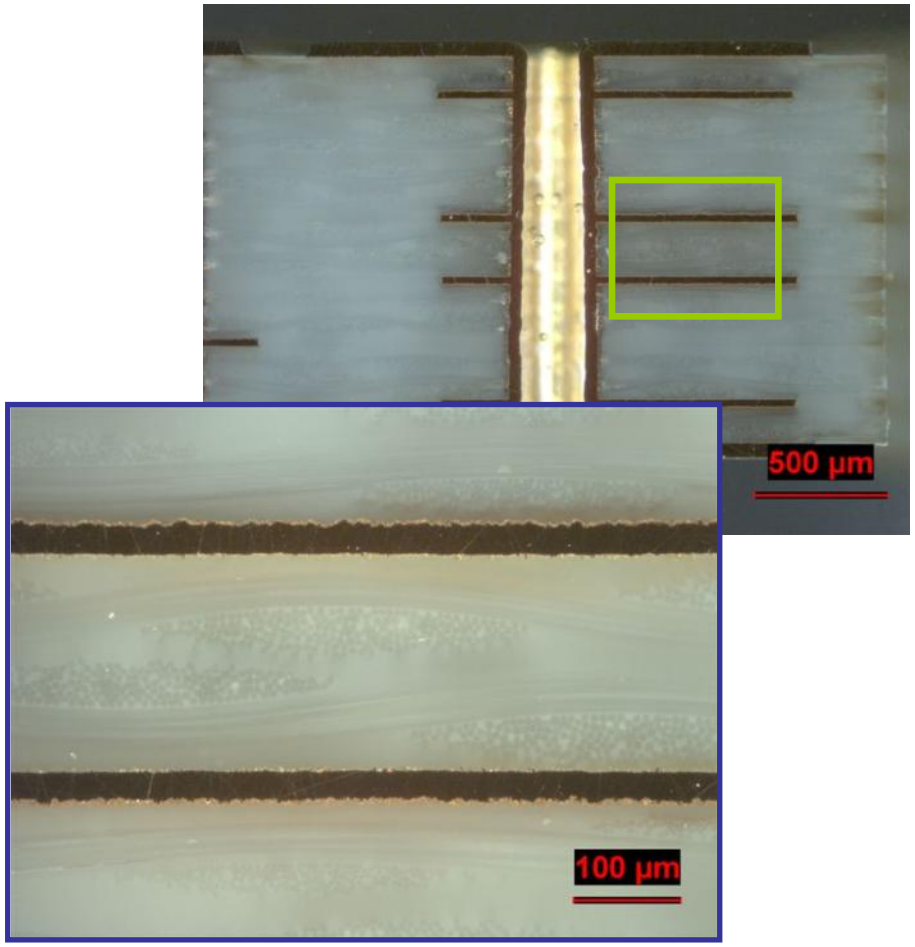
ULP + Adhesion Promoter / LE OR:



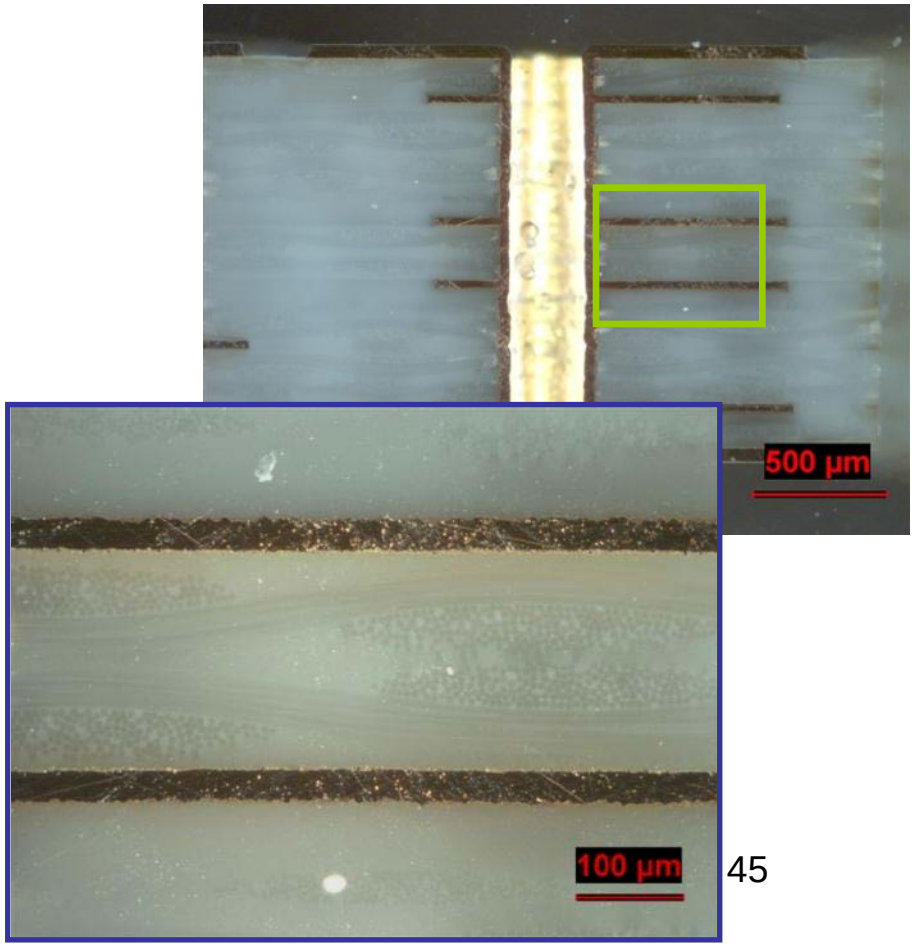


cross section after 6x reflow

VLP-RTF / STD OR:

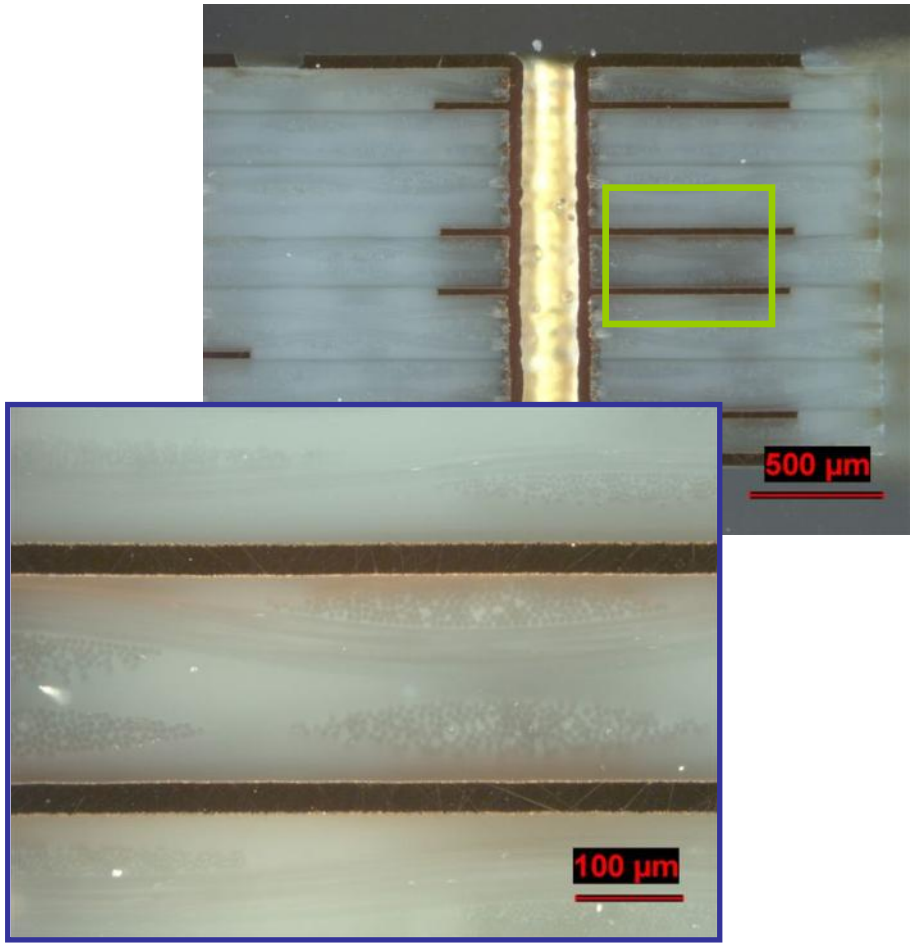


VLP-RTF / LE OR:

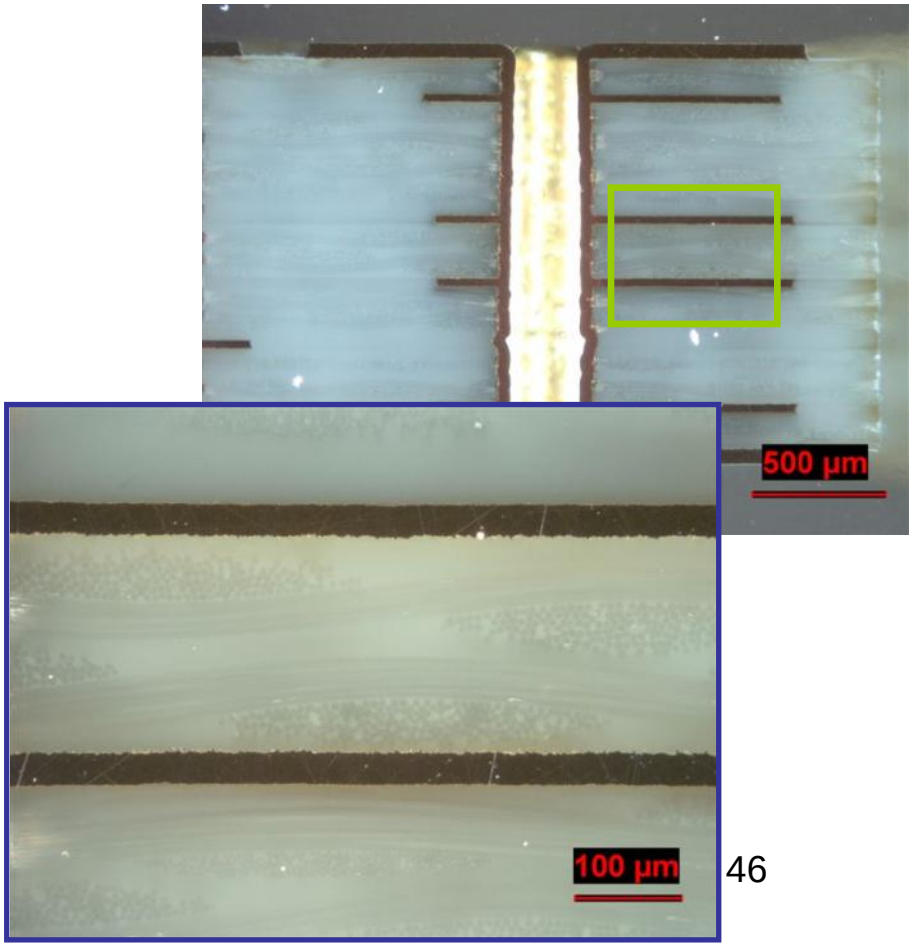


cross section after 6x reflow

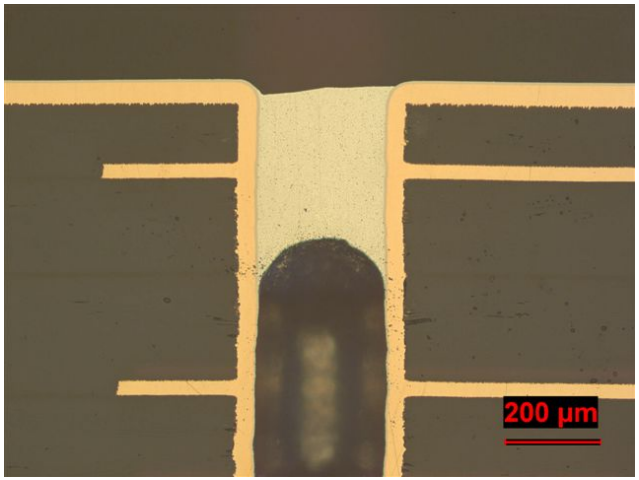
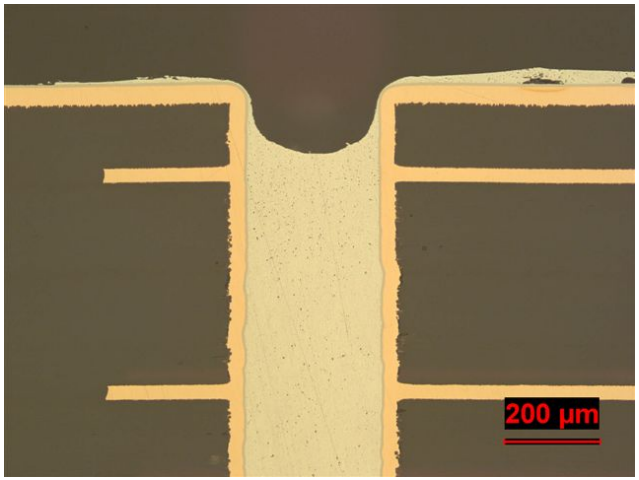
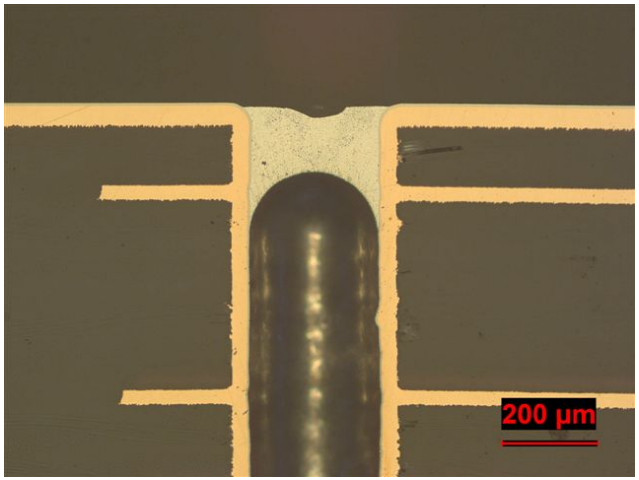
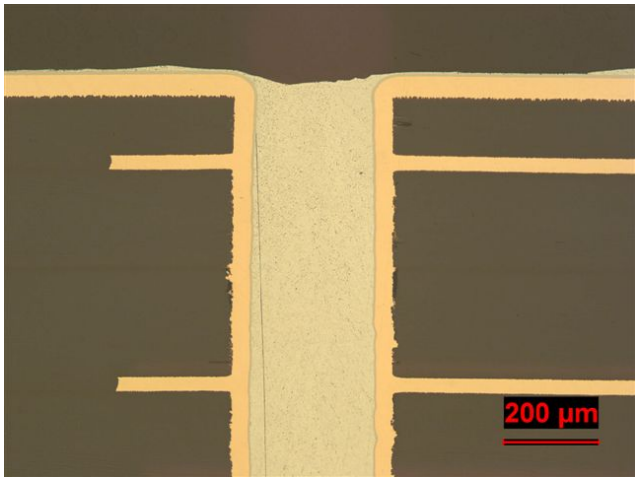
VLP / STD OR:



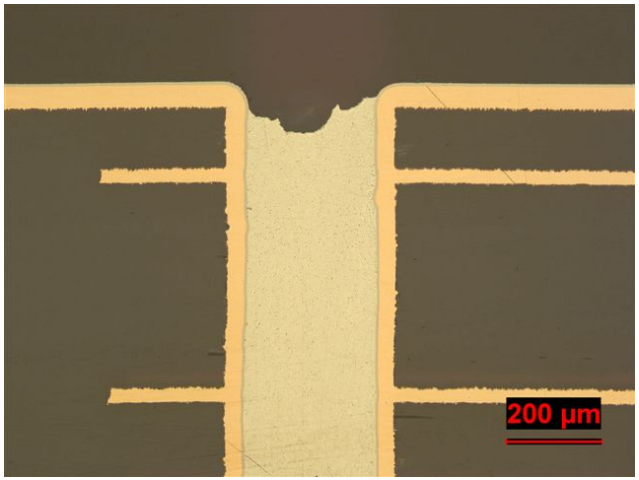
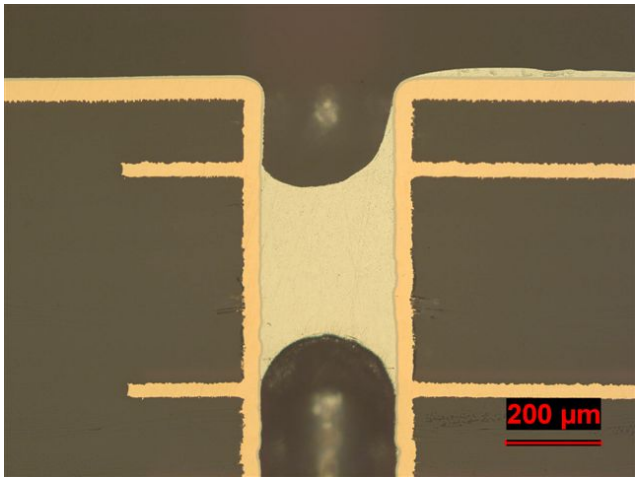
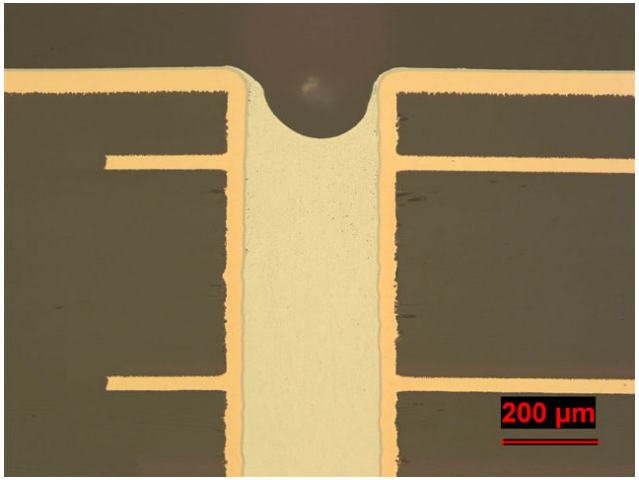
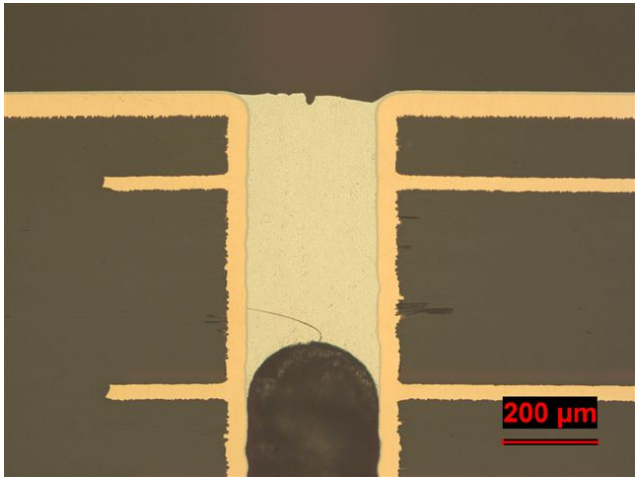
VLP / LE OR:



after 6x solder shock

	standard OR:	low etch OR:
ULP:		
ULP + Adhesion Promoter:		

after 6x solder shock

	standard OR:	low etch OR:
VLP-RTF:		
VLP:		

summary / reliability testing

- solder float tests
  - all samples have survived solder float testing
  - no delamination issues have been observed
- reflow simulation testing
  - the reflow simulation testing at 230 deg C shows no irregularities
  - none of the samples show delamination

Thank You