SMT Manufacturability and Reliability in PCB Cavities

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Abstract
Considering technological advances in multi-depth cavities in the PCB manufacturing industry, various subtopics have materialized regarding the processing and application of such features in device manufacturing.

In a previous paper[1] the topic of solder paste printing on PCBs on standard SMT equipment and with multiple cavity depths was investigated. The success of solder paste printing is a prerequisite for further assembly and reliability of the entire electronic construct. In this paper we intend to examine the overall manufacturability and subsequently analyze the reliability of multi-depth cavity PCBAs, presupposing the presence of solderable features within these cavities.

The intended methods of evaluation for manufacturability will be the evaluation of solder paste volume (PV) and warpage performance.

The intended methods of evaluation for reliability will be the evaluation of mechanical loading (drop test) and thermal loading (TCT, reflow) on PCBA test vehicles.

The aim of these investigations is to identify any possible criteria of a solderable multi-depth cavity PCB, which may affect manufacturability and/or reliability, and if so to which magnitude. Thus, we expect to locate general and possibly specific advantages and/or limitations of such a product under a standard manufacturing environment.

In an effort to achieve a broader understanding of the entire process and product scope, the participants in the trial are an HDI PCB manufacturer, stencil manufacturer and a global EMS manufacturer.

Introduction
Two major drivers in the electronics industry are electrical and mechanical miniaturization. Whereas lines and spaces have been getting smaller over the years, mechanical miniaturization has thus far been mostly limited to decreasing layer-count and material thickness.

As PCB cavities increasingly become part of the solution required for component and product miniaturization, efficiency, effectiveness and reliability of manufacturing with such cavities becomes more relevant. In a previous paper from the same authors a methodology of printing solder paste in multi-depth cavity PCBs was analyzed. The results clearly demonstrated that at least one proposed technical solution can prove effective in terms of solder paste transfer efficiency and volume during a multi-depth single stencil print.

Above and beyond the ability to effectively bring solder paste into the PCB cavities, the manufacturability and reliability aspects must also be examined in order to provide a better picture of how cavity PCBs and above all PCBs with multi-depth cavities can be employed in standard SMT manufacturing. This is the target of this paper.

Employing similar means of solder paste printing, stencil manufacturing, PCB manufacturing and SMT manufacturing as those described in the previous paper (means which will for the sake of completeness also be described here) data has been gathered and tests performed which will demonstrate the variations currently inherent to this manufacturing constellation.

The test methodology applied in this investigation employs commonly used reliability test specifications. The target here is to supply comparable data where possible.

The results will conclude that no major deviations from cavity-relevant elements could be observed during manufacturing. Furthermore, in terms of mechanical reliability comparable results for non-cavity plane and cavity plane were recorded.

Test vehicle

The decision to use the JEDEC JESD 22-B111 test vehicle is based on the target of making these analyses as comparable as possible to standard testing methods and materials. Some modifications have been made to the overall JEDEC JESD 22-B111 test vehicle design to account for the local depth reduction (i.e. cavities), but the general design, dimensions and structure remains the same.

Four versions of the test vehicle were manufactured to account for the following test factors:

- No cavity (POS 1)
- 1 layer removed (POS 2)
- 2 layers removed (POS 3)
- 3 layers removed (POS 4)

The boards have been populated as shown as in Table 1.

Table 1 – Number of needed cards and components for drop test (DT) and TCT

	DT		TCT	
	Cards	Components	Cards	Components
POS 1	9	5	4	15
POS 2	9	5	4	15
POS 3	9	5	4	15
POS 4	9	5	4	15
Total	**36**	**180**	**16**	**240**

The created vehicle contained a footprint (see Figure 1) of a daisy chain level 2 components with following specification:

- Package size 12x12x0,86mm
- 288 I/O
- Die size: 10x10mm
- 0,5mm pitch
- LF35 solder ball

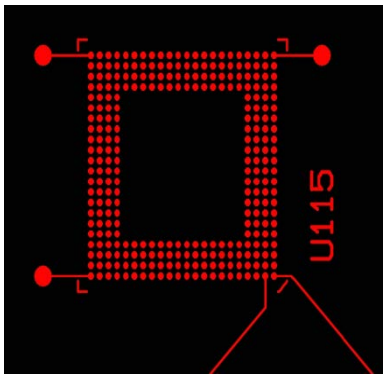


Figure 1 - Footprint of daisy chain component

This footprint was placed according the JEDEC JESD 22-B111 on all four versions. Minimum distance from the test pattern to the cavity wall for the experiment was 2mm. Each component is connected to a PTH terminal on the edge of the card through microvias throughout the inner layers (see Figure 2).

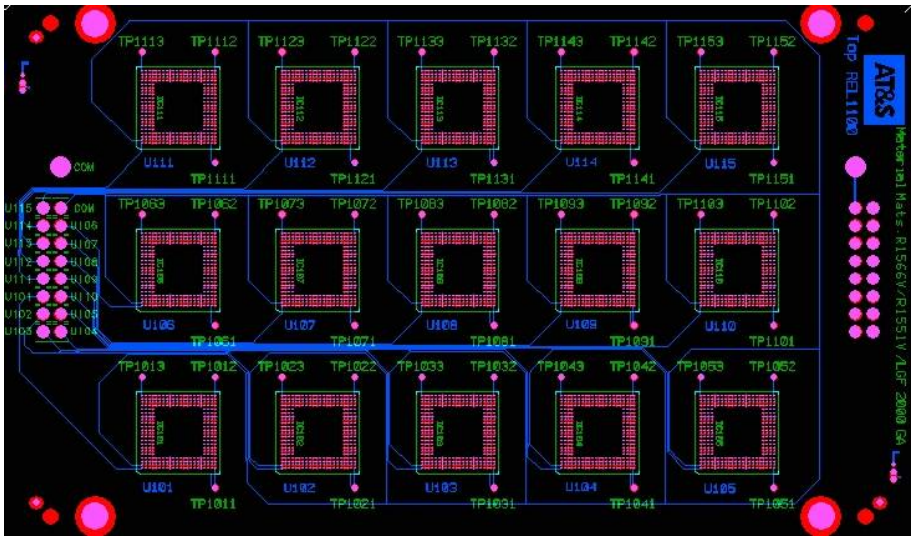


Figure 2 - JEDEC Standard no. 22-B111

The build for the 1,1mm thick PCB was a 10 layer multi-layer with Panasonic R1551W material (halogen-reduced epoxy resin based prepreg) with exception to the outer layers, which contained Mitsui MRG300 RCC-Foil (Resin Coated Copper-Foil. This stack up and production method based on patented technology[2] enables the removal of multiple layers at varying depths. The specific depth is achieved by the application of a paste on the release layer with subsequent relamination of the entire board. A laser cutting process then trims and cuts at the predetermined shape to separate the relaminated layers from the release layer. The final step is then "cap removal" and paste stripping (see Figure 3). What remains is the solder footprint pattern. Diverse surface finishes and also application of solder mask can be employed in the cavities. Entek HT (Organic surface protection) was used as a surface finish for all solder able surfaces (see Figure 4).

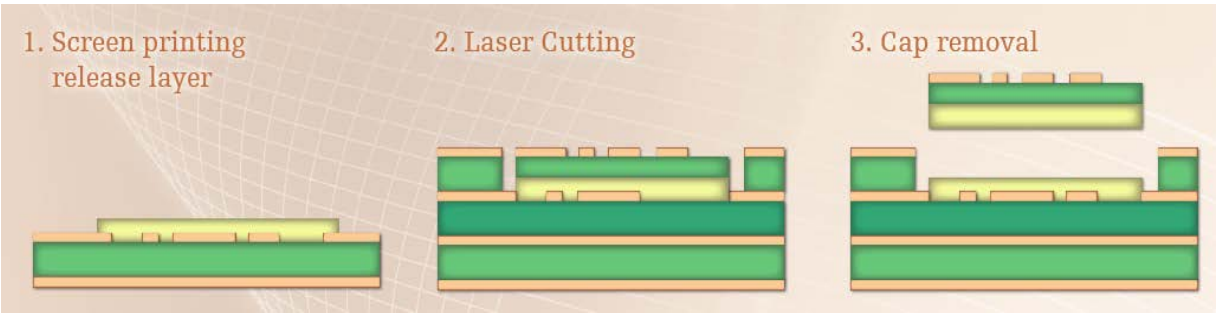


Figure 3 - Schematic process flow of cavity formation

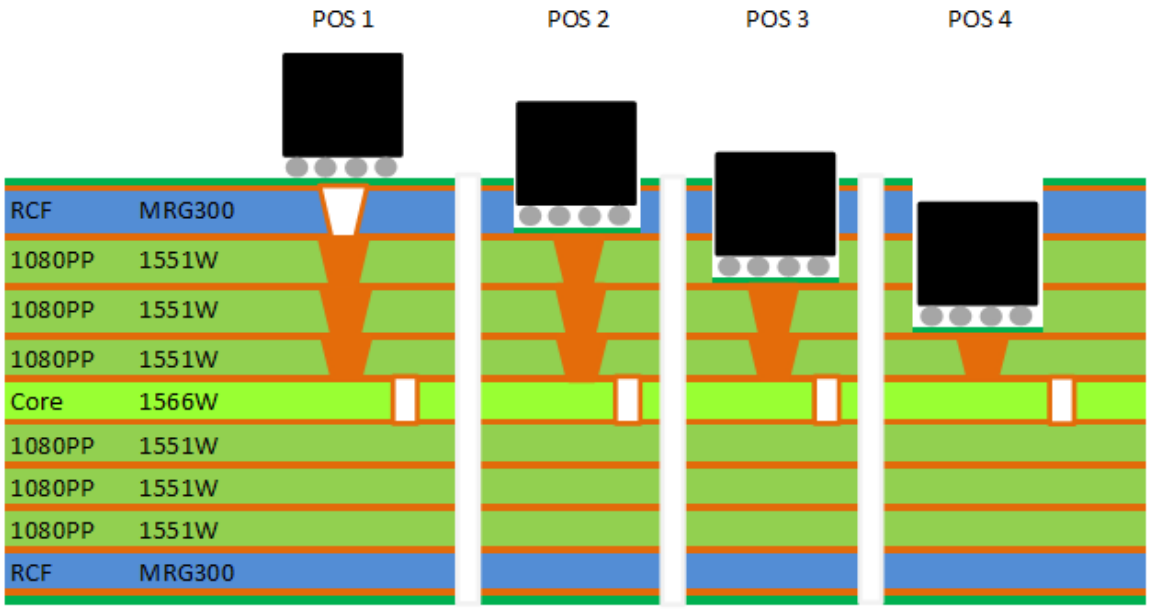


Figure 4 - Test vehicle build-up with recessed areas (PCB and components are not to scale)

Test material, equipment and manufacturing equipment
The solder paste used for these trials is a commonly used SAC type 3 lead-free solder paste.

The solder paste printing system used in this trial is a two part system consisting of a step stencil (Christian Koenen) and a customized squeegee. Four stencils were used in alignment with the four test vehicle variations, all of which were laser cut and electro polished stainless steel stencils glued in polyester mesh and tensioned in an aluminum frame. The outer dimensions of the stencils were (736 x 736 x 40 mm³). Stencil base thickness was 0,1mm, 0,3mm and 0,4mm and 0,5mm corresponding the cavity depth. One stencil (0,1mm) was a standard stencil (no accommodation for cavities). The three remaining stencils were provided with local depth reduction in the respective print area (see Figure 5). Stencil thickness in the print area was 100µm for all stencils.

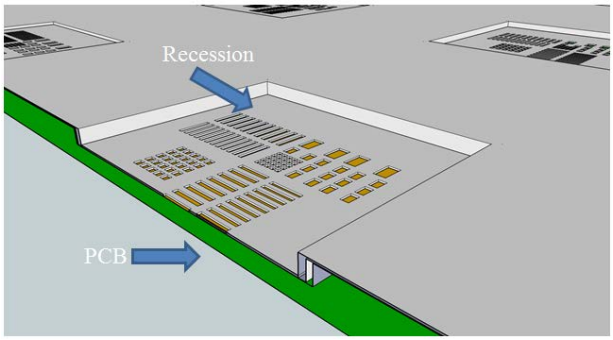


Figure 5 - Overview Step Stencil on PCB (demonstration)

The customized steel squeegee is 196mm in length and is designed with movable sections to account for depth. Therefore the multi-depth top side contour of the stencil is accounted for through the varying pressure of the movable squeegee sections (Figure 6).

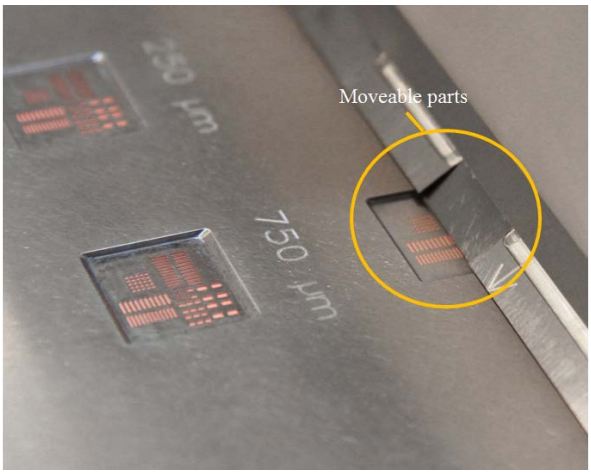


Figure 6 - Squeegee blade with moveable parts (demonstration)

The sloped edges of the step openings in the stencil ensure that excess paste is removed from the stencil during printing (see Figure 7).

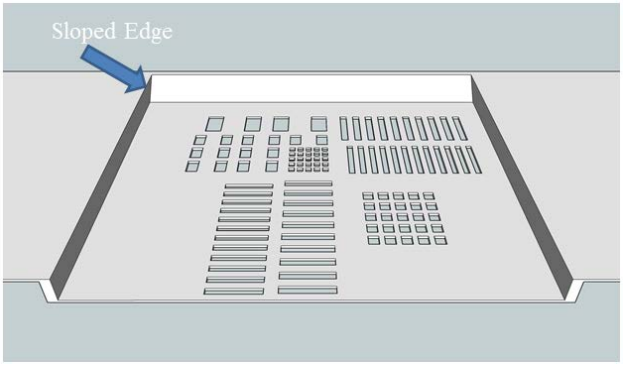


Figure 7 - Cross section of Step stencil with sloped edge (demonstration)

The printer used was a DEK265. The parameters employed are shown in Table 2.

Table 2 - Printing parameters

Parameter	Value	Unit
Speed F/B	30/ 30	mm/s
Squeegee pressure F/B	35/ 35	N
Snap off speed	10,0	mm/s
Cleaning	Each PCB	-

The stencil and customized squeegee were subsequently installed and registered. The squeegee must be aligned to the specific cavities for which the movable parts are designed. This was done manually using the alignment of arrow markings on both stencil and squeegee (Figure 8).

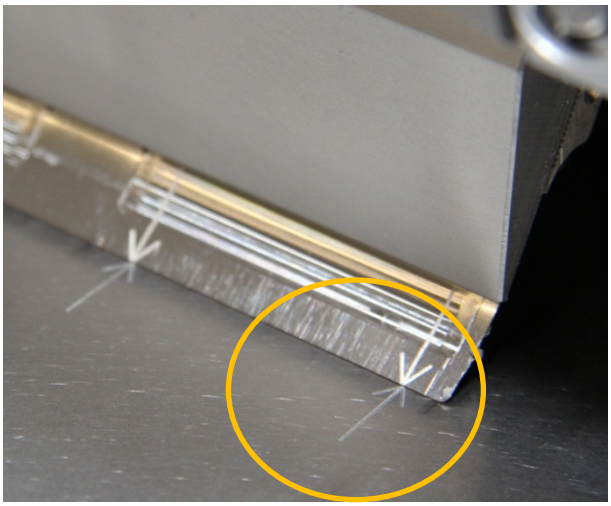


Figure 8 - Alignment marking on Squeegee and stencil

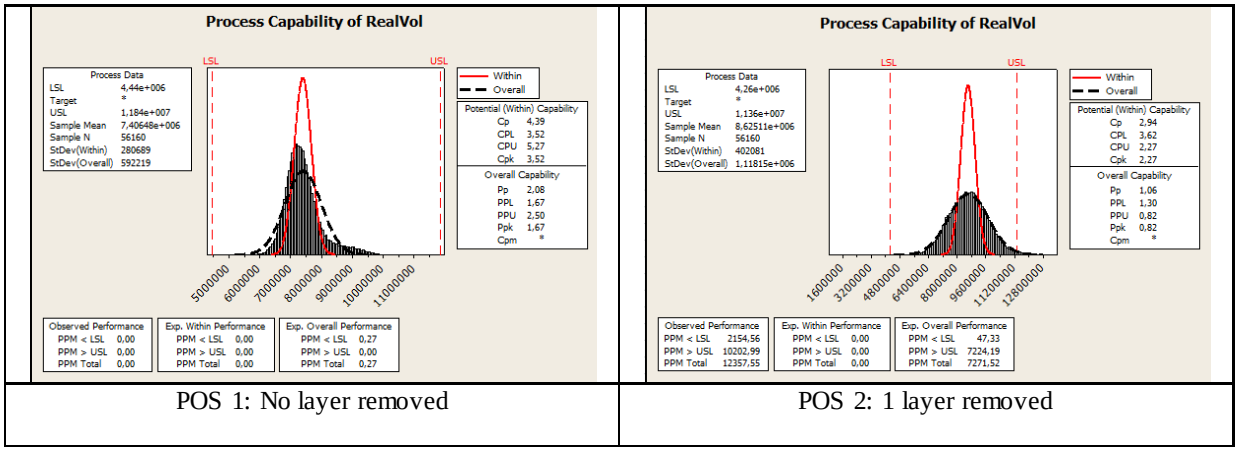
The type 3 solder paste was mixed accordingly and applied to the step stencil surface. Using the print parameters described above, several test prints were then carried out to verify effectiveness and accuracy.

For the purpose of this investigation one of the factors which shall determine manufacturability is solder paste volume. As the solder paste was applied using the same general resources (stencil type, equipment, etc.) the target was to observe variations, if any, in absolute volume when comparing the 0µm to cavity depths and amongst the variable cavity depths themselves. Post printed test vehicles were analyzed inline for solder paste volume employing a commonly used Koh-Young optical inspection device.

Table 3 - cpk values of paste volume for all test vehicles (POS 1, POS 2, POS 3 and POS 4)

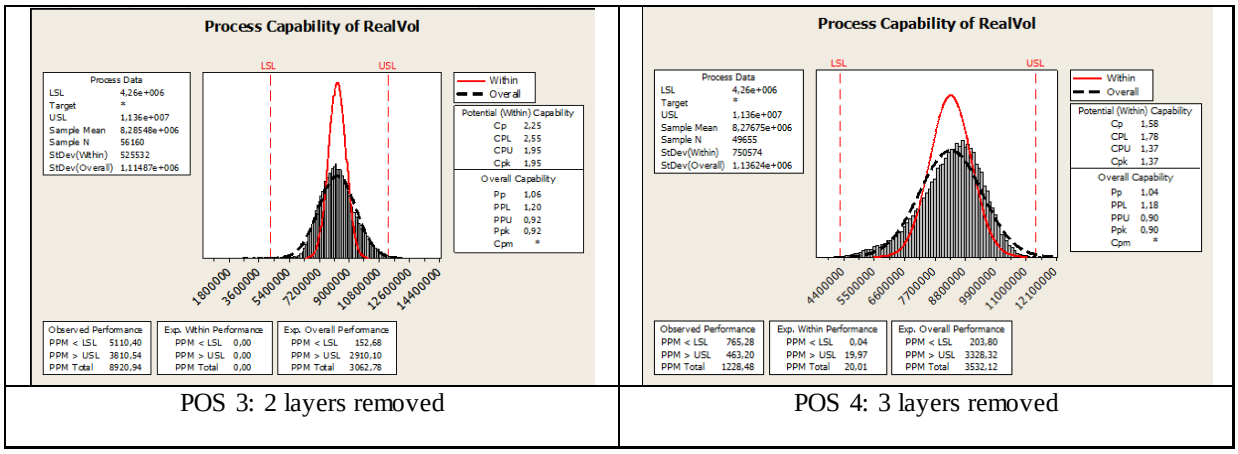
POS	cpk
1	3,53
2	2,27
3	1,95
4	1,37

When comparing the cpk values (see Table 3), one finds a clear trend in process capability under these standard conditions. While the test vehicle without cavity (0µm) displayed a comparatively high cpk (therefore consistently sufficient volume), with each reduction in layer count we see sufficient but somewhat diminishing process capability. No major deviations (voids, skips, etc.) were observed with any test vehicles during the one-pass production trials (Figure 9).



POS 1: No layer removed

POS 2: 1 layer removed



POS 3: 2 layers removed

POS 4: 3 layers removed

Figure 9 – Process capability of paste volume for all test vehicles (POS 1, POS 2, POS 3 and POS 4)

The pick and place (PNP) programming for all versions of test vehicles remained the same due to the PNP device Siplace D3 capability to determine final component placement depths by mechanical force gauging. No deviations and/or performance variations were observed in pick and place regardless of test vehicle constellation. We can therefore deem manufacturability as sufficient for this particular trial and equipment setup.

Reflow of the test vehicles was carried out successfully without any deviations observed. Furthermore all test vehicles passed the IPC-650-TM, Method 2.4.22, test for warpage, therefore eliminating (under these conditions) warpage as a hindrance to manufacturability. A standard JEDEC lead-free reflow profile was used for the trials (see Figure 10).

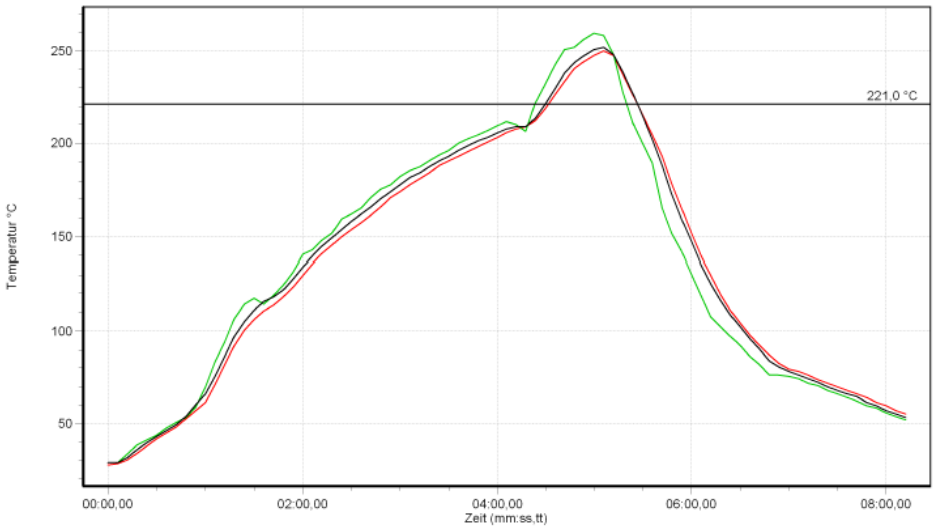


Figure 10 – JEDEC Lead-free Reflow profile

Test methods and results

Drop Test

The drop test specification was based on the JEDEC JESD22-B111 (see

Table 4). The test vehicles were soldered at the test terminal PTHs and test events were monitored online as opposed to post hoc testing and verification.

Table 4 – Drop Test Specifications

DT Device	Teknopaja
AT&S Spec	TI GR.PH-LAB-33EG
International Spec	JEDEC JESD22-B111
Acceleration:	1500g ± 10%
Pulse Duration:	0,5ms ± 10% (peak width at 10% of maximum pulse height)
Cpk:	> 1,3
Measurement Current:	1,0 mA
Voltage:	1,0 V
Resistance:	1000 Ohm
Tested Structures:	SMD and EC – daisy chains (assembled cards)
Pass/ Fail – Criteria:	Minimum acceptance criterion for components is 10 drops of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.

For these trials five center components were chosen to be assembled due to overall higher exposure to tension during this type of drop test (see **Figure 11**). As Figure 12 illustrates, these particular areas of the test vehicle deviate farthest from a neutral axis.

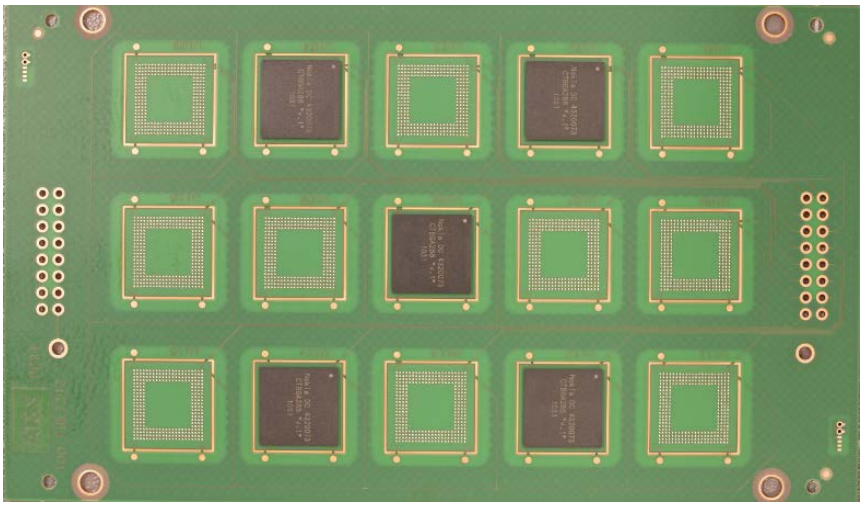
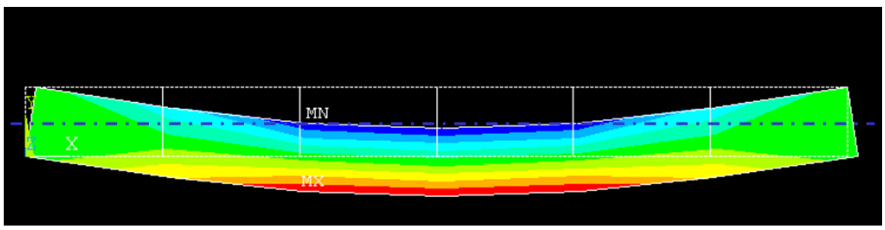


Figure 11 - Position of components for drop test



Neutral Axis

MN – Minimum tension

MX – Maximum tension

Figure 12 - Model of tension distribution at drop test

Drop test results

The 0µm test vehicle (no cavity) demonstrated the highest level of performance during drop test with an η of 527 (Figure 13). For each removed layer drop test performance was otherwise successively lower.

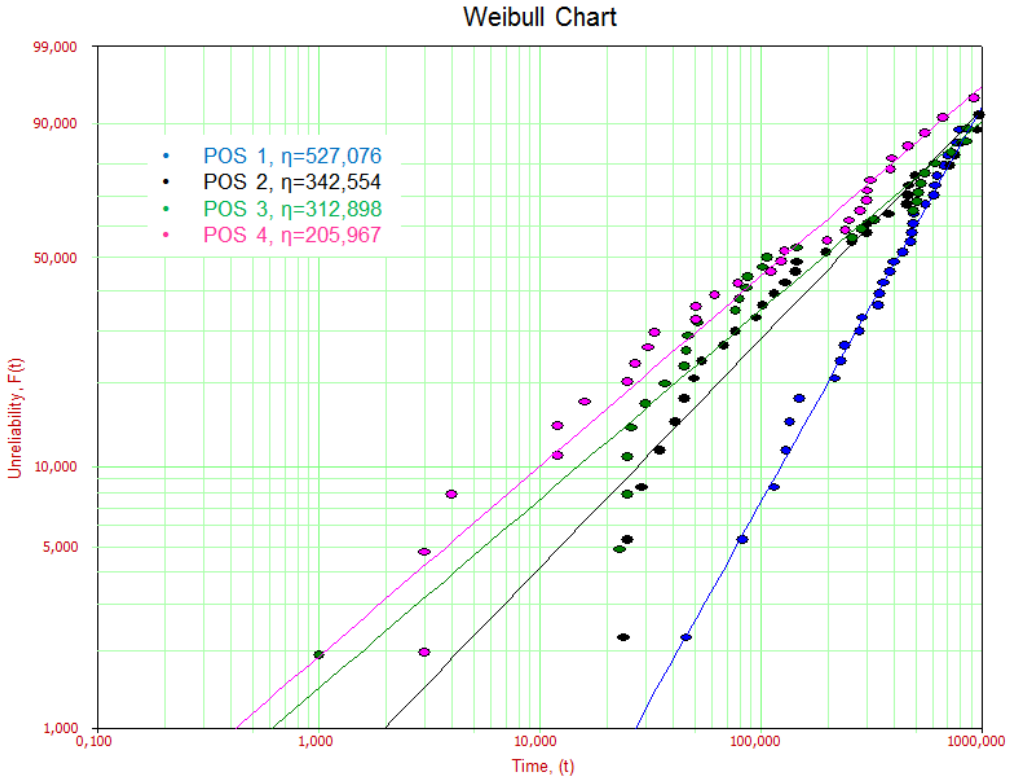


Figure 13 - Weibull chart for all test vehicles (POS 1, POS 2, POS 3 and POS 4)

The earliest failure occurred with the test vehicle POS 3. Upon investigation of the earliest failures, cross sections revealed cracks in solder near the component pad, i.e. no defects found at PCB solder joint (see Figure 14). Test vehicle POS 4 demonstrated, however, a somewhat inferior performance in general when compared with the other test vehicles.

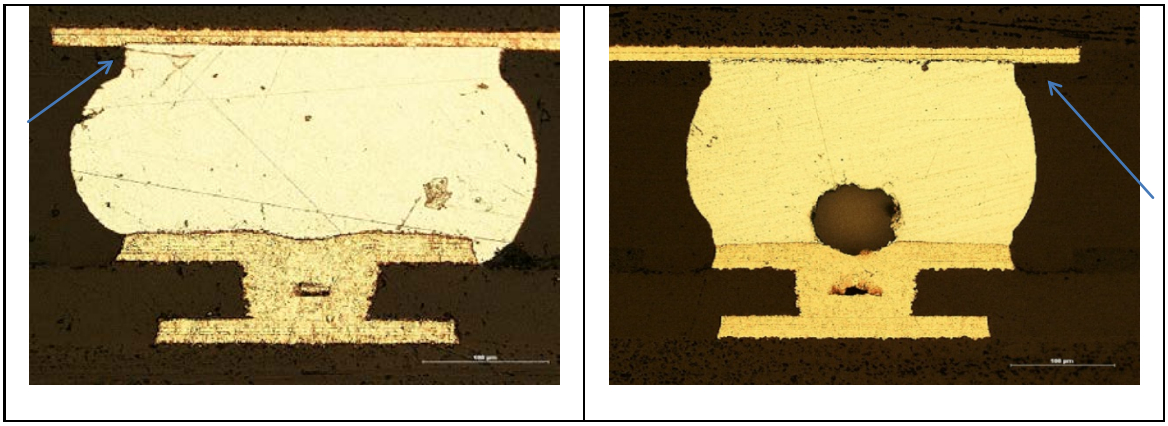


Figure 14 - Crack in solder near component pad

Test vehicles POS 2 and POS 3 displayed a similar performance in drop testing with exception of the first failure. To sum up a steady reduction in η was observed with increasing cavity depth. The specific values and the relationship to paste printing cpk will be evaluated further on in this text.

The contour plot Figure 15 clearly demonstrates a significant relationship between the cavity performances versus the outer layer (0µm POS 1) performance. The contour plot graphically illustrates the η and β of the Weibull fit. The curve plots show that η and β will fall within the marked areas at the following drop at a probability of 50%. If these plots do not converge, a statistically significant difference exists between the respective population (POS 2, POS 3 and POS 4 versus POS 1).

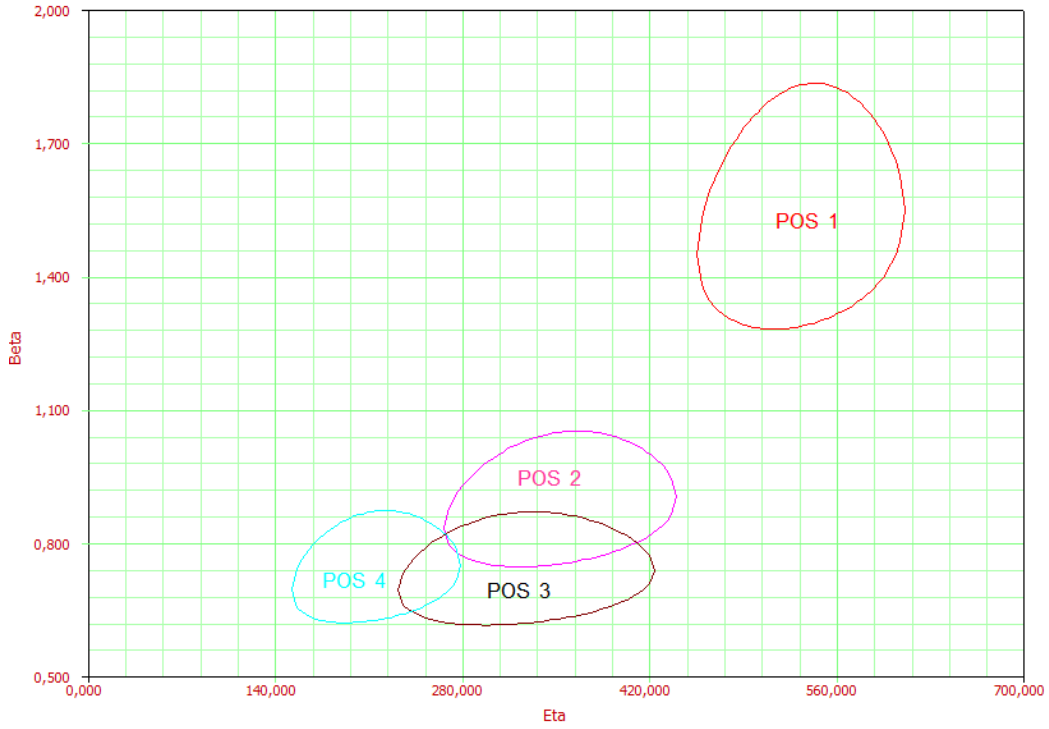
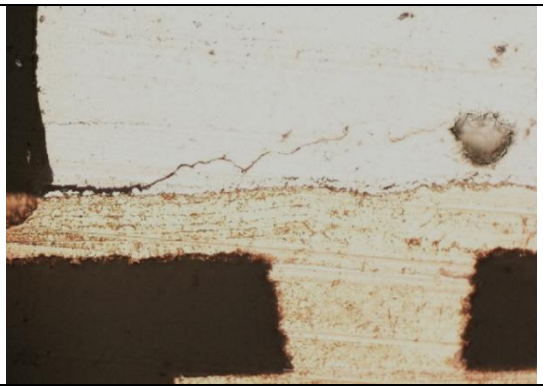
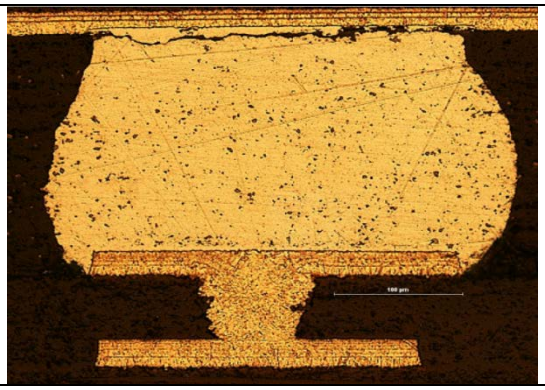


Figure 15 - Contour plot for all components for all test vehicles (POS 1, POS 2, POS 3 and POS 4)

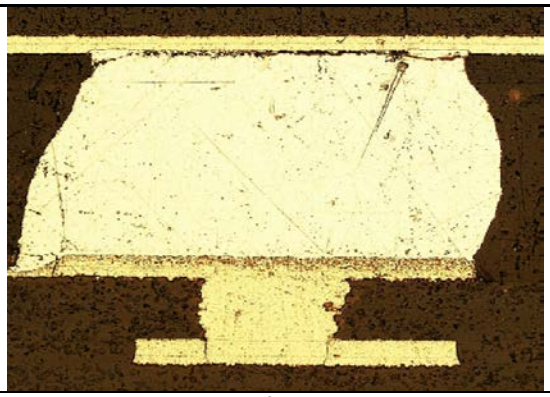
In general the observation was made that, concerning defect mode, no particular location was more prevalent than any other. Furthermore, no particularly frequent defect mode was visible during investigation (i.e. cracks in all locations throughout solder joints, bulk solder and PCB) (see Figure 16).



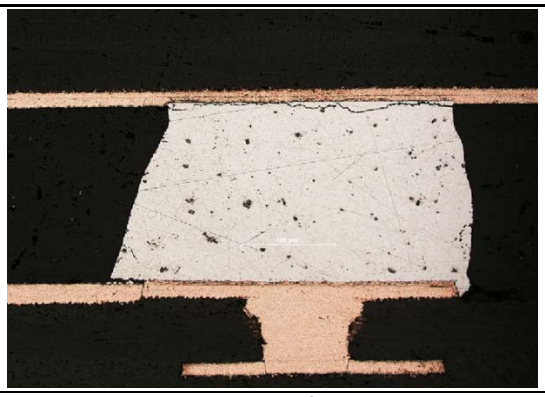
Crack in solder (239 drops, POS 1)



Crack in solder (720 drops, POS 2)



Crack in solder, pad/via deformation (555 drops, POS 3)



Crack in solder, pad/via deformation (666 drops, POS 4)

Figure 16 - Typical failure modes for drop test

TCT

The TCT specification was based on the JEDEC JESD22-A104C (see Table 5). The test vehicle based on JEDEC JESD22 B111 was soldered at the test terminal PTHs.

Table 5 - TCT specification

FUE7292	TCT parameter
Chamber:	one chamber design
Chamber parameter :	Step per cycle / Chamber / Sample Temperature / Min. Soak Time / Cycle count[3] 1 / Cold / -40 +0/-10°C / 5min / 1000 2 / Heat-up / - / - 3 / Hot / +125 +15/-0°C / 5min 4 / Cool-down / - / - The heating and cooling rate has to be set in such a way that in total 2 cycles per hour are achieved.
Measurement system:	Event Detection 4 - Point Measurement
Resistance limit:	1000 Ohm
Tested structures:	Via chains (assembled cards)
Pass/ Fail – criteria:	Assembled cards: Minimum acceptance criterion for components is 500 cycles of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.

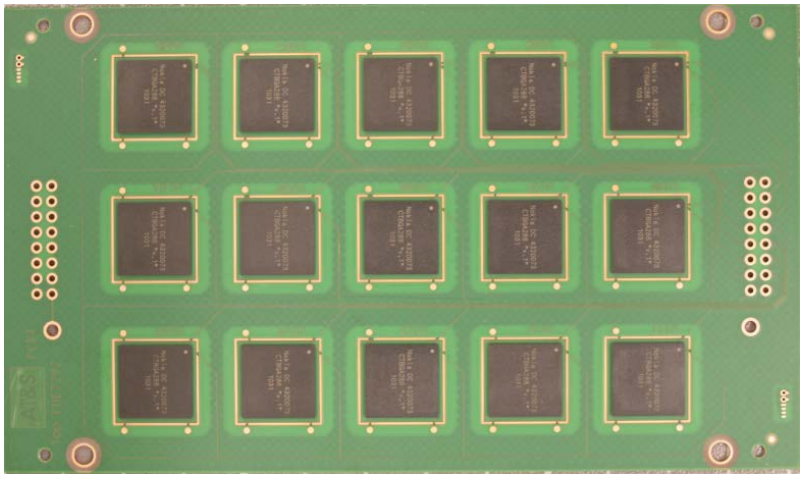


Figure 17 - Position of components for TCT

Four test vehicles were tested, each with 15 SMD daisy chains. Test events were monitored online as opposed to post hoc testing and verification (**Error! Reference source not found.**, Figure 18).

Figure 18 - Online test event registration

The boards were subjected to a constant change in temperature in the range of -40°C ↔ +125°C in a one chamber test device. The amount of cycle deemed as target was 1000 cycles.

An event is registered as a failure after demonstrating a resistance change of >1000 Ohm.

In all cavity constellations the test vehicle passed 1000 cycles without failure. No further cross sections or analyses were made due to the lack of any relevant failure. The only exception worth noting were a string of failures in the POS 1 (no cavity) starting at 627 cycles (Figure 19).

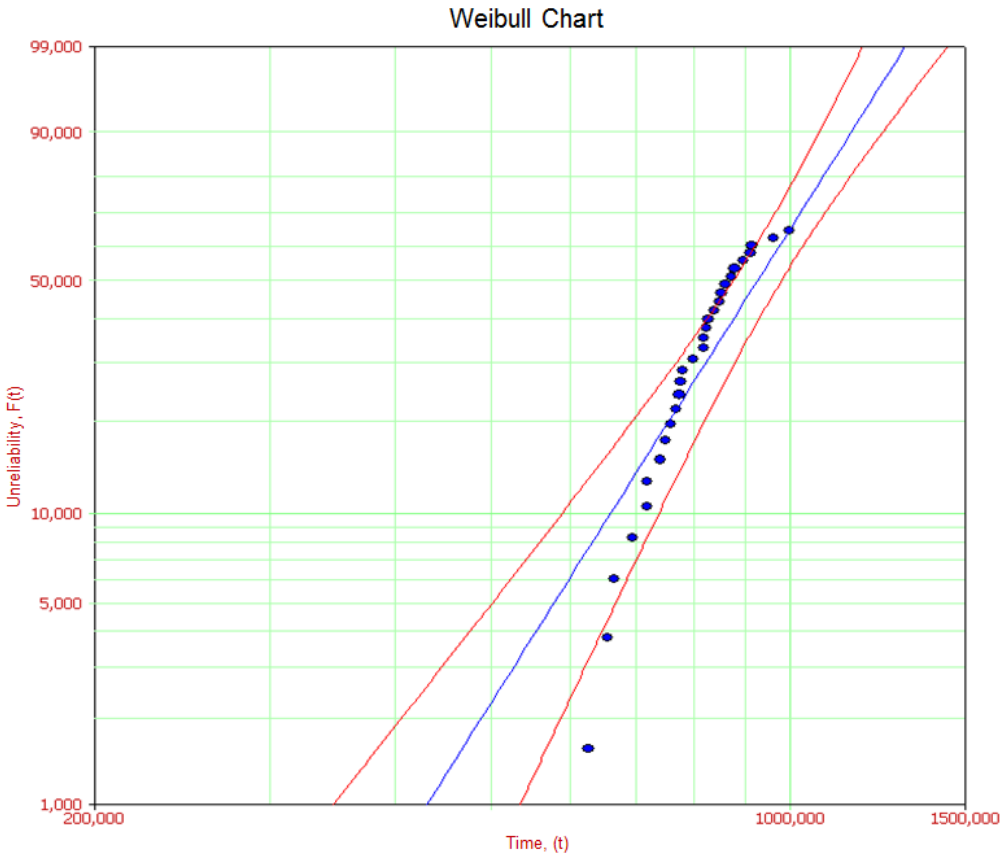
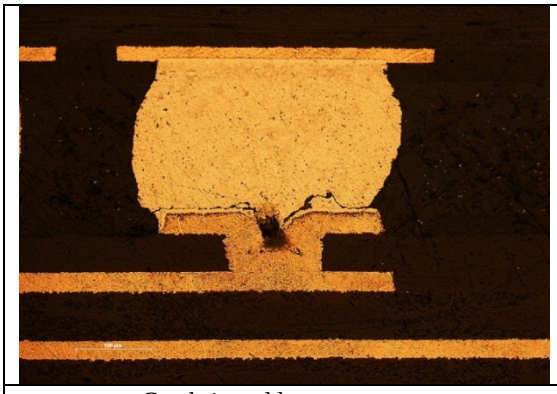


Figure 19 - Weibull for TCT of POS 1

Cross sections were made to investigate failure position and failure modes. Two failure modes were found; both revealed cracks in the solder (one near component, one near PCB, see Figure 20).



Crack in solder near component

Cracks in solder near PCB

Figure 20 - Failure modes for TCT

Conclusion/ Summary

It is worth noting in the conclusion of this analysis that the preparation, manufacturing and availability of materials (i.e. stencil, squeegee, PCB, solder paste, etc.) posed no obstacle to the overall investigation. This fact is important when highlighting our focus on the manufacturability when employing these elements.

Therefore, we posit that in consideration of standard SMT parameters with standard SMT equipment manufacturability is given, albeit with some additional considerations to be made. These considerations generally refer to solder paste volume. We found a correlation between solder paste volume and cavity depths, and a correlation of solder paste volume to drop test performance (see Figure 21). The reduction in solder paste volume cpk is graphically congruent to the reduction in drop test η. Therefore, it is fair to say that while under certain terms this system provides manufacturability,

considerations could be made to find methods to increase solder paste volume in deeper cavities and therefore positively affect reliability. Such considerations could be the aim of future analyses on this subject.

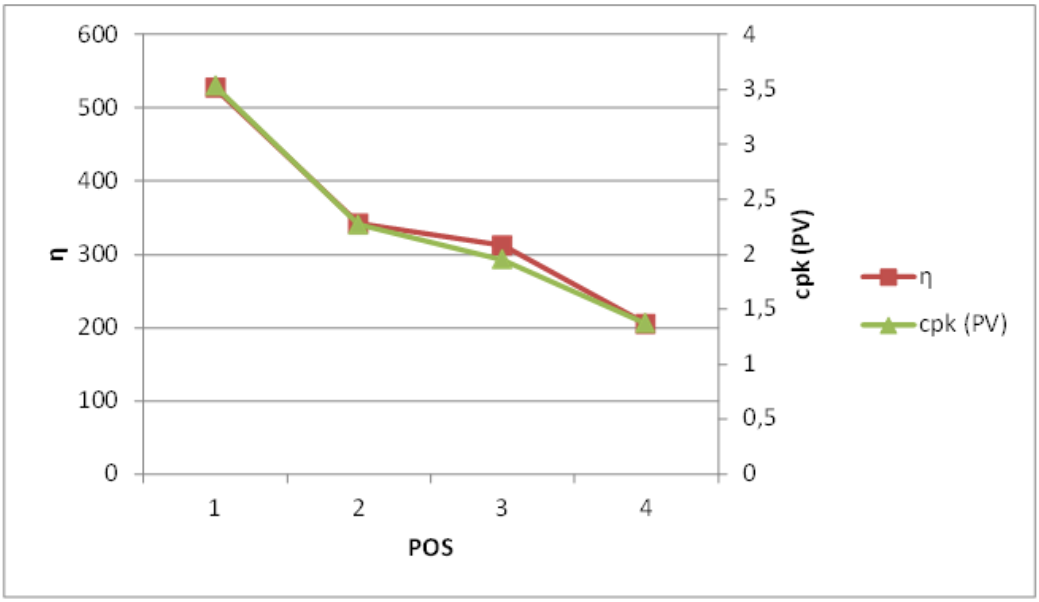


Figure 21 – Chart of cpk and η

Regarding reliability some clear trends were visible, both within the grouping of cavity test vehicles and the test vehicles as a whole. TCT performance for the components assembled in the cavities provided no indication of variable performance to standard outer layer constructs. The POS 1 board clearly showed superior drop test performance, whereas the cavity boards, while somewhat worse than POS 1, demonstrated similar behavior. One possible explanation for this general demarcation would be choice of material throughout the test vehicle. The inner layers made use of a 1080 prepreg whereas the outer layer contained and RCC-foil. There is good reason to believe that the rigidity of a glass reinforced woven material (prepreg) could present inferior drop test performance in general when compared to the elastic properties of an RCC-foil (see Figure 15). However, further analysis in this regard would exceed the scope of this paper. In light of the test vehicle construction and test results one could extrapolate further considerations to improve reliability performance. Underfill applied to the components above and within the cavities, for example, could be expected to exhibit a superior drop test performance.

Further scope of investigation on this topic may include involving further test variables and considerations of specific technology design rules.

References

[1] **Application of solder paste in PCB cavities,** Markus Leitgeb and Christopher Michael Ryder, Originally distributed at the International Conference on Soldering and Reliability" , Toronto, Ontario, Canada; May 4-6, 2011

[2] **2.5D® Technology,** ® Registered Trademark AT 257759 by AT&S

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HIGHTECH STENCILS

FLEXTRONICS
INDUSTRIAL AND EMERGING INDUSTRIES

Content

- Target
- Test vehicle
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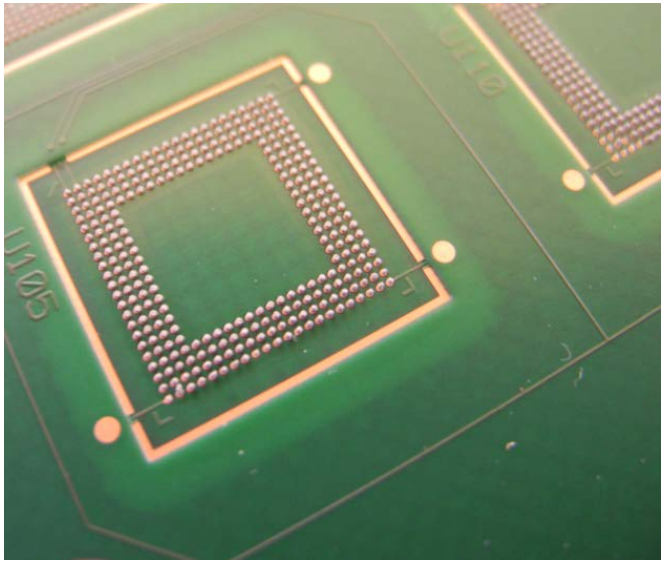
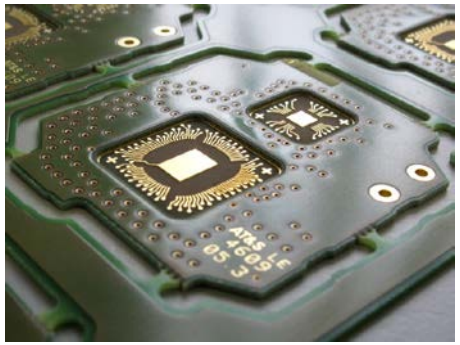
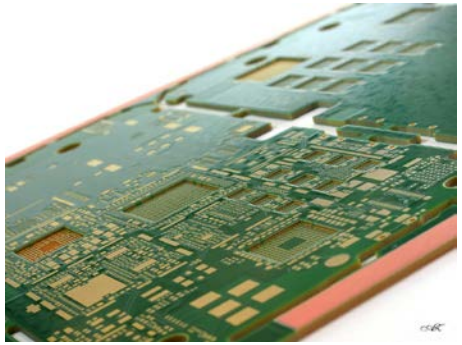
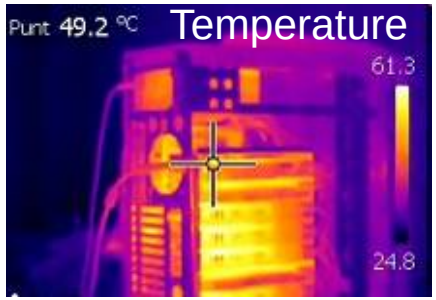


Target

PCB cavities → Manufacturing → Reliability

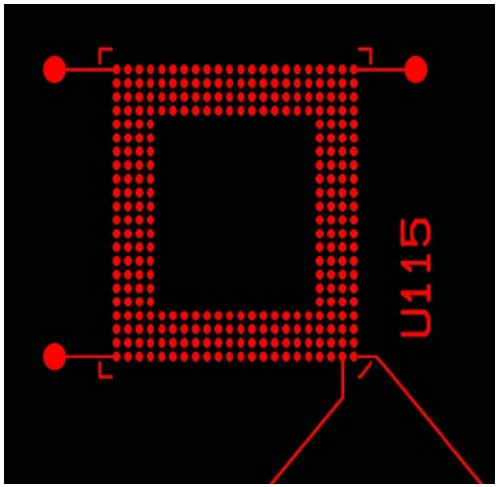






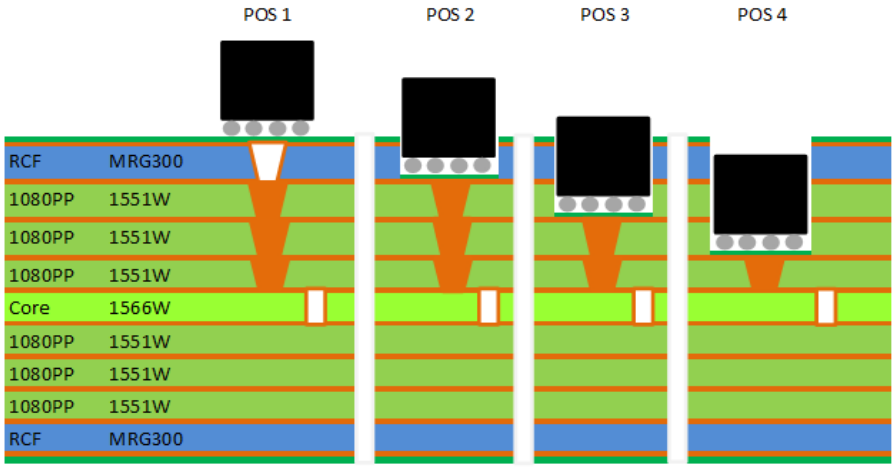
Test vehicle

Component



- Package size 12x12x0,86mm
- 288 I/O
- Die size: 10x10mm
- 0,5mm pitch
- LF35 solder ball

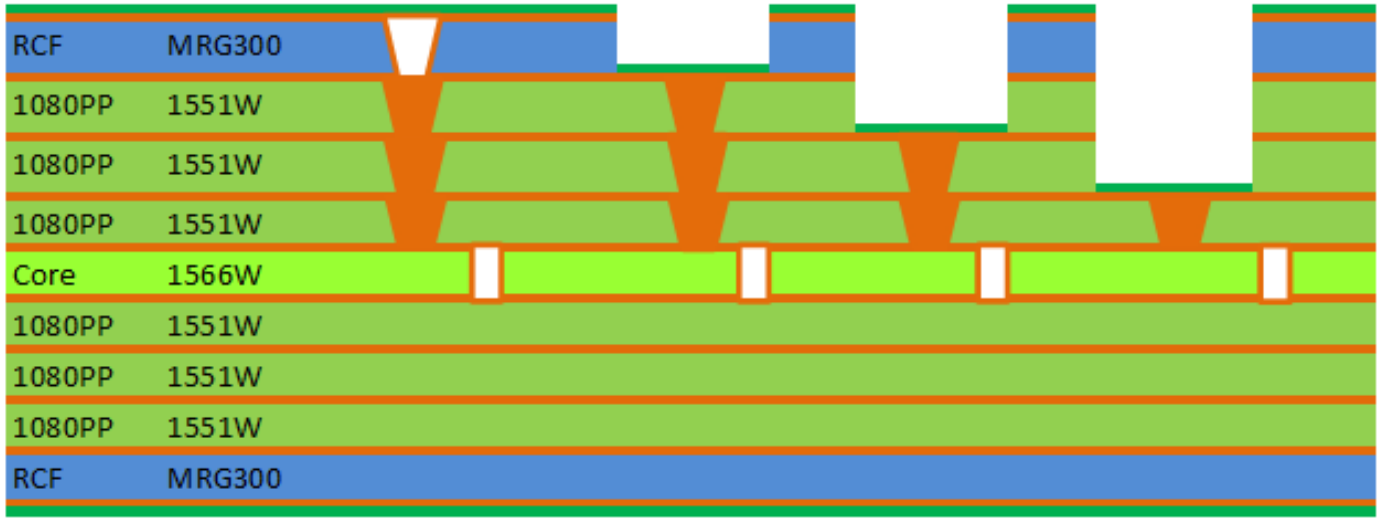
PCB based on JEDEC JESD22-B111



- 10layer PCB with stacked vias
- POS 1: no layer removed
- POS 2: 1 layer removed
- POS 3: 2 layers removed
- POS 4: 3 layers removed

Production of the test vehicle

Solder mask

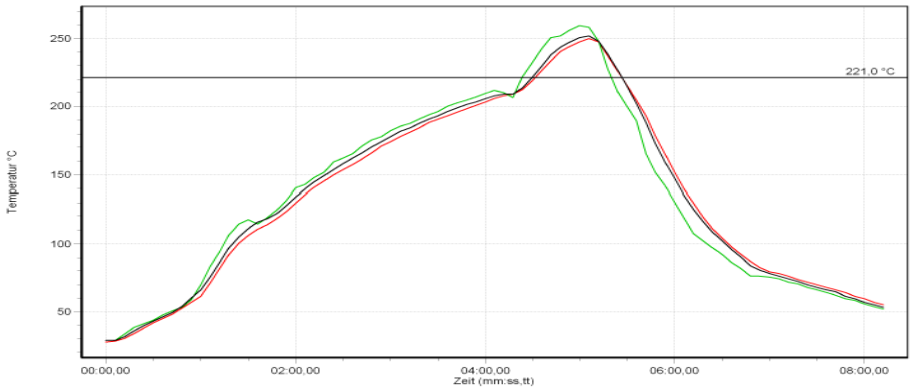


- Solder footprint
- Surface finish (OSP)
- Solder mask
- Very accurate depth tolerance
- High flexibility in depth and shape

Assembly line

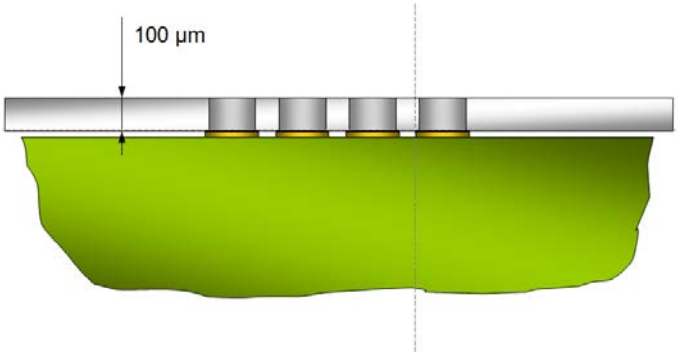
Reference image

- Printer: DEK265
- Solder paste: Lead free type 3
- Assembly machine: Siemens D3
- Reflow oven: Rehm

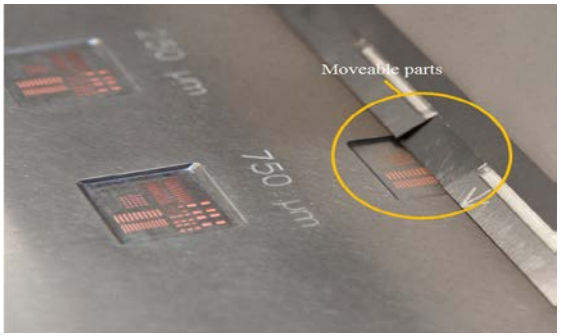


Printing system

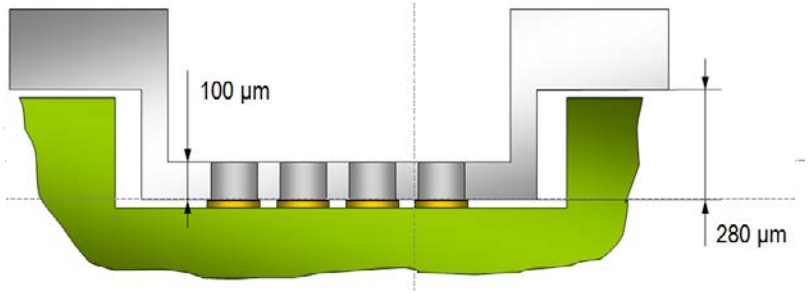
POS 1: Stencil



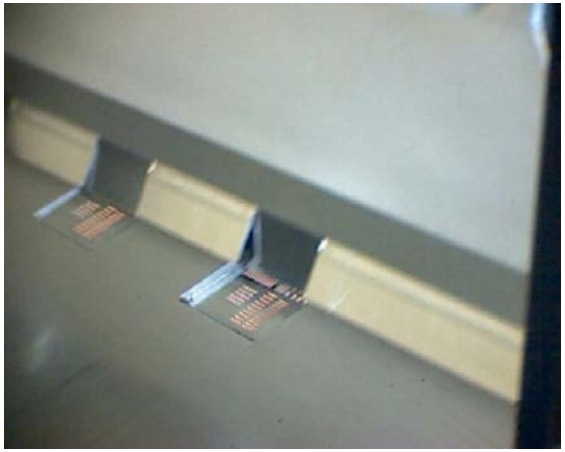
Squeegee



POS 2,3,4: Step stencil

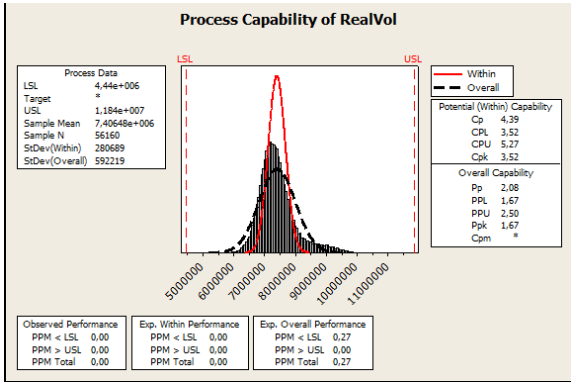


Printing process

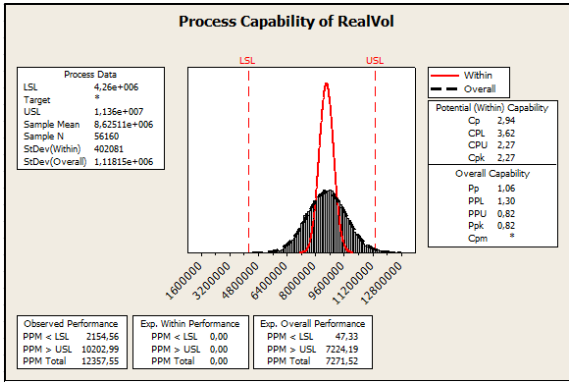


Solder paste printing capability

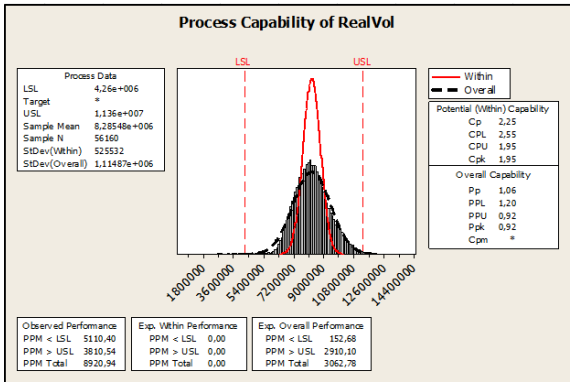
POS 1



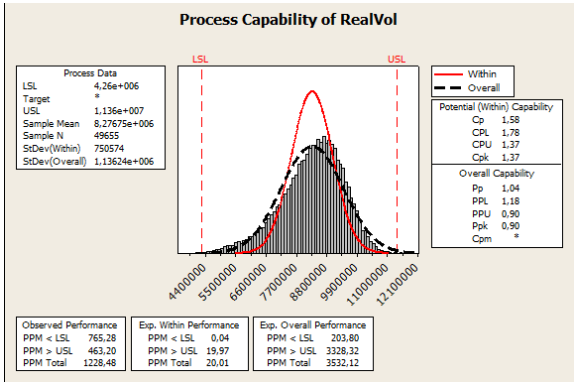
POS 2



POS 3

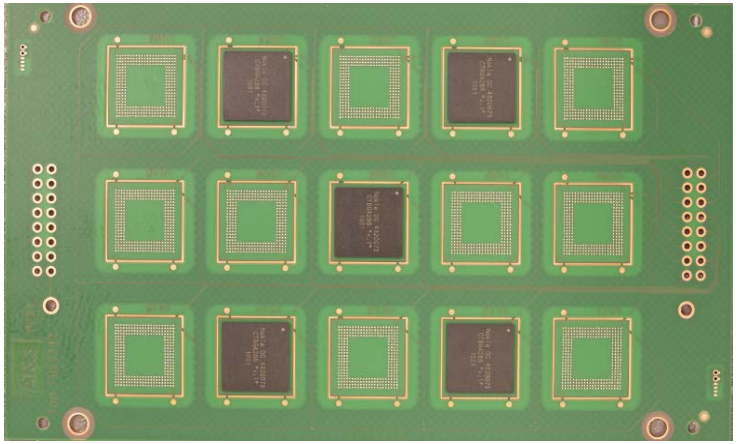


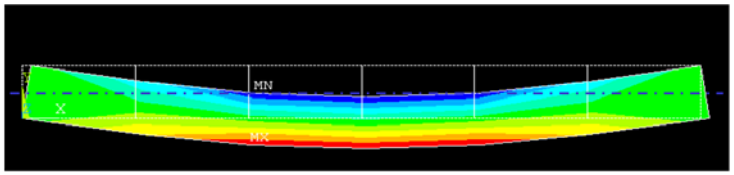
POS 4



Drop test

JEDEC	"Mobile Customer"
Acceleration:	• 1500g ±30%
Pulse Duration:	• 0,5ms ± 30% (peak width at 10% of maximum pulse height)
Cpk:	> 1,3
Measurement Current:	1,0 mA
Voltage:	1,0 V
Resistance:	1000 Ohm
Tested Structures:	Via chains (assembled cards)
Pass/ Fail – Criteria:	• Minimum acceptance criterion for components is 10 drops of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.

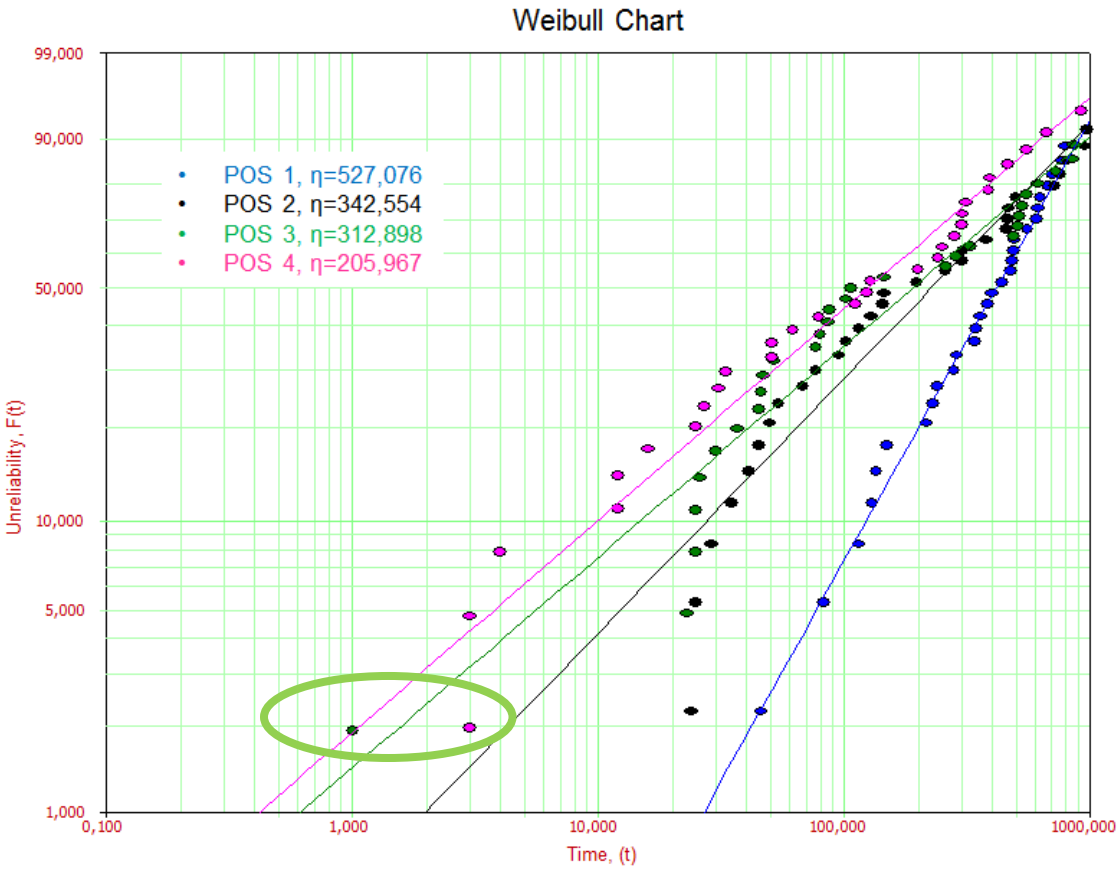




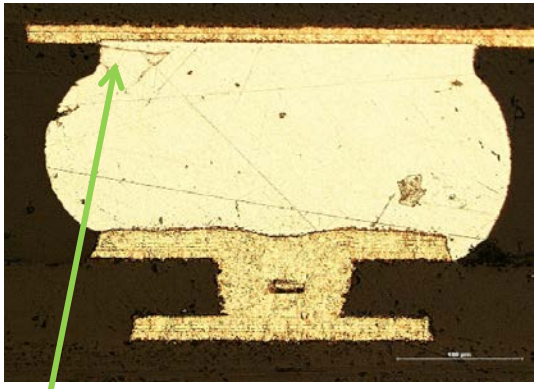
Neutral Axis
MN – Minimum tension
MX – Maximum tension

- Mechanical loading: 1500g±30% (JEDEC JESD22-B111)
- Online test method: Monitoring device soldered to terminals
- 36 cards tested: 9 cards per position
- 5 center components per card

Drop test results



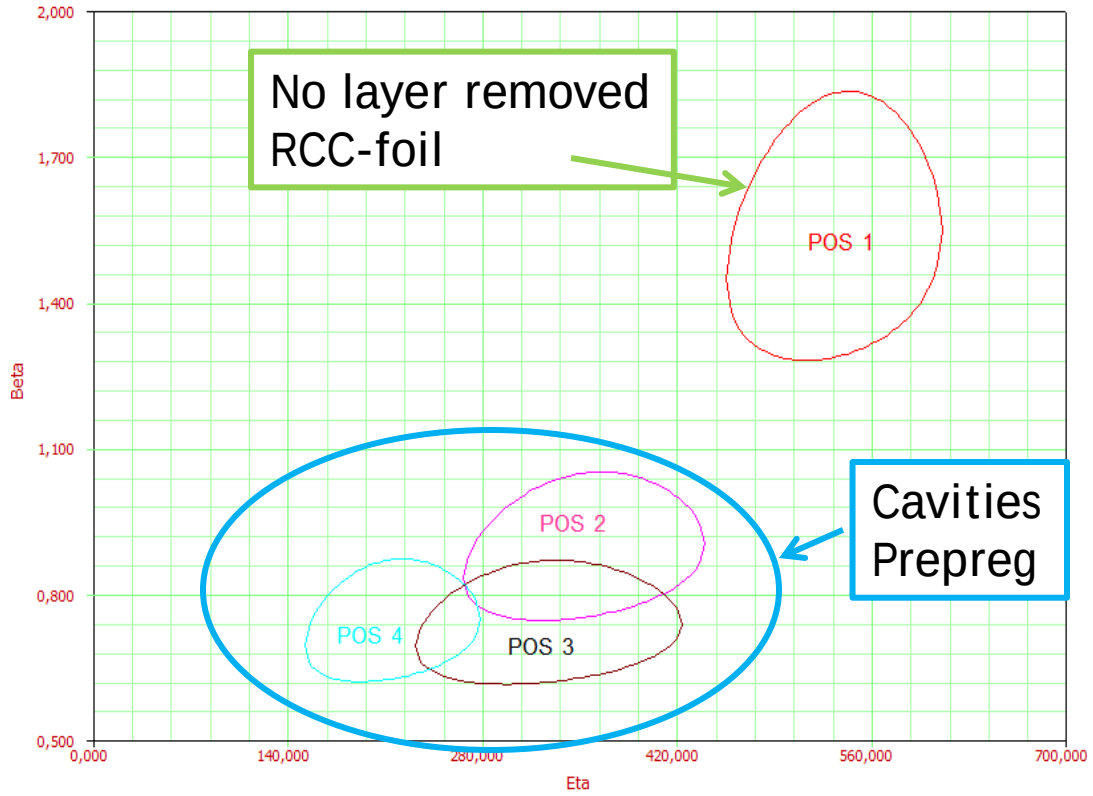
Failure at 1st drop



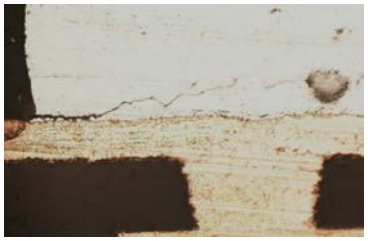
Crack in solder near component

Drop test results

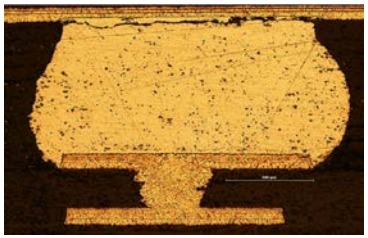
Contour plot (50% probability at next drop)



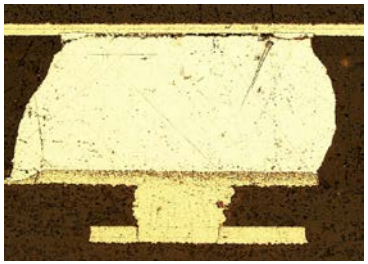
POS 1
239 drops



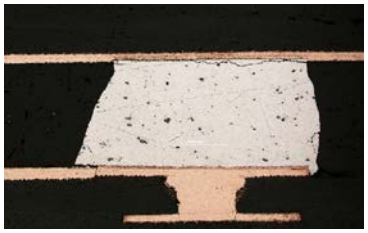
POS 2
720 drops



POS 3
555 drops

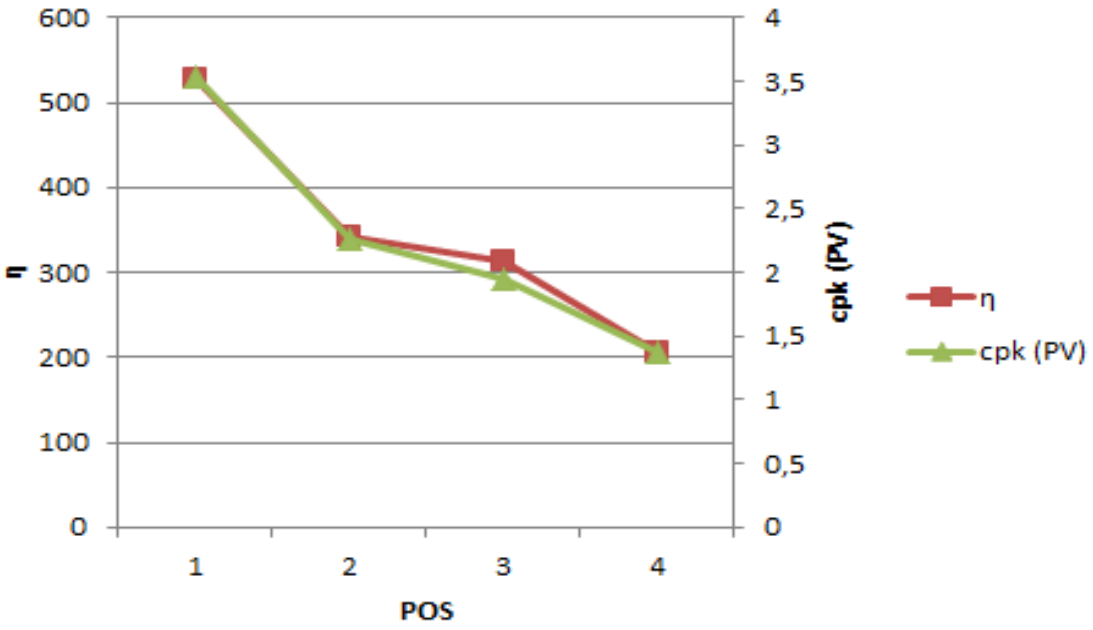


POS 4
666 drops



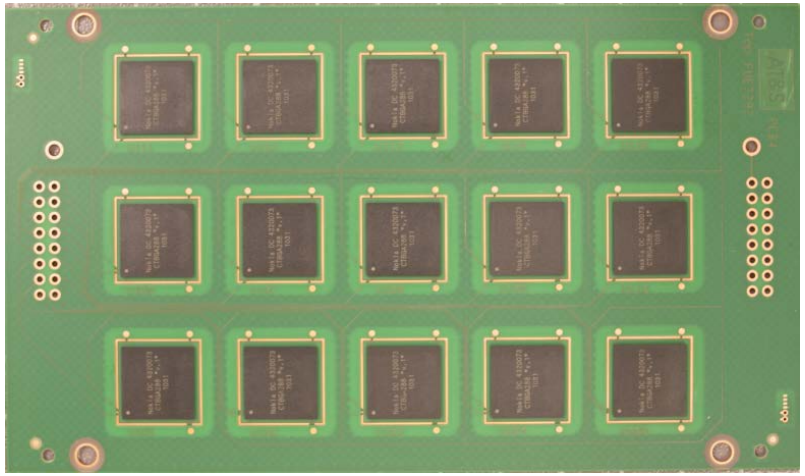
Drop test evaluation

Correlation between Drop test and paste printing



Temperature Cycle Test TCT

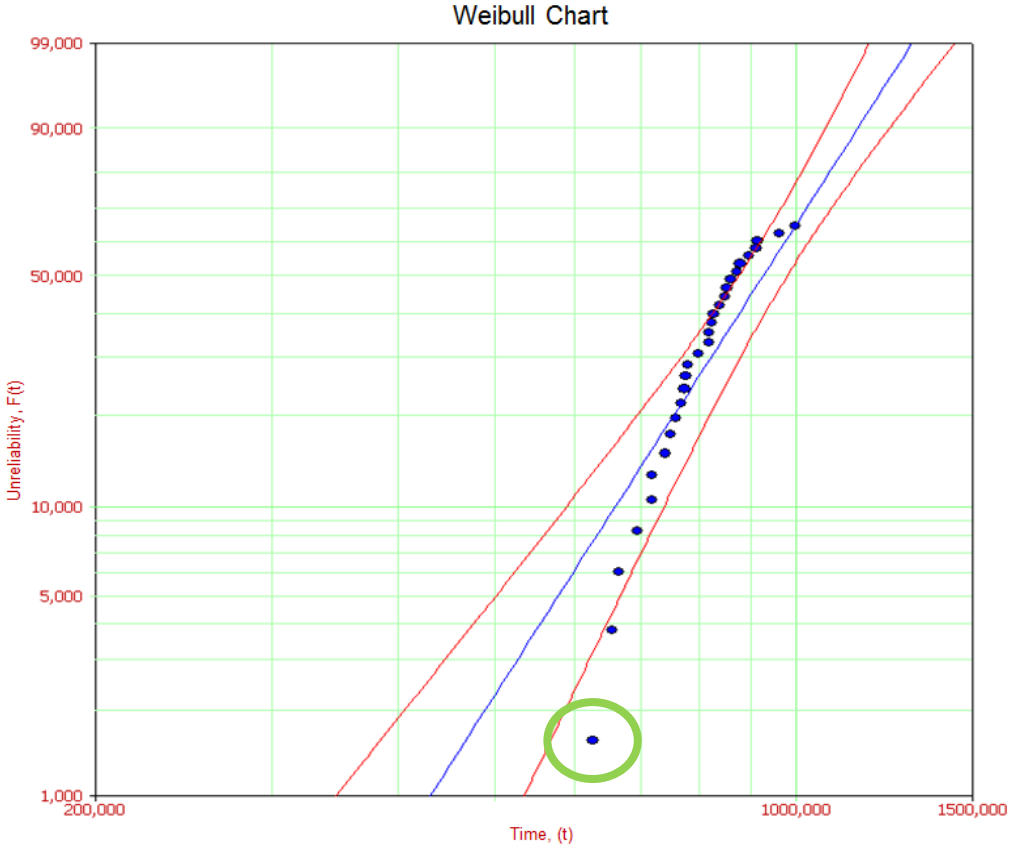
FUE7292	TCT parameter
Chamber:	one chamber design
Chamber parameter :	Step per cycle / Chamber / Sample Temperature / Min. Soak Time / Cycle count[3] 1 / Cold / -40 +0/-10°C / 5min / 1000 2 / Heat-up / - / - 3 / Hot / +125 +15/-0°C / 5min 4 / Cool-down / - / - The heating and cooling rate has to be set in such a way that in total 2 cycles per hour are achieved.
Measurement system:	Event Detection 4 - Point Measurement
Resistance limit:	1000 Ohm
Tested structures:	Via chains (assembled cards)
Pass/ Fail – criteria:	Assembled cards: Minimum acceptance criterion for components is 500 cycles of lower confidence bound at 5% risk level with 90% confidence interval, or better reliability than this.



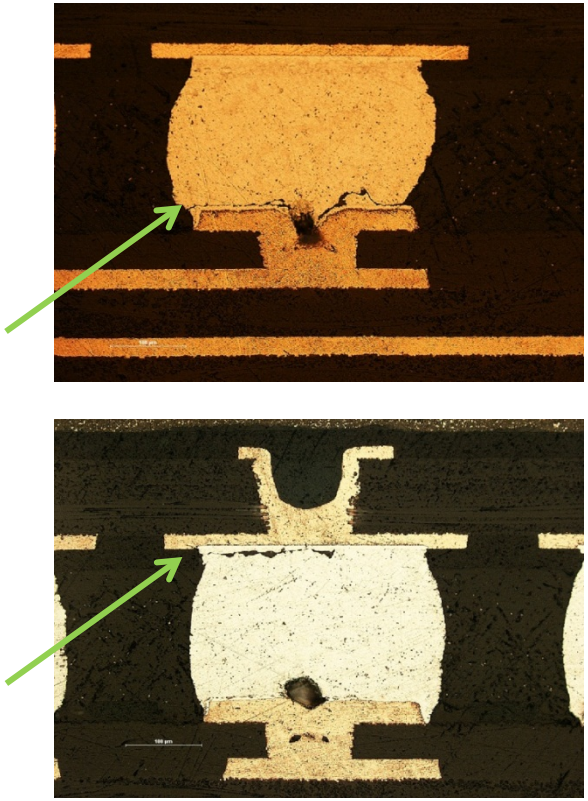
- Thermal loading: -40° C ↔ +125° C (JEDEC JESD22-A104C)
- Online test method: Monitoring device soldered to terminals
- 16 cards tested: 4 cards per position
- 15 components per card

TCT results

POS 2, POS 3 and POS 4 passed 1000cycles
POS 1: failure after 627cycles



Failure modes (627cycles)



Cracks in solder

Summary

The manufacturing and materials (stencil, squeegee, PCB, solder paste) posed no obstacle.

Cavity boards showed similar drop test performance and were somewhat worse than outer layer construct (RCC-foil vs. Prepreg).

The reduction in solder paste volume cpk is graphically congruent to the reduction in drop test η.

TCT performance for the components assembled in the cavities provided no indication of variable performance to standard outer layer constructs.

Outlook

Based on analysis results, the following factors could be considered as process and product optimization:

- Increasing solder paste volume in deeper cavities may positively affect reliability.
- Underfill could be expected to further enhanced reliability performance.
- Use of RCC-foil at cavity layer may also positively affect drop test performance.