Warpage Issues and Assembly Challenges Using Coreless Package Substrate

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Abstract

Coreless technology in package substrate has been developed to satisfy the increasing demand of lighter, smaller and superior electrical performance regarding as the future trend in electronic application. However, there are major challenges of reducing coreless substrate warpage in terms of both substrate manufacturing and assembly process. Substrate manufactures typically provide substrate warpage within satisfying customers specification which does not allow much margin left in assembly considering the number of reflows and curing profiles which the package undergoes during assembly. However, it is very difficult to provide satisfying this level of warpage because coreless substrate is one-third as thin as conventional one and does not use stiff core material. The key element for success in coreless technology is to solve the warpage issue at manufacturing site because the decrease of bare substrate warpage is important to improve the assembly yield. To figure out these problems, design optimization, mechanical/thermal treatment and low CTE material are suggested in this study. Final part discusses assembly result and issue for future work.

Keywords
Coreless, Thin core, Warpage, Package and Coefficient of thermal expansion (CTE)

1. INTRODUCTION

As the functionality and performance of network systems, high-end servers, and mobile communication devices improves, the demand for high pin counts, data transmission speed and signal integrity is increasing and pushing microvia build-up technologies to the limits. One of solutions for high speed applications is to reduce the core layer thickness from 800 um down to 400 um or even to 200 um, or to remove the core layer for better electrical performance, which is the so called coreless substrate.

Through-holes in the rigid core layer of conventional packaging substrate are formed by a mechanical drilling. The core layer is much thicker than any one build up layer. Through-hole diameter is more than 100um, with consequent problem of reflection and/or delay in high frequency signal transmission. Because coreless substrate is made of insulating layers without a rigid core layer and laser drilling instead of mechanical drilling thereby can be treated, the signal routing capability is improved by reducing core via pitch and associated capture pad diameter [1-3]. In addition, high density thin core substrates offer improved design flexibility for routing of high speed signals with specific voltage referencing and shielding requirements [4-5]. They also provide better electrical performance by lowering inductance. The self impedance depending on core thickness is simulated as shown in Figure 1. As decreasing overall thickness of substrate, the self impedance is decreased. In case of coreless substrate, it shows lower impedance at entire frequency range and better power delivery performance than any other products due to the shorter electrical path and the higher pin counts. The simulation data are well corresponding to previous results [6]. As shown in Figure 2, coreless substrate is one-third as thin as conventional one and consists of only build-up layers and Cu plates without stiff core. Therefore, it is significant for warpage issue at both manufacturing and assembly process. Previous warpage level without using any warpage reduction technologies was 60~70% higher than customers specification based on 20~30 mm^2 size and 0.3mm thickness coreless substrate.

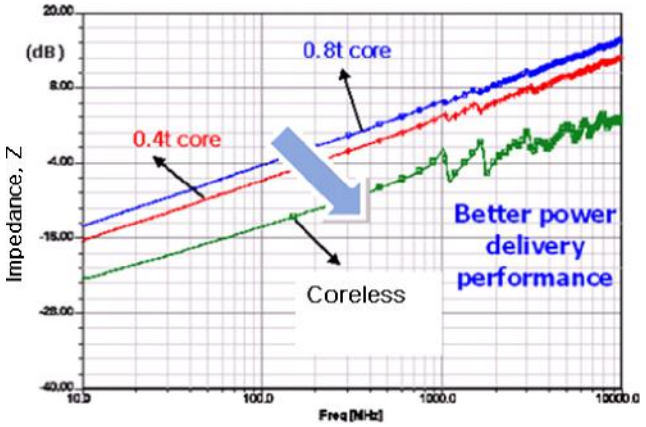
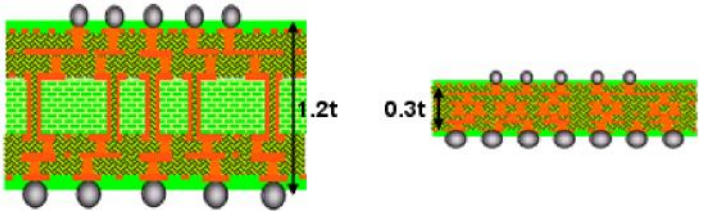


Fig. 1. Predicted self impedance depending on core thickness.



(a) Conventional package substrate (b) Coreless package substrate

Fig. 2. Comparison of conventional and coreless package substrate.

In this paper, characteristic properties between coreless and conventional package substrate are compared. In addition, proper selection of low CTE material, design optimization and minimizing mechanical/ thermal stress is discussed to reduce warpage in manufacturing process.

2. EXPERIMENTS

2.1. Material

CTE mismatch between the die and substrate leads to relative displacement during reflow, and under these conditions, eventually result the solder bump failures. Due to these severe problems, in manufacturing side of coreless package substrates, selecting proper build-up materials having low CTE and high stiffness are important to get low warpage and better reliability. Two types of build-up material are investigated as summarized in Table 1. Type B is used to show the effect of low CTE build-up material which consists of woven glass in the matrix of the resin and filler.

TABLE 1. LOW CTE BUILD-UP MATERIAL USED IN THIS STUDY.

	Code	Type A	Type B
Glass cloth	-	x	o
Thickness	um	37.5	50
CTE α1	ppm/oC	46	19
		120	7

2.2. Manufacturing process

Coreless process uses carriers such as metal or polymer type. The process consists of carrier and separation technologies for easy sample handling and fabrication as shown in Figure 3. After finishing build-up process, the carrier needs to be removed in order to leave only coreless substrate, and finally precede back-end process.

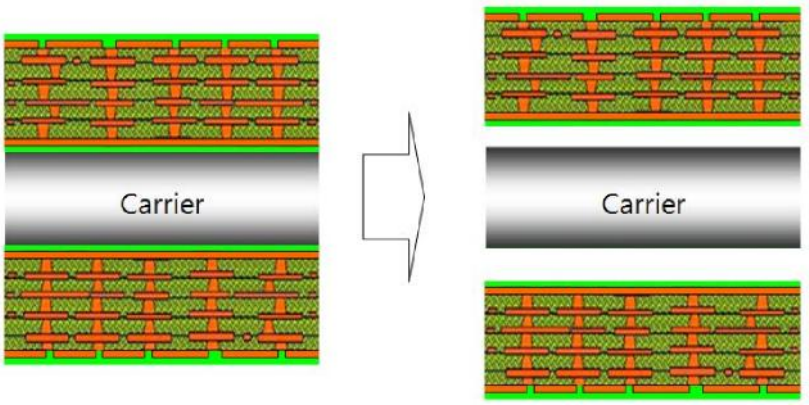


Fig. 3. Coreless substrate manufacturing process (a) build-up six times on carrier (b) after separation from carrier.

2.3. Shadow moiré

Warpage during reflow process was measured by means of shadow moiré. Figure 4 shows the schematic description of shadow moiré. This method is ideal for obtaining full-field contour maps at the temperature range of reflow process (RT to below 300^{o}C). The advantage of this equipment is that we can measure the level of warpage at any temperature region in reflow process. A master grating (100 line/mm) is placed in front of the Printed Circuit Board (PCB) specimen and illuminated by a collimated light beam at an angle to the grating. The master grating and its shadow on the surface of the specimen then produces a fringe pattern viewed normally to the master grating.

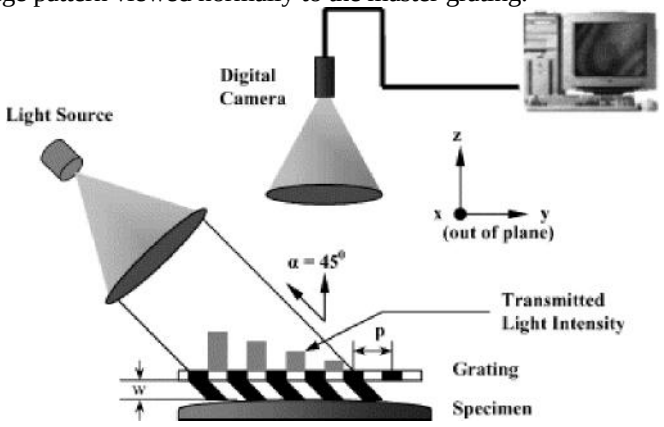


Fig. 4. Schematic representation of shadow moiré equipment.

2.4. Assembly process

2.4.1. Substrate/Die

The substrate size is the range of 20x20 ~ 30x30mm^2 with 6 layers. The minimum bump pitch is 180um and the total number of bumps is the range of 1000~2000. The solder composition is SnCu0.5Pb3, so called SAC305. The total substrate thickness is 0.3mmt. Substrate is baked to ensure that moisture is removed before flip chip attach process. The die size is 5x7mm^2. The total die thickness is 800um and not back grinded.

2.4.2. Chip attachment

Singulated test chip is then assembled using a flux and with a lead free reflow profile of 250^{o}C peak temperature.

2.4.3. Underfill process

Prior to underfill process the parts are baked at 150^{o}C for 2 hours to ensure that moisture is driven out before underfill dispense. The curing condition of underfill material is at 150^{o}C for 2 hours.

3. RESULTS & DISCUSSION

3.1. Warpage study in coreless substrate

It is difficult to predict the warpage in PCB level because PCB consists of the several different composites such as Cu,

polymeric resin, fillers and glass fabric. Especially for polymeric resin, they show viscoelastic behavior, as in the case of a polymer-based composite, thereby the complex interactions between the viscoelastic component (matrix) and the elastic part (reinforcement) will induce a residual stress state affecting both the material integrity and the final component shape [7-9]. These residual stresses are also generated as curing the build-up material due to its shrinkage. In addition, it is generally known that considerable amount of thermal stresses would generate upon cooling from the processing temperature due to the large difference in CTEs (Coefficient of thermal expansion) of build-up material and Cu plate, and some part of them reserve as the residual stress in the composite as cooled to room temperature [10-11]. This can be derived from periodic work by heating and wet process in PCB fabrication as shown in Figure 5.

Fig. 5. Warpage derived from periodic work by heating and wet process in PCB fabrication.

When bi-metal structure is applied into coreless substrate, it is better to understand warpage mechanism regarding to CTEs. Timoshenko et al. [12] have been studied for understanding warpage behavior when bi-material strip structure is used during various heating process.

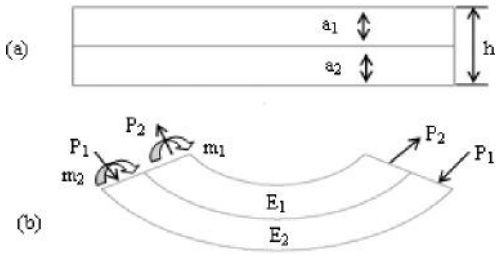


Fig. 6 (a) Bi-material strip structure and (b) after thermal loading.

As shown in Figure 6 (a), let α_1 and α_2 denote the CTE of the two materials (1) and (2) where the E_1 and E_2 are their modulus of elasticity, a_1 and a_2 their thicknesses and the h is the thickness of the strip. The width of the strip is taken as equal to unity. If α_2 is bigger than α_1, the deflection will be convex down by thermal loading as shown in Figure 6 (b). All the forces acting over the section of material (1) on the concave side can be represented by an axial tensile force P_1 and bending moment M_1. For material (2) on the convex side all forces acting on the cross-section can be represented by an axial compressive force P_2 and bending moment M_1. Due to the fact that there are not external forces acting on the strip, all forces acting over any cross-section of the strip must be in equilibrium, therefore,

(1)

(2)

Letting ρ= radius of curvature of strip,
E_1I_1 = the flexural rigidity of the material (1)
E_2I_2 = the flexural rigidity of the material (2), then,

Substituting in (2),

(3)

On the bearing surface of both materials the unit elongation occurring in the longitudinal fibers of materials (1) and (2) must be equal, therefore,

From above equation using (1) and (3), we can draw the following general equation for the curvature of a bi-material strip structure,

The curvature is proportional to the difference in elongation of the two materials and inversely proportional to the thickness of the strip. It is seen that the magnitude of the ratio $E_1/E_2 = n$ does not produce any substantial effect on the curvature of the strip even the n are 1, 1/2, or 2. Many previous studies showed that the difference of curvature depending on various n is quite small which is within only 3 percent. When the curvature 1/ρ is obtained, the warpage ö of the strip can be easily evaluated.

$$\frac{1}{\rho} = \frac{6(\alpha_2 - \alpha_1)(T_2 - T_1)(1+m)^2}{h\left[3(1+m)^2 + (1+mn)\left(m^2 + \frac{1}{mn}\right)\right]} \quad \text{where } m = \frac{h_1}{h_2}, \; n = \frac{E_1}{E_2}$$

As shown in Figure 7(a), it is simple to understand warpage behavior during heating or cooling when multi-layer structure is modified to bi-layer structure. Coreless substrate is easily varied from smile to cry shape and vice versa on heating or cooling due to the CTE mismatch between upper and down layer described in Figure 7(b).

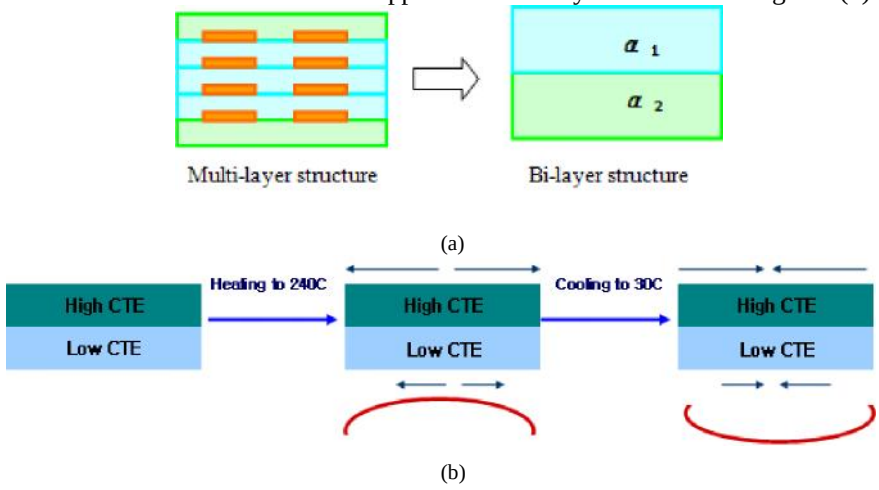
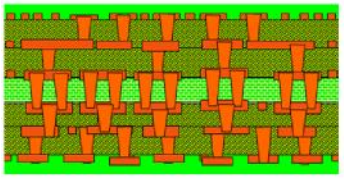


Fig. 7. (a) Bi-layer model in coreless substrate (b) estimation of warpage behavior during heating or cooling.

3.2. Characteristic properties of coreless substrate

Coreless package substrate is asymmetric structure due to its different Cu density at each layer as shown in Figure 8. This different Cu density is caused by different electrical function of each layer. Front layers (1L~3L) which are connected to die have microvia and fine pattern/pitch, however, back layers (4L~6L) which are connected to motherboard are used for ground function. Therefore, generally Cu potion of back layers is bigger than that of front layers. Moreover, coreless substrate is thin and does not contain rigid core material with glass fabrics, therefore, it is easy to bend at reflow condition due the CTE mismatch between upper and lower layer which is already mentioned in Figure 7.



Layer	Cu portion	%
1L	351.6 mm2	66.2 %
2L	378.3 mm2	70.3 %
3L	404.3 mm2	76.4 %
4L	429.7 mm2	81.2 %
5L	428.5 mm2	81.0 %
6L	407.8 mm2	77.1 %

Fig. 8. Cu density & the shape of Cu pattern at each layer.

Warpage variance is the difference between warpage at RT and warpage at 240°C. As shown in Figure 9, warpage behavior between coreless and thin core FCB substrate are different. The coreless substrate performs significant warpage variation of 25~50% higher than thin core substrate at the peak temperature in the reflow process. However, warpage of thin core FCB substrate shows relatively flat at entire temperature region. In case of coreless FCB substrate, it is expected that chip attachment is more deteriorated because warpage is varied depending on heating condition. Therefore, it is

necessary to develop coreless substrate which has less warpage variance at reflow condition.

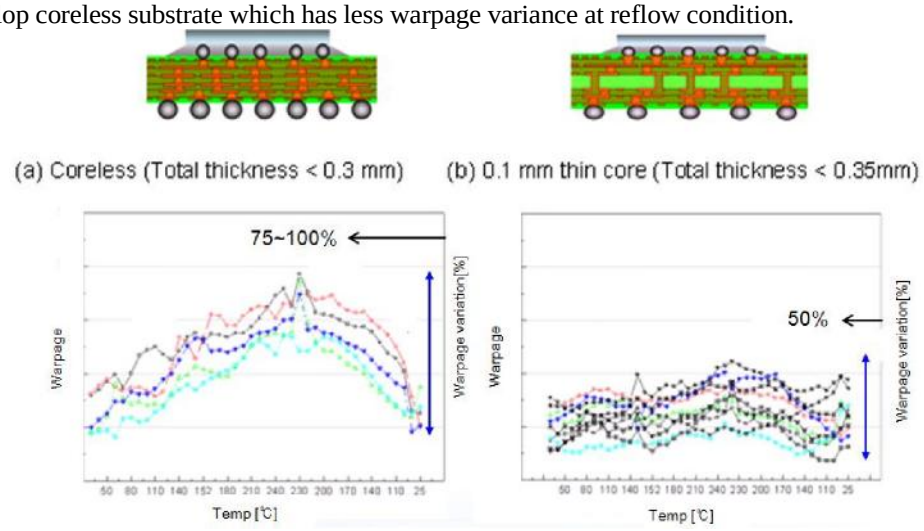


Fig. 9. Warpage behavior for (a) coreless package substrate (b) thin core package substrate with Type A insulating layer.

3.3. Warpage reduction technologies

In coreless package, many challenges, such as die bonding, non-wetting can be generated by bare substrate warpage and warpage variation during reflow. To figure out these problems, it is important to reduce bare substrate warpage within customer's specification. It is also important to reduce warpage variation during reflow which is characteristic property in coreless package substrate. Warpage reduction technologies in coreless substrates used in this study can be divided into three categories such as design optimization, thermal & mechanical stress and low CTE materials as shown in Figure 10.

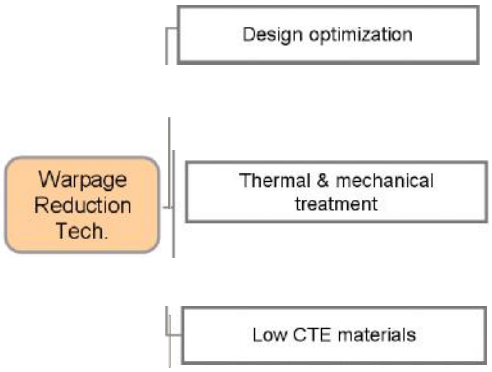


Fig. 10. Brief instruction of warpage reduction technologies used in this study.

3.3.1 Design optimization

Residual stress which is taking an effect on warpage is derived from various sources such as CTE mismatch between build-up material and Cu plate, curing shrinkage of build-up material and mechanical/thermal stress in manufacturing process. However, for design optimization, it is more important to consider CTEs of various materials. As mentioned before, design optimization is needed to reduce warpage variation at various heating condition. The problems deriving from CTE mismatch have become more issue in coreless substrate due to its thin and no stiff core in its structure. Therefore, it is important to fabricate CTE balanced coreless structure to minimize residual stress, thereby reduce warpage and warpage variation.

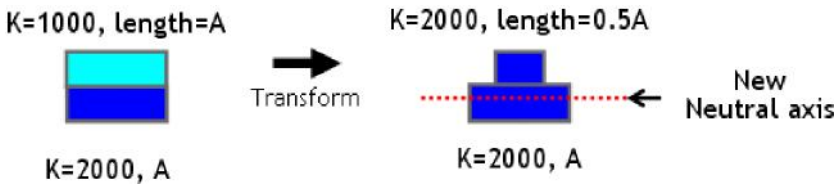
Neutral axis

Assuming that the beam with rectangular shape consists of same materials, the neutral axis will be situated at the midsection of the beam. The neutral axis is defined as the point in a beam where there is neither tension nor compression forces. So if the beam is loaded uniformly from above, any point above the neutral axis will be in compression, whereas any point below it will be in tension as described in Figure 11(a). However, if the beam consists of two different materials such as wood (K=1000) and metal (K=2000), the neutral axis will be changed [13]. In this paper, we suggest setting new neutral axis considering its stiffness. When two different materials are applied to the beam as shown in Figure 11(b),

By using the concept of neutral axis concept and MROM, we represent the process of design optimization tool as shown in Figure 13. For proper design analysis, volume and thickness of Cu /insulation layer at each layer is calculated

the new neutral axis is somewhat below geometrical center line. In case of coreless package substrate, it is important to set new neutral axis be equal to the geometrical centerline on bi-metal structure.

(a) The beam with neutral axis



(b) New neutral axis considering its stiffness

Fig. 11. (a) I-beam with neutral axis (b) New neutral axis considering its stiffness, K=stiffness.

Modified rule of mixture

Composite theory is needed to calculate the CTE of upper and lower layer in coreless package substrate. Single rule of mixtures (SROM) are generally used to composite system. The simple approach of SROM is that the properties of the composites are equal to the volume fraction contributions of the components as shown in equation (4).

(4)

Letting f = fiber, m=matrix and =CTE, V=volume,

However, most composites depend not only on the contributions of the components (composition factors) but also on the "quality of the interfaces" involved with energy transfer between the phases (bonding factors), the arrangement of the phases with respect to each other (arrangement factors such as particle sizes and distributions), and defects (defect factors such as pores and cracks). All of these can be incorporated into the single rule of mixture (SROM) to create modified rule of mixtures (MROM). The MROM which is used in this paper is representing in equation (5) [14-15].

(5)

Finite element method (ANSYS) is used to verify two equations. The result of finite element method (ANSYS) is better fitted into MROM than SROM as shown in Figure 12. Therefore, MROM is used to find the CTE balanced structure in this study.

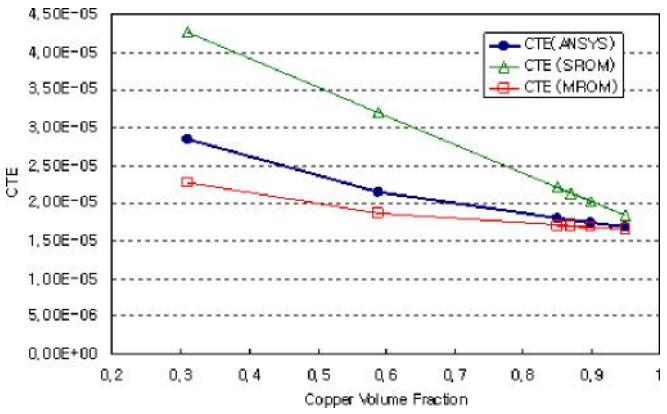


Fig. 12. The comparison of Single Rule of Mixture (SROM) and Modified Rule of Mixture (MROM).

considering CTE. The volume of SR opening and micro via hole is also considered to ensure accurate calculation. For CTE balance, we set geometrical center line and calculate average CTE of upper and lower layer respectively by using MROM. Finally, we find the optimal SR thickness to approach which geometrical center line is equal to new neutral axis.

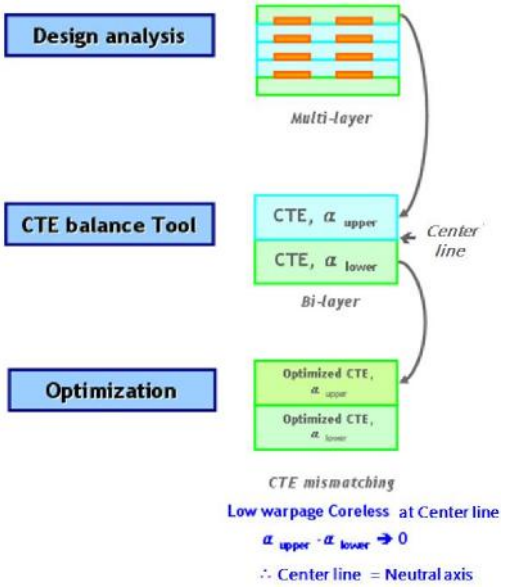


Fig. 13. The concept of coreless substrate design evaluation tool (D.E.T.).

To evaluate the effect of design optimization, three different experimental conditions depending on front SR thickness were used as shown in Figure 14. As mention earlier, design optimization is needed to reduce warpage variation at various heating condition. Moreover, it is observed that bare substrate warpage is also decreased as CTE balance is reached with SR thickness control. Thermally induced warpage is an increasingly important issue in managing the manufacturing yield and reliability of electronic devices. This can be derived from periodic work by heating and wet process in PWBs fabrication. It is generally known that considerable amount of thermal stresses would generate upon cooling from the processing temperature due to the large difference in CTEs of build-up material and Cu plate, and some part of them reserve as the residual stress in the composite as cooled to room temperature. Therefore, warpage induced by CTE mismatch would be occurred during manufacturing process. The CTE balance between upper and lower layers is important and in case of FSR/BSR = 20um/50um (DOE 3), it shows balanced CTE value of 21.51 ppm and 21.74ppm respectively at the base of center line and incoming warpage value was the lowest one among 3 different DOEs as shown in Figure 15.

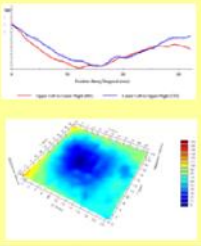
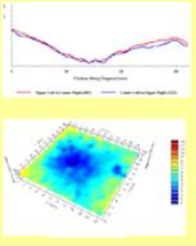
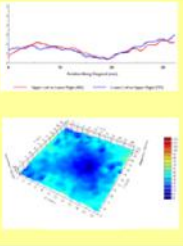
TEST	DOE1	DOE2	DOE3
FSR [um]	30	25	20
BSR [um]	50	50	50
Warpage (%)	100%	76%	54%
Warpage shape			

Fig. 14. Incoming warpage depending on FSR/BSR thickness ratio [front SR (FSR), back SR (BSR)].

By using the concept of neutral axis concept and MROM, we represent the process of design optimization tool as shown in Figure 13. For proper design analysis, volume and thickness of Cu /insulation layer at each layer is calculated

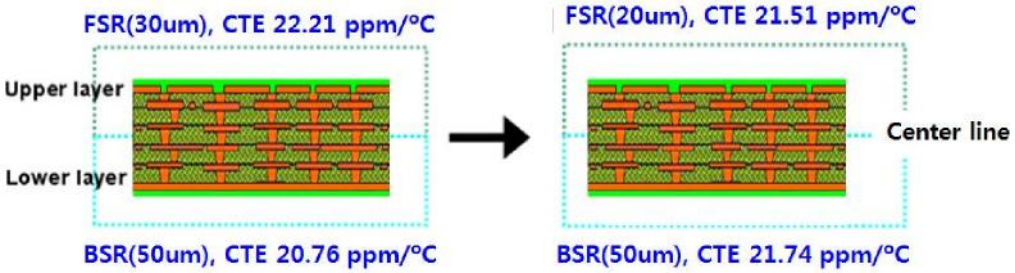


Fig. 15. CTE calculation of upper and lower layer by D.E.T. (design evaluation tool).

For DOE 3 which is showing CTE balanced design, warpage variation is also decreased to 67% compare to DOE1 as shown in Figure 16. From D.E.T. suggested in this study, warpage variation is also minimized if exact CTE balance is reached.

Temperature	25°C	180°C	240°C	160°C	25°C	ΔW
DOE1						100%
DOE2						95%
DOE3						67%

Fig. 16. Warpage variation depending on FSR/BSR thickness ratio.

3.3.2 Thermal/Mechanical treatment

Warpage is very serious problem during reflow process due to the CTE mismatch arisen by different material property and design. For thermal/mechanical treatment, new jig was invented and applied to reflowing process as shown in Figure 18. In this study, it was suggested to use cover jig made by aluminum. For a proper flip-chip bump formation, the bump area in cover jig was open as shown in Figure 17. The reason to use cover jig in this study is that substrate panel shows stress free status above 220°C with the lowest warpage, 60~70% warpage reduction compare to initial status as shown in Figure 18. The role of cover jig applied in this study is sustaining the minimum warpage at stress free temperature when constant loading is applied to panel during cooling. Without using cover jig, warpage was increased over twice after reflowing. However, by applying new cover jig, more than 30% of warpage was reduced when it is compared with conventional jig.

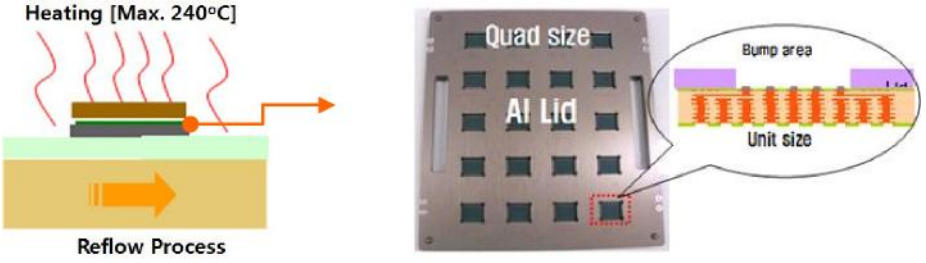


Fig. 17. Introduction of reflow process and the shape of reflow jig.

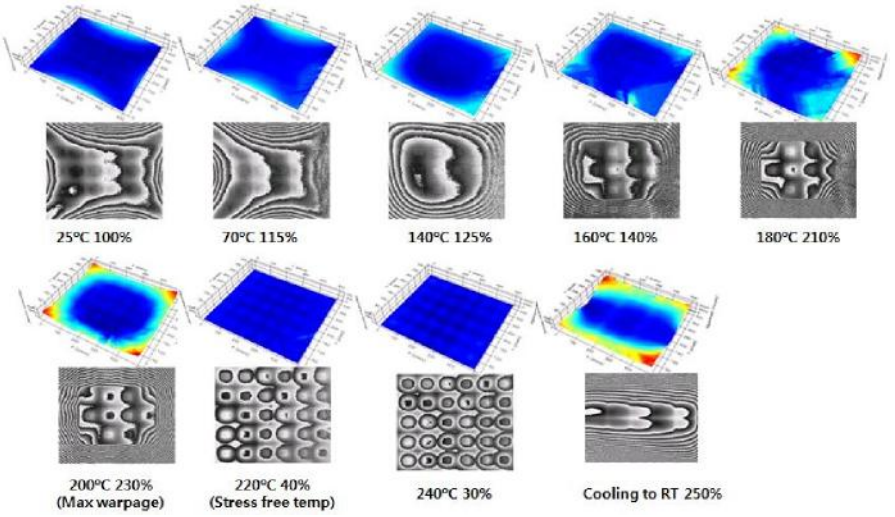
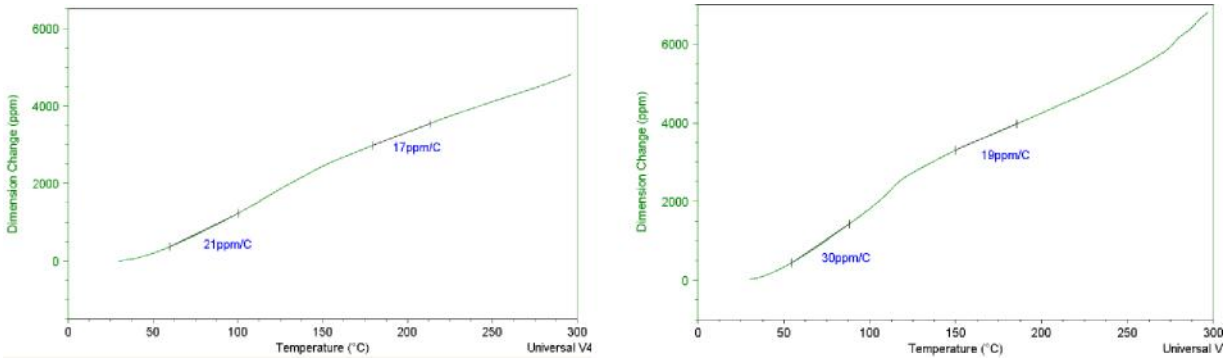


Fig. 18. Warpage shape during reflow process without cover jig.

3.3.3 Low CTE build-up material

CTE mismatch among the components of electronic package is un-avoidable since electronic package involves different set of materials with dissimilar CTE values. The major problems associated with CTE mismatch include thermal stresses and warpage. In this study, CTE measurement was done using thermal mechanical analyzer (TMA) in the temperature range of 30~300 °C.



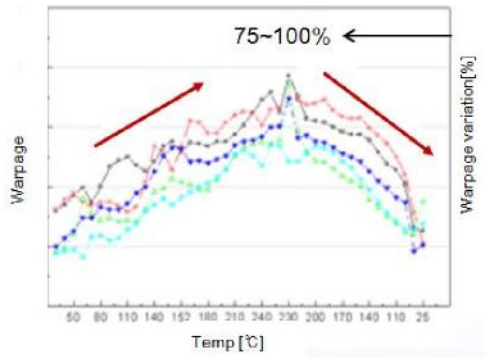
(a) Thin core package substrate (b) Coreless package substrate

Fig. 19. The CTE of thin core package substrate and coreless package substrate (x axis).

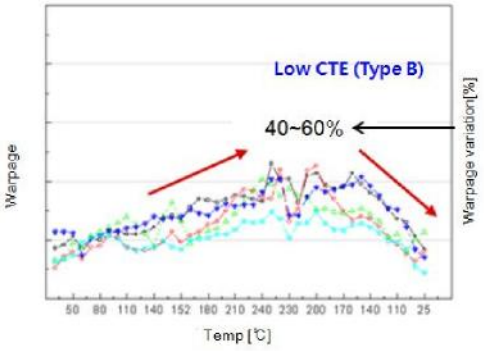
The specimen was scanned twice. The first scan was aimed to eliminate the moisture and erase the thermal history in composites. Figure 20 shows a profile of TMA scan with x-axis for thin core package substrate and coreless package substrate. The CTE of coreless substrate is around 30ppm/^{o}C below Tg. As mentioned earlier, because coreless substrate do not contain stiff core structure with glass fabric, overall CTE of coreless substrate is much bigger than that of thin core substrate. From this result, we can estimate that the weak solder bump interconnection between substrate and chip during package would be more generated due to the more gap of CTE mismatch between substrate and chip.

To observe the effect of Low CTE build-up material, type B, which contains glass cloth in composite, was used in this study (Table 1). Figure 20 shows the effect of type B for both coreless and thin core substrate during reflow process. Initial warpage for both coreless and thin core specimen was decreased about 20% when type B is applied instead of type A due to the low CTE and high modulus properties of type B. Warpage reduction by using low CTE material can be derived by minimizing factors to influence of warpage during manufacturing process such as handling, carrying, and thermal cycle etc. Moreover, warpage variation during reflow was also decreased about 25% for thin core substrate and 35~40% for coreless substrate.

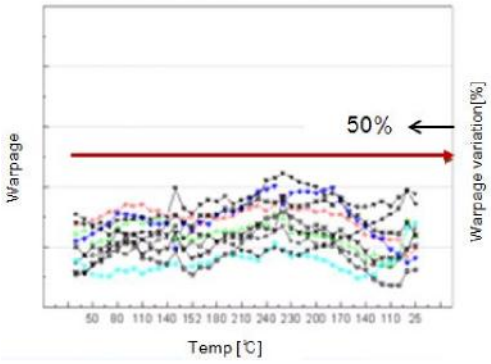
On the bearing surface of both materials the unit elongation occurring in the longitudinal fibers of materials (1) and (2) must be equal, therefore,



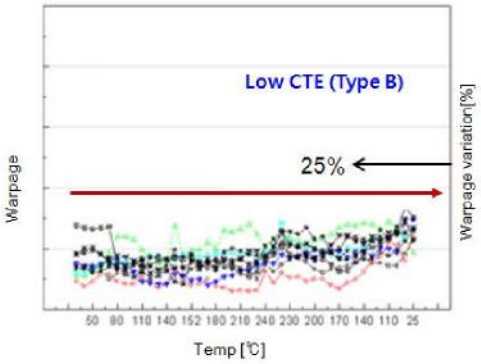
(a) Coreless substrate with type A



(b) Coreless substrate with type B



(c) Thin core substrate with type A



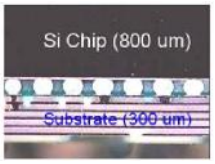
(d) Thin core substrate with type B

Fig. 20. Warpage behavior for Low CTE material (Type A= 46ppm, Type B=19ppm) in coreless ((a),(b)) and thin core ((c), (d)).

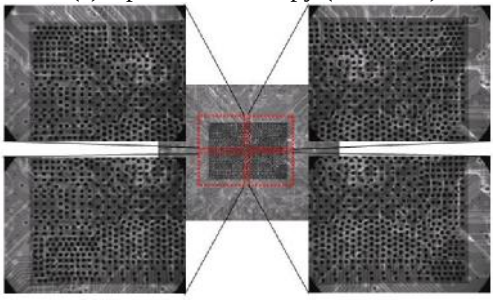
3.4. Assembly result & discussion

Coreless substrates in flip chip applications have several advantages over standard build-up substrates with 400 or 800um core thickness such as lower parasitic resistance and inductance, and high density interconnections for fine pitch I/O applications. Even if bare substrate warpage is satisfied with customers need, coreless substrates might have package warpage issues during assembly process. Assembly and reliability of coreless substrates are quite challenging because they are one-third as thin as conventional one. This chapter will briefly discuss assembly results and discussion for 20~30 body coreless package substrate.

In this study, first level package of coreless package was evaluated. Before test, we inspected and ensured there were no micro cracks and bump missing for 50units. For proper handling the substrates, fixtures during chip attach, reflow and underfill process were used in order to avoid any warpage. To evaluate proper assembly yield, chip attachment, underfill void and warpage were analyzed.



(a) Optical microscopy (x-section)



(b) X-ray microscopy

Die attach basically consists of mounting the chip over substrate, reflowing for solder joint and curing of underfill material. At first, the flip chip attachment of bare die onto coreless package substrate was analyzed through visual inspection and X-ray microscopy. For all 50 pieces of coreless package, die was placed at the right poison on coreless package substrate without any bump bridge or non-wetting. This result was confirmed by visual inspection and x-ray microscopy as shown in Figure 21. Underfill void was also inspected by scanning acoustic tomography (SAT). There was no defect (void) at entire underfill region as shown in Figure 22.

Fig. 22. Underfill void inspected by SAT.

In case of warpage, average warpage of all bare substrates (50peices) was satisfying customers specification. Warpage after each process step was also evaluated with known bare substrate warpage. It is seen from Figure 23 that warpage decrease after die attach and underfill process about 18.4%. The shape of incoming warpage is smiling shape. Therefore, the trend of reducing warpage is due to the CTE mismatch between the chip (~3PPM) and coreless substrate (~20PPM). As cooling down to 30^{o}C, coreless package is inclined to bend with crying shape.

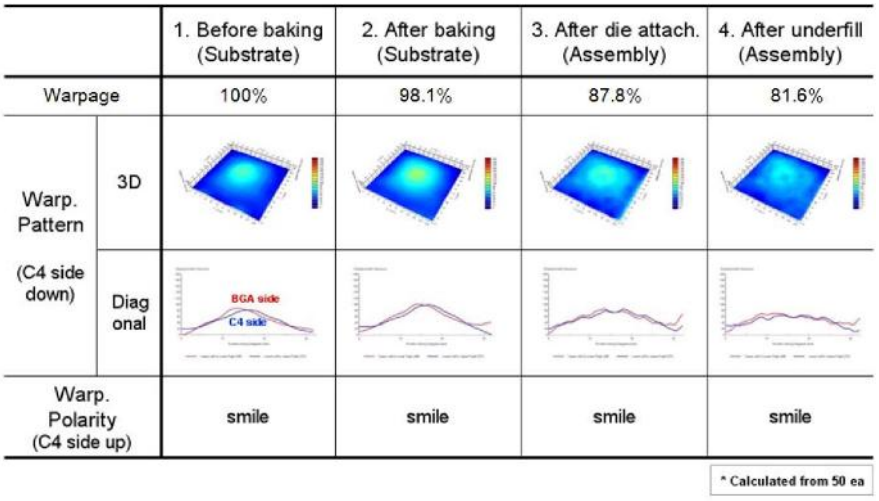


Fig. 23. Warpage trend during assembly process.

4. CONCLUSIONS

Coreless package substrate offering advantages in terms of electrical performance, fine pattern/pitch and thin substrate has been developed. The key element to success with coreless technology is to solve the warpage issue in terms of both manufacturing and assembly process.

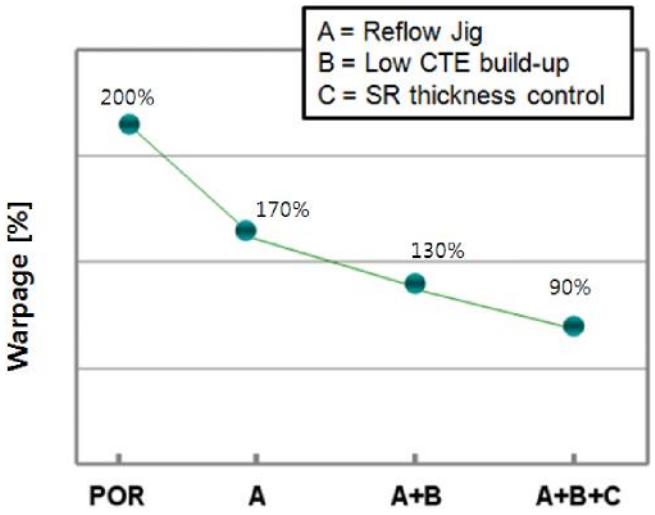


Fig. 24. Summary of warpage reduction effect.

In this study, we have pointed out three technologies to reduce the warpage, 1) design optimization 2) thermal/ mechanical treatment 3) low CTE materials. As shown in Figure 24, when all technologies are applied, the average warpage meets our goal. All warpage reduction technologies represented in this study show great effort. Even if bare substrate warpage is satisfied with customers need, coreless substrates might have issues for package warpage during the assembly process. As increasing substrate size and die size, assembly and reliability of coreless package are more challenging.

In near future, it is necessary to develop coreless package in terms of package size, device size, substrate thickness and composition, mold encapsulant material, die attach thickness and material. The coreless technology into volume production today has not always been an easy road. However, we expect that the effort to understand coreless substrate such as bi-metal theory, CTE balanced structure and minimizing mechanical/thermal stress mentioned in this study will help to overcome these barriers.

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Warpage issues and assembly challenges using coreless package substrate

Samsung Electro-mechanics

Jinho Kim

I Introduction

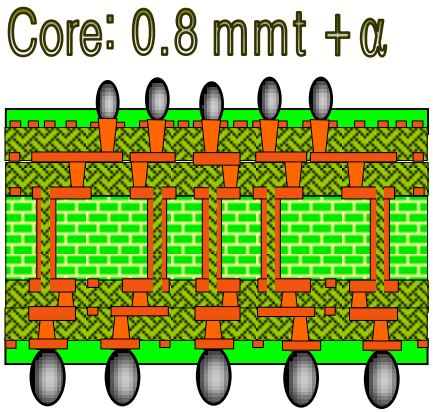
II Result & Discussion

- **Benefits of coreless substrate**
- **Manufacturing process**
- **Warpage issues**
- **Warpage reduction technologies**
- **Assembly result & discussion**

III Conclusion

I Introduction

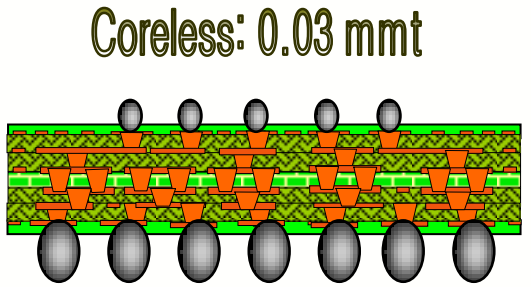
Characteristic properties of Coreless substrate



Conventional Substrate

Based on 6 layers

Substrate thickness ↓
Density ↑
Electrical performance ↑



Coreless Substrate

- **Substrate thickness** (No stiff core material)
- **High density** (Fine L/S & fine via formation by eliminating the PTH's in the core)
- **Better electrical performance** (Reduced EMI and Parasitic Inductance)
- **Thermally & mechanically induced warpage** will be problem to be solved for better reliability

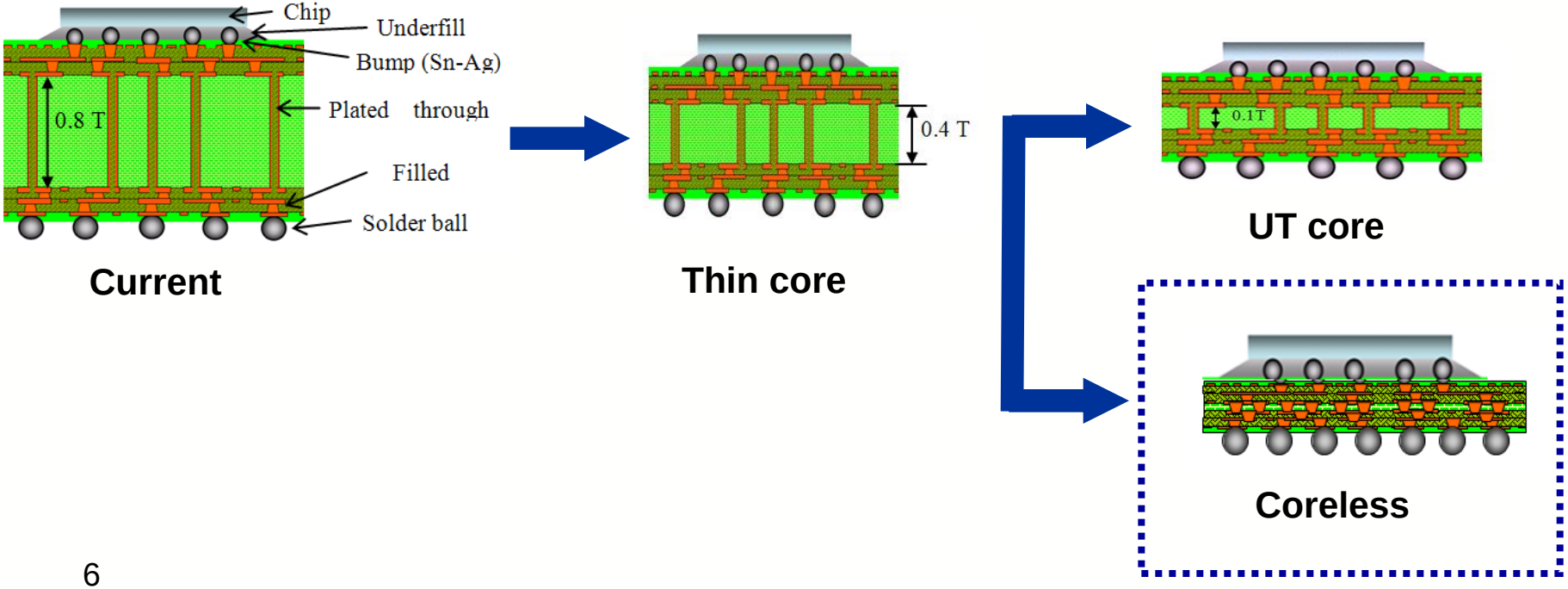
II Result & Discussion

- Benefits of coreless substrate
- Process comparison
- Warpage issues
- Warpage Mechanism
- Warpage reduction technology

Benefits of coreless substrate

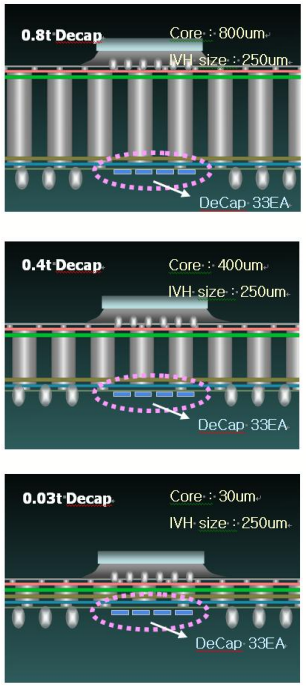
Thin substrate

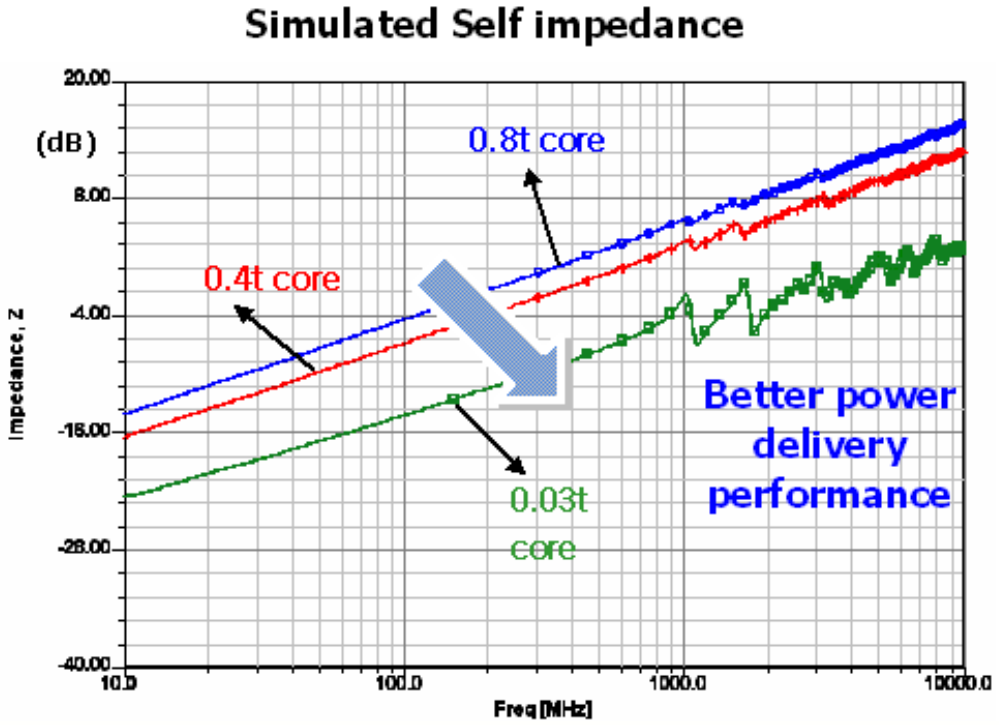
- Coreless substrate is thinner than any other substrates.
- A reduction in dielectric thickness → low aspect ratio of drilling and plating → tighter line to line space & via formation.



Better electrical performance

- Our simulation result shows coreless substrate has low impedance at entire frequency range
- Improving design flexibility for routing of high speed signals



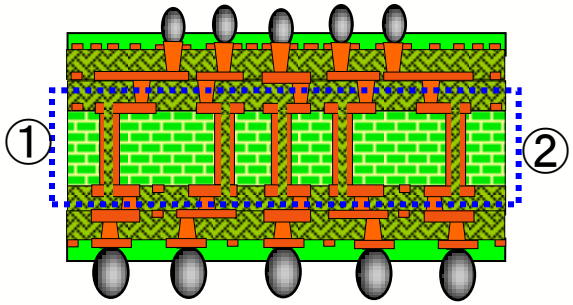


Process Comparison

Conventional substrate vs. Coreless substrate

◆ Removable process in conventional substrate

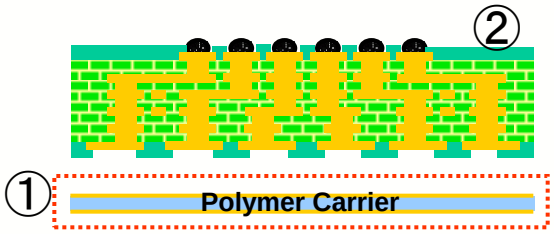
- Core fabrication (①)
- CNC drill & PTH plugging (②)



Conventional

◆ Additional process in coreless substrate

- Carrier fabrication (①)
- Modify back-end machine for handling thin panel after routing (②)



Coreless

Warpage Issue

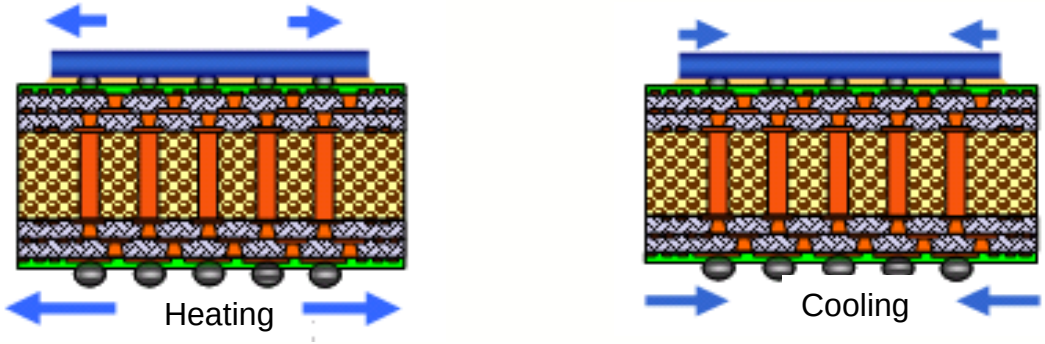
Maximum permissible warpage for current substrate

- **First level warpage : Bare PCB ≤ 127um**

  - Minimize **thermally & mechanically induced warpage** during process
  - It is difficult for coreless substrate to balance with current spec.
  - **More focused part in this study**

- **Second level warpage : Chip attached PCB ≤ 200um**

Chip attachment (RT → 260°C → RT)

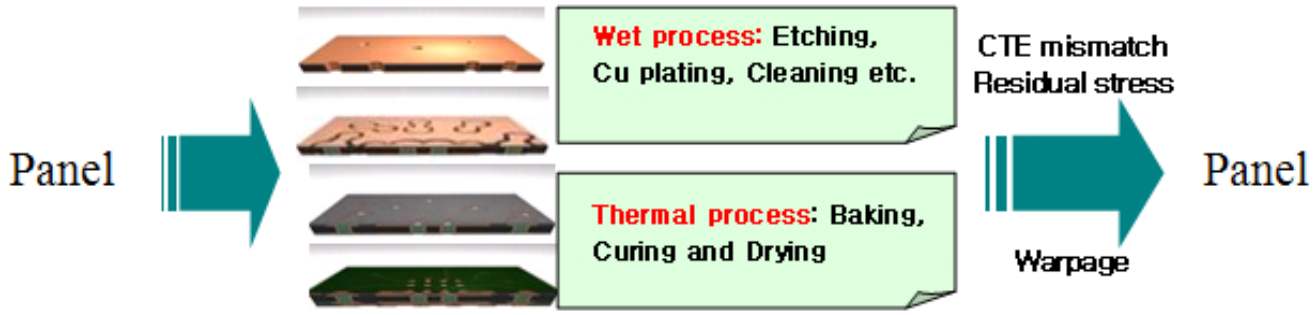


Warpage is more generated during packaging due to the CTE mismatch between die(~3 PPM) and substrate (~20 PPM)

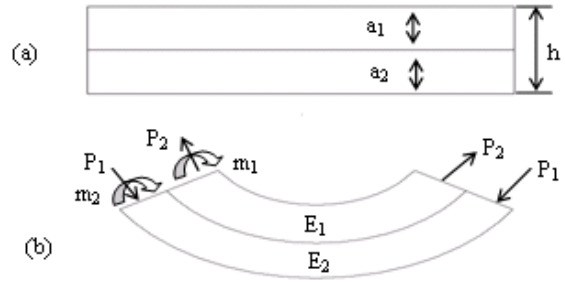
Warpage Mechanism

Incoming warpage during manufacturing process

- Incoming warpage is derived from periodic work by heating and wet process.
- Thermally induced warpage from CTE mismatch due to unbalanced design.



CTE mismatch : Bi-metal structure

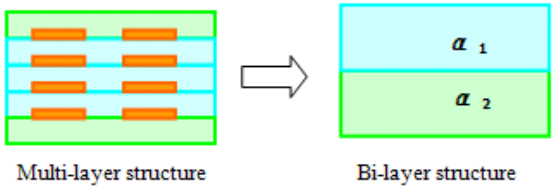


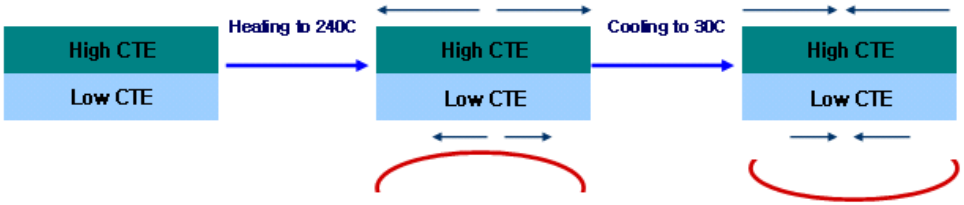
Material strip structure

After thermal loading

α_1 and α_2 : CTE of the two materials (1) and (2)
E_1 and E_2 : Modulus of elasticity
a_1 and a_2 : Thicknesses
h : Thickness of the strip.

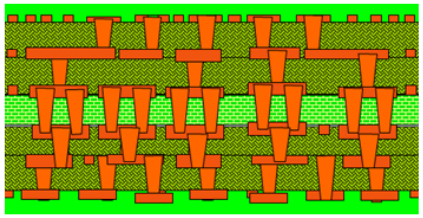
➢ **Coreless structure can be considered to Bi-metal structure.**





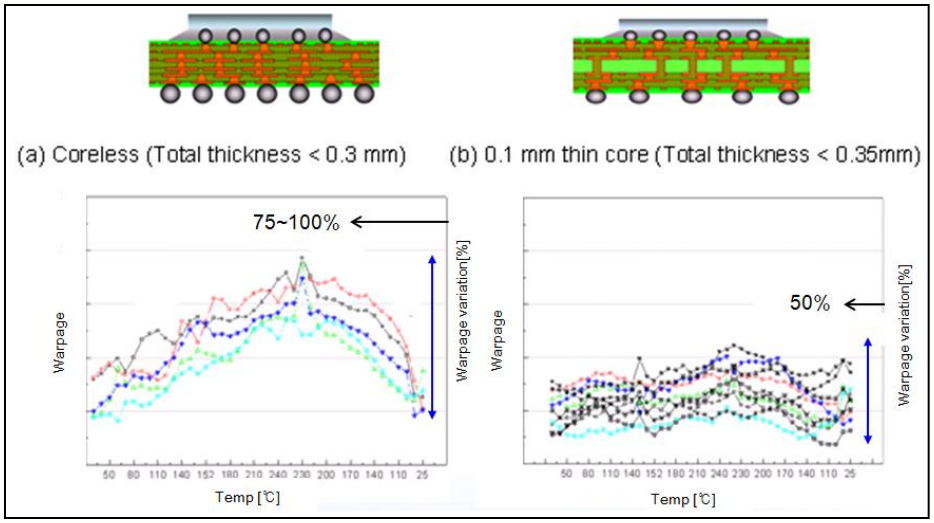
- If α_1 is bigger than α_2, the deflection will be convex down by thermal loading and the deflection will be concave up by cooling.

Coreless substrate



Layer	Cu portion	%
1L	351.6 mm2	66.2 %
2L	378.3 mm2	70.3 %
3L	404.3 mm2	76.4 %
4L	429.7 mm2	81.2 %
5L	428.5 mm2	81.0 %
6L	407.8 mm2	77.1 %

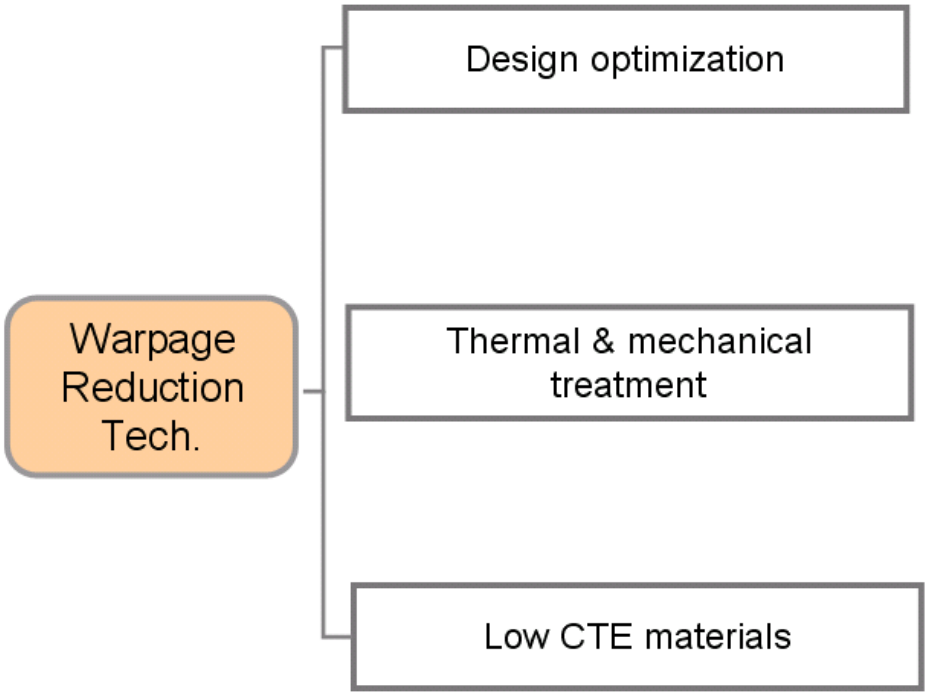
- Coreless substrate is asymmetric structure due to different Cu density
  → Cu potion of back layers is bigger than that of front layers.



- Warpage behavior between coreless and thin core substrate
  → In case of coreless substrate, chip attachment will be more difficult.

Warpage Reduction Technologies

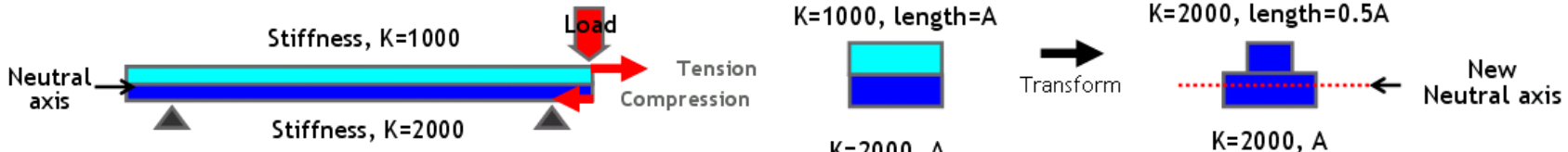
- Three categories for warpage reduction technologies



Design optimization

➢ Neutral axis

- When considering Bi-metal structure, it is important to set neutral axis for proper design optimization.
  : Neutral axis is not center, it should consider its stiffness.

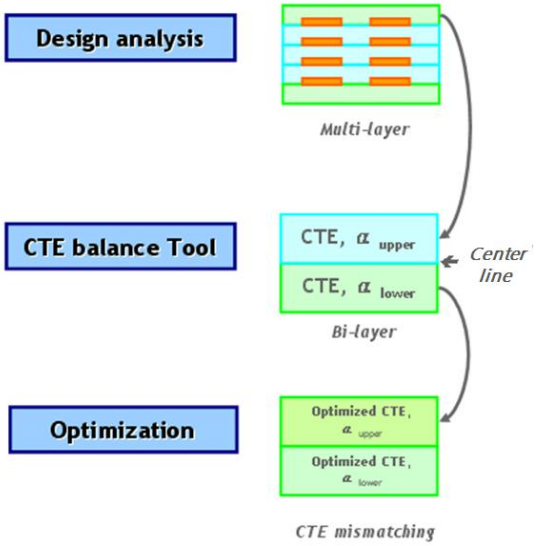


- The beam with neutral axis
- New neutral axis considering its stiffness

Design optimization

➢ Neutral axis of coreless substrate

- Neutral axis of coreless substrate can be calculated by using modified rule of mixture.
- For proper design analysis, volume and thickness of Cu/Insulation layer is calculated by their CTEs.
- For CTE balance, we set geometrical center line and calculate average CTE of upper and lower layer respectively and find $\alpha_{upper} - \alpha_{lower} \rightarrow 0$, which is geometrical center line is equal to new neutral axis.



Low warpage Coreless at Center line

$\alpha_{upper} - \alpha_{lower} \rightarrow 0$

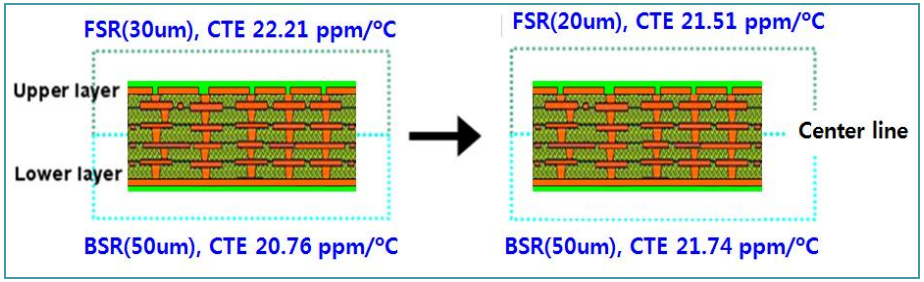
$\therefore$ Center line = Neutral axis

- The concept of coreless substrate design evaluation tool

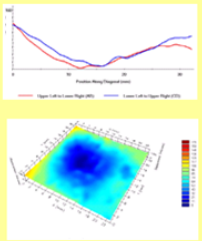
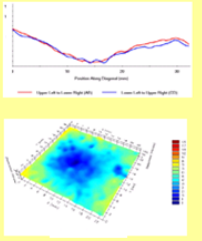
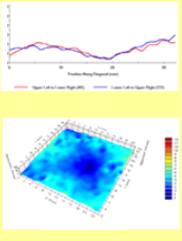
Design optimization

➢ SR thickness control

- In case of DOE 3, it showed the balanced CTE value (Front=21.51ppm, Lower=21.74ppm)
  : DOE 3 shows the lowest warpage and warpage variation.



• CTE calculation of upper and lower layer by design evaluation tool

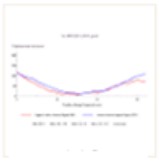
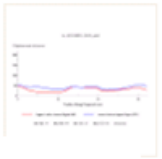
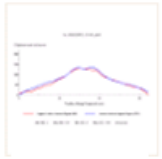
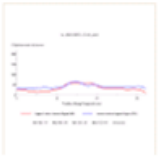
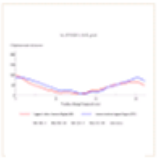
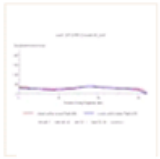
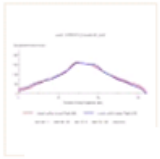
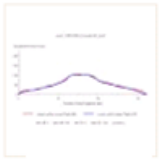
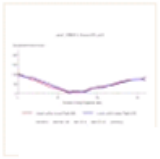
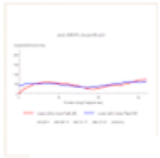
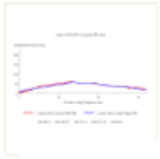
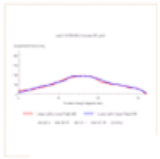
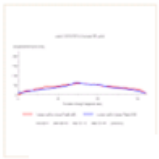
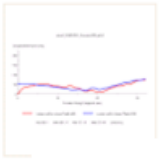
TEST	DOE1	DOE2	DOE3
FSR [um]	30	25	20
BSR [um]	50	50	50
Warpage (%)	100%	76%	54%
Warpage shape			

• Incoming warpage depending on FSR/BSR thickness ratio [front SR (FSR), back SR (BSR)]

Design optimization

➢ SR thickness control

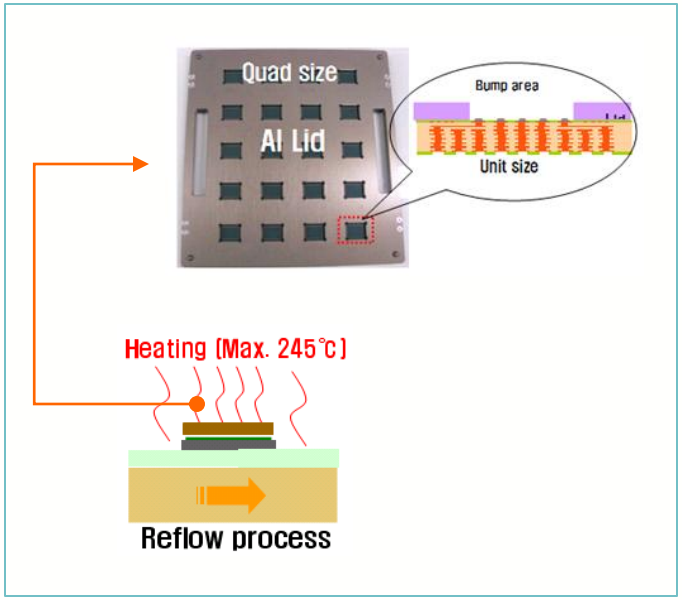
- DOE3 also shows the lowest warpage variation during heating & cooling.

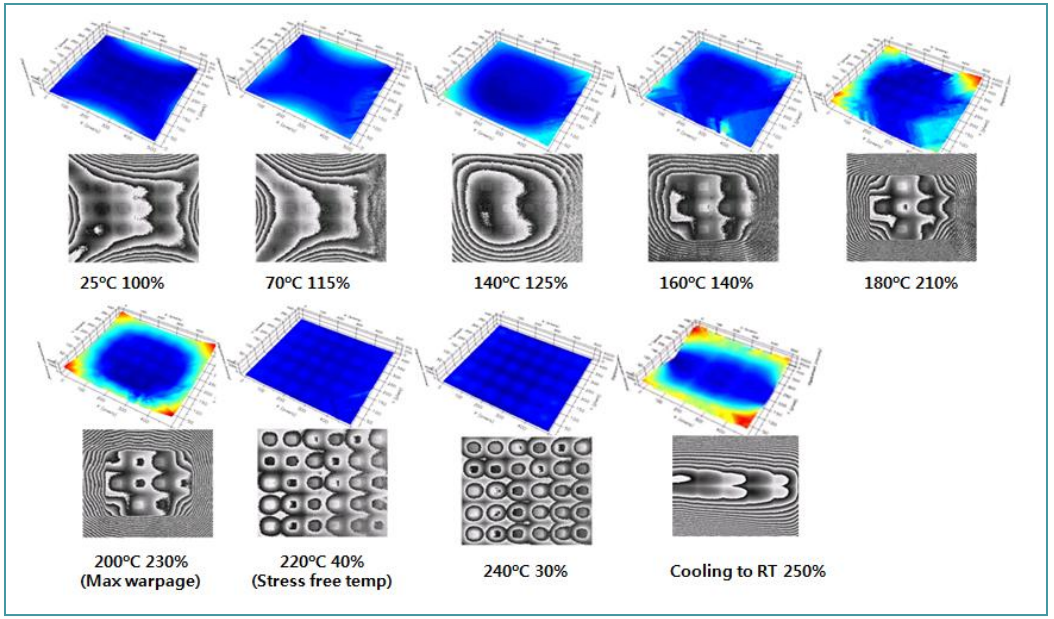
Temperature	25°C	180°C	240°C	160°C	25°C	ΔW
DOE1						100%
DOE2						95%
DOE3						67%

Thermal/Mechanical treatment

➢ New reflow jig (cover jig)

- 100% of Initial warpage is increased to 250% without cover jig.
- During reflow, it shows the lowest warpage at stress free temperature (>220°C).
  : Warpage at stress free temp. decreases about 60~70% compared to initial warpage.
  : By using new reflow jig, the lowest warpage is maintained during cooling process.
  : It shows 30 % of warpage reduction after using cover jig.



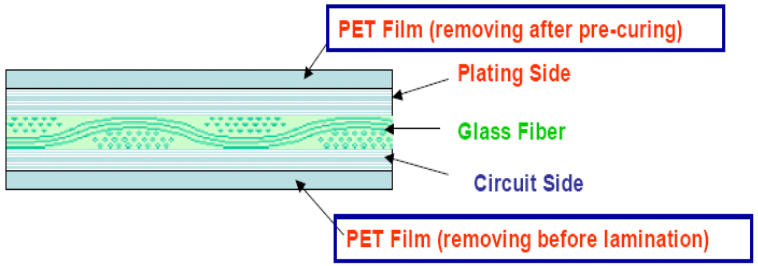


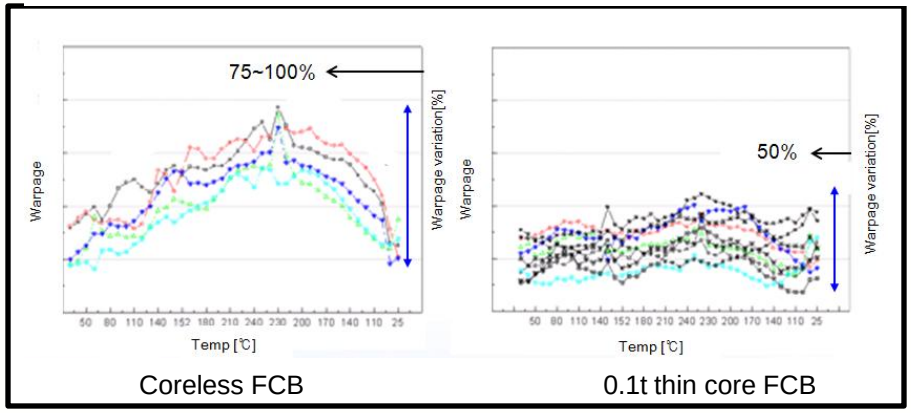
Low CTE build-up material

➢ Glass reinforced low CTE build-up

- Both incoming warpage and warpage variation are reduced after applying low CTE material.
  → Initial warpage : 20% reduction
  Warpage variation : Coreless 35~40% reduction, thin core 25% reduction

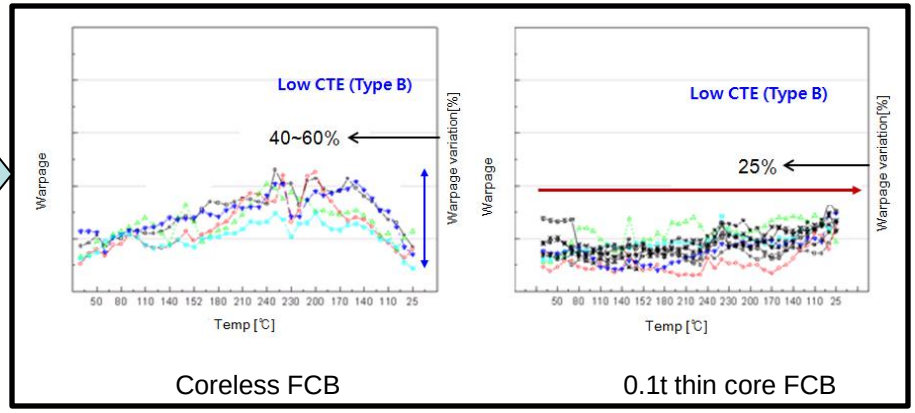
	Code	Type A	Type B
Type	-	Non-woven	Woven
Reinforcement (SiO_2)	-	Filler	Filler + Glass cloth
Dielectric Thickness	um	37.5	50
Tg (TMA)	℃	156	166
CTE (α1)	ppm/℃	46	19
(α2)		120	7
Young's Modulus	GPa	4	11.2





Coreless FCB 0.1t thin core FCB

Type A insulating layer



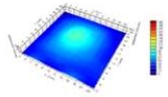
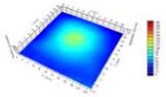
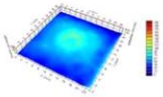
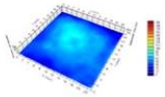
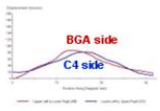
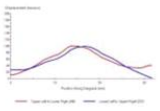
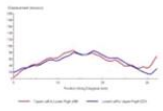
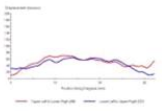
Coreless FCB 0.1t thin core FCB

Type B insulating layer

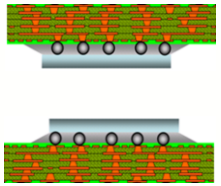
Assembly Yield

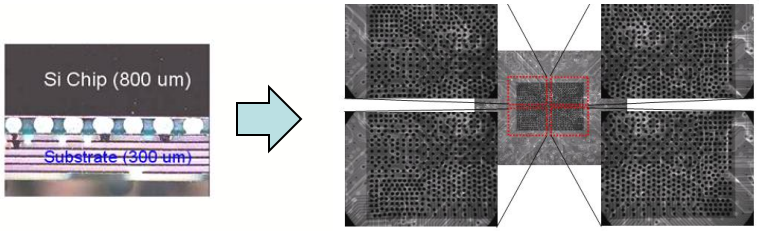
No warpage and bump void issue for 20~30 body coreless substrate

- Incomping warpage is reducing due to CTE mismatch between the chip (~3PPM) and coreless substrate (~20PPM).

		1. Before baking (Substrate)	2. After baking (Substrate)	3. After die attach. (Assembly)	4. After underfill (Assembly)
Warpage		100%	98.1%	87.8%	81.6%
Warp. Pattern (C4 side down)	3D				
	Diagonal				
Warp. Polarity (C4 side up)		smile	smile	smile	smile

* Calculated from 50 ea



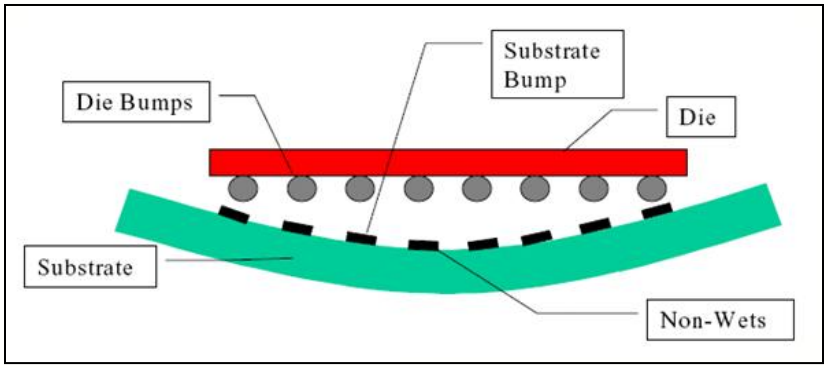


110MHz Echo-Mode

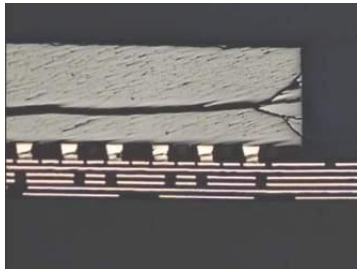
X-ray microscopy Image after chip attachment
: No micro crack or bump missing

No underfilling void
by scanning acoustic tomography (SAT)

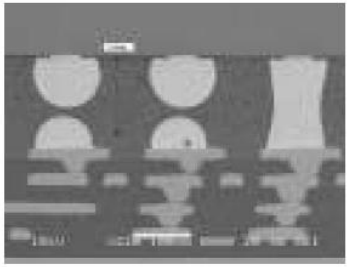
Die crack and non-wet issue for large body coreless substrate (> 40body)



Previous study in 2008



Die crack



Non-wet at the edge

➢ Future work

- CTE mismatch between coreless substrate and the die will be more severe as increasing substrate size and die size.

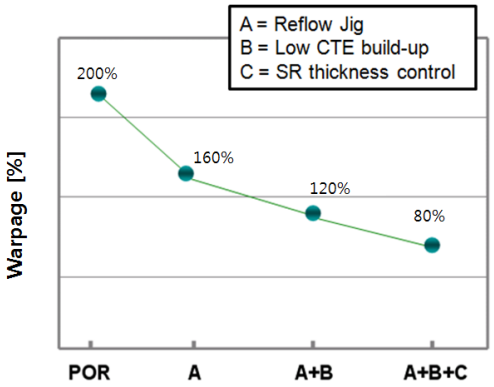
- To figure out this problem, it is necessary to develop new packaging method or equipment for coreless substrate.

III Conclusion

- Coreless package substrates have several advantages compared to conventional package substrates such as thinner substrate, better electrical performance and stable manufacturing process.

- For proper design analysis, neutral axis is applied considering volume and thickness of Cu/Insulation layer.

- Incoming warpage at the substrate manufacturing site is reduced by design optimization, thermal/mechanical treatment and low CTE material.



- There is no warpage and bump void issue for 20~30 body coreless substrate.

- In the future, it is necessary to evaluate the effect of package size, die size and die thickness in coreless substrate and confirm to have the flatness of the final package depending on many factors including material sets and structures.