An Investigation into the Predictability of PCB Coplanarity for Room vs. Lead Free Assembly Temperatures

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ABSTRACT
With the advent of larger packages and higher densities/pitch the Industry has been concerned with the co-planarity of both the substrate package and the PCB motherboard. The iNEMI PCB Co-Planarity Working group generated a snapshot in time of the dynamic co-planarity of several PCB's designs from four market sectors. This paper presents the summarized results of the project's investigation of the question if room temperature co-planarity measurements can predict the co-planarity at Lead-Free assembly temperatures. This paper will also investigate the trends in dynamic co-planarity between market sectors and global versus local area of concern measurements as well as share the learning and issues of undertaking dynamic co-planarity measurements of PCB motherboards.

INTRODUCTION
In Q3, 2008 iNEMI initiated the SMT Coplanarity project to develop metrologies and recommendations to enable the measurement and specification for board land coplanarity to ensure high quality, high yield SMT processes for current and next generation components and boards.

Several of the reasons/drivers for the establishment of this WG were;

- The current specifications for component lead coplanarity and board bow and twist have not kept pace with the developments in packaging and board technology. Currently some system manufacturers are experiencing poor SMT yields using materials that meet the current specifications.
- The converse is also true. Some of the newest component technologies are hampered as they fail to meet the current component standards; however have demonstrated high yields in SMT assembly.
- It is clear that updated standards are needed that can provide the needed assurance of quality while maintaining the continuous innovation that is basis of the industry.
- New measurement techniques have enabled the measurement of flatness during simulated SMT conditions allowing more relevant standards to be developed.
- Several Standards bodies have already issued standards using these new measurement techniques for components. These standards efforts could be extended to ensure the flatness of system boards as well.

EVALUATE AND ESTABLISH METROLOGY

After various discussions with industry members the team chose to use the Shadow Moiré technique because of its capability to measure warpage from room to elevated temperatures (260°C). This is a known method used in substrate/component coplanarity evaluations and several members of the WG had access to this type of metrology. The following section outlines the equipment and methodology used in this evaluation. A more detailed report of the test methodology is available upon request.

Both the global PCB (large area/full board) and at least two local areas of interest (BGA sites) on each board were measured and analyzed throughout the temperature range.

TEST PROCEDURE

Hardware/Software

Several systems were used to gather data included Akrometrix TherMoiré PS400, AXP, PS600 and PS24 units. A 100 lines per inch (lpi) grating was utilized for the PS400, AXP, and PS600 systems. A 50 lpi grating was utilized on the PS24. The primary impact of using the coarser 50 lpi grating is that the sample to grating distance could be increased without notably compromising the clarity of the ShadowMoiré image. When correlating data between sample test sets, submitted data from any system should include a declaration of the following:

- System Model
- X and Y extents or Field of Vision (FOV) employed
- Grating Pitch
- Spacing from Grating Glass to Sample Surface
- Type of Sample Support, Uniform Area Support (UAS) fixture or 2 parallel support braces (edge support).
- Temperature Profile applied
- Software used for Analysis (TherMoiré v. 2.X or Akrometrix Studio v. 5+)

Sample Prep and Surface Finish

Each sample was purged of any absorbed moisture. Outgassing of any residual moisture could fog the grating glass and compromise multiple data point images. Prior to imaging the samples were kept in either a sealed bag or a nitrogen dry box along with a humidity indicator card (HIC), which demonstrates the proper dryness of the samples inside. Since the moisture/storage history of all samples were unknown, in order to reduce the amount of outgassing the samples were baked for 24 hours at 125°C to insure dryness prior to measurement in the TherMoiré heating chamber. Note that the bake time was increased from 12 to 24 hours in an attempt to decrease outgassing effects causing lost data points. However, the 24 hour bake time did not improve the situation, so a 12 hour bake to remove moisture should be sufficient for future testing.

Figure 01 shows the ideal surface finish and color for use with the shadow moiré technique is one that is diffuse and white. Such a sample surface will result in the least amount of noise and highest contrast for the moiré fringe pattern. In order to achieve this surface type, a thin layer of high-heat white paint was applied on top of the sample. This coating should be scattered uniformly across the whole sample but still be “semi-transparent” so that surface features are not completely covered.

Sample Placement

There was a great deal of early discussion on how to support the PCB’s when measuring at elevated temperature, especially for thinner PCB’s. Since the goal was to model what the dynamic coplanarity is during SMT reflow, supporting the PCB with a jig, pallet, Uniform Area Support (UAS) fixture or other means would prevent sagging at elevated temperatures but may not represent what is truly happening during the reflow cycle. Since the use of pallets during SMT assembly is growing but not universal at this time, the WG decided to model the SMT Assembly process using the two rail edge support method.

Thermocouple Placement

The test method attached one thermocouple to the top surface and multiple thermocouples to the bottom surface of the sample depending on the number of BGA sites to be measured:

Thermocouples were attached to the sample surface using thermal grease and Kapton® tape as described in JEDEC standard JESD22B112

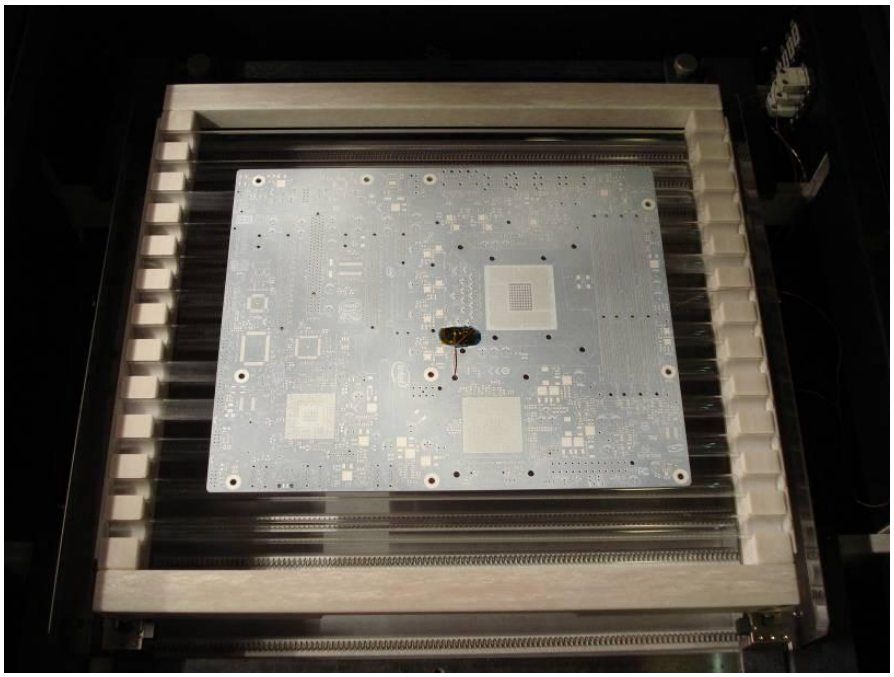


Figure 01 Painted Sample on UAS Fixture

Thermal Profile and Temperature Range of Data

Measurement points were taken from room temperature through the heating cycle to 260 °C and back down through the cooling cycle to room temperature at 20°C increments for a total of 25 measurements.

Three thermal profiles were evaluated in this study. Profile #1 had a heating and cooling rate of approximately 0.3°C/s to better aid in achieving uniform temperatures throughout the board. Profile #2 attempted to more closely emulate a typical temperature profile found in a PCBA production environment. Profile #3 used a soak cycle to bring the PCB to a more uniform temperature prior to recording the measurement. Figure 02 shows the comparison of the #1 & #3 thermal profiles used in the Industry Snapshot Data. Process 1 is the temperature of the bottom thermocouple and process 2 is the temperature of the top thermocouple. The results of the warpage magnitude between a continuous ramp temperature profile and a soaking cycle temperature profile on a specific test vehicle is shown in Table 01. The coplanarity values were within 3µm of each other for all measured temperature. It was decided by the WG that there was no benefit in having a PCB soak cycle that only added time to the testing process.

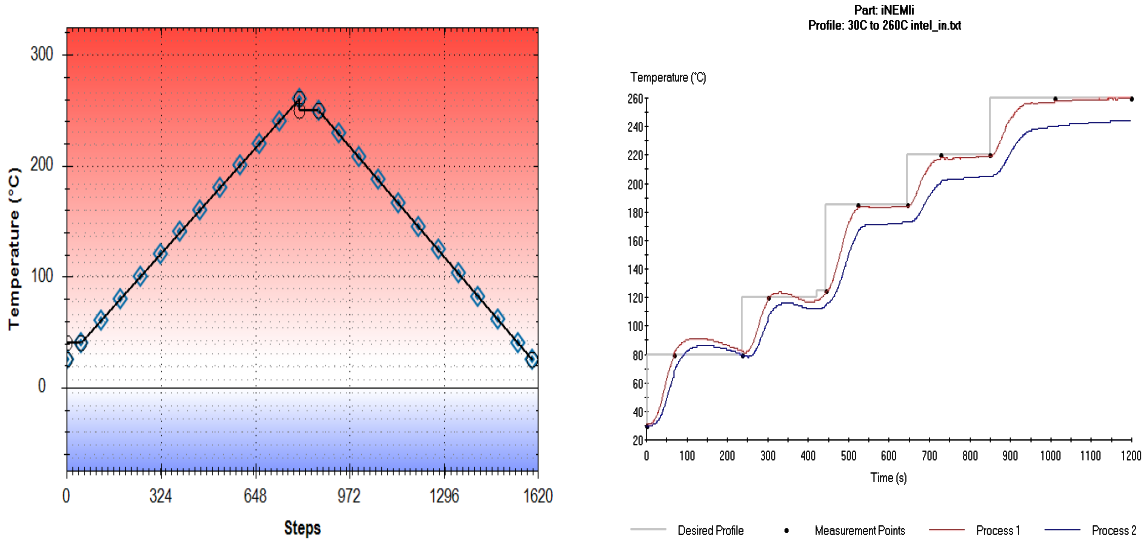


Figure 02: Comparison of 2 thermal profiles

Table 01: Comparison of the warpage measurement between a continuous ramp temperature profile and a soaking cycle temperature profile

Temperature profile	Measurement Temperature					
	28˚C	80˚C	125˚C	185˚C	220˚C	260˚C
Continous ramp	62 µm	63 µm	66 µm	63 µm	60 µm	60 µm
Soak at measurement	57 µm	60 µm	63 µm	62 µm	58 µm	58 µm

Coplanarity Ratio System

Since one of the goals of this project was to establish a correlation between the global PCB warpage and the local BGA site coplanarity, a new gauge, Coplanarity Ratio, was used. This allowed for direct comparison of many sizes of BGA and PCB's with this unitless ratio. Figure 02 describes the Coplanarity Ratio as the coplanarity value (um) at any temperature divided by the diagonal length (mm) of the measured area. For example, if a 150 × 200 mm PCB has a co planarity of 1000 microns and a 30 × 40 mm BGA has a co planarity of 200 microns, their co planarity ratios are both 4 microns/mm. Coplanarity ratio can be calculated by mils/inch or microns/millimeter. The calculations of these two cases are presented in the following.

Example of the Coplanarity Ratio calculations:

$$1000/\sqrt{150^2+200^2} = 1000/250 = 4(um/mm)$$

$$200/\sqrt{30^2+40^2} = 200/50 = 4(um/mm)$$

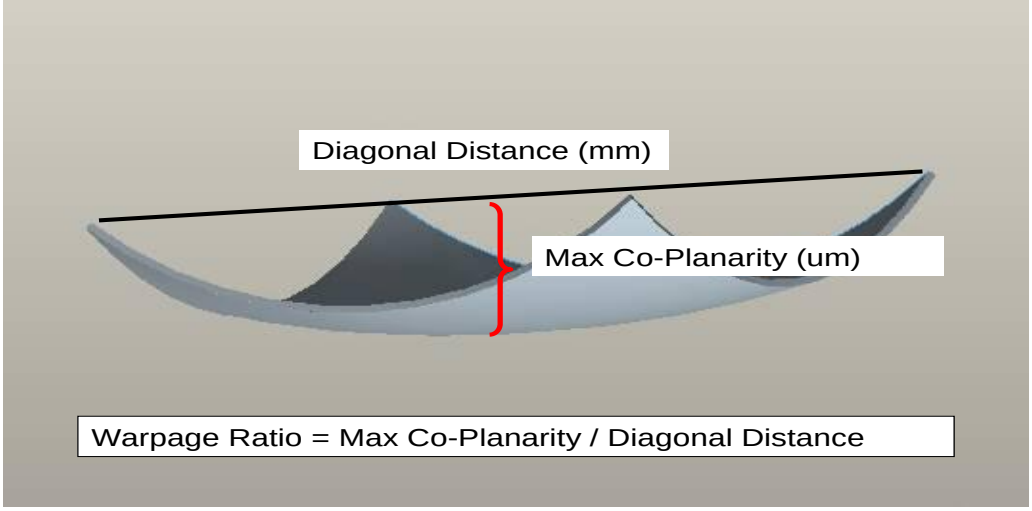


Figure 02: Coplanarity Ratio Diagram

METROLOGY ANALYSIS

PCB Gravitational Deformation

It was found that the thin PCB's and any thick multi-up PCB which had large rout lines would sag or deform under it own weight during the measure cycle using the two rail support system. This was a concern for the WG and should be heavily considered for future testing or process definition. Figure 03 shows an example of a thick panel with a heavy rout line down the middle of two PCBs (2 up panel) and one side/PCB of the same data set (Half panel).

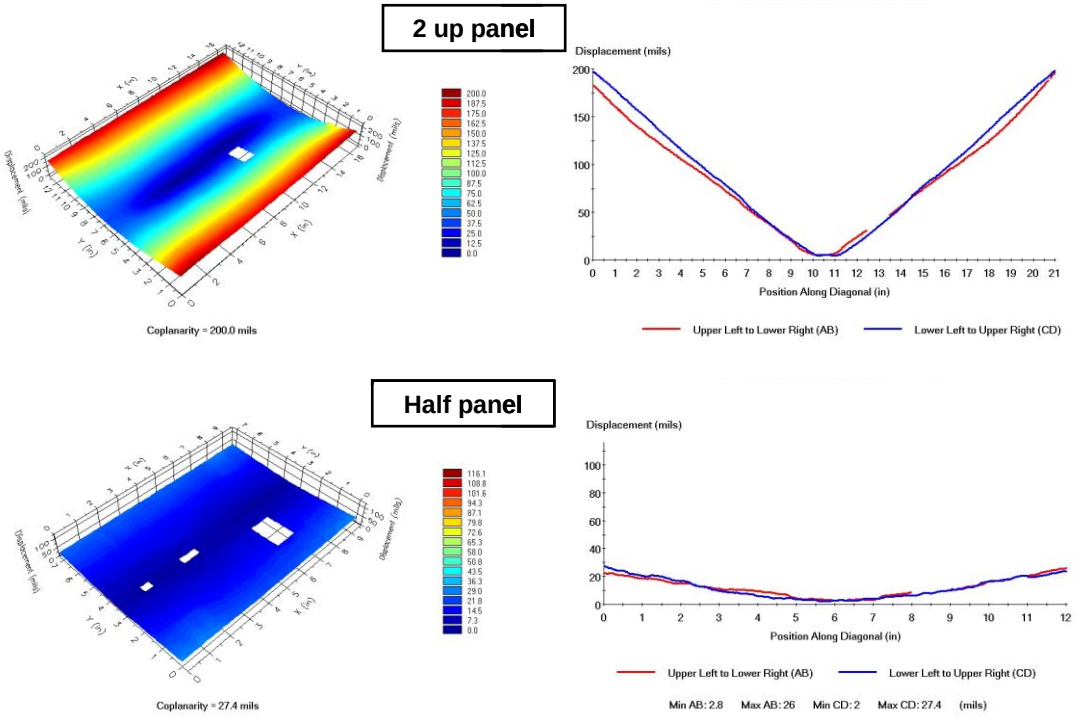


Figure 03: Affects of Gravitational Sag

The WG's recommendation is that the support methodology should model the SMT assembly process, but be aware of the effects of heat and gravity on the total board curvature. Fortunately, the Akrometrix systems have algorithms that can compensate for this gravitational sagging. It uses a Least Square Fit algorithm (LSF). The LSF rotation was applied to the data obtained during this project.
The LSF rotation must be applied during analysis to obtain correct co planarity values. Choosing LSF rotation also allows concave or convex shape to be defined as in JEDEC standard JESD22B112 or JEITA standard ED-7306.

LSF (Least Squares Fit) Rotation is a method of orienting the displacement (Z) data measured to remove overall 'slant' of the 3D shape and rotating it so its 'least squares' representative plane is parallel to a common XYZ coordinate system. For this project, the result is that the measured shape is retained, but the angle it sits in the oven is removed so that a 'true' co planarity relative to the measured area itself is obtained. Figure 04 below illustrates the need for and application of LSF for this project. (Z curvature has been exaggerated for clarity.)

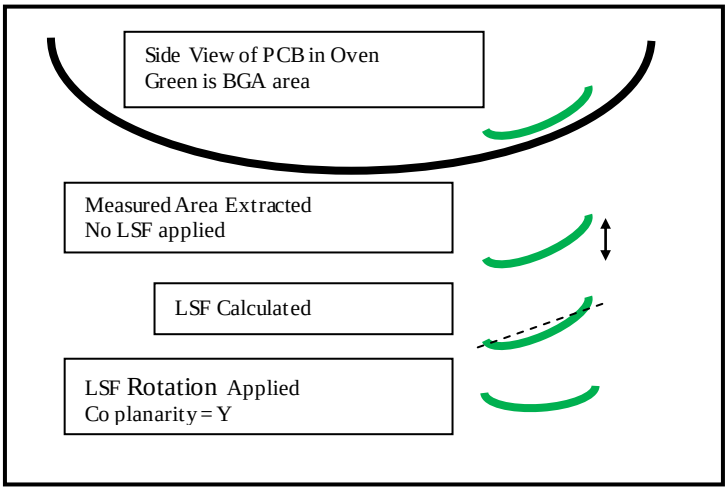


Figure 04: Least Square Fit Rotation method

Outgassing Effects, volatile polymer components

Although global and local data from more than 100 PCBs was collected in this study, for some board designs, vapors from the samples at elevated temperatures coalesced on the grating glass above the samples. Figure 05 shows that when enough vapor deposited on the grating at any one point, the moiré effect at that point no longer was visible to the TherMoiré's camera, resulting in the loss of that local data point. In some cases, outgassing was so severe, with so much material depositing on the grating the surface could no longer be analyzed and an entire sample measurement at that temperature, for that PCB, was lost.

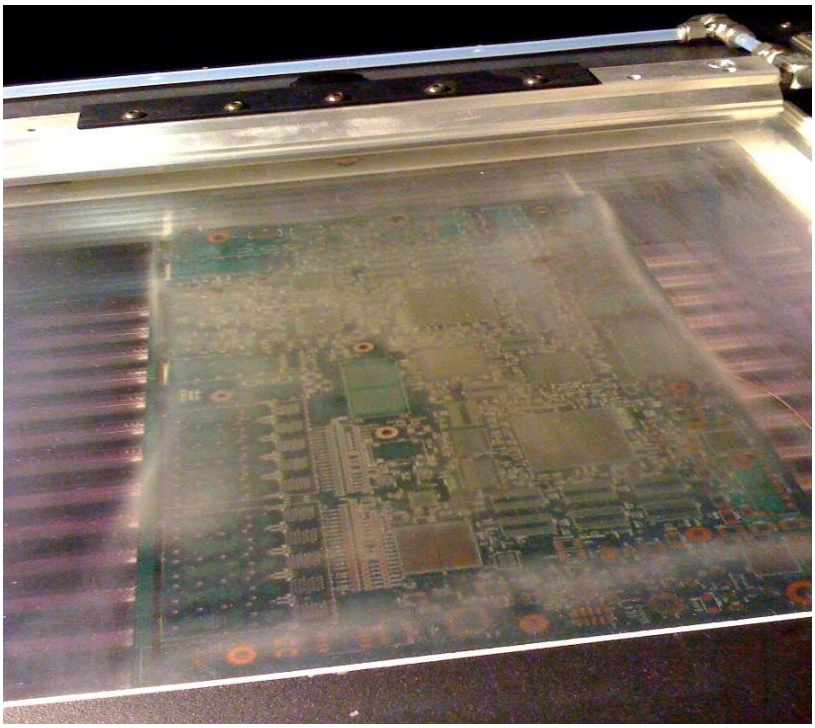


Figure 05: Outgassing vapors on the grating glass.

The vapors in question are released closer to 250°C, and the increased bake time at 125°C may have reduced the moisture content further but had no noticeable effect on the loss of data points.

The work group tried to increase the grating distance which had no effect. As shown in Figure 06, where missing data points result in breaks in some of the plot lines, the best method for eliminating the negative effects of outgassing may be to simply test enough samples that a trend is determined. With multiple samples, any data lost for a single sample has less effect on the overall analysis.

Multiple Thermal Cycle Measurement of a PCB Board

In an effort to understand the best time for the Warpage measurements to occur during the PCB Fabrication through Assembly cycle the WG investigated the effect of multiple measurement cycles. This experiment compared warpage variations of a single PCB board between repeated thermal cycles. PCBs were subjected to 5 TherMoire temperature cycles at 3 different sites with various supports and temperature ramp profiles. The Flextronics Austin and Intel Chandler Austin labs each ran a single PCB using the Max Rate temperature profile while being supported across 2 rails at opposing PCB edges. The Akrometrix Atlanta lab ran a PCB using the 0.3°C/sec while being supported across the Uniform Area Support (UAS) fixture. The rail supports would allow for gravitational sagging as the PCB reaches and exceeds its Tg temperature and softens in rigidity. The UAS provides a more level and planar support across the PCB's surface area. Testing at all three facilities showed a general trend of warpage reduction that held across multiple temperature cycles for any support condition.

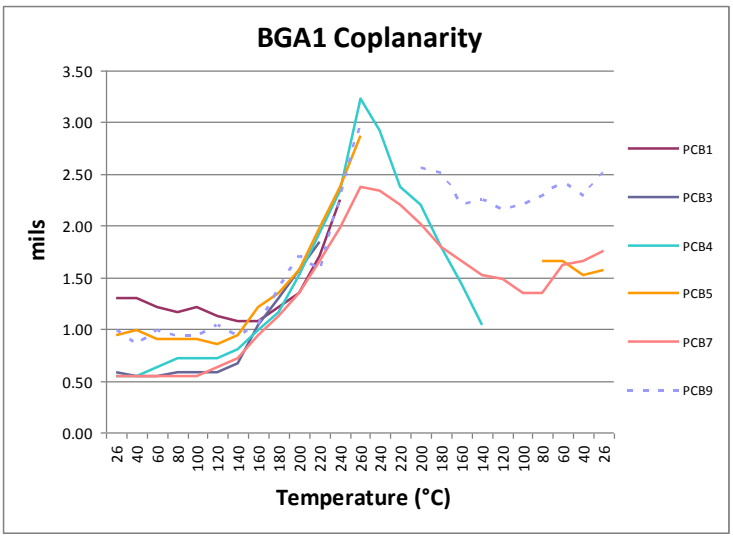
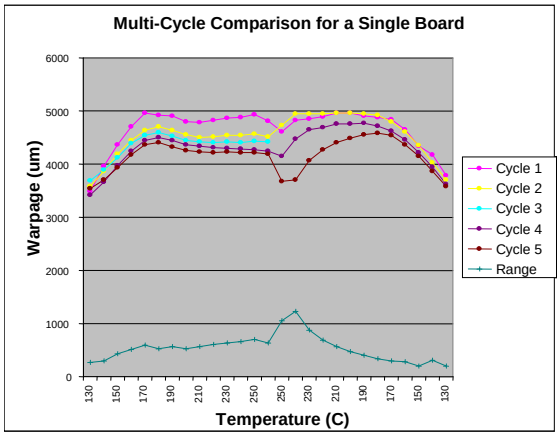
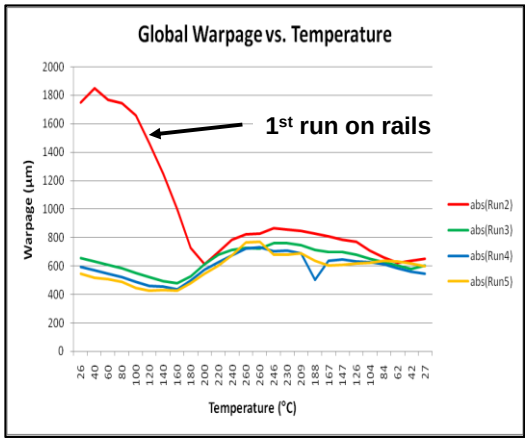


Figure 06: Data loss caused by outgassing of samples

Figure 07 shows that the warpage reduces in magnitude with each subsequent temperature cycle with a large drop in warpage from the first reading and second readings.





2 rail support system UAS full support system run 3-5

Figure 07: Multi Cycle Warpage vs. Temperature for a two rail and a fully supported system

The UAS supported run implies that once Tg temperature is achieved the soften structure of the PCB can be strongly influenced by the measurement support structure utilized. In this case the initial run #1 impressed a gravitational sag that it held upon cooling when it was supported across pair rods during the initial run. Therefore run #2 started at a higher warpage value than subsequent runs. Then upon reaching Tg while supported in an UAS fixture the PCB dramatically flattened and remained in that general flattened contour throughout subsequent runs.

INDUSTRY SNAPSHOT

Once the WG had developed the measurement methodology they decided to get a Snapshot in time (2011) of what the coplanarity of BGA and PCB's are for real product in the market place. They focused on four market segments, Desktop, Notebooks, Workstations and High End Servers. These unassembled product PCB's were obtained from various OEM/ODM's in the industry. The WG measured 10 PCB with 2 BGA per PCB from each lot. The following data is from this dataset and utilizes the Coplanarity Ratio for analysis. This section analyzes the series of questions raised in the SOW during project formation.

***Local Area of Interest (BGA) Vs. Global Relationship*:**

The Local Area of Interest (BGA) is the most important area to the SMT process. Both Room Temperature and Dynamic Coplanarity are important since they affect both the ability to screen the solder paste and the formation o f the solder joint.

The Global warpage value is more important for processing whole boards through equipment and installation into racks while the Solder Joint formation is more dependent on the BGA/Local Area of Interest Coplanarity.

Table 02: Coplanarity Ratio Values for all Market Sectors and Lots (Means + 3 STD)

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
Notebook Sector	**1.64**	**3.78**	**7.22**	**24.03**
SNB0210	2.13	4.75	5.49	17.74
SNB0310	1.23	2.99	6.96	23.35
TNB0110	1.54	3.11	6.81	12.67
VNB0110	1.74	3.35	7.80	11.37
VNB0210	1.74	2.48	6.14	8.86

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
Desktop Sector	**1.79**	**3.75**	**5.77**	**10.52**
ADT0110	1.39	3.75	3.90	5.80
EDT0110	1.87	3.40	4.17	7.54
NDT0110	1.89	3.69	7.57	13.71
TDT0110	1.38	1.96	4.52	6.94

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
HE Server Sector	**1.81**	**2.62**	**2.30**	**3.96**
HSE0110	2.18	2.81	1.05	2.00
CSE0210	1.18	2.06	1.17	2.14
CSE0110	1.81	2.64	1.42	2.12

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
WS Server Sector	**1.80**	**3.48**	**1.92**	**3.98**
CSW0205	1.92	2.37	1.61	1.88
CSW0305	0.85	1.50	1.93	3.86

Table 02 shows the average coplanarity ratio for each lot and for the entire market sector. This shows that there is less variability in the BGA coplanarity ratios between the market sectors, than for the Global warpage. Even with a large Global warpage seen with the Notebook & Desktop sector, the BGA areas were relatively flat and consistent across the market sectors.

Can the Room Temperature Coplanarity predict the Maximum Coplanarity?

To better understand the initial room temperature to maximum coplanarity relationship the WG correlated the maximum coplanarity ratio at any temperature with the initial room temperature ratio. Figure 08 shows this correlation of Initial Room Temperature to Maximum Coplanarity for all the BGA's in the study. The trend line shows that the Maximum Coplanarity for all the Industry Snapshot data analyzed is 1.93 times the Room Temperature coplanarity. This Snapshot data is a composite of various materials, BGA sizes and board designs from the four market sectors under evaluation and contains a lot of outliers. Still the approximation of 2X is interesting and appears again in the individual lot results found in Table 03

Table 03 shows the Ratio of the Maximum Coplanarity Ratio divided by the Room Temperature Coplanarity Ratio for the same data found in Table 02. This data seems to indicate that the individual lot results may be design dependent. The thicker and higher layer count boards have lower Max/RT ratio's than the thinner Desktop and Notebook designs. It is also interesting that the variation within a market sector can be quite large, as shown by both the Notebook and Desktop data. Although the sample size of the lots within these market sectors is small, it is does raise the questions concerning what is it about the design of these boards that lead to the various warpage values since the size, thickness and layer counts were very similar within the market sector. NOTE: The WG believes that this is an important area for further study and understanding. To calculate a precise Max/RT ratio for any specific design measuring 25-30 boards per design over several fabrication lots is sufficient to generate a design specific Maximum to Room Temperature Warpage ratio at a 90% confidence level. This number can then be used as a more precise predictive value of Elevated warpage from Room Temperature measurements.

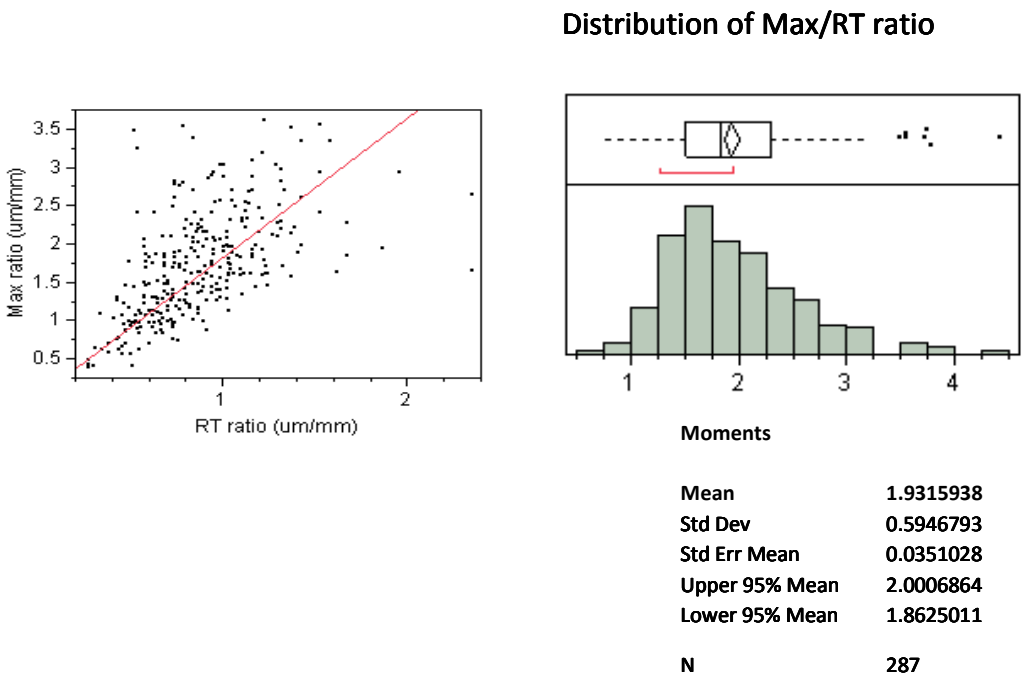


Figure 08: BGA data showing the relationship of Maximum to Room Temperature Coplanarity

Table 03: Maximum Coplanarity Ratio divided by initial Room Temp Coplanarity Ratio (means + 3 sigma).

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
Notebook Sector	**2.30**	**3.33**
SNB0210	2.23	3.23
SNB0310	2.44	3.35
TNB0110	2.02	1.86
VNB0110	1.92	1.46
VNB0210	1.43	1.44

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
Desktop Sector	**2.09**	**1.82**
ADT0110	2.69	1.49
EDT0110	1.82	1.81
NDT0110	1.95	1.81
TDT0110	1.42	1.53

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
HE Server Sector	**1.44**	**1.72**
HSE0110	1.29	1.90
CSE0210	1.74	1.83
CSE0110	1.46	1.49

Average Warpage Ratio in um/mm	BGA Max/RT	Global Max/RT
WS Server Sector	**1.94**	**2.07**
CSW0205	1.23	1.16
CSW0305	1.76	2.00

Can one BGA size predict a different size BGA's coplanarity on a board?

The WG was unable to find neither a correlation based on the data set nor any statistical correlation between the BGA Coplanarity and the Diagonal length. Figure 09 shows the composite graph of the Maximum BGA Coplanarity as a function of BGA diagonal length for all BGA's. The data did not show a hard correlation between BGA sizes. There is large range of Coplanarity values for any size BGA. There seems to be other overriding factors that affect coplanarity other than simply the BGA size.

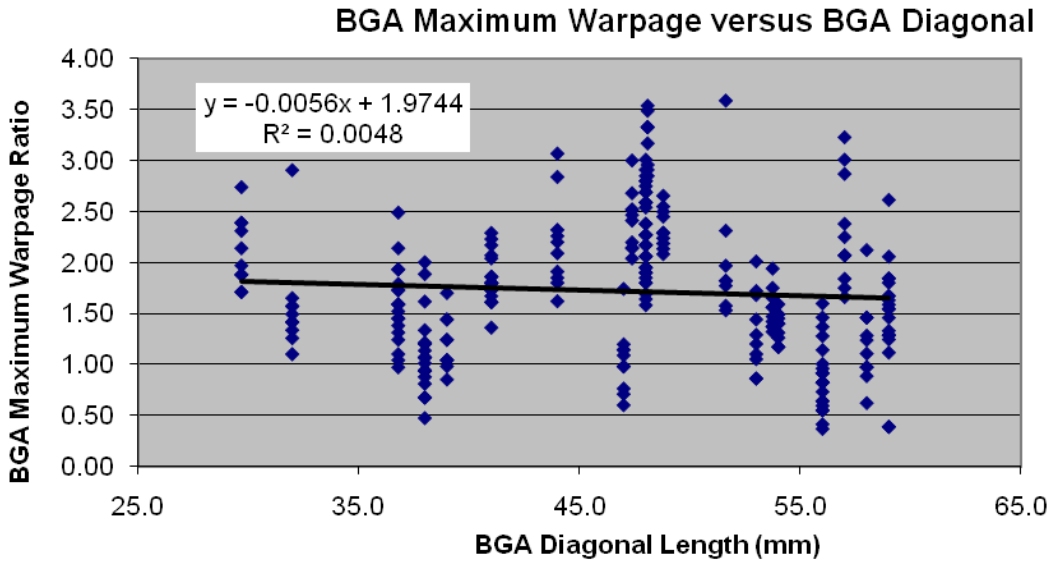


Figure 09: BGA maximum Warpage as a function of BGA diagonal length

Temperature of Max Deformation:

The Max deformation did not always occur at the highest temperature or at any one temperature for all the lots/market sectors. Figure 10 shows that each market sector had a distinct signature at which temperature the maximum deformation/warpage occurred. It should be noted that the slight skew of the Notebook (NB) data was caused by truncating the data at 180°C. The Global and the BGA areas do not always experience the max deformation at the same temperature. Therefore taking measurements at only two temperatures could miss the maximum coplanarity for that design/board. It is recommended to run the entire temperature range from Tg to solidus to capture the maximum coplanarity value.

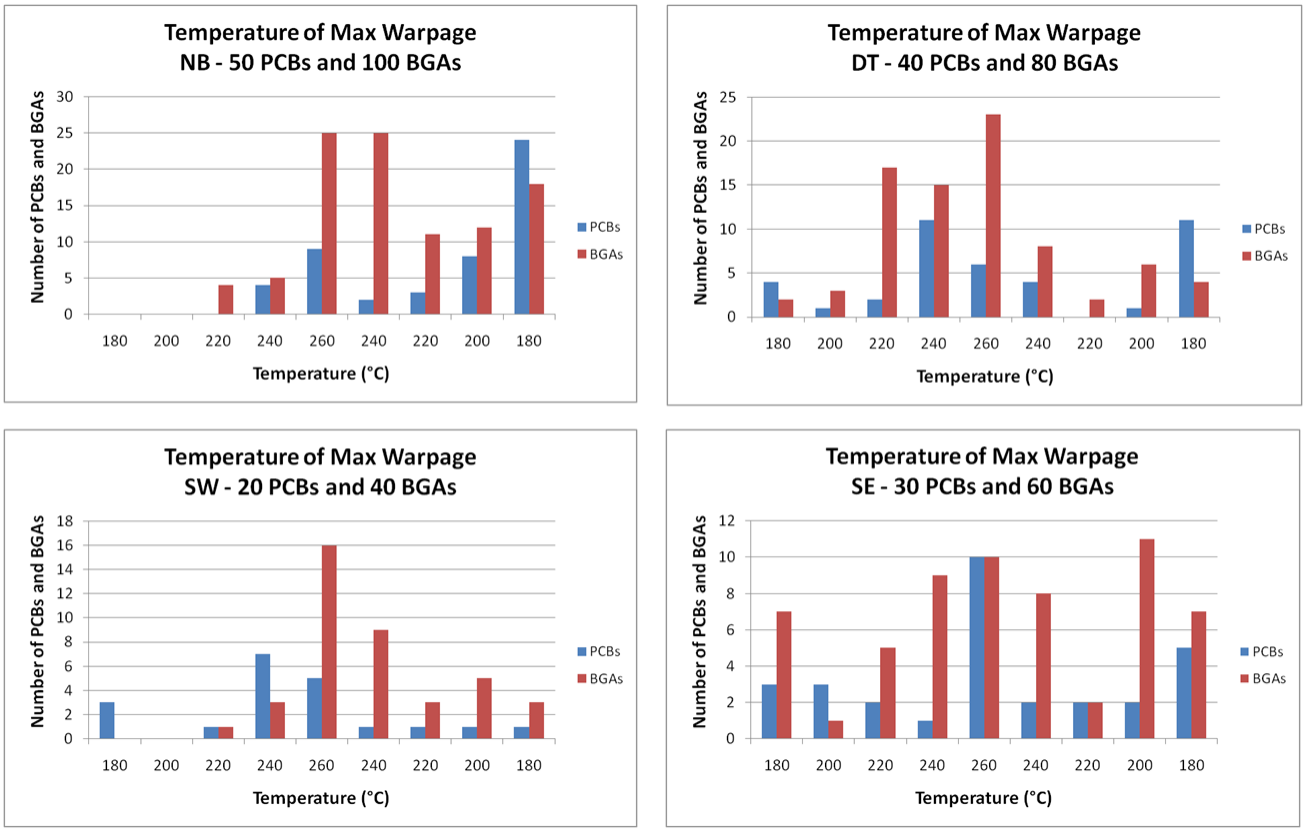


Figure 10: Temperature of Maximum Warpage for the four market Sectors

CONCLUSIONS

Test Method:
Shadow Moiré is a viable test methodology for determining coplanarity values at elevated temperatures.

The heating and cooling rates do not greatly affect the coplanarity values within the heating rates used in this evaluation.

Using a soak cycle did not significantly improve or change the coplanarity value for any specific temperature.

Outgassing of the PCB can occur at elevated temperatures that can affect the ability to measure the PCB. Multiple PCB's are required to get an average value that mitigates the loss of any individual PCB or temperature range.

Simulating the planned assembly set-up/reflow carrier is necessary to get a valid coplanarity value that is useful for the assembly operation. The use of rails during measurements can introduce sag into the PCB and using a full PCB support /pallet can reduce the sag but may introduce a non real situation or coplanarity value. The use of pallets or rails must be agreed upon by the PCB fabricator and the assembly house.

Data Analysis:
Multiple thermal passes resulted in a reduced coplanarity value with each pass, especially during the first three passes.

Thinner PCB's have higher warpage or coplanarity values than thicker PCB's. This may be an artifact of gravitational sag caused by the use of rails on thin PCB's.

Design of the PCB/BGA area appears to be the largest factor in coplanarity within a market sector. Thickness and layer count are less important, except for their design/copper distribution effects.

There is no obvious trend of increasing coplanarity ratio with increased BGA size for any of the market sectors, and there are always outliers. The ability to predict one BGA's coplanarity using another BGA of a different size is difficult.

The maximum warpage did not always occur at the maximum temperature and the temperature for maximum warpage for the BGA and Global PCB did not always occur at the same temperature.

RECOMMENDATIONS FOR SMT ASSEMBLY

Warpage/Coplanarity Characterization Process:
A statistically valid characterization study of dynamic coplanarity should be performed on each BGA/local area of interest for each new design including the temperature range from the laminate transition temperature (Tg) up to the peak assembly temperature and cooled to the solder solidus temperature in increments of 20°C to capture all movement of the BGA/Global areas during the critical times.

Once the characterization study has been completed, measurements of a sample size from each lot's BGA Room Temperature value can be used to predict the Maximum Coplanarity value for that design/lot using this calculated Max/RT ratio.

Coplanarity measurements need to be done within the BGA land area/local areas of interest. It is much harder to predict the effect on coplanarity of the BGA from the Global values.

PCB Warpage/Coplanarity specifications should include both 'Room Temperature Global' and an Elevated Temperature 'BGA Land Area/Local Area of Interest' limits and/or requirements.

Test Conditions:
A slower cycle including soak time is not required for valid measurements, ramping the heating cycle at 0.3°C/sec can accomplish a simulated assembly profile.

All data collection needs to be done on fresh (non-thermal cycled) boards due to the change in coplanarity values brought by each thermal cycle. This will assure the worst case data. Pre-baking to remove warpage-affecting moisture is required.

All Dynamic Elevated Temperature measurements should use the support system (rails or pallets/jigs) based on the method of SMT assembly being used for the PCB. Using a support system like the UAS system developed by Akrometrix is recommended for thin PCB's

Any specification using dynamic elevated temperature will have to address the amount of data loss due to outgassing which would make the reading at that temperature invalid. Averaging over several boards helps with this analysis but can skew the data if too much data is lost with the lot.

Dynamic Warpage Methodology Recommendation:
OEM/ODM/Board Design Owner characterizes the PCB design dynamically using the Warpage/Coplanarity Characterization Process. NOTE: This may require a design modification if the Maximum Coplanarity exceeds the allowed specification value.

OEM/ODM calculates the Max/RT ratio for use in setting the Room Temperature Coplanarity Ratio value

In lieu of any Industry specification the ODM/EMS/CMS/SMT Assembler jointly can set a Room Temperature specification for each design from the characterization study. This specification may need to be component specific based (family of parts/components) since the coplanarity requirements maybe vary with BGA package/size/technology level.

PCB supplier will measure each lot at Room Temperature (a statistically valid sample size) and report on the Certificate of Conformance (COC).

Recommended Next Steps
The WG recommends that IPC reviews the Warp & Twist and Bow specification and establishes a Dynamic Coplanarity Ratio for the BGA area or Local area of interest.

The WG recommends that IPC reviews the test methodology for the Warp & Twist and Bow test method and develop one that includes the BGA or Local area of interest.

The WG recommends that IPC and JEDEC form a joint evaluation WG to analyze the Dynamic Coplanarity specification and jointly set the requirements for board and package. Using iNEMI and other consortia data would be advantageous.

The WG recommends a study of the influence of PCB Fabricator on any single design be untaken to quantify the effects of PCB Fabrication/Processes.

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AN iNEMI INVESTIGATION INTO THE PREDICTABILITY OF PCB COPLANARITY FOR ROOM VS. LF ASSEMBLY TEMPERATURES

John Davignon, iNEMI Chair
Intel Corporation

Ken Chiavone and Jiahui Pan
Akrometrix

James Henzi
Cisco Systems, Inc.

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Agenda

- Introduction
- Drivers
- Baseline Level Setting:
  - Test Methodology Procedure
  - Thermal Profile and Heat up Rate
  - Multi-Cycle measurements
  - Gravitational Sag
  - Outgassing Issue
  - Coplanarity Ratio System
- Results of Project
  - Global Vs. Location of Interest
  - Room Temperature to Maximum Coplanarity
  - Relationship of BGA Size to Coplanarity
  - Temperature of Maximum Deformation
- Conclusions
- Recommendations
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  - Industry
- Proposed Dynamic Coplanarity Methodology

This presentation will cover the items in RED. The full report is in your proceedings

Introduction

iNEMI SMT Coplanarity project was to develop metrologies and recommendations to enable the measurement and specification for board land coplanarity.

Drivers:

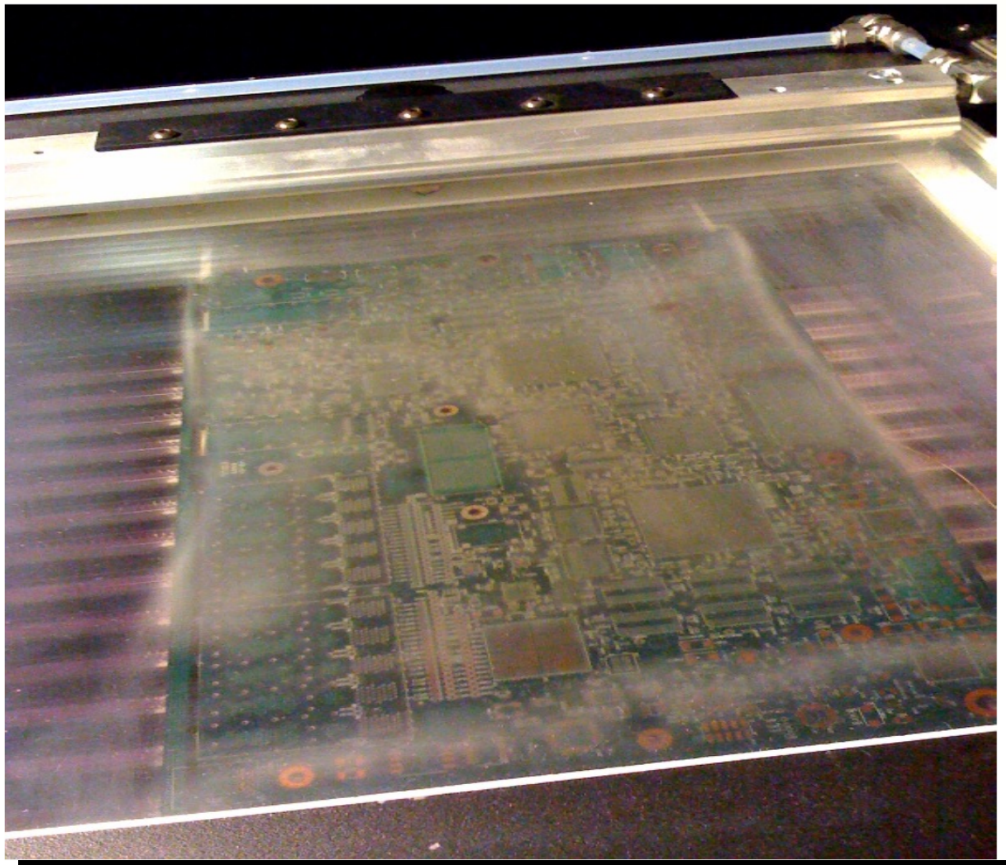
- **The current specifications for board bow and twist have not kept pace with the developments in packaging and board technology.**

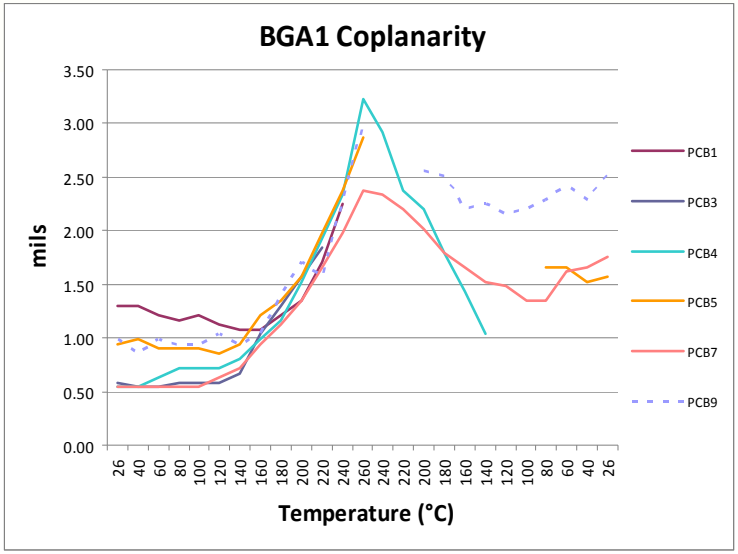
- **Several Standards bodies have already issued standards using new measurement techniques for components. Can these be extended to system boards as well.**

Industry Snapshot Market Sectors Evaluated

Market Sector	Server	Workstation	Desktop	Notebook
Thickness	.093"-.135"	.062"-.093"	.062"	.040"-.062"
Layers	14 - 32	8 - 12	4 - 6	6 - 10

Outgassing of PCB's

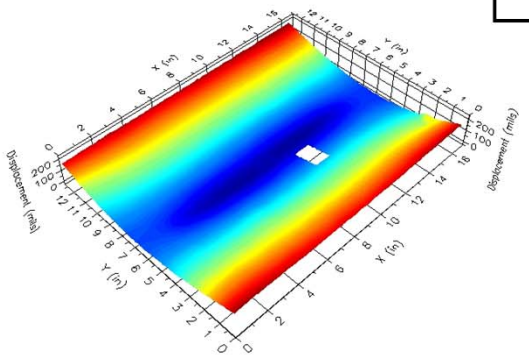




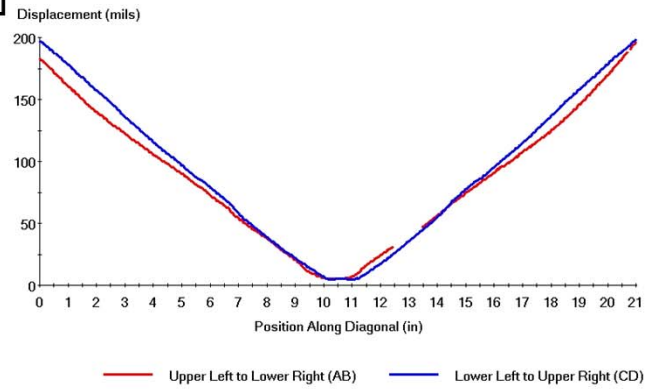
Overcome by averaging over a lot, needs investigation

Gravitational Sag

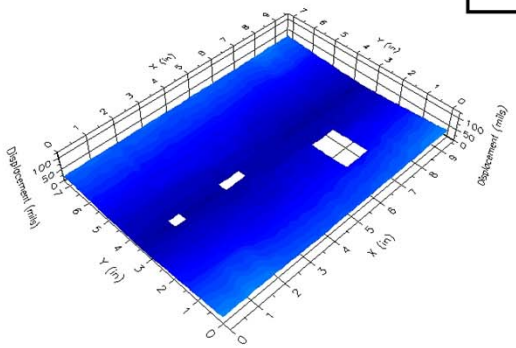
2 up panel



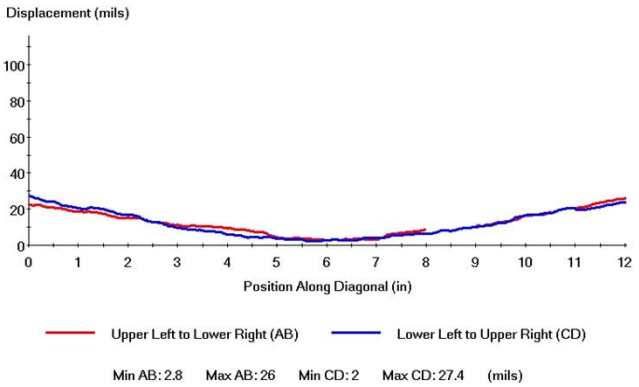
Coplanarity = 200.0 mils



Half panel



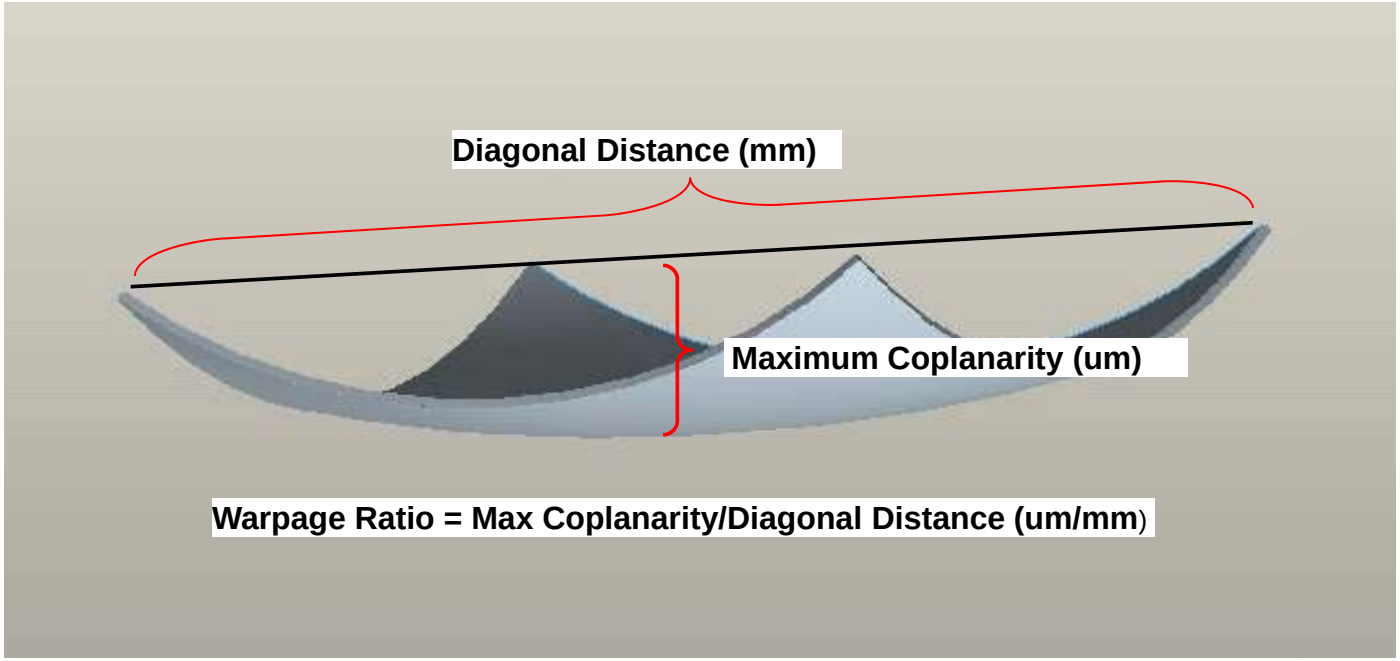
Coplanarity = 27.4 mils



Min AB: 2.8 Max AB: 26 Min CD: 2 Max CD: 27.4 (mils)

Support or not to support that is the question

Coplanarity Ratio System



Example of Coplanarity Ratio:

$$1000\ \text{um} \ / \sqrt{150^{2} + 200^{2}}\,\text{mm} = 1000 \ / 250 (= 4\ um \ / \ mm)$$

$$200\ \text{um} \ / \sqrt{30^{2} + 40^{2}}\,\text{mm} = 200 \ / 50 \ (= 4\ um \ / \ mm)$$

This ratio allows for direct comparison of many sizes of BGA & PCB's

Correlation of Global Vs. BGA

Average Coplanarity Ratio *(Means + 3 Sigma)*

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
Notebook Sector	**1.64**	**3.78**	**7.22**	**24.03**
SNB0210	2.13	4.75	5.49	17.74
SNB0310	1.23	2.99	6.96	23.35
TNB0110	1.54	3.11	6.81	12.67
VNB0110	1.74	3.35	7.80	11.37
VNB0210	1.74	2.48	6.14	8.86

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
Desktop Sector	**1.79**	**3.75**	**5.77**	**10.52**
ADT0110	1.39	3.75	3.90	5.80
EDT0110	1.87	3.40	4.17	7.54
NDT0110	1.89	3.69	7.57	13.71
TDT0110	1.38	1.96	4.52	6.94

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
HE Server Sector	**1.81**	**2.62**	**2.30**	**3.96**
HSE0110	2.18	2.81	1.05	2.00
CSE0210	1.18	2.06	1.17	2.14
CSE0110	1.81	2.64	1.42	2.12

Average Warpage Ratio in um/mm	BGA		Global	
	RT	Maximum	RT	Maximum
WS Server Sector	**1.80**	**3.48**	**1.92**	**3.98**
CSW0205	1.92	2.37	1.61	1.88
CSW0305	0.85	1.50	1.93	3.86

There is less variability between the market sectors average BGA coplanarity.

iNEMI SMT Coplanarity WG

Correlation of Room Temperature to Max Coplanarity Ratio *(means + 3 Sigma)*

Average Warpage Ratio in um/mm	BGA Max/RT		Global Max/RT	
Notebook Sector	**2.30**		**3.33**	
SNB0210	2.23		3.23	
SNB0310	2.44		3.35	
TNB0110	2.02		1.86	
VNB0110	1.92		1.46	
VNB0210	1.43		1.44	

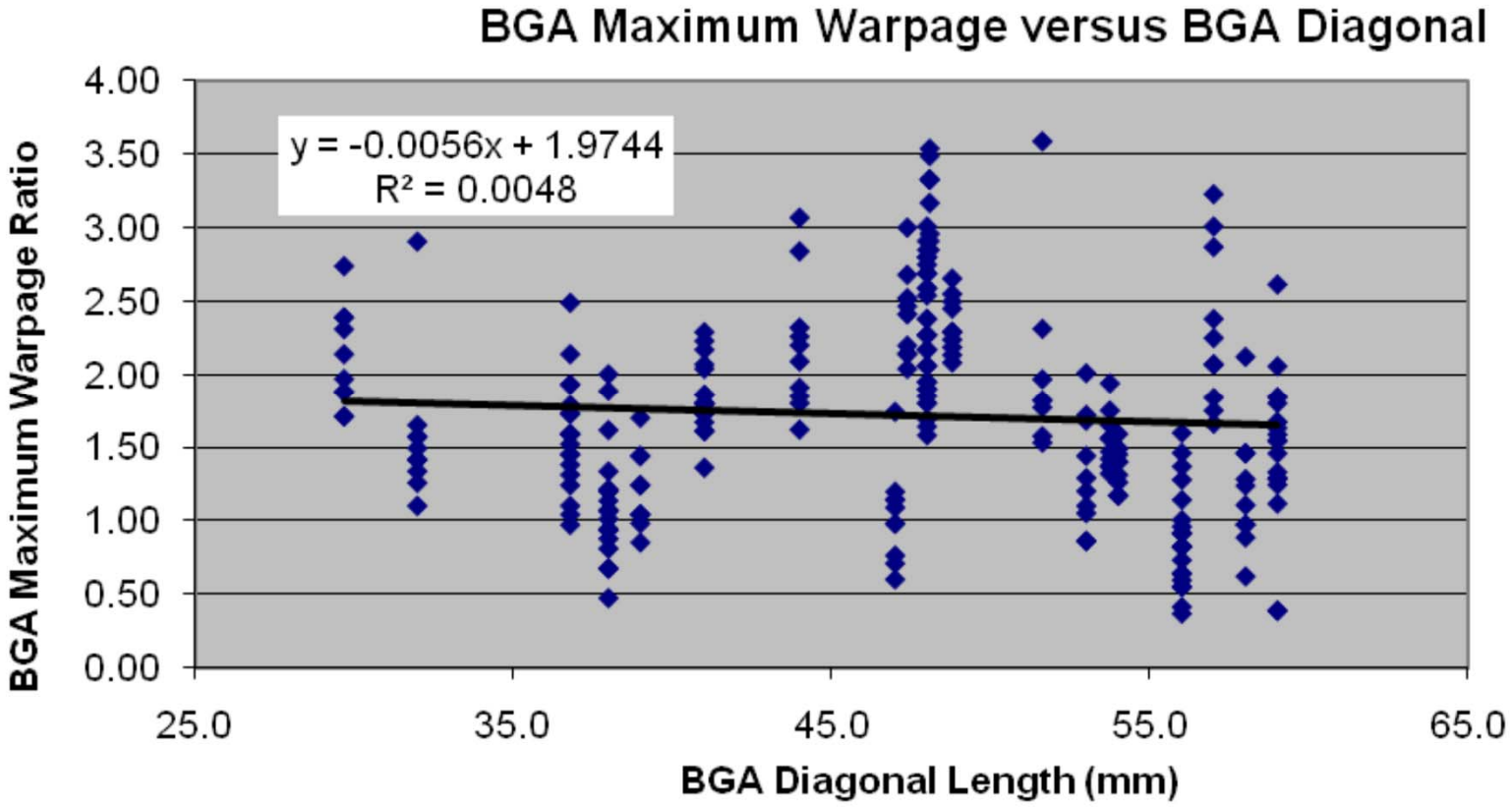
Average Warpage Ratio in um/mm	BGA Max/RT		Global Max/RT	
Desktop Sector	**2.09**		**1.82**	
ADT0110	2.69		1.49	
EDT0110	1.82		1.81	
NDT0110	1.95		1.81	
TDT0110	1.42		1.53	

Average Warpage Ratio in um/mm	BGA Max/RT		Global Max/RT	
HE Server Sector	**1.44**		**1.72**	
HSE0110	1.29		1.90	
CSE0210	1.74		1.83	
CSE0110	1.46		1.49	

Average Warpage Ratio in um/mm	BGA Max/RT		Global Max/RT	
WS Server Sector	**1.94**		**2.07**	
CSW0205	1.23		1.16	
CSW0305	1.76		2.00	

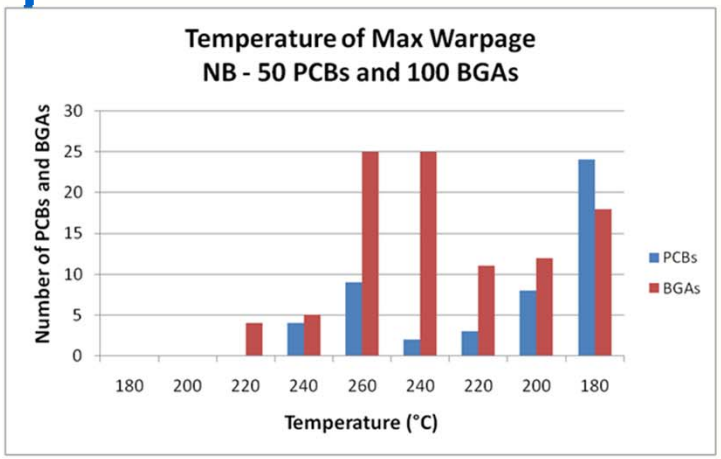
Variation within a Market Sector, Design Related?

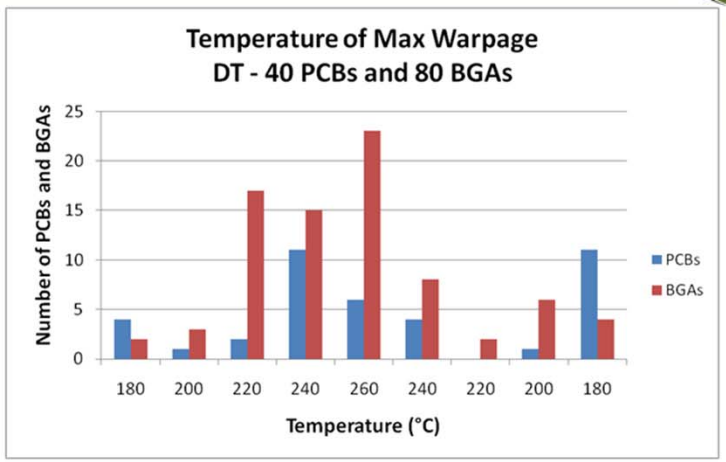
Correlation of BGA size to Coplanarity

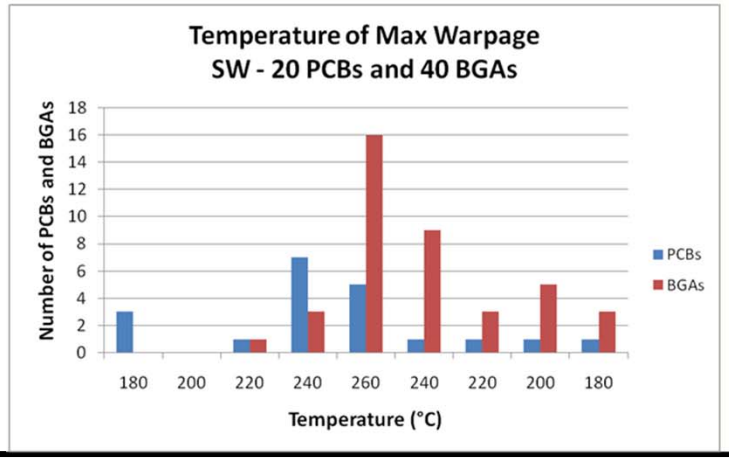


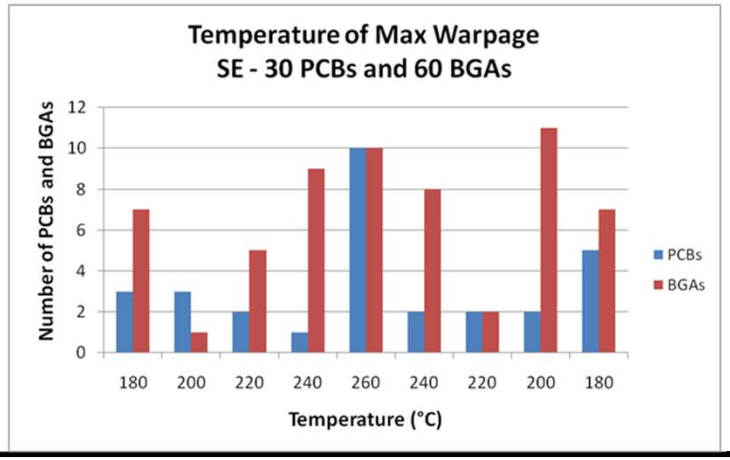
It would be difficult to use one BGA coplanarity to predict the coplanarity of another BGA size

Temperature of Maximum Deformation









The Max deformation did not always occur at the highest temperature nor at any one temperature

Conclusions

- Shadow Moiré is a viable test methodology for determining dynamic coplanarity values
- The Coplanarity Ratio will facilitate comparison and specifications
- The Coplanarity of the BGA area has less variability between market sectors than the Global Coplanarity
- Max to Room Temp coplanarity relationship can be calculated (Dynamic Coplanarity Methodology)

Conclusions (cont)

- No apparent trend in coplanarity ratio with increased BGA size
- PCB/BGA area design may be a large factor in BGA coplanarity
- The maximum warpage did not always occur at the maximum temperature or the same temperature for the BGA and PCB

Industry Recommendations

- The WG recommends that IPC establishes a Dynamic Coplanarity Ratio Test Method for the BGA area

- The WG recommends that IPC and JEDEC form a joint evaluation WG to analyze the Dynamic Coplanarity specification and jointly set the requirements for board and package.

Proposed Dynamic Coplanarity Method

- OEM/ODM Characterizes the PCB design dynamically across the full assembly temperature range. Include BGA areas
- OEM/ODM calculates the Max/RT ratio for use in setting the Room Temperature coplanarity value
- OEM/ODM/PCB Assembler jointly set a Room Temperature specification for each design using the Max/RT ratio. NOTE: This specification may need to be component specific.
- PCB supplier will measure each lot at Room Temperature (a statistically valid sample size) and report value on the Certificate of Conformance (COC).

Acknowledgements

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Thank You!

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