IPC Workshop on Head-in-Pillow Defects
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Topic 1: Introduction to Head-in-Pillow Defects

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Objective: What you will learn in this module?

UWhat is a Head-in-Pillow Defect?

UWhy are they a concern for OEMs and EMS companies?

UWhat is the mechanism for formation of HiP defects?

UWhat are the factors that cause HiP?

UWhat are the inspection tools to detect HiP?

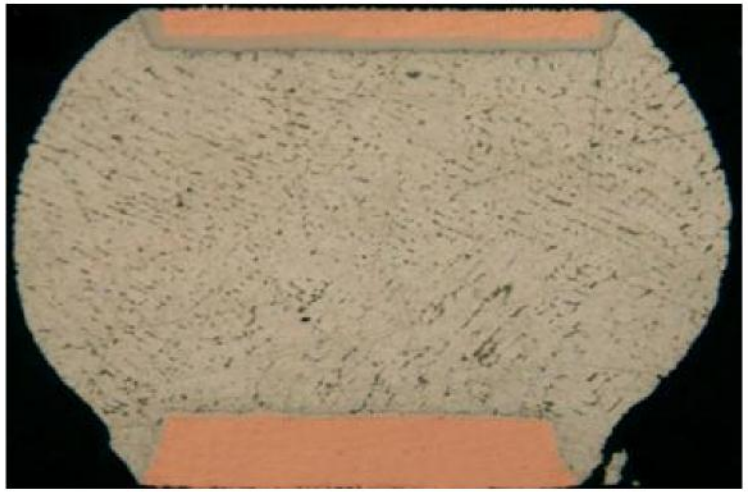
UHow can we prevent or mitigate HiP?

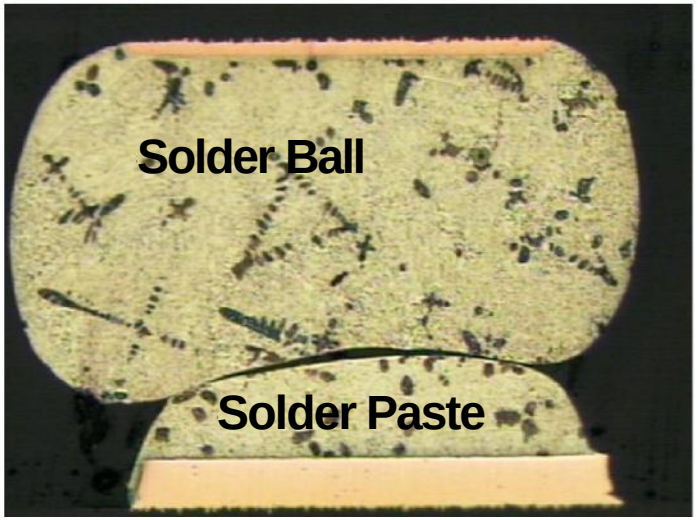
UWhat are the test methodologies to evaluate solder pastes for mitigating HiP defects?

UHiP case study.

Head in Pillow (HiP) Joint

- Definition: Non-coalescence (Non wetting) between the solder ball and the solder paste during reflow process.
  - Also referred to as “Ball and Socket" defect or „Head on Pillow Defect”.
  - Not an „open“ joint as there is weak intermittent contact.
  - Occurs mostly on corner balls at low DPMO.



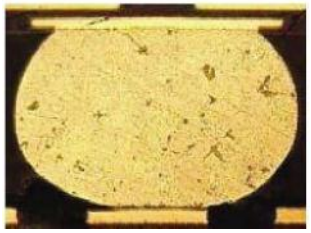


X-Section of a Good Joint X-Section of a HiP Joint

Why HiP is a Concern?

UWhich defect is worse?

- „Open" or HiP Joints?



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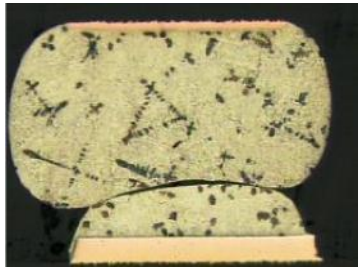
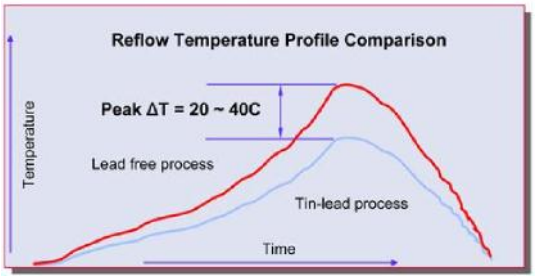


UHiP are very difficult to detect

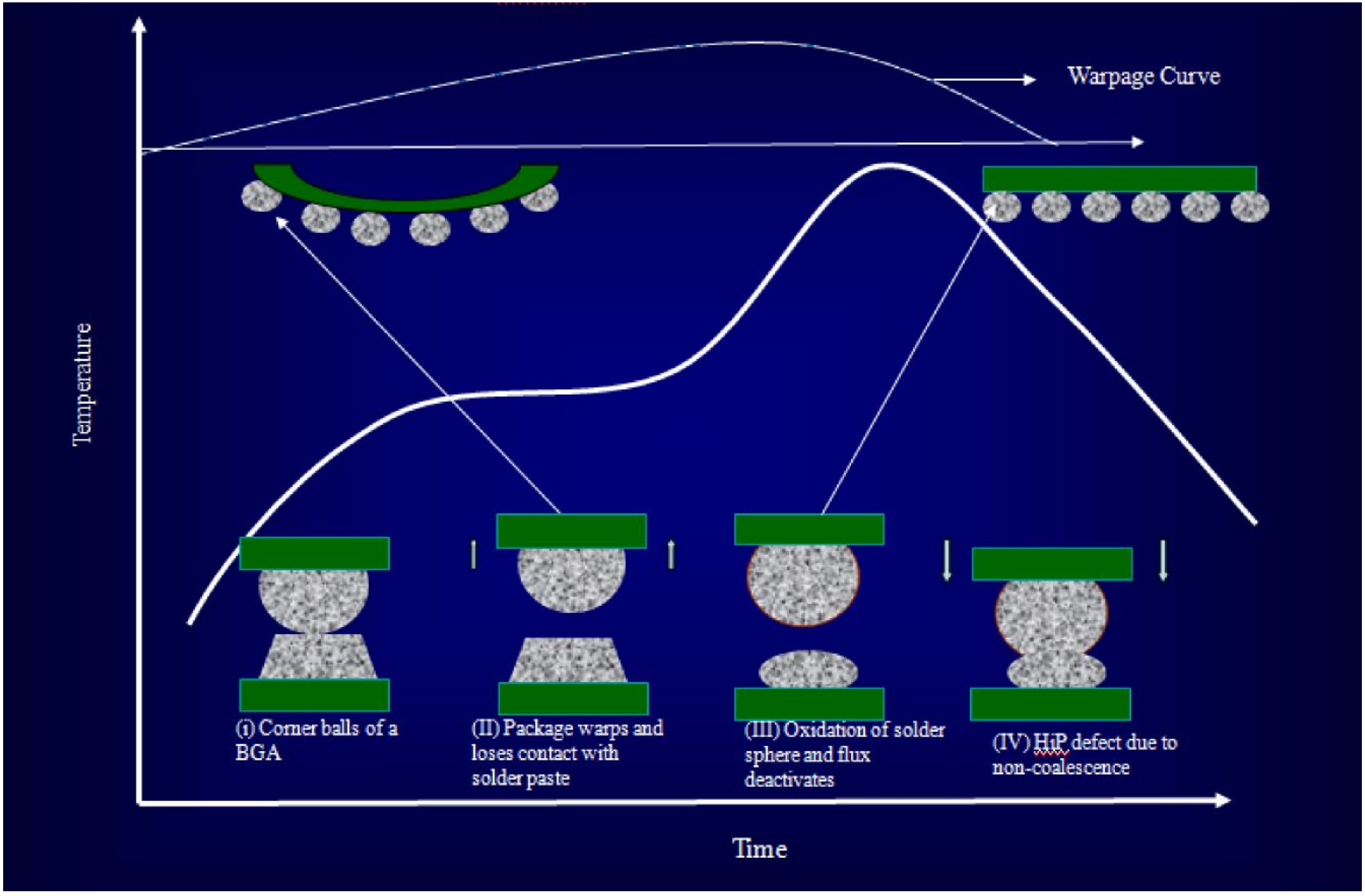
- Escape electrical inspection.
- Shows as infant failures after shipped to customers.

UIncidence rates more in Pb-free assembly.

- Higher temperatures increases warpage
- Increased oxidation due to more Sn content of SAC



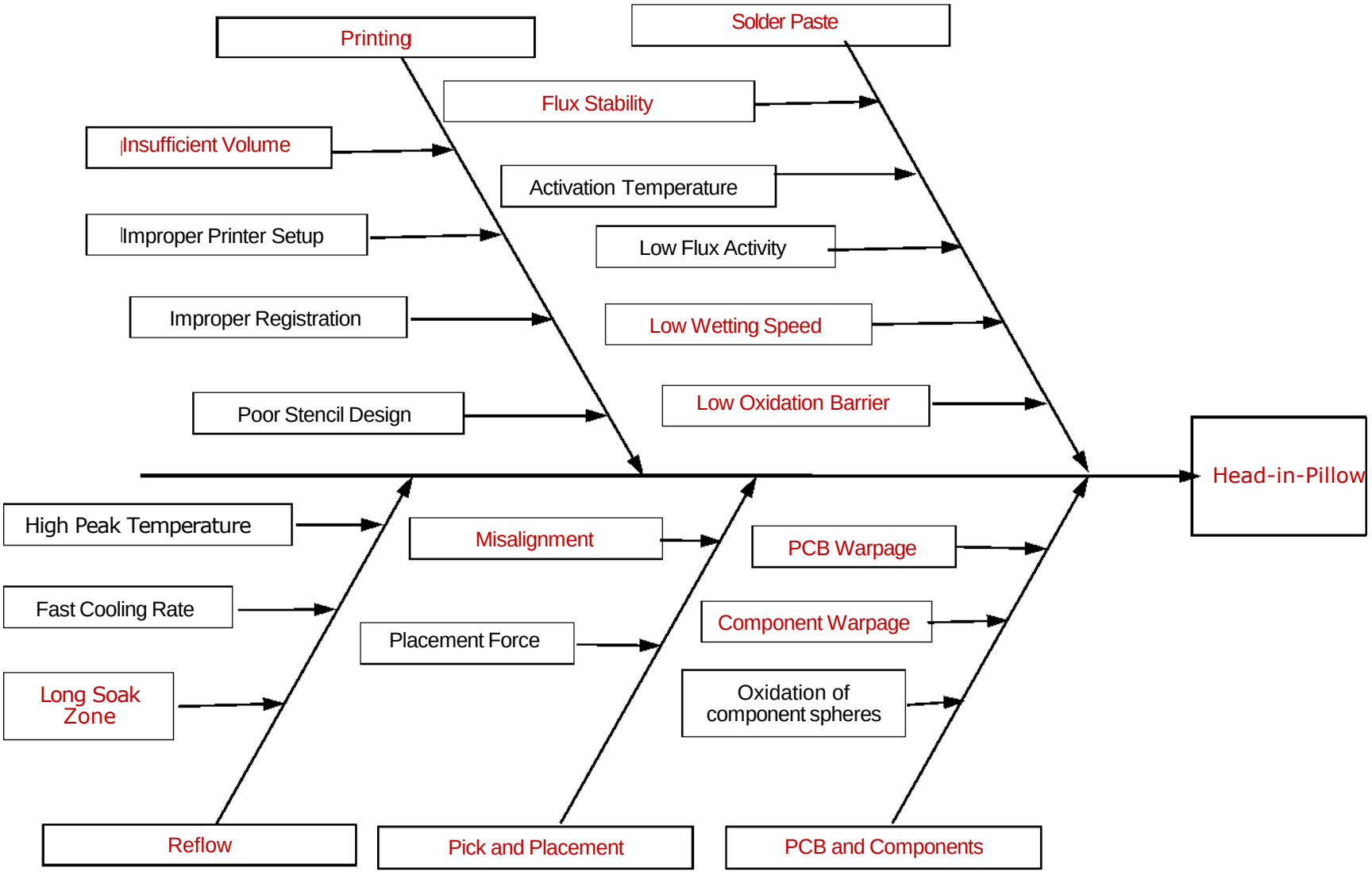
HiP Mechanism



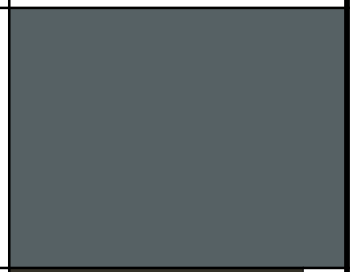
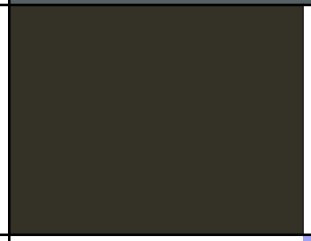
Necessary Conditions for HiP Defect

- Warpage must occur during reflow process.
- The ball has to reestablish contact again with the solder paste.
- Flux must be inactive or exhausted when solder ball makes contact with solder paste again.

Fishbone Diagram

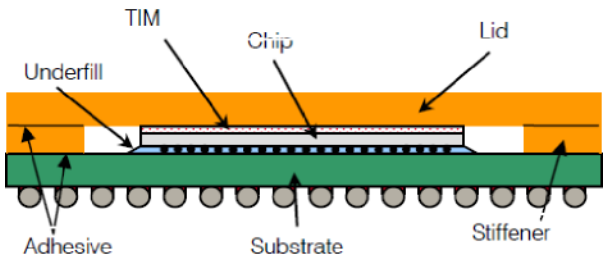


HiP in Packages

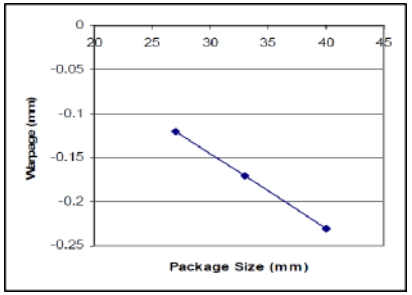
Type of Package	IOs	Pitch (mm)	Size	DPMO Rate	HiP Image
Flip Chip Plastic BGA	948	1	40 X 40	-	
Flip Chip Plastic BGA. Max warpage 12 mils	748	1	35 X 35	3273	
Connector BGA, 10 row	300	0.88		-	
DRAM Flip Chip BGA	144	0.8	18.5 X 11	16913	

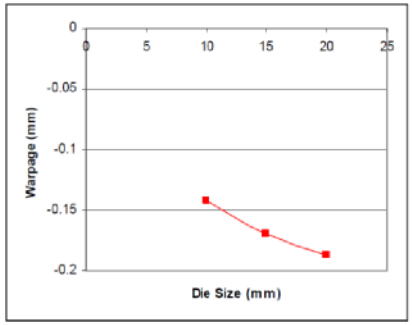
Primary Factor: Warpage

- Warpage is the primary factor for causing HiP defect. It lifts the balls causing oxidation.
  - Package warpage caused due to CTE mismatch between substrate (16-18 ppm/ C) and silicon (3 ppm/ C).
- Timing of warpage
  - How much warpage and when does it occur?
  - When / or does the package flatten out and make contact with the molten solder paste on the PCB pad.
  - At the time of contact how active is the flux?



- Attributes affecting warpage.
  - Package Construction
    - Package size: Larger packages will have more warpage.
    - Package type :Flip chip package warps more than wirebond
    - Die size: Large die size will cause more warpage





Primary Factor: Warpage

Package Construction

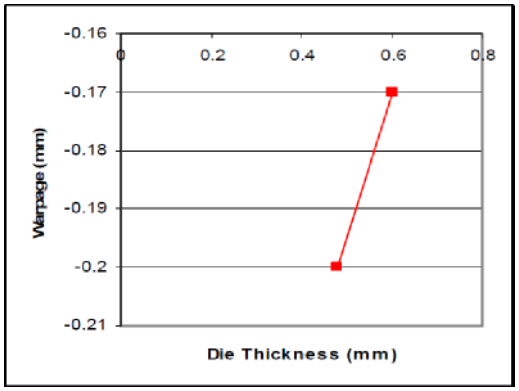
- Die thickness : Thicker die reduce warpage
- Substrate layer count: More layers will have larger warpage

Material Properties

- CTE/Modulus/Tg of molding compound and underfill
- CTE/Modulus/Tg of substrate layers
- CTE/Modulus/Tg of die attach

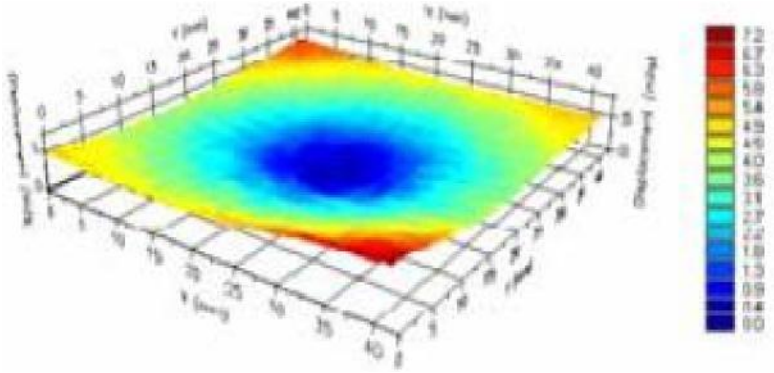
Processing history

- Precondition
- SMT assembly process variations (e.g Peak temperature, heating rate)
- Moisture exposure
- Number of reflows



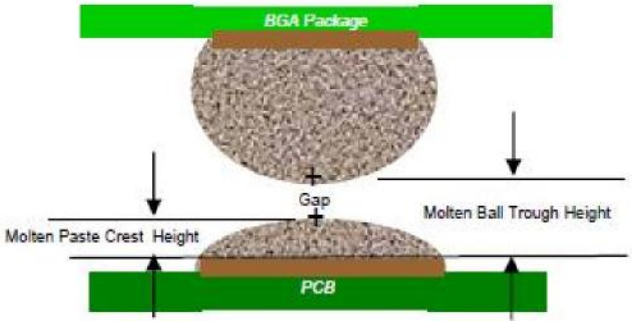
Primary Factor: Warpage

- Shadow Moire Interferometer is used to measure warpage at different points of the reflow process.
- Understanding warpage curve is important for mitigating HiP defects.
  - Flip chip packages usually have a concave shape initially and become convex at high temperature.
  - In these cases, HiP will occur at the corners.
- Timing of warpage is more critical than maximum initial warpage at room temperature.

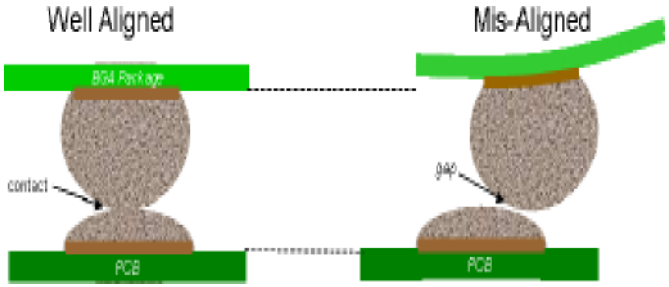


Secondary Factors

- Insufficient solder paste volume at corner balls.
  - – Increasing paste volume at corner balls will increase the likelihood of the solder ball making contact with solder paste.



- Solder ball misalignment
  - Misalignment alone would not cause HiP defects
  - If there is significant warpage coupled with misalignment, a gap can be created between solder ball and solder paste.



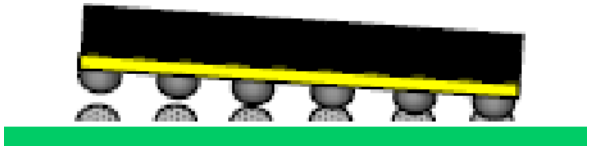
Secondary Factors

UReflow parameters have a big impact on HiP defects

- Delta temperature (difference between hottest and coldest joints) across the package, causes BGA to tilt.
  - Oxidation will occur on the cooler side resulting in HiP defects
  - A ramp to spike profile will increase the temperature difference.

• Low Time Above Liquidus (TAL) will increase HiP defects, since there will be less time for coalescence.

• Very long soak time could consume flux and increase HiP defects



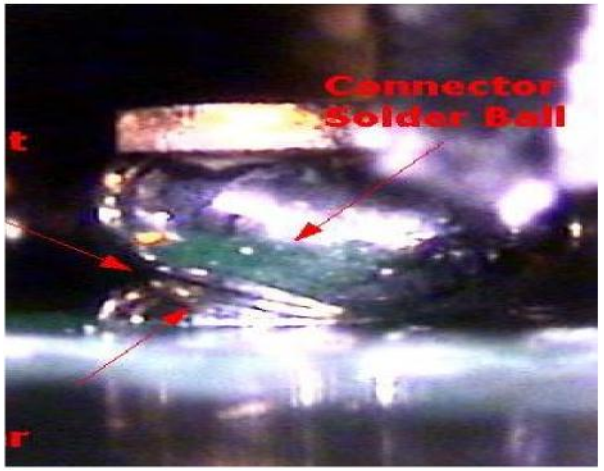
UContamination on the solder ball and the paste

- Contaminants can be oxides, silicon, halides etc.
- Result of process contamination during assembly and package handling.

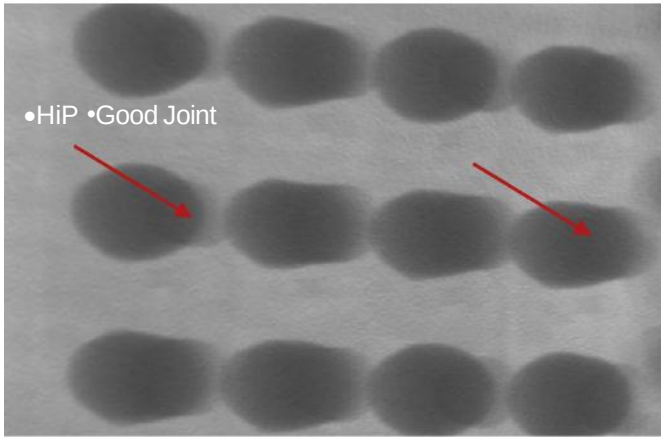
Detection Tools

UOptical side view inspection

- Can only detect corner joints

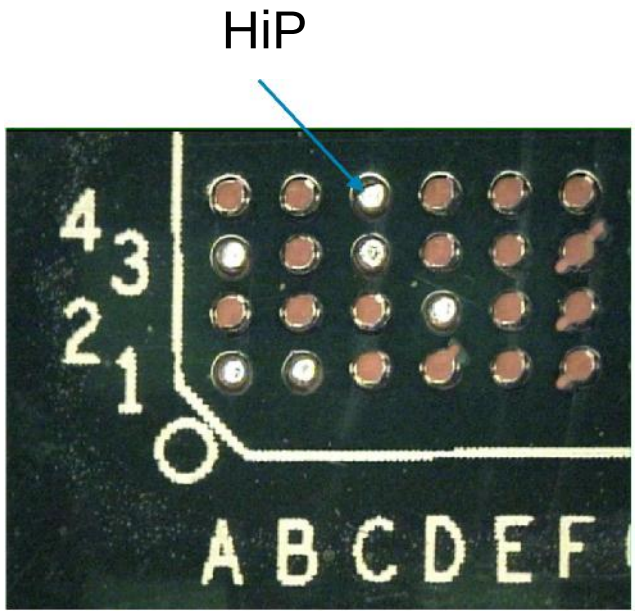


- 2D oblique X-ray inspection
  - HiP joints show as clear separation between ball and paste
  - Very tedious method



Detection Tools

- Pry analysis
  - Destructive method
  - Small BGAs can be pryed using a screw driver.
  - HiP joint break at interface than at pads.



- 5DX Analysis (Foxconn will cover the this in detail in Topic 5)
  - Automated inspection
  - Uses a BGA algorithm technique called “Eclipse Edge Recognition” technique.
  - Algorithm has to be modified based on types of packages
  - Risk of false calls and escapes

Mitigation Strategies

Permanent Solution

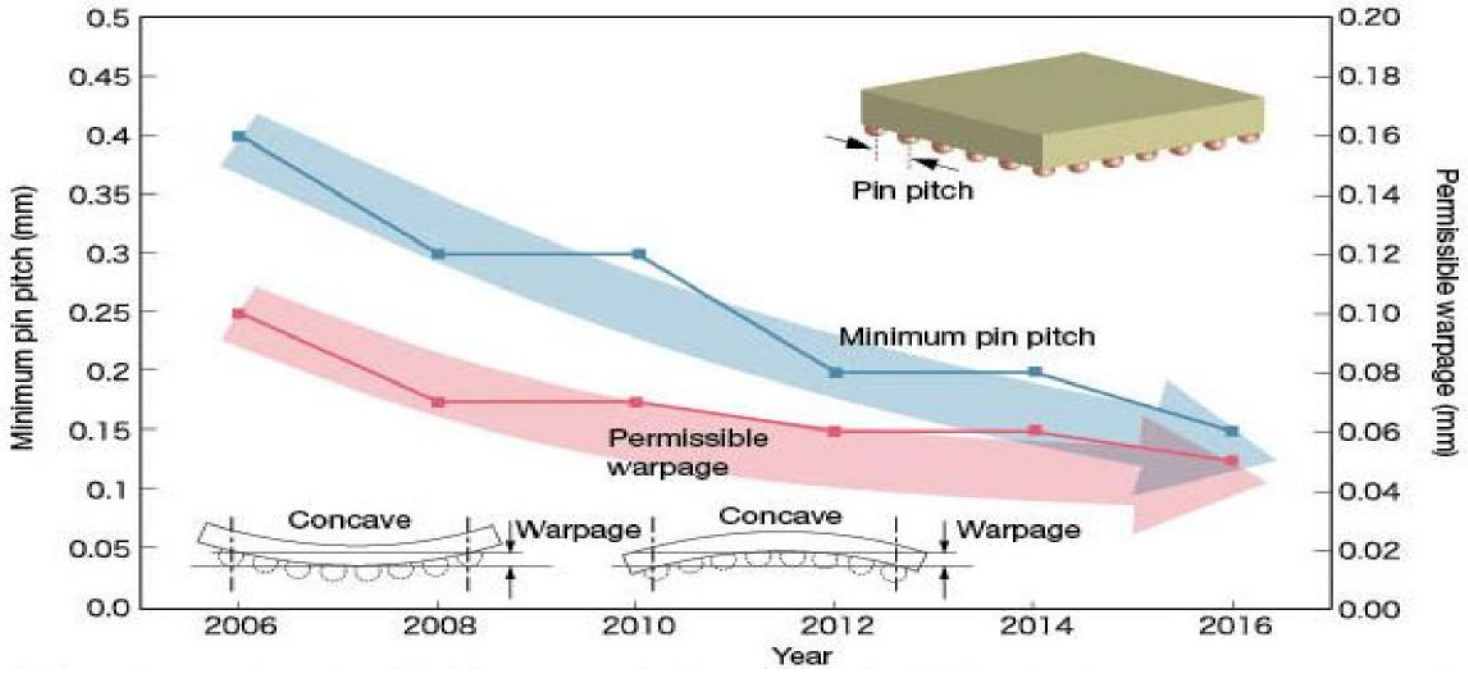
- Eliminating dynamic warpage during reflow process

Temporary Solution

- Solder paste selection
- Flux dipping of components
- Optimizing reflow profile
- Bulls eye stencil

Mitigation Steps

- Reducing dynamic warpage in components
  - Current JEDEC warpage limit is 8 mils. All BGA should packages meet this standard
  - Elimination of warpage is challenging due to material constraints
  - Warpage expected to decrease in next 5 years



Ref: JEITA Roadmap

Mitigation Steps

- Using solder paste with the following properties

Adjustment of flux fluidity to protect solder particles from oxidation.

A flux that can retain its activity for prolonged reflow profiles.

Increased heat resistivity during preheat stage. Solder paste with excellent release characteristics. Flux with shorter wetting time

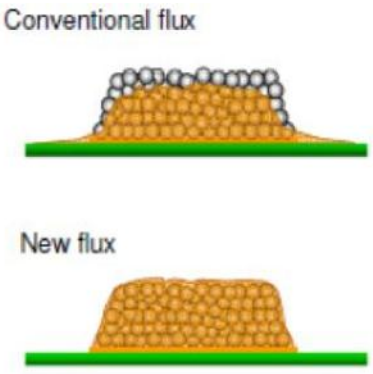
Consistent high print volumes

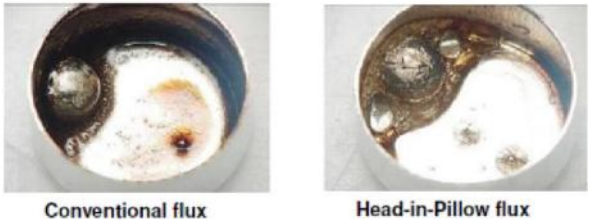
Flux with good stability over time and temperature.

Reduced speed of pad wetting and maximum speed of ball wetting, resulting in rapid ball collapse

Thermally driven activator package to reduce surface oxides during the liquidus phase of reflow

Non eutectic solder pastes with longer pasty region.

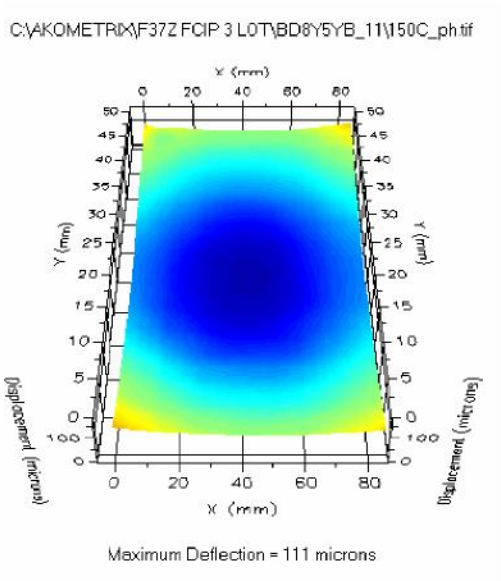


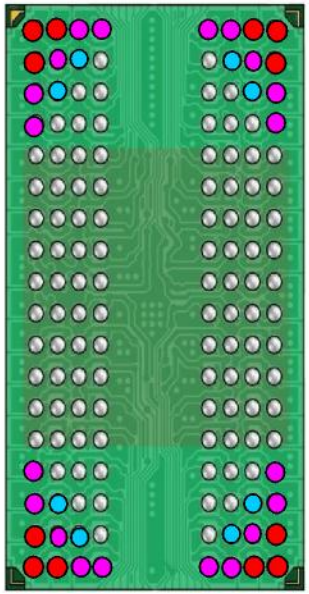


Reference: Bath et.al

Mitigation Steps - Process

- Bulls eye stencil (increase aperture on corner pads)





= Circular 1:1

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= Circular +.002”

= Circular +.003

- Increases chance for bridging.
- Stencil has to be designed specifically for each package.
- Works only if warpage is convex.

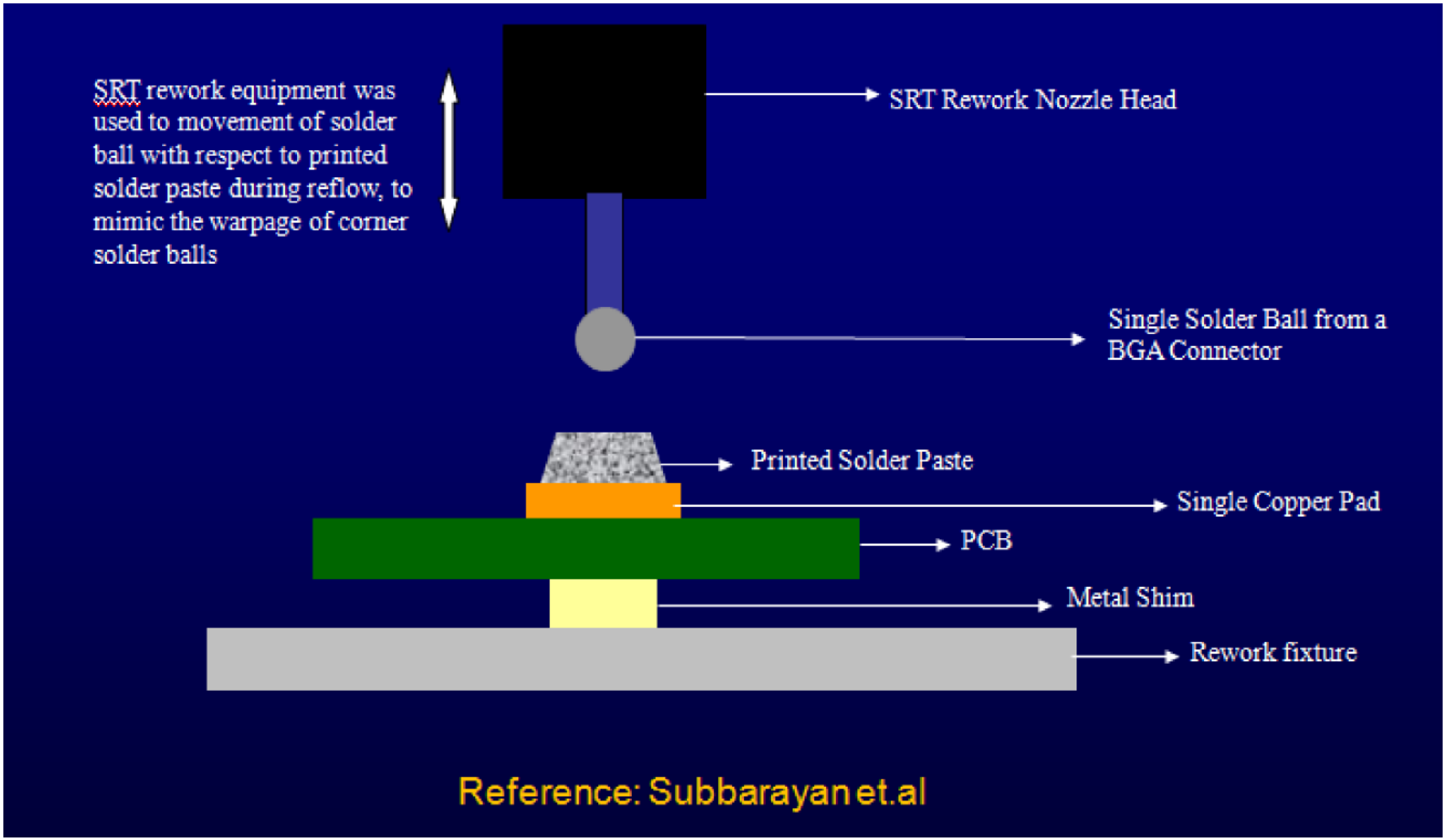
Mitigation Steps - Process

- Reflow Process:
  - Profile which minimizes delta T across the component.
  - A shorter soak time that will minimize flux exhaustion.
- Flux dipping of solder balls.
  - Cumbersome process step
- Using Nitrogen during reflow process will improve wetting and mitigate HiP defects.

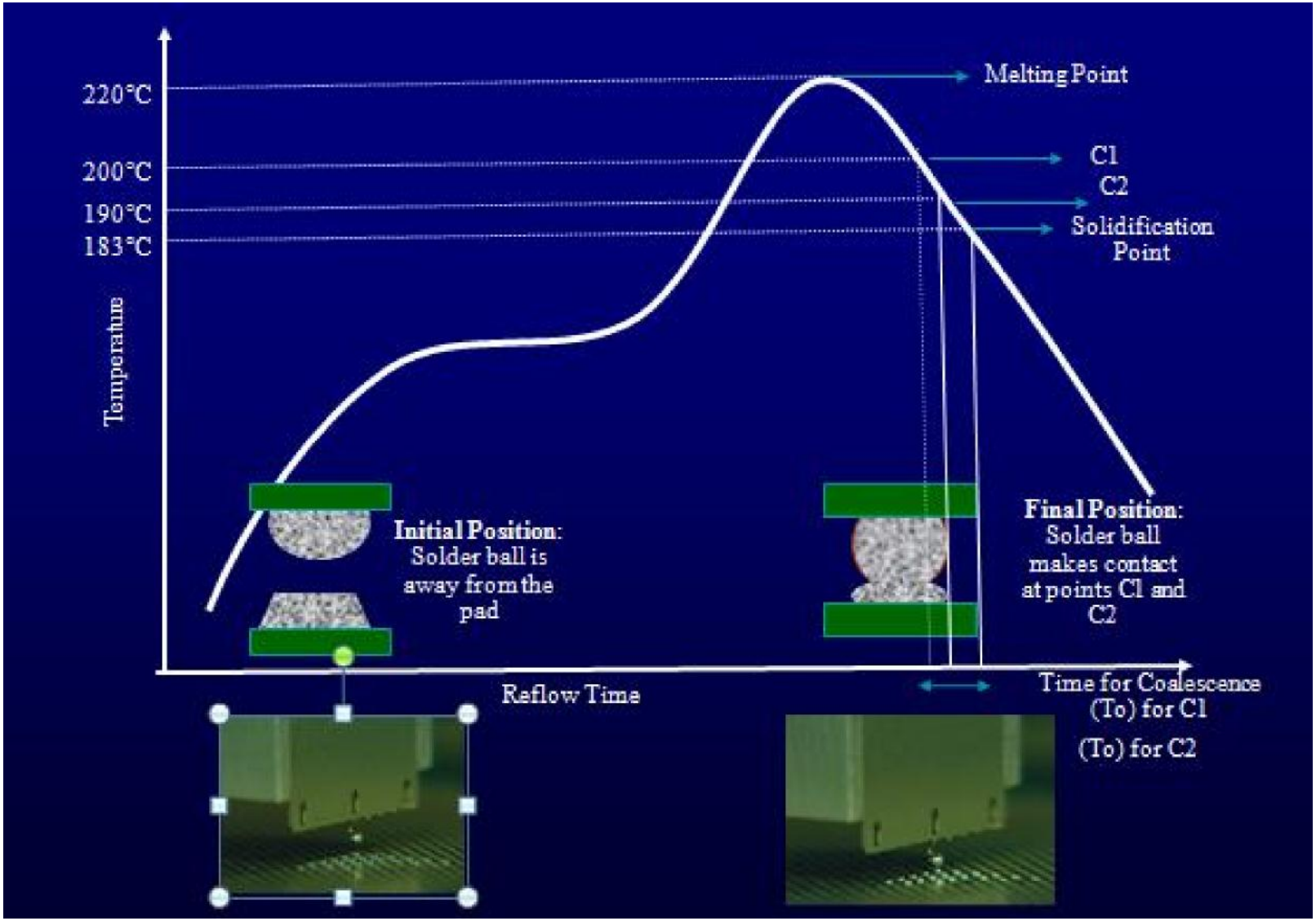
Test Methodologies to Evaluate Solder Pastes

- A Design of Experiment on a TV with packages that has a known history of HiP defects.
  - –Since HiP occurs in low DPMO, this method will require large sample size and resources.
- Koki test method on ball spheres.
  - –Quick method but doesn‟t exactly replicate the actual HiP condition.
- Cisco-Jabil Test Method (Topic 2 and Topic 3 will cover this in detail)
  - –BGA rework equipment was used to place a solder ball on a pad.
  - –Gap between solder ball and gap was controlled to mimic the warpage of corner balls during reflow process.
- Senju Wetting Balance method (Topic 4 will cover this in detail)

Cisco Jabil Test Method

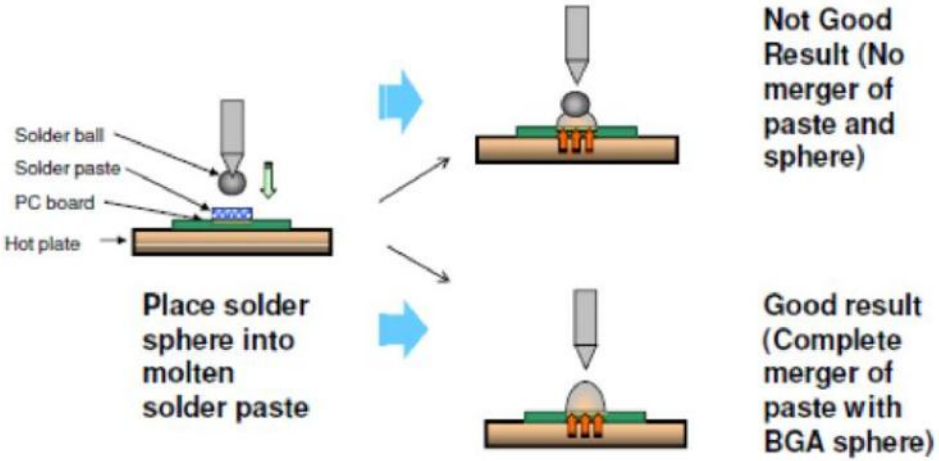


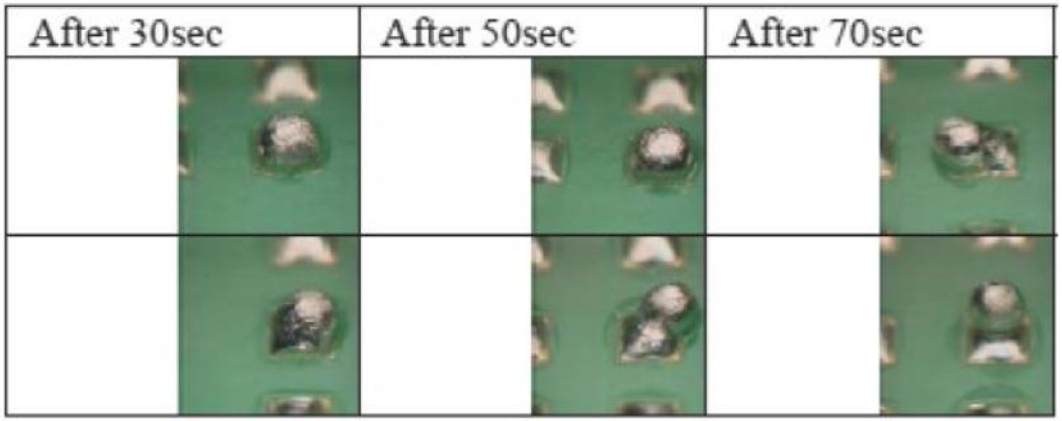
Cisco Jabil Test Method Conditions



Koki Test Method

- USolder paste printed and melted.
- UBalls placed at different intervals during reflow

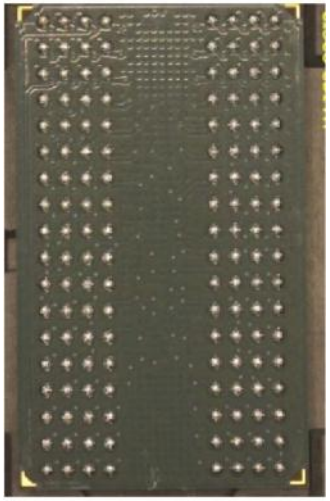




Reference: Jasbir et.al

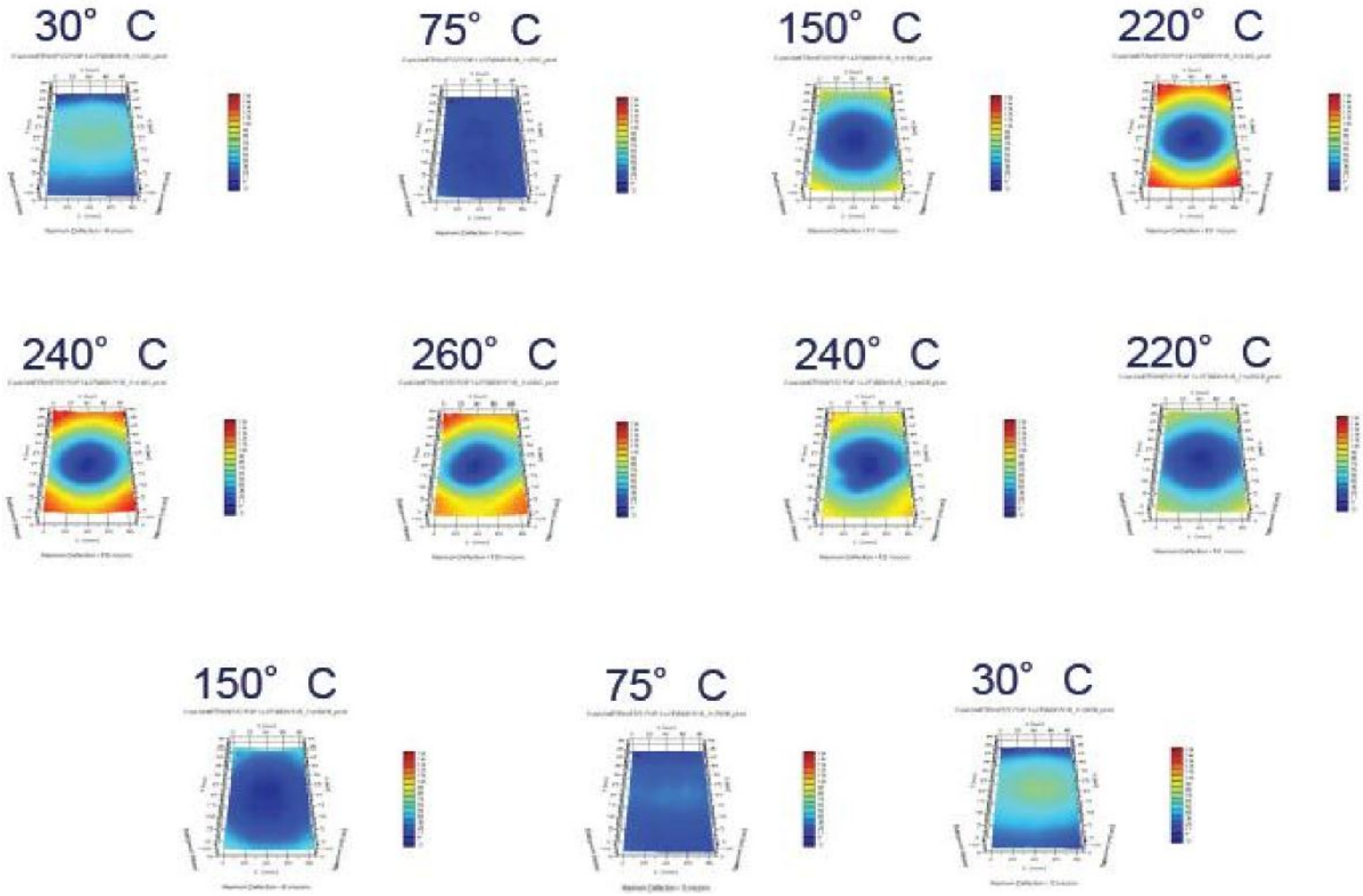
Case Study - FBGA144

- Package type: DRAM, Thin Flip Chip BGA
- Root Cause: RLDRAM warpage
- Number of IOs: 144
- Pitch: 0.8 mm
- Observations:
  - HiP defects not limited to corners



Temperature (°C)	Min	Max	Coplanarity (mils)
26 Initial	-2.5	1.5	4
150 Heating	-0.6	1.6	2.1
170 Heating	-1	1.9	2.9
183 Heating	-1.2	2.2	3.4
200 Heating	-1.4	2.4	3.8
220 Maximum	-2.1	3	5.1
200 Cooling	-1.6	2.4	4
183 Cooling	-1.3	2	3.4
170 Cooling	-1.1	1.8	2.9
26 Final	-2.7	1.5	4.2

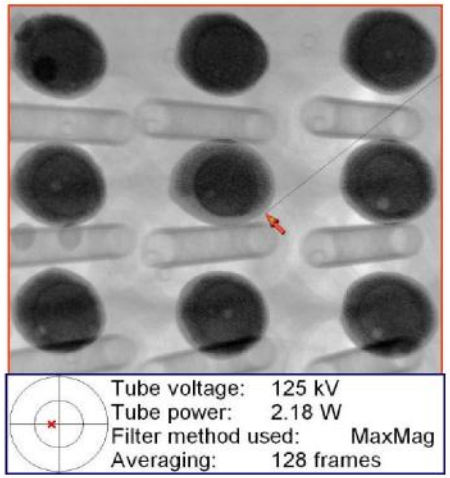
Shadow Moiré Analysis

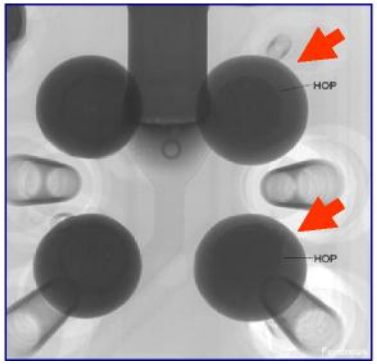


X-Ray Failing Signatures

Signature 1

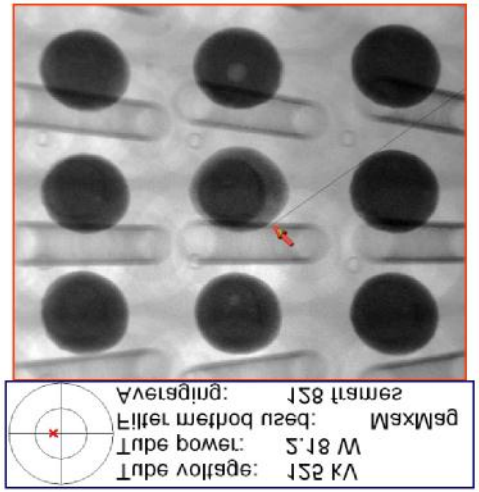
Darker Pad





Signature 2

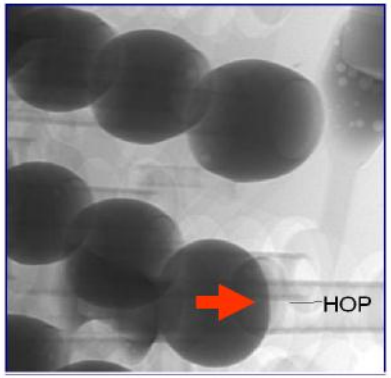
Off Circular Ball Shape

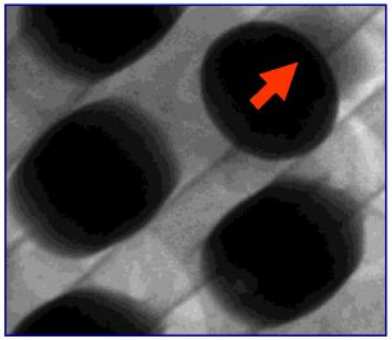


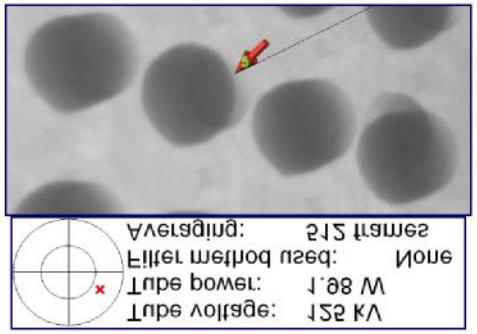
Signature 3

Clear Separation - Ball & Pad

Require Oblique Angle View

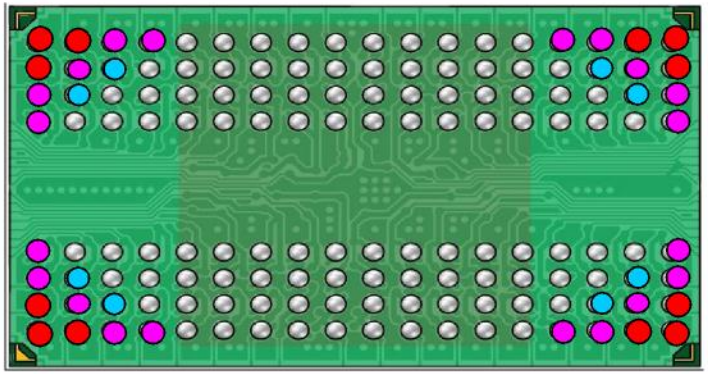






Process Mitigation Plan

Bull Eye Stencil Design



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+

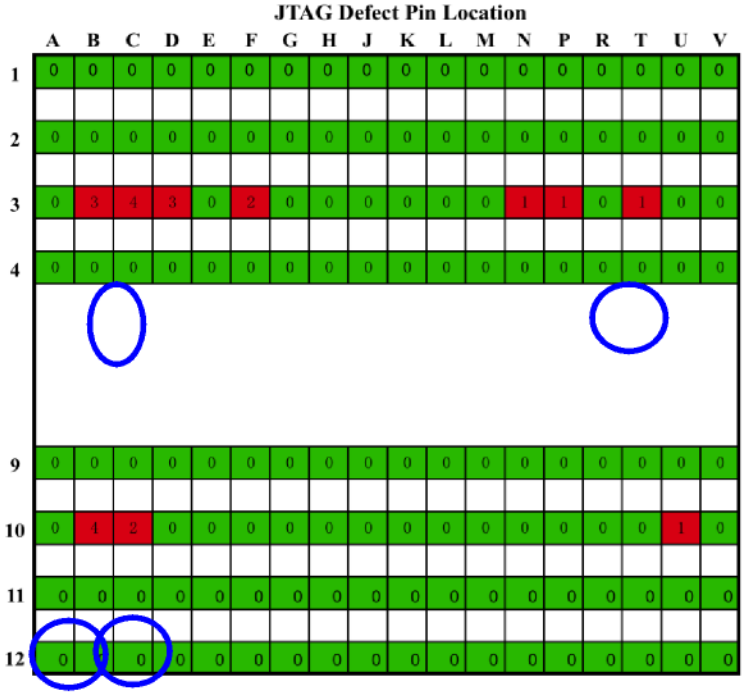
HiP Solder Paste Change

Reflow Profile

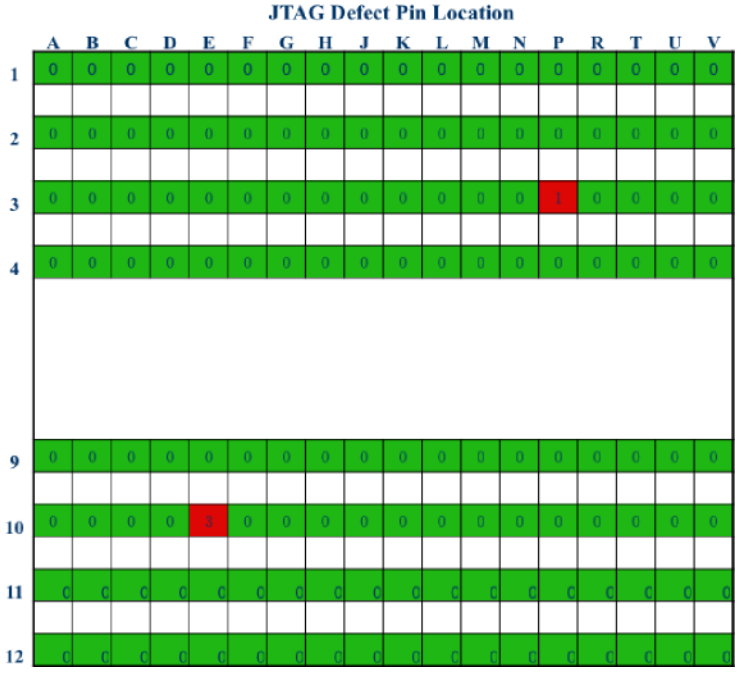
Reduce soaking time

JTAG Failing Pin Map

Total Sample: 1440
4 HiP



Total Sample: 608
0 HiP



Key Takeaways

UHiP are tough to detect.

UHiP causes infant failures after shipped to customers.

- Incidence rates will increase with Pb-free assembly.

UHiP occurs when there is no contact until the peak temperature but contact during cooling stage.

- Inactive flux when there is contact.

UFishbone diagram to analyze factors affecting HiP.

UHiP can be mitigated by right type of solder paste.

Pop Quiz

UWhich of the following scenario will result in HiP?

- A) No contact between solder ball and solder paste through the reflow process
- B) No contact initially but the solder ball makes contact with the solder paste when the flux is no longer active
- C) No contact initially but the solder ball makes contact with the solder paste when the flux is still active
- D) Solder ball and solder paste are in contact with each other through the reflow process

References

- Subbarayan, G., Priore, R., Sethuraman, S. “A Novel Test Methodology to Evaluate Solder Pastes for Mitigating Head in Pillow Defects”, *Journal of Surface Mount Technology International*, Volume 23, Issue 3, 2010.
- Amir, D., Aspandiar, R., Buttars, S., Chin, W., Gill, P., „Head-and-Pillow SMT Failure Modes“, *SMTAi*, San Diego, 2009.
- Bath, J., Garcia,G., Uchida,N., “ Investigation and development of tin-lead and lead-free solder pastes to reduce the Head-in-Pillow component soldering defect.

Acknowledgements

UScott Priore, Steven Perng - Assembly Sciences and Technology

UContact Information

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Questions?